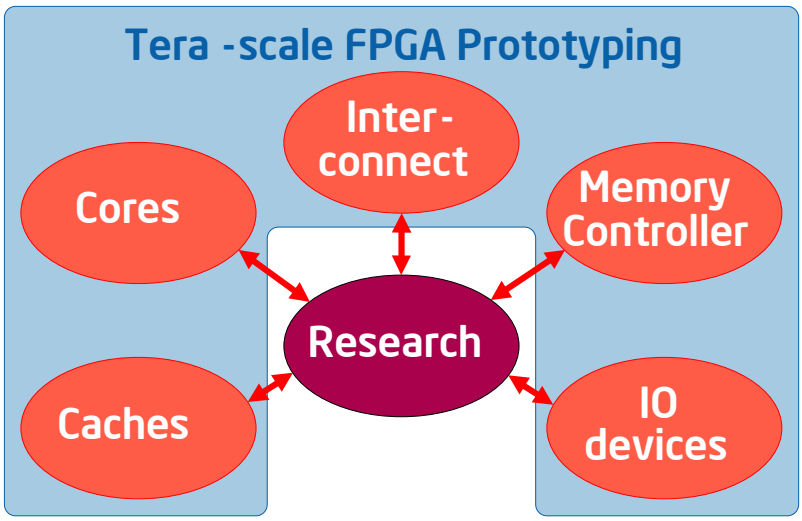
Tera-scale FPGA Prototyping

- Full system FPGA emulation of a Tera-scale computing system including: cores, interconnect, caches, memory and I/O
- High speed FPGA emulation allows to run real OS and future application workloads
- High bandwidth, flexible node-to-node interconnect enables implementation of different topologies



- Fast setup of experiment
- Verified blocks
- Architectural flexibility
- Mix and match of Intel® product design architectures and experimental architectures

- Designed for emulation scalability – emulation frequency is independent from number of nodes
- Backplane for system control + access of debug / trace data
- Building block library approach for cores, caches, memory and I/O
- Fills a gap between simulators and testchips like the Teraflops Research Processor (aka "Polaris") for architectural experiments:

	Turn around time	Simulation speed	Months of resources
Simulator	Hours	KIPS	1s-10s
FPGA	Days	MIPS	10s-100s
Silicon	Months - years	GIPS	100s-1000s

Comparison between Simulation , FPGA prototyping and Test silicon

Research at Intel
www.intel.com/research