

EXHIBIT 1

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

IN RE)
INTEL CORP MICROPROCESSOR)
ANTITRUST LITIGATION) MDL Docket No. 05-1717-JJF
_____)
ADVANCED MICRO DEVICES, INC., a)
Delaware corporation, and AMD)
INTERNATIONAL SALES & SERVICE LTD,)
a Delaware corporation,,)
)
Plaintiffs,)
)
v) Civil Action No. 05-441-JJF
)
)
INTEL CORPORATION, a Delaware)
corporation, and INTEL KABUSHIKI KAISHA,) DM _____
a Japanese corporation,)
)
Defendants.)

**DECLARATION OF WILLIAM T. SIEGLE
IN SUPPORT OF AMD'S MOTION TO COMPEL**

I, William T Siegle, declare as follows:

1. I joined AMD in 1990 and worked for the Company until my retirement in May, 2005. In early 1999, I assumed responsibility for worldwide silicon wafer production (including microprocessors). Although I relinquished microprocessor manufacturing responsibility at the end of 2001 to my colleague, Gary Heerssen, because of Mr Heerssen's subsequent illness I remained as a de facto head of microprocessor manufacturing through 2002, and I served in a dual role that included manufacturing until Mr Heerssen's successor, Daryl Ostrander, was named in 2004. When I left the Company, my title was Senior Vice President and AMD Chief Scientist.

2. As a result of my AMD job responsibilities, I am knowledgeable about the nature, location and capabilities of AMD's various microprocessor fabrication facilities around the

world. I submit this declaration in support of AMD's motion to compel production of documents and other information bearing upon Intel's attempts to prohibit, limit or dissuade its foreign customers from purchasing x86 microprocessors made by AMD or to punish them for doing so.

3. As discussed in greater detail in the paragraphs that follow, AMD manufactured x86 microprocessors domestically through 2002, and it continued to supply customers, including foreign customers, with domestically manufactured processors from its Austin, Texas plant for more than a year thereafter. With the exception of some 486 foundry chips produced in Scotland in the mid-1990s, up to 2000, AMD manufactured all of its x86 microprocessors *exclusively* at facilities located in the United States. In that year, AMD brought on line a new production facility in Dresden, Germany.

4. For reasons detailed in AMD's complaint, the excellence of the products we introduced in the late 1990s did not translate into the demand for AMD microprocessors that we had hoped for and anticipated. Thus, while we had expected to continue operations at our Austin plant even as Dresden ramped up to capacity, ultimately worldwide orders were not sufficient to keep both plants operating at efficient levels. We thus abandoned plans to update the technology for microprocessor production at Austin and instead dedicated it to the production of lower margin memory products beginning in 2003. Significantly, to the extent that Intel's conduct — both here and abroad — artificially limited customer demand for AMD microprocessors, that conduct significantly contributed to AMD's decision to cease their manufacture in Austin and to withdraw from the U.S. export market. In the absence of Intel's misconduct, and the consequent limits it placed on AMD's business, we would have continued to manufacture microprocessors in Austin during 2003 and for at least several years thereafter, and remained engaged in the export of U.S. manufactured microprocessors.

Background

5 Microprocessors like other semiconductors are produced in very sophisticated, high-technology “*fabrication*” facilities known in the industry as “*fabs*.” AMD has generally supplied its microprocessor requirements from a single fab.¹ When it first began participating in the semiconductor market in 1969, AMD manufactured chips at a fab (denominated “Fab 1”) located adjacent to its Silicon Valley headquarters. In 1979, AMD opened Fab 5 in Austin, Texas, which was followed by two other Austin facilities, Fab 10 which opened in 1982 and Fab 14/15 which opened in 1985.

6 Semiconductor technology is constantly advancing, and as Intel founder Gordon Moore observed, the density of transistor circuitry generally grows at a pace that allows the number of transistors on a given die (the piece of silicon on which they are embedded) to double every eighteen months. However, the process technology necessary to manufacture these ever-more dense parts must keep pace. As a result, while fabs are generally designed to support three generations of leading-edge technology, reinvestment is generally required for each new generation. New facilities are planned when the reinvestment becomes too great, when the disruption to production (in making the upgrades) is too severe, or when the expected business volumes demand additional capacity beyond what an upgraded fab can provide.

7 AMD opened Fab 25 in 1995 to build its fifth generation K5 product and to augment Am486 production being built in AMD’s California Submicron Development Center. The fab’s capacity, after an expansion, measured in wafer starts,² was roughly 5,000 per week,

¹ AMD has operated other less technologically advanced fabs for the manufacture of lower value products, such as flash memory and less sophisticated logic circuitry.

² A “wafer” is the slice of silicon material on which microprocessor die are built. Typically configured in 8” (200 mm) or, more recently, 12” (300 mm) rounds, the number of processors that can be built from a single wafer depends on the die size of the chip and its

equal to approximately 25-30 million microprocessors per year given their die size at the time

8 Given the relentless pace of innovation in the microprocessor world, work began almost immediately on AMD's next generation fab, designated Fab 30. AMD broke ground for this facility in Dresden, Germany in 1996. The fab came on line in 2000, but it did not achieve its 5,000 wafer-starts-per-week capacity until the second quarter of 2003 and did not ramp up to achieve this benchmark consistently until the third quarter of 2004. Fab 30 was engineered to initially implement 180nm (or 0.18 micron) technology, with easy extendibility to the 130nm generation, utilizing a copper interconnect process (contrasted to the aluminum interconnect utilized at Fab 25) that AMD had designed with Motorola to achieve higher densities.

The Debate Over the Future of Fab 25

9. With the debut of AMD's sixth generation chip in 1997 (referred to as the "K6"), AMD began building marketshare. The K6 was a clearly viable alternative to Intel products and superior in some graphic applications, enabling AMD to gain a level of acceptance at major computer manufacturers that AMD had not previously enjoyed.

10 The introduction in 1999 of the even more highly-regarded K7, a seventh generation product marketed as the Athlon chip (Bill Gates called it a "home run"), introduced the realistic prospect that the Company might for the first time realize its long-held ambition to achieve a 30% marketshare. The K7 was a clearly superior product to Intel offerings in many applications. It introduced a new micro-architecture that provided power/performance advantages over the existing Intel products and enabled AMD to leapfrog Intel in processing speed and be the first to reach the gigahertz milestone (one billion clock cycles per second), the PC industry's equivalent of breaking the sound barrier. As was the case with the K6,

process complexity

manufacture of the K7 began in Austin

11 Beginning in early 1999, my manufacturing group was reviewing our capacity strategy, and the role of Fab 25 in light of the distinct possibility that the Company might generate demand for its products beyond the capacity of Fab 30 to fill. AMD was strongly motivated to continue microprocessor production in Austin. Not only did it represent an important presence in the community, but AMD did not want to lose the highly skilled and experienced microprocessor production work force, the proximity the fab had to AMD's Austin circuit design team, and the close coupling with the joint development work with Motorola, being carried out in the nearby Motorola Austin facilities. A two-fab strategy would also provide us greater manufacturing flexibility. Furthermore, many executives made their home in Austin, and there was an important emotional attachment to the fab. Continued production at Fab 25 was practical. Although some of the equipment in the fab was reaching the end of its useful life for microprocessors, we estimated that the fab could be retrofitted with state-of-the-art tools and converted to cutting-edge copper technology supporting 130nm production for less than \$500 million, a fraction of the \$2-3 billion price tag attached to a completely new facility. And such an upgrade would delay the need to bring on line the next facility slated for construction, then denominated Fab 35.

12. The question remained one of demand. AMD's Founder, Chairman and CEO, Jerry Sanders, repeated the Company's goal of achieving a 30% marketshare at the 2000 shareholder's meeting, and declared that if it were met, the Company intended to continue microprocessor production at Austin:

"Our long-held goal has been, and remains, to capture a 30 percent unit share of the PC processor market by the end of 2001. With the production capacity of Fab 25 in Austin and Fab 30 in Dresden, by

the end of next year we will have in place the production capacity to achieve this goal "

13 My AMD manufacturing co-executive (and manufacturing successor), Gary Heerssen, was tasked with the job of analyzing the economics of our fab production in light of a growing success in the marketplace and recommending a future course for Fab 25. In a presentation he made in the Fall of 2000 to a group of Company senior executives, he concluded that assuming AMD captured and maintained a 30% marketshare, demand would be sufficient to support both fabs. In a slide entitled "How am I Leaning?" Gary reflected the thinking of many of us when he answered "Upgrade Fab 25; Defer Fab 35 "

14. Mr. Heerssen refined his analysis later in the year. In an October 2000 presentation made to the AMD Executive Council, Mr. Sanders' semiannual senior executive forum, Heerssen analyzed whether Fab 25 could be efficiently utilized given a variety of production volume scenarios including (a) attaining a 30% marketshare by 2002 in part by attracting Tier 1 Commercial business; (b) attaining it but only by 2005 or 2006; (c) attaining only a 26% marketshare; and (d) attaining no appreciable marketshare increase. He concluded with the following slide recommending an upgrade of Fab 25 and its continued use as a

Conclusion

AMD

- Best match of capacity to demand is from Fab 25 upgrade to copper**
 - ✓ Opportunity for upside support to Best Guess Case
 - ✓ Defers need for Fab 35 to ~ 2006

- Without Fab 25 upgrade, demand can be met only with substantial addition of foundry source**

- Financial return of Fab 25 upgrade is at least 2X that of Fab 35**
 - ✓ Very negative short term cash flow avoided

CC1:750757 *Also, leverages considerable exp. expertise in F20*

Allows continued transition development project to Fab 30

microprocessor facility:

15 Plans were thereafter initiated to upgrade Fab 25 and establish a dual fab strategy. The conversion of Fab 25 to copper technology so as to keep it in microprocessor service was budgeted in the December 4, 2000 version of our Group's Three Year Plan in 2000.

Reassessment in Light of Insufficient Demand to Fill Two Fabs

16 Despite the Company's unit marketshare improving from a low of 7% in 1995 to 17% in 2000, the optimism of 1999 and early 2000 gave way to disappointment. The 30% marketshare aspirational goal that Mr. Sanders had set began to look unattainable (in any near term) given the volume of customer orders.

17. Ultimately, we determined that current and near future demand for AMD microprocessors would not support two 130nm copper fabs, and thus the cost of upgrading Fab 25 could not be justified. As individual group financial plans were consolidated into a company-wide budget, our manufacturing group plan was amended to abandon the Fab25 upgrade, based on the fact that the unit volumes that could be committed would not produce a viable financial plan with the continued use of a partially loaded Fab 25. We did not entertain the alternative of running one of the two fabs at less than optimum capacity since, given the very high fixed costs associated with a fab, our average costs per unit would have been driven to non-competitive levels. Any shortfall that might develop, we concluded, could hopefully be covered by utilizing independently owned foundries to produce AMD processors.

18 Eventually we settled on a plan to convert Fab 25 to produce lower-margin flash memory in support of a joint venture with a Japanese semiconductor company. Flash shipments began in 2002, though the decision to discontinue microprocessor production at Fab 25 did not become irreversible until 2004, by which we had ramped flash production to full capacity. Using

the fab to make flash was viewed as the most viable way to get continuing value from a capital asset in which we had much invested and to avoid the prospect of significant employee layoffs. Earlier this year, AMD's interest in the joint venture was spun off into an independent, publicly-owned company, Spansion, which now owns Fab 25.

Microprocessor Production at Fab 25 Had Demand Been Greater

19. In short, Fab 25 was removed from microprocessor service because of the absence of sufficient anticipated orders to support two fabs.

20. I defer to those closer to the marketplace for the reasons why we were unable to garner sufficient orders for our very highly regarded Athlon family of processors. Had there been sufficient demand to justify its renovation and continued operation, we would not have closed Fab 25 but instead continued to use it for microprocessors. Based on the analyses we did at the time, we concluded that there was very little prospect of garnering a sustained marketshare of 30% or any lower percentage that would have justified operating two 5,000 wafer-start fabs. Had our forecasts been different, we undoubtedly would have upgraded Fab 25 to 130nm copper technology, which would have enabled it to participate in the production of not only our K7 Athlon product but also the K8 generation of products that we introduced beginning in 2003, including the Opteron, Turion64 and Athlon64.

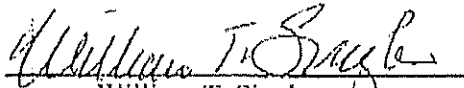
21. Moreover, had greater demand existed for AMD product in the years prior to the closure of Fab 25, it clearly would have had to come from domestic production. Although Fab 30 began fabricating microprocessors in 2000, it underwent the usual gradual ramp-up for the next three years until reaching its designed capacity of 5,000 wafer starts for the first time during the second quarter of 2003. During the period 2000-2002, on the other hand, Fab 25 was ramping down. From 2000 until its conversion to flash memory production in 2003, the only

AMD-owned facility that could have produced additional processors, had there been additional orders, would have been Fab 25.

22 After Fab 25 was committed to making memory chips, it is likely that we would have sourced additional AMD microprocessors from a foundry (an independently owned fab that manufactures microprocessors as a service) had we received orders beyond the capacity of Fab 30 to fill. (As noted above, the decision to convert Fab 25 to flash memory production was made with the hope that any shortfall could be covered by a foundry) At the time, of the four foundries capable of 130 nm microprocessor production, two were located in the United States (Motorola and IBM), introducing the distinct possibility that we would have sourced any shortfall by subcontracting for domestically produced microprocessors

I declare under the penalty of perjury of the laws of the United States and the State of Connecticut that the foregoing is true and correct

Executed this 27th day of October, 2006 at Southbury, Connecticut.


William T Siegle

IN THE UNITED STATES DISTRICT COURT
DISTRICT OF DELAWARE

CERTIFICATE OF SERVICE

I hereby certify that on October 30, 2006, I electronically filed the foregoing document with the Clerk of Court using CM/ECF which will send notification of such filing(s) and have sent by Hand Delivery to the following:

Richard L. Horwitz, Esquire
Potter Anderson & Corroon LLP
1313 North Market Street
P. O. Box 951
Wilmington, DE 19899

and have sent by Federal Express to the following non-registered participants:

Darren B. Bernhard, Esquire
Howrey LLP
1299 Pennsylvania Avenue, N.W.
Washington, DC 20004-2402

Robert E. Cooper, Esquire
Daniel S. Floyd, Esquire
Gibson, Dunn & Crutcher LLP
333 South Grand Avenue
Los Angeles, California 90071-3197

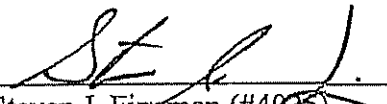

Steven J. Fineman (#4025)
Richards, Layton & Finger, P.A.
One Rodney Square
P.O. Box 551
Wilmington, Delaware 19899
(302) 651-7700
fineman@rlf.com

EXHIBIT 2

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

IN RE)
INTEL CORP. MICROPROCESSOR)
ANTITRUST LITIGATION) MDL Docket No. 05-1717-JJF
_____)
ADVANCED MICRO DEVICES, INC., a)
Delaware corporation, and AMD)
INTERNATIONAL SALES & SERVICE LTD,)
a Delaware corporation,,)
)
Plaintiffs,)
) Civil Action No. 05-441-JJF
v.)
)
INTEL CORPORATION, a Delaware) DM _____
corporation, and INTEL KABUSHIKI KAISHA,)
a Japanese corporation,)
)
Defendants.)

**DECLARATION OF DEWEY OVERHOLSER
IN SUPPORT OF AMD'S MOTION TO COMPEL**

I, Dewey Overholser, declare as follows:

1. I am employed by AMD, Inc. in the position of Master Product Control Planner, and I work out of one of AMD's Austin, Texas facilities. I am responsible for developing capacity plans from sales forecasts using data concerning engineering yields and factory cycles. I also gather information and prepare other reports for my group including analyses of billings, backlog and inventory.

2. As part of my employment, I have access to various AMD databases. One is the PBDM, which was AMD's primary data warehouse for sales-related reporting from about 1999 to August 2004. The PBDM database has been frozen as of August 2004 and continues to be the primary database for reporting historical sales data. This database was prepared and is maintained in the ordinary course of AMD's business.

3. I generated a spreadsheet from the PBDM database for purpose of identifying all sales made of microprocessors manufactured at AMD's Fab 25 in Austin, Texas from 2002 through the present. From my analysis of that report, I have determined that AMD sold very substantial quantities of Fab 25-produced microprocessors to its customers during calendar years 2002 and 2003, amounting to almost \$388 million in 2002 and almost \$40 million in 2003. Some Fab 25-produced microprocessors were also sold in 2004, but in very limited quantities. AMD made its final 2004 sale on May 7, 2004; its final export sale was made on April 16, 2004.

4. During this entire period, Fab 25 supplied both foreign customers and those located in North America. But most Fab 25 product was sold into the export market. The following table provides a percentage breakdown by quarter:¹

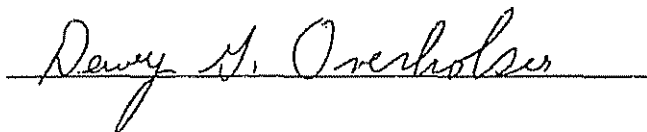
		% Export	% N. America
2002	1Q	75%	25%
	2Q	73%	27%
	3Q	75%	25%
	4Q	64%	36%
2003	1Q	65%	35%
	2Q	92%	8%
	3Q	7%	93%
	4Q	0%	100%
2004	1Q	0	100%
	2Q	2%	98%

5. I have also reviewed a series of reports calls "Actuals Packages," which is a summary of fab data that AMD generates quarterly from production databases it maintains in the ordinary course of its business to track microprocessor manufacturing. According to these reports, even after AMD Fab 30 came on line in 2000, Fab 25 continued to be an important

source of microprocessors for the Company. For the calendar years 2000, 2001 and 2002 Fab 25 produced microprocessors in the following numbers: 30,733,000, 22,267,000 and 8,565,000. Fab 25 continued to manufacture K-7 microprocessors through the fourth quarter of 2002, when it was taken out of microprocessor production.

I declare under penalty of perjury that the foregoing is true and correct.

Executed this 26 day of October, 2006, at Austin, Texas.

A handwritten signature in cursive script, reading "Dewey M. Overholser", is written over a horizontal line.

¹ The export percentages are somewhat understated since AMD's North American data include sales to Canada, which should rightly be included in the export column. The PBDM database does not separately break out U.S. sales.

IN THE UNITED STATES DISTRICT COURT
DISTRICT OF DELAWARE

CERTIFICATE OF SERVICE

I hereby certify that on October 30, 2006, I electronically filed the foregoing document with the Clerk of Court using CM/ECF which will send notification of such filing(s) and have sent by Hand Delivery to the following:

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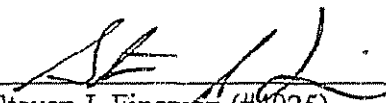

Steven J. Fineman (#4025)
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One Rodney Square
P O. Box 551
Wilmington, Delaware 19899
(302) 651-7700
fineman@rlf.com

EXHIBIT 3

ADVANCED MICRO DEVICES INC

FORM 10-K (Annual Report)

Filed 03/29/99 for the Period Ending 12/27/98

Address	ONE AMD PL MS 68 SUNNYVALE, CA 94088-3453
Telephone	4087322400
CIK	0000002488
Symbol	AMD
SIC Code	3674 - Semiconductors and Related Devices
Industry	Semiconductors
Sector	Technology
Fiscal Year	12/27

UNITED STATES
SECURITIES AND EXCHANGE COMMISSION
Washington, D.C. 20549

FORM 10-K

(Mark One)

ANNUAL REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE
ACT OF 1934.

For the fiscal year ended December 27, 1998

OR

TRANSITION REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES
EXCHANGE ACT OF 1934.

For the transition period from to

Commission File Number 1-7882

ADVANCED MICRO DEVICES, INC.

(Exact name of registrant as specified in its charter)

Delaware

94-1692300

(I R S Employer Identification No)

(State or other jurisdiction of
incorporation or organization)

One AMD Place,
Sunnyvale, California

94086

(Zip Code)

(Address of principal executive
offices)

Registrant's telephone number, including area code: (408) 732-2400

Securities registered pursuant to Section 12(b) of the Act:

(Title of each class)	(Name of each exchange on which registered)
----- \$ 01 Par Value Common Stock	----- New York Stock Exchange

Securities registered pursuant to Section 12(g) of the Act:

None

Indicate by check mark whether the registrant (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Exchange Act of 1934 during the preceding 12 months (or for such shorter period that the registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days. Yes X No

Indicate by check mark if disclosure of delinquent filers pursuant to Item 405 of Regulation S-K is not contained herein, and will not be contained, to the best of registrant's knowledge, in definitive proxy or information statements incorporated by reference in Part III of this Form 10-K or any amendment to this Form 10-K.

Aggregate market value of the voting stock held by non-affiliates as of March 1, 1999

\$2,665,120,199

Indicate the number of shares outstanding of each of the registrant's classes of common stock, as of the latest practicable date.

146,161,636 shares as of March 1, 1999.

DOCUMENTS INCORPORATED BY REFERENCE

- (1) Portions of the Annual Report to Stockholders for the fiscal year ended December 27, 1998, are incorporated into Parts II and IV hereof.
 - (2) Portions of the Proxy Statement for the Annual Meeting of Stockholders to be held on April 29, 1999, are incorporated into Part III hereof.
-
-

NOTE 9. SEGMENT REPORTING

In June 1997, the Financial Accounting Standards Board issued the Statement of Financial Accounting Standards No. 131 (SFAS 131), "Disclosures about Segments of an Enterprise and Related Information," which we have adopted in the current year.

As required by SFAS 131, we have determined that we have two principle businesses and operate in two segments: (1) our AMD segment, which consists of our three product groups - Computation Products Group, Memory Group and Communications Group and (2) our Vantis segment, which consists of Vantis. Our reportable segments are organized as discrete and separate functional units with separate management teams and separate performance assessment and resource allocation processes. The AMD segment produces microprocessors, core logic products, Flash memory devices, EPROMs, telecommunication products, networking and I/O products and embedded processors. The Vantis segment produces complex and simple, high-performance CMOS PLDs.

The accounting policies of the segments are the same as those described in the summary of significant accounting policies. We evaluate performance and allocate resources based on segment operating income (loss).

The AMD segment did not have intersegment sales prior to the fourth quarter of 1997. The Vantis segment did not have intersegment sales for any of the years presented below.

(Thousands)	1998	1997	1996

Net sales:			
AMD segment			
External customers	\$2,337,144	\$2,113,276	\$1,704,925
Intersegment	88,455	25,896	-
	-----	-----	-----
	2,425,599	2,139,172	1,704,925
Vantis segment external customers	204,997	243,099	248,094
Elimination of intersegment sales	(88,455)	(25,896)	-
	-----	-----	-----
Net sales	\$2,542,141	\$2,356,375	\$1,953,019
	=====		
Segment income (loss):			
AMD segment	\$ (185,242)	\$ (127,406)	\$ (270,270)
Vantis segment	21,600	36,753	16,960
	-----	-----	-----
Total operating loss	(163,642)	(90,653)	(253,310)
Litigation settlement	(11,500)	-	-
Interest income and other, net	34,207	35,097	59,391
Interest expense	(66,494)	(45,276)	(14,837)
Benefit for income taxes	91,878	55,155	85,008
Equity in net income of FASL (AMD segment)	11,591	24,587	54,798
	-----	-----	-----
Net loss	\$ (103,960)	\$ (21,090)	\$ (68,950)
	=====		
Total assets:			
AMD segment			
Assets excluding investment in FASL	\$3,881,268	\$3,187,506	\$2,886,689
Investment in FASL	236,820	204,031	197,205
	-----	-----	-----
	4,118,088	3,391,537	3,083,894
Vantis segment assets	134,880	123,734	61,389
	-----	-----	-----
Total assets	\$4,252,968	\$3,515,271	\$3,145,283
	=====		
Expenditures for long-lived assets:			
AMD segment	\$ 993,679	\$ 683,346	\$ 480,746
Vantis segment	2,491	1,754	4,272
	-----	-----	-----
Total expenditures for long-lived assets	\$ 996,170	\$ 685,100	\$ 485,018
	=====		
Depreciation and amortization expense:			
AMD segment	\$ 463,719	\$ 390,577	\$ 343,053
Vantis segment	3,802	3,888	3,721
	-----	-----	-----
Total depreciation and amortization expense	\$ 467,521	\$ 394,465	\$ 346,774
	=====		

Notes to Consolidated Financial Statements

Our operations outside the United States include both manufacturing and sales. Our manufacturing subsidiaries are located in Germany, Malaysia, Thailand, Singapore and China. Our sales subsidiaries are in Europe and Asia Pacific.

The following is a summary of operations by entities within geographic areas for the three years ended December 27, 1998:

(Thousands)	1998	1997	1996
Sales to external customers:			
United States	\$1,148,610	\$1,024,718	\$ 917,174
Germany	265,429	219,255	142,339
Other Europe	464,760	464,105	393,444
Asia Pacific	663,342	648,297	500,062
	\$2,542,141	\$2,356,375	\$ 1,953,019
Long-lived assets:			
United States	\$1,718,435	\$1,705,084	\$ 1,613,286
Germany	333,851	102,810	12,586
Other Europe	3,927	3,735	4,492
Asia Pacific	212,255	179,060	157,038
	\$2,268,468	\$1,990,689	\$ 1,787,402

Sales to external customers are based on the customers' billing location. Long-lived assets are those assets used in each geographic area.

We market and sell our products primarily to a broad base of customers comprised of distributors and Original Equipment Manufacturers (OEMs) of computation and communication equipment. One of our OEMs accounted for approximately 12 percent of 1998 net sales. One of our distributors accounted for approximately 12 percent and 13 percent of 1997 and 1996 net sales, respectively. No other distributor or OEM customer accounted for 10 percent or more of net sales in 1998, 1997 or 1996.

NOTE 10. Stock-Based Benefit Plans

STOCK OPTION PLANS We have several stock option plans under which key employees have been granted incentive (ISOs) and nonqualified (NSOs) stock options to purchase our common stock. Generally, options are exercisable within four years from the date of grant and expire five to ten years after the date of grant. ISOs granted under the plans have exercise prices of not less than 100 percent of the fair market value of the common stock at the date of grant. Exercise prices of NSOs range from \$0.01 to the fair market value of the common stock at the date of grant.

On September 10, 1998, the Compensation Committee of our Board of Directors approved a stock option repricing program pursuant to which our employees (excluding officers and vice presidents) could elect to cancel certain unexercised stock options in exchange for new stock options with an exercise price of \$19.43, which was equal to 20 percent above the closing price of our common stock on the New York Stock Exchange on September 10, 1998. Approximately 2 million options were eligible for repricing, of which we repriced approximately 1.7 million. We extended the vesting schedules and expiration dates of repriced stock options by one year.

On July 10, 1996, the Compensation Committee of our Board of Directors approved a stock option repricing program pursuant to which our employees (excluding officers) could elect to cancel certain unexercised stock options in exchange for new stock options with an exercise price of \$11.88, equal to the closing price of our common stock on the New York Stock Exchange on July 15, 1996. Approximately 6.1 million options were eligible for repricing, of which we repriced approximately 5.3 million. We extended the vesting schedules and expiration dates of repriced stock options by one year, and certain employees canceled stock options for four shares of common stock in exchange for repriced options for three shares of common stock.

EXHIBIT 4

ADVANCED MICRO DEVICES INC

FORM 10-K405

(Annual Report (Regulation S-K, item 405))

Filed 03/20/01 for the Period Ending 12/31/00

Address	ONE AMD PL MS 68 SUNNYVALE, CA 94088-3453
Telephone	4087322400
CIK	0000002488
Symbol	AMD
SIC Code	3674 - Semiconductors and Related Devices
Industry	Semiconductors
Sector	Technology
Fiscal Year	12/27

**UNITED STATES
SECURITIES AND EXCHANGE COMMISSION**
Washington, D.C. 20549

FORM 10-K

(Mark One)

ANNUAL REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE
ACT OF 1934.

For the fiscal year ended December 31, 2000

OR

TRANSITION REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES
EXCHANGE ACT OF 1934.

For the transition period from to

Commission File Number 1-7882

ADVANCED MICRO DEVICES, INC.

(Exact name of registrant as specified in its charter)

Delaware
(State or other jurisdiction
of incorporation or organization)

94-1692300
(I.R.S. Employer
Identification No.)

One AMD Place,
Sunnyvale, California
(Address of principal executive offices)

94086
(Zip Code)

Registrant's telephone number, including area code: (408) 732-2100

Securities registered pursuant to Section 12(b) of the Act:

(Title of each class) -----	(Name of each exchange on which registered) -----
\$.01 Par Value Common Stock	New York Stock Exchange

Securities registered pursuant to Section 12(g) of the Act:

None

Indicate by check mark whether the registrant (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Exchange Act of 1934 during the preceding 12 months (or for such shorter period that the registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days Yes No

Indicate by check mark if disclosure of delinquent filers pursuant to Item 405 of Regulation S-K is not contained herein, and will not be contained, to the best of registrant's knowledge, in definitive proxy or information statements incorporated by reference in Part III of this Form 10-K or any amendment to this Form 10-K

Aggregate market value of the voting stock held by non-affiliates as of February 26, 2001

\$7,175,108,834

Indicate the number of shares outstanding of each of the registrant's classes of common stock, as of the latest practicable date.

314,747,355 shares as of February 26, 2001.

DOCUMENTS INCORPORATED BY REFERENCE

- (1) Portions of the Annual Report to Stockholders for the fiscal year ended December 31, 2000, are incorporated into Parts II and IV hereof
 - (2) Portions of the Proxy Statement for the Annual Meeting of Stockholders to be held on April 26, 2001, are incorporated into Part III hereof.
-

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NOTES TO CONSOLIDATED FINANCIAL STATEMENTS

Under certain circumstances, cross-defaults result under the Convertible Subordinated Notes, the Indenture for the Senior Secured Notes and the Dresden Loan Agreements, which consist of a loan agreement and other related agreements between AMD Saxony and a consortium of banks led by Dresdner Bank AG.

8. INTEREST EXPENSE & INTEREST INCOME AND OTHER, NET

Interest Expense

(Thousands)	2000	1999	1998
Total interest charges	\$ 86,488	\$ 116,255	\$ 96,206
Less: interest capitalized	(26,451)	(47,002)	(29,712)
<i>Interest expense</i>	<i>\$ 60,037</i>	<i>\$ 69,253</i>	<i>\$ 66,494</i>

In 2000, 1999 and 1998, interest expense consisted primarily of interest incurred on the Company's Senior Secured Notes sold in August 1996, interest on the Company's Convertible Subordinated Notes sold in May 1998 and interest on the Company's \$250 million four-year secured term loan, net of interest capitalized primarily related to the facilitization of *Fab 25* and *Dresden Fab 30*

Interest Income and Other, Net

(Thousands)	2000	1999	1998
Interest income	\$ 59,228	\$ 26,461	\$ 31,478
Other income, net	27,073	5,274	2,729
	<i>\$ 86,301</i>	<i>\$ 31,735</i>	<i>\$ 34,207</i>

Other income consists of gains from the sales of investments and other assets.

9. SEGMENT REPORTING

For purposes of disclosures required by Statement of Financial Accounting Standards No. 131 (SFAS 131), AMD operated in three reportable segments during 2000: the Core Products, Voice Communications and Foundry Services segments. AMD has previously shown two reportable segments, however, as a result of the sale of Legerity, effective July 31, 2000, the Company re-evaluated its segment reporting structure. Prior period segment information has been restated to conform to the current period presentation. The Core Products segment includes microprocessors, Flash memory devices, Erasable Programmable Read-Only Memory (EPROM) devices, embedded processors, platform products and networking products. The Voice Communications segment includes voice communications products of the Company's former subsidiary, Legerity, until July 31, 2000, the effective date of its sale. The Vantis segment included the programmable logic devices of the Company's former subsidiary, Vantis, until June 15, 1999, the date of its sale. The Foundry Services segment included fees for services provided

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS

to Legerity and Vantis. The accounting policies of the segments are the same as those described in the Summary of Significant Accounting Policies. The Company evaluates performance and allocates resources based on these segments' operating income (loss).

The following table is a summary of operating income (loss) by segment for 2000, 1999 and 1998:

(Thousands)	2000	1999	1998
Net sales:			
Core Products segment			
External customers	\$ 4,361,398	\$ 2,559,939	\$ 2,180,655
Intersegment sales	-	32,626	88,455
	4,361,398	2,592,565	2,269,110
Voice Communications segment-external customers	140,309	167,760	156,489
Vantis segment-external customers	-	86,701	204,997
Foundry Services segment-external customers	142,480	43,204	-
Elimination of intersegment sales	-	(32,626)	(88,455)
Total net sales	\$ 4,644,187	\$ 2,857,604	\$ 2,542,141
Segment operating income (loss):			
Core Products segment	\$ 831,749	\$ (342,007)	\$ (161,722)
Voice Communications segment	34,987	13,943	(23,520)
Vantis segment	-	5,639	21,600
Foundry Services segment*	22,000	1,509	-
Total segment operating income (loss)	888,736	(320,916)	(163,642)
Gain on sale of Vantis	-	432,059	-
Gain on sale of Legerity	336,899	-	-
Litigation settlement	-	-	(11,500)
Interest income and other, net	86,301	31,735	34,207
Interest expense	(60,037)	(69,253)	(66,494)
Benefit (provision) for income taxes	(256,868)	(167,350)	91,878
Equity in net income of FASL (Core Products)	11,039	4,789	11,591
Extraordinary item - debt retirement, net of tax benefit	(23,044)	-	-
Net income (loss)	\$ 983,026	\$ (88,936)	\$ (103,960)
Total assets:			
Core Products segment			
Assets excluding investment in FASL	\$ 5,506,007	\$ 4,066,346	\$ 3,846,486
Investment in FASL	261,728	273,608	236,820
	5,767,735	4,339,954	4,083,306
Voice Communications segment	-	37,744	34,782
Vantis segment	-	-	134,880
Foundry Services segment*	-	-	-
Total assets	\$ 5,767,735	\$ 4,377,698	\$ 4,252,968
Expenditures for long-lived assets:			
Core Products segment	\$ 803,065	\$ 611,903	\$ 991,959
Voice Communications segment	2,409	1,729	1,720
Vantis segment	-	6,141	2,491
Foundry Services segment*	-	-	-
Total expenditures for long-lived assets	\$ 805,474	\$ 619,773	\$ 996,170
Depreciation and amortization expense:			
Core Products segment	\$ 578,302	\$ 512,203	\$ 462,505
Voice Communications segment	768	1,044	1,214
Vantis segment	-	2,273	3,802
Foundry Services segment*	-	-	-
Total depreciation and amortization expense	\$ 579,070	\$ 515,520	\$ 467,521

*Operations of the Foundry Services segment are conducted using assets of the Core Products segment.

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS

The Company's operations outside the United States include both manufacturing and sales. The Company's manufacturing subsidiaries are located in Germany, Malaysia, Thailand, Singapore and China. Its sales subsidiaries are in Europe, Asia Pacific and Brazil.

The following is a summary of operations by entities within geographic areas for the three years ended December 31, 2000:

(Thousands)	2000	1999	1998
Sales to external customers:			
United States	\$ 1,875,408	\$ 1,131,983	\$ 1,148,610
Europe	1,553,808	835,673	730,189
Asia Pacific	1,214,971	889,948	663,342
	-----	-----	-----
	\$ 4,644,187	\$ 2,857,604	\$ 2,542,141
	=====	=====	=====
Long-lived assets:			
United States	\$ 1,220,193	\$ 1,469,412	\$ 1,718,435
Germany	1,064,308	812,773	333,851
Other Europe	3,188	3,847	3,927
Asia Pacific	348,778	237,204	212,255
	-----	-----	-----
	\$ 2,636,467	\$ 2,523,236	\$ 2,268,468
	=====	=====	=====

Sales to external customers are based on the customer's billing location. Long-lived assets are those assets used in each geographic area.

The Company markets and sells its products primarily to a broad base of customers comprised of distributors and OEMs of computation and communications equipment. One of the Company's OEMs accounted for approximately 11, 13 and 12 percent of 2000, 1999 and 1998 net sales, respectively. No distributor accounted for 10 percent or more of net sales in 2000, 1999 and 1998.

10. STOCK-BASED INCENTIVE PLANS

Stock Option Plans. The Company has several stock option plans under which key employees have been granted incentive (ISOs) and nonqualified (NSOs) stock options to purchase the Company's common stock. Generally, options vest and become exercisable over four years from the date of grant and expire five to ten years after the date of grant. ISOs granted under the plans have exercise prices of not less than 100 percent of the fair market value of the common stock on the date of grant. Exercise prices of NSOs range from \$0.01 to the fair market value of the common stock on the date of grant. As of December 31, 2000, 3,231 employees were eligible and participating in the plans.

In 1998, the Compensation Committee of the Company's Board of Directors approved a stock option repricing program pursuant to which the Company's employees (excluding officers and vice presidents) could elect to cancel certain unexercised stock options in exchange for new stock options with an exercise price of \$9.71, which was equal to 20 percent above the closing price of the Company's common stock on the New York Stock Exchange on September 10, 1998. Approximately four million options were eligible for repricing, of which the Company

EXHIBIT 5

Archives
Columns
Features
Print Archives
1994-1998

Special
BYTE Digest
Michael Abrash's
Graphics
Programming Black
Book
101 Perl Articles

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The Slot Thickens

February 1998 / Cover Story / Disposable PCs / The Slot Thickens

Jerry Sanders, founder and CEO of Advanced Micro Devices, dropped a bombshell during his keynote speech at the recent Microprocessor Forum: In 1999, AMD's future K7 processor will come in a cartridge that's physically compatible with Intel's proprietary Slot 1. But AMD's new CPU interface, tentatively dubbed Slot A, won't be electrically compatible with Slot 1.

Before the audience of stunned engineers could digest that information, Sanders continued. The K 7 will abandon the x86-standard Socket 7 bus in favor of the I/O bus on Digital Equipment's Alpha 21264 processor. And to wrap up the surprise, Sanders added that future 21264 chips will adopt the same cartridge and will work interchangeably with K7 cartridges on Slot A motherboards.

Even Digital was caught off-guard. Although Digital and AMD had worked out the deal, Digital didn't know Sanders was going public so soon. Sanders probably wanted to launch a preemptive strike against the growing speculation that AMD wasn't prepared for life after Socket 7. The new alliance with Digital will bring a blazingly fast I/O interface to AMD's processors while opening up a larger market of commodity-priced motherboards to Digital's RISC chips.

Flexible

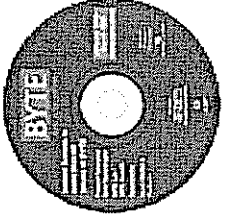
My approach to software engineering is far more pragmatic than it is theoretical--and no language better exemplifies this than C++.

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BYTE Digest

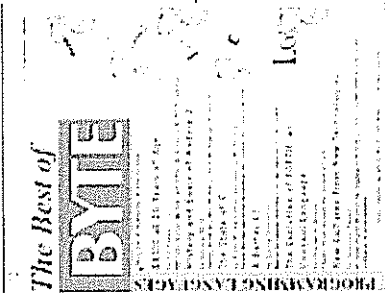
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The Best of BYTE

Volume 1: Programming Languages

In this issue of *Best of BYTE*, we bring together some of the leading programming language designers and implementors...

AMD had to do something, because Intel's P6-series processors (the Pentium Pro and the Pentium II) introduced a proprietary CPU interface that's protected by numerous patents. Cloning it is technically easy, but it's legally difficult. And even if the patents did not exist, AMD is forbidden to clone the P6 interface by a 1996 settlement ending a long-running court battle over Intel's intellectual property.

Intel's P6 interface takes several physical forms, all adhering to the same electrical-bus protocol. Pentium Pro chips use Socket 8. Pentium II chips come in a Single Edge Contact (SEC) cartridge that fits Slot 1, Slot 2, or a smaller slot for notebook computers. The SEC cartridge is really an enclosed daughterboard with a heat sink that slides down through a pair of vertical channels into a slot on the motherboard (see the photo).

The P6 interface has a 64-bit-wide system bus that runs at 66 MHz, which will soon increase to 100 MHz when Intel releases the 440BX chip set. It also has a separate 64-bit-wide back-side bus for the Level 2 (L2) cache.

In Slot 1 systems, the back-side bus typically runs at half the frequency of the CPU core. In Slot 2 systems, it can run as fast as the core (333 MHz and higher with Deschutes).

Because Intel isn't licensing the P6 interface to competitors who make x86-compatible processors, nobody else can make chips that work on the same motherboards as Intel's processors. That's a big change from Socket 7, which any vendor can use.

However, Intel's patents cover only the P6-bus protocol, not the physical cartridges or connectors. Those parts are available from multiple suppliers. AMD's plan is to leverage the growing infrastructure for the parts by introducing a CPU interface that's physically compatible. It's less costly than inventing a new interface and lobbying suppliers to support it.

Also, Slot A motherboards would be very similar to Slot 1 motherboards, requiring only a different core-logic system chip set and some minor layout changes. That would make life easier for motherboard manufacturers.

(Actually, Slot A probably won't be exactly the same as Slot 1. To prevent accidental damage to motherboards and CPUs, Slot A will almost certainly be keyed in a slightly different way so users can't insert an Intel cartridge into AMD's slot or vice versa.)

AMD needed a next-generation I/O interface to go along with Slot A. The company chose Digital's 21264 interface (which is known internally as EV-6), because it offers significant advantages over Socket 7: much higher clock frequencies and better support for multiprocessing.

While Socket 7 currently runs at 66 MHz and will soon step up to 100 MHz, EV-6 can run at a blazing 333 MHz. That's over three times faster than Socket 7 or Intel's P6

bus. And although EV-6 doesn't define a separate back-side bus for an L2 cache, designers are free to add one if they wish -- allowing more flexibility for different markets. For instance, Digital's high-end 21264 implements a 128-bit-wide back-side bus, twice as wide as Intel's.

How can EV-6 run at 333 MHz when even a 100-MHz motherboard is difficult to engineer? Because EV-6, strictly speaking, isn't a bus. It's a 64-bit, point-to-point I/O channel between the CPU and the system chip set. That's a major departure from today's x86 buses.

In a Socket 7 system, the CPU, L2 cache, main memory, and PCI bus all hang off the same local I/O bus. P6 systems are similar, except that the L2 cache is on a back-side bus. In both those systems, the local I/O bus must also handle the Accelerated Graphics Port (AGP), if one is present. In a multiprocessor system, additional CPUs also share the bus. This all adds up to a great deal of bus traffic.

In an EV-6 system, the CPU talks directly to the chip set over a private channel. The chip set, in turn, branches off to all the other buses: main memory, PCI, and AGP. Each of those buses runs at its own speed. Main memory could run at 66 or 100 MHz while the PCI bus runs at 33 MHz and AGP runs at 66 MHz. In a multiprocessor system, each CPU has its own private channel (clocked as high as 333 MHz) to the chip set. (See the figure "Digital's EV-6 Architecture".)

At 333 MHz, EV-6 has 2.6 GBps of raw bandwidth, more than three times as much as a Socket 7 or P6 bus at 100 MHz. That's an enormous advantage, because the prime factor limiting performance in modern CPUs is the time they take to access memory. A high-end system could exploit EV-6's extra bandwidth by hanging the memory on a 128-bit-wide bus on the chip set. That would double the amount of raw bandwidth to memory. Even if the memory is on a conventional 64-bit bus, EV-6's headroom should mean fewer stalls while the CPU refills its cache lines.

The downside: EV-6 chip sets are more complicated to design, and chip sets for multiprocessor systems will be expensive, because they'll need at least 64 additional pins for each CPU. AMD is working with third-party vendors such as VIA to design EV-6 chip sets.

For Digital, the big win is that future Alpha processors that have EV-6 and a Slot A cartridge will plug into the same motherboards as AMD's K7 processor. Only the BIOS needs to change. Since modern BIOSes use flash ROM, it's a quick software upgrade.

Today, Alpha systems are relatively expensive because they require special motherboards and chip sets that aren't made in large volumes. If AMD is successful, there will be a lively commodity market for Slot A motherboards. Together with lower-priced Alpha CPUs (such as an EV-6 variant of the 21164 PC), this could bring Alpha system prices down to the \$1500 range. The Alpha would be a mass-market product, such as the x86.

"The Alpha will benefit from the economies of scale of having a large-volume

infrastructure," says Aaron Bauch, Digital's technical marketing manager.

Some observers wonder if the industry will support two or more different CPU interfaces that require different motherboards and core-logic chips. A few years ago, that would have been a major concern. But the industry has grown so large that companies can profitably support multiple standards.

"It's no big deal to design a custom motherboard for different CPUs," says Don Clegg, vice president of marketing for Tyan Computer, a major motherboard manufacturer. "But we'd like to see the motherboard form factors remain industry-standard: AT, ATX, NLX. If the board doesn't fit a standard chassis, it will become more like the notebook market."

There are other considerations that might determine how many companies support AMD's slot. Tyan won't say if it plans to build Slot A motherboards but notes that it enjoys good relations with Intel and would like to keep it that way.

On the other hand, Intel's encroachment into the motherboard and core-logic business is squeezing some companies out of the market. Therefore, they may have little choice but to support an alternative.

AMD's plan could have a greater chance of succeeding if other x86 vendors also adopt EV-6. Digital says it's willing to license the technology to anyone. However, Cyrix told BYTE it will not use EV-6. Instead, Cyrix hints it may clone Intel's P6 interface, despite the scary patents. Cyrix was recently acquired by National Semiconductor, and National has a patent cross-licensing agreement with Intel. Cyrix thinks that agreement might cover the P6 interface. If Intel sees things differently, Cyrix could fight it out in court.

"I don't intend to lose," says Steve Tobak, vice president of corporate marketing for Cyrix. "We've never lost in court to Intel before."

The third independent vendor of x86 processors, Centaur Technology, isn't talking about its plans beyond Socket 7. It's possible that Centaur could stick with the socket longer than others, because Centaur aims for the low-end market, where Socket 7 is not really a handicap.

Can AMD and Digital succeed in establishing a viable alternative to Intel's P6 standard? There's a good chance they could pull it off. AMD captured about 10 percent of the x86 market in 1997. That's down from 30 percent in 1992, when AMD's 386 competed strongly with Intel. But with the market expanding beyond 100 million units a year, even 10 percent could be enough to sustain Slot A.

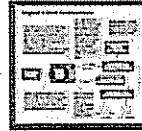
AMD has grander ambitions, though. Jerry Sanders says AMD must recapture about 30 percent market share to pay for the expensive R&D and chip foundries required to compete with Intel in the future.

That will be much more difficult to achieve, unless the swing to lower-priced PCs cuts deeply into Intel's high-margin business. Intel's profit margins are soaring above 60 percent -- higher than Apple's in the 1980s. If sub-\$1000 systems continue to grow in popularity, Intel will have to sacrifice either profit margins or market share.

It's a balance of technology and business. Intel may choose to preserve its current business model, keep its shareholders happy, and allow AMD to recapture the market share it enjoyed in the heyday of the 386.

Digital's EV-6 Architecture

[illustration link \(42 Kbytes\)](#)



Intel's CPU slots make it easier to install upgrades, but they'll also make millions of Socket 7 motherboards obsolete.

Upgradable or Obsolete?

[photo link \(90 Kbytes\)](#)



Intel's CPU slots make it easier to install upgrades, but they'll also make millions of Socket 7 motherboards obsolete.



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EXHIBIT 6

REDACTED IN ITS ENTIRETY

EXHIBIT 7

**INTEL WORLDWIDE MANUFACTURING AND ASSEMBLY/TEST SITES
AT A GLANCE**

	FACILITY NAME	YEAR BUILT	PRODUCTS	CURRENT PROCESS TECHNOLOGY	WAFER SIZE (mm)	Clean Room KSq. Feet	FUTURE PLANS
Fab Sites							
Chandler, Arizona	Fab 12	1996	Logic	65 nanometer	300 mm	210	
	Fab 22	2001	Logic	0.13 micron	200mm	150	
	Fab32	Under con- struction	Logic	45 nanomegler	300mm	171	Production expected 2007
Santa Clara, California	D2	1988	Flash, comms, cellular and handheld product development	0.13-micron, 90 nanometer,	200 mm	204	65nm by end of 2006
Colorado Springs, Colorado	Fab 23	2001	Communications Products	0.13 micron	200 mm	161	300mm wafer preparation being added in 2006
Leixlip, Ireland	Fab 10/14	1993/ 1998	Logic/Flash	0.35 micron, 0.25 micron, 0.18 micron, 0.13 micron	200 mm	195	No change
	Fab 24	2004	Logic	90-nanometer	300 mm	224	65nm production in early 2006
	Fab 24-2	2005		65-nanometer			
Jerusalem, Israel	Fab 8	1985	Legacy logic & MEMS	0.35-micron, 0.50-micron, 0.70-micron, 1.0- micron	150 mm	54	
Qiryat Gat, Israel	Fab 18	1999	Logic/Flash	0.18 micron, 90 nanometer	200 mm	107	.018 micron phase out in 2006
	Fab 28	Under con- struction	Logic	45 nanometer	300mm	200	Production expected 2008
Hudson, Massachusetts	Fab 17	1994	Logic	0.13-micron	200 mm	117	Reconfigura- tion to increase capacity to be complete in 2006
Rio Rancho, New Mexico	Fab 11	1993	Flash, cellular and handheld	0.13 micron	200 mm	303	mod 4 converting to 300mm in 2006
	Fab 11X	2002	Logic	90-nanometer	300 mm	243	will annex F11 mod 4 in 2006

**INTEL WORLDWIDE MANUFACTURING AND ASSEMBLY/TEST SITES
AT A GLANCE**


FACILITY NAME	YEAR BUILT	PRODUCTS	CURRENT PROCESS TECHNOLOGY	WAFER SIZE (mm)	Clean Room	FUTURE PLANS
Hillsboro, Oregon						
D1C	1999	Logic Development	90 nanometer	300 mm	150	65 nanometer in late 2006
Fab 20	1996	Logic	0.13-micron	200 mm	140	
D1D	2003	Logic Development	65 nanometer, 45 nanometer	300 mm	212	45 nanometer in 2007
Assembly Test Sites						
Cavite, Philippines						
CV1	1997	Logic and communications	N/A	200 mm	268	
CV2	1998	Flash memory	N/A	200 mm	149	
PD1	1997	Flash memory	N/A	200 mm	50	
PD2	2001	Logic Products	N/A	200 mm	152	
				300 mm		
CD1	2004	Logic Products	N/A	200 mm	170	
				300 mm		
CD6	Under construction			200 mm	177	Starts Ramp in 2007
				300 mm		
Penang, Malaysia						
PG6	1988	Logic and communications	N/A	200 mm	96	
PG7	1994	Logic and communications	N/A	200 mm	115	
PG8	1997	Logic Products	N/A	200 mm	171	Low cost expansion conducted in 2005
				300 mm		
Kulim, Malaysia						
KM1	1996	Logic Products		200 mm	103	
				300mm		
KM2	1997	Logic Products and Board Manufacturing		200mm	110	
				300mm		
KM5	Under construction	Communications and Logic Products	N/A	200 mm	225	Starts ramping end of 2007
				300 mm		
San Jose, Costa Rica						
CR1	1997	Logic Products	N/A	200 mm	152	Expanded in 2H 2005
				300 mm		
CR3	1999	Logic Products	N/A	200 mm	197	
				300 mm		
Fab7-T	Renovation began 2005	Various	N/A	200 mm	43	Operation anticipated early 2006 for about two years
				300 mm		
Ho Chi Minh City, Vietnam						
SS1	Under construction	Logic Products	n/A		254	Operation anticipated 2008
				300mm		

EXHIBIT 8

REDACTED IN ITS ENTIRETY

EXHIBIT 9

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Resources

Intel chief executive confirms massive \$12bn spending promises for this year

Archived by: 7 March 2009

Intel chief executive confirms massive \$12bn spending promises for this year Richard Ball
Despite doom-laden predictions of a downturn in the chip market, Intel is sticking with plans to spend \$12bn this year on chip making tools and in research and development.

Chief executive Craig Barrett reiterated his massive spending promises at last week's Intel developer forum (IDF), the firm's twice-yearly technology conference.

"Intel will spend nearly \$12bn this year on R&D and new manufacturing capacity," Barrett confirmed. The split is expected to be around \$7.5bn on capital equipment and \$4.3bn on R&D.

"This year alone we will begin producing 300mm wafers, introduce copper metalisation, ramp 0.13µm technology and deploy a host of other technologies," he added.

Barrett made light of a possible recession in the market. "I've been in this industry for about 27 years, and we've been through a number of these cycles... And what we really have to do is prepare for the next upswing," he said.

"The simple way to be prepared for the upswing is that you never save your way out of a downturn."

Amongst a swathe of other announcements at IDF, Intel expanded its push into communications silicon by announcing seven optical networking devices.

These include two forward error correction chips and four physical layer chips for 10Gbit/s optical networks.

The firm also plans to make further inroads into the wireless Internet market, and showed off its Web Tablet.

Powered by a StrongARM processor, the device runs the VxWorks operating system and applications are based on Java. The in-built Web browser and user interface come from Espial.

The Web Tablet is designed to interface to, and get its Internet connection from, a standard PC.

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EXHIBIT 10

REDACTED IN ITS ENTIRETY

EXHIBIT 11



TECHNOLOGY

MirrorBit® Technology

MirrorBit® ORNAND™ Architecture

MirrorBit® Eclipse™ Architecture

MirrorBit® Quad Technology

Manufacturing Technology

▶ Fabrication Facilities

Assembly, Test, Mark and Pack Facilities

Automated Precision Manufacturing (APM)

Manufacturing Fabrication Facilities (Fabs)

SpanSion® maintains world-class manufacturing facilities, known as "fabs," across North America and Asia. In every SpanSion facility, we use advanced decision-making and control technologies to optimize, integrate and automate material processing at nearly every stage in the manufacturing process. We have one research and development fab, the Submicron Development Center, and three production fabs. Additionally, we have agreements in place with leading-edge foundries.

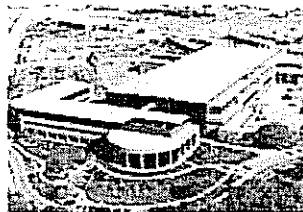
Submicron Development Center (SDC)



The Submicron Development Center (SDC) is located in Sunnyvale, California and supports advanced process technology, research and development efforts utilizing some of the most advanced in semiconductor manufacturing equipment. In addition, the SDC works closely with primary manufacturing facilities to help ensure smooth transfer of process technology into volume production.

*"Fab 25 produces the Flash memory solutions that are enabling SpanSion to redefine the NOR Flash memory industry. Since its conversion from a logic fab to Flash in 2002, we have moved process nodes from 170nm to 65nm—an impressively fast rate of approximately one node per year. We armed a leading-edge, flexible- design fab with innovative Automated Precision Manufacturing technology and dedicated, creative people and got terrific results."
— Jim Doran, Executive Vice President and Chief Operating Officer*

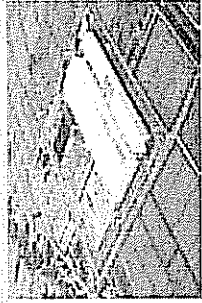
Fab 25



Fab 25 is a major presence on the southeast side of Austin, Texas. With more than 120,000 square feet of Level 1 clean room space, Fab 25 manufactures SpanSion's state-of-the-art MirrorBit® Flash memory solutions on 65nm and 90nm process technology and MirrorBit® Quad memory solutions on 90nm, with plans to add 65nm

by the end of 2007.

SpanSion SP1

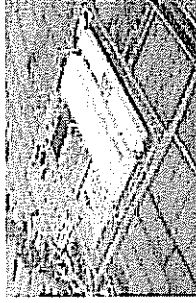


SP1 is the first fab built by Spansion as an independent company and is the industry's

first 300mm NOR Flash Memory Facility. SP1 is co-located and shares certain resources with Spansion's other facility in Aizu, JV3.

By leveraging this next-generation facility, and cost advantage and technology advantages of MirrorBit technology, Spansion can deliver on our promise to bring more value to customers by producing differentiated products and redefine the Flash memory industry. Spansion plans to begin producing 65nm MirrorBit® products by the end of 2007, followed by 45nm.

Spansion JV3



JV3, also located in Aizu-Wakamatsu, Japan, is Spansion's primary producer of 110nm MirrorBit devices on internal aluminum metal layer technology. Other current and legacy devices can also be manufactured there. Built during the joint venture between AMD and Fujitsu, this fab has approximately 118,000 square feet of Level 1 clean room space.

EXHIBIT 12

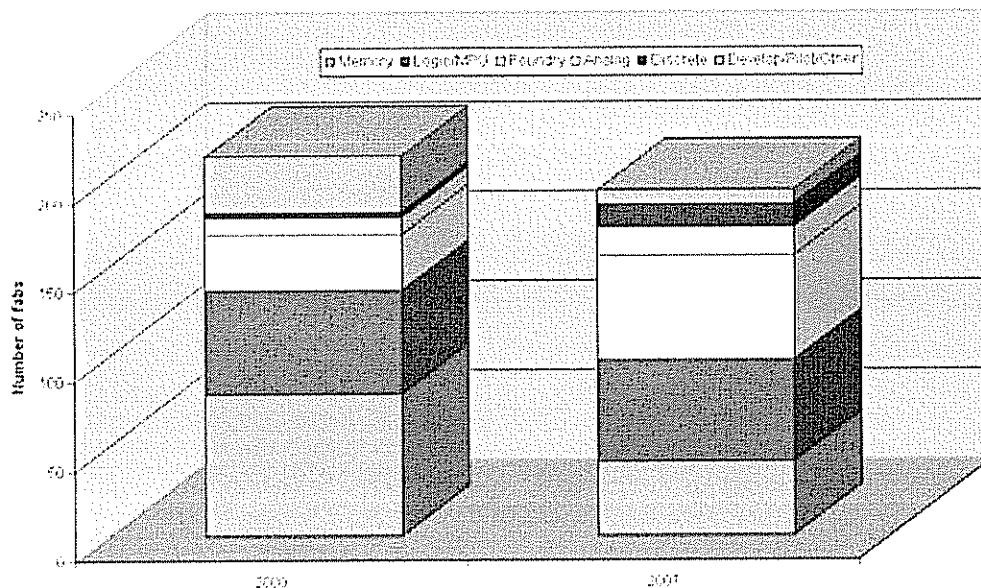
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Fab Repurposing Raises New Opportunities

Thomas Morrow, SEMI Vice President Global Expositions and Marketing, SEMI, San Jose -- Semiconductor International, 6/20/2008

Although new 300 mm fabs dominate the headlines, 200 mm fabs continue to do much of the heavy lifting in the global semiconductor market. In fact, 200 mm wafer capacity still exceeds 300 mm capacity in equivalent units (though 300 mm capacity is expected to surpass worldwide 200 mm wafer by year end) According to the SEMI World Fab Capacity Report, the number of 200 mm fabs has decreased from 213 to 193 from 2000 to 2007 (Figure), but total 200 mm wafer capacity has increased 42% to 5.54 million wafers per month over the same period, indicating the significant productivity gains possible in older device geometries

200 mm Fabs Worldwide



Many of these fabs continue to thrive because they have effectively adapted to new product strategies and incorporated new production solutions. Many of these adaptations have included radical repurposing of production lines. Previously dedicated to logic, memory and other products, many 200 mm fabs have been repurposed to foundry applications. Other 200 mm fabs are being repurposed or upgraded to support growth in the analog and discrete markets.

Spansion's Fab 25 in Austin, Texas, illustrates a common lifecycle of technology transitions and product mix changes. Fab 25 produced its first silicon in 1995, an AMD 486 processor fabricated with 0.35 μm technology. AMD managed Fab 25 through 0.25 and 0.18 μm nodes through 2002, when the fab was converted to memory production with ~\$500M in capacity and technology improvements. Since 2002, Fab 25 has implemented 170, 130, 110, 90 and 65 nm nodes and transitioned from aluminum to copper interconnects. AMD's current production strategy is to introduce new products through Fab 25, then moving volume to its new 300 mm plant in Japan. Since 2001 and covering the logic to flash transition, Fab 25's output increased 181%, while total expenses have been reduced to only 61% of 2001 levels.

Conversion to MEMS is another possible option for legacy fabs. Bosch announced 200 mm wafer-size conversion to its MEMS project. Scheduled to begin production in 2009, it will include 4600 m² of cleanroom space and reach 800 wafer/day capacity output. Advanced CMOS, HV-CMOS and MEMS processes will run in the new facility, initially down to 0.8 µm, with plans to push to 0.18 µm.

Some fab repurposing has been accomplished to support the concept of "the agile fab," consisting of reduced cycle time and the cost of operation and moving to high-product-mix manufacturing. Multi-function and multi-task furnace, dry etching, wet cleaning, ion implantation and other tools add flexibility to production operations. Fab automation implementations in 200 mm have also enabled increasingly agile fabs.

"Priority No. 1 in the industry has to be reducing cycle time," said Areih Lev Greenberg, senior principal at Qimonda AG (Munich, Germany). He stressed that cycle time rules because it leads to faster introduction of new products, product delivery to customers, and time to money. In addition, he said, it mitigates risk by reducing average selling prices (ASPs) and the impact of excursions due to faster response.

"New technologies lead to an increased number of litho mask layers and degradation of factory cycle time," Greenberg said, requiring breakthrough approaches to continuously reduce cycle time. He sees the future with simpler, smaller tools replacing the inherently complicated tools. He also believes that reduced tool setup times and standard lot size changes will make a big difference.

AMD has been implementing several fab agility, productivity and repurposing efforts under the name of LEAN manufacturing, first implemented at its 200 mm Fab 30. Doug Grose, senior vice president of manufacturing, process technology development and supply chain at AMD, sees "dramatic improvements in efficiency and productivity at AMD through aggressive and consistent process improvement using LEAN methodologies."

In addition to preventive maintenance and other cost reduction efforts, many of AMD's productivity and flexibility gains have been achieved through new work flow layout. According to Grose, lot travel distance has been reduced from 925 m to 363 m (>60% reduction); lead time variability went from 2.86 days to 0.83 days (71% reduction); and lead time went from 4.21 days to 2.64 days (37% decrease).

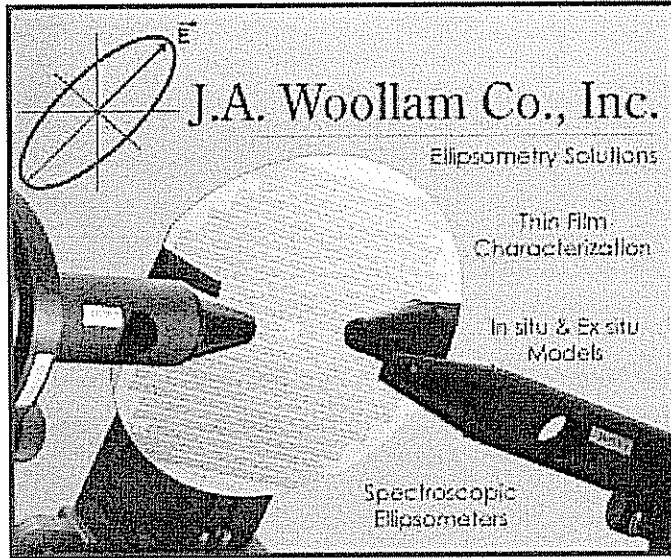
In December, ISMI/Sematech announced a 19-point Next Generation Factory (NGF) Program to answer the industry's pressing need for lower costs and reduced cycle time. The 300 mm program includes setup reduction, small lot size and other features to support flexible, high-mix production. While focused on 300 mm, some of the work will be transportable to older 200 and 150 mm factories. The SEMI Equipment Productivity Working Group (EPWG) was established to work with ISMI to help guide investment prioritization across the industry/food chain in next-generation factory technologies.

At SEMICON West 2008, a special forum is dedicated to fab upgrades and repurposing. The forum, "How to Breath New Life Into Old Fabs," will be on Tuesday, July 15, at 12:30-5:30 p.m. at Yerba Buena Center for the Arts. For additional information, visit www.semiconwest.org.

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The advertisement features a central graphic of a globe with a grid of latitude and longitude lines. To the left of the globe is a technical diagram of an ellipse with a vertical axis labeled 'E'. Below the globe, two dark, mechanical-looking components are shown, resembling parts of an ellipsometer. The background is a light gray with a fine, repeating pattern of the company name.

EXHIBIT 13

REDACTED IN ITS ENTIRETY

EXHIBIT 14

REDACTED IN ITS ENTIRETY

EXHIBIT 15

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EXHIBIT 16

REDACTED IN ITS ENTIRETY

EXHIBIT 17

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