IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

IN RE INTEL CORPORATION MICROPROCESSOR ANTITRUST LITIGATION	)))	MDL No. 05-1717-JJF
	)	
ADVANCED MICRO DEVICES, INC. and AMD INTERNATIONAL SALES & SERVICE, LTD.,	))))	C.A. No. 05-441-JJF
Plaintiffs,	)))	
v.	))	
INTEL CORPORATION and INTEL KABUSHIKI KAISHA,,	))))	
Defendants.	))	
PHIL PAUL, on behalf of himself and all others similarly situated,	))))	C.A. No. 05-485-JJF
Plaintiffs,	))))	
vs.	))))	
INTEL CORPORATION,	))	
Defendant.	)	

NOTICE OF TAKING DEPOSITION OF
ADVANCED MICRO DEVICES, INC. AND
AMD INTERNATIONAL SALES & SERVICE, LTD.
(AMD MANUFACTURING DATA)

PLEASE TAKE NOTICE that, pursuant to Rule 30(b)(6) of the Federal Rules of

Civil Procedure, defendant Intel Corporation and Intel Kabushika Kaisha will take the

deposition of Advanced Micro Devices, Inc. and AMD International Sales & Service, Ltd.

on June 4, 2009 beginning at 9:00 a.m., at the offices of Gibson Dunn & Crutcher LLP, 333

South Grand Avenue, Suite 4700, Los Angeles, California 90071, or at such other time and

place as the parties may agree. The deposition will be recorded by stenographic and sound-and-visual (videographic) means, will be taken before a Notary public or other officer authorized to administer oaths, and will continue from day-to-day until completed, weekends and public holidays excepted.

Reference is made to the "Description of Matters on Which Examination is Requested" attached hereto as Exhibit A and incorporated herein by this reference. In accordance with Rule 30(b)(6) of the Federal Rules of Civil Procedure, AMD is hereby notified of its obligation to designate one or more officers, directors, or managing agents (or other persons who consent to do so) to testify on its behalf as to all matters embraced in the "Description of Matters on Which Examination is Requested" and known or reasonably available to AMD.

OF COUNSEL:

POTTER ANDERSON & CORROON LLP

By: /s/ W. Harding Drane, Jr.

Robert E. Cooper
Daniel S. Floyd
Gibson, Dunn & Crutcher LLP
333 South Grand Avenue
Los Angeles, CA 900071
(213) 229-7000

Darren B. Bernhard
Howrey LLP
1299 Pennsylvania Avenue, N.W.
Washington, DC 20004
(202) 783-0800

Dated: April 13, 2009
911631/29282

Richard L. Horwitz (#2246)
W. Harding Drane, Jr. (#1023)
Hercules Plaza, 6th Floor
1313 N. Market Street
P.O. Box 951
Wilmington, DE 19899-0951
(302) 984-6000
rhorwitz@potteranderson.com
wdrane@potteranderson.com

Attorneys for Defendants
Intel Corporation and Intel Kabushiki Kaisha

EXHIBIT A

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DESCRIPTION OF MATTERS ON WHICH EXAMINATION IS REQUESTED

I. DEFINITIONS

1. "AMD" shall mean and refer collectively to plaintiffs Advanced Micro Devices, Inc. and AMD International Sales & Service, Ltd., including their respective past and present officers, directors, agents, attorneys, employees, consultants, or other persons acting on either of their behalf.

2. "AMD databases" means all databases, electronic tools, files, or other internal systems that reference, contain, list, record, document, and/or process the manufacture, storage or shipment of x86 microprocessor products sold by AMD, including but not limited to the fabrication, assembly, test, inventory and distribution processes whether at an AMD-owned facility or a third party facility. Such databases encompass those already produced in this litigation or that are the subject of ongoing discussions between the parties. The AMD databases also include the Business Operations Forecast ("BOF") and the OARS database.

II. SUBJECT MATTER

1. The origin, existence, location, and structure of AMD databases.

2. General knowledge of AMD's policies and/or procedures for entering, processing, recording, moving and deleting data in or from AMD databases.

3. The definition and interpretation of data fields, values, abbreviations, and codes in AMD databases.

4. Documents or data maintained or recorded by AMD to inform, describe, or relate to entries made in AMD's databases, or to validate entries for any purpose.

5.   The business and operational practices employed by AMD to record data in the AMD databases, including what information is used to determine any subsequent adjustments.

6.   The existence of automated or manual linking procedures and other possible interactions among AMD databases.

7.   AMD's responses, including the interpretation and clarification of responses, previously produced in response to Intel's questions regarding AMD's databases.

8.   The manufacturing data that AMD has produced to Intel in this case.

9.   The data and methodology AMD uses to calculate any measure of yield, including but not limited to any yield that AMD has documented in its internal reports or in any external statements.

10.   The data and methodology AMD uses to calculate or forecast the demand for its x86 microprocessors, including but not limited to an explanation of how AMD uses the BOF, OARS and any other databases to determine how many x86 microprocessors to manufacture and on what schedule.

11.   For each wafer start, whether meant for commercial sale or for an other purpose such as engineering, development, qualification or distribution of samples, on which AMD x86 microprocessors were manufactured at any point between 1996 and the present:

   (a) the facility in which that wafer start was run;

   (b) the identity of each type of x86 microprocessor die manufactured, including but not limited to the model name or number, speed and "OPN" (or "SKU" or any other identifying information) on that wafer;

(c) the quantity of each type of x86 microprocessor die manufactured on that

wafer;

(d) the date(s) on which the wafer was run in the facility;

(e) whether that wafer resulted in a wafer out;

(f) the sort data for each wafer out, including but not limited to information

regarding saleable versus non-saleable die, down-binned or down-cached die,

and otherwise saleable die that was not sold or sent to assembly due to poor

frequency, cache defects or any other defects;

(g) the generation and type of logic process technologies used, at the most

detailed level available, in processing that wafer; and

(h) for any wafer start not meant for commercial sale, whether the wafer start was

a "full flow" run or a "short flow" run.

12.   For each facility in which AMD x86 microprocessors were assembled at

any point between 1996 and the present, for each wafer containing x86 microprocessor

die received by the facility:

(a) the number of die that are not affixed to a package at any point in time;

(b) for each die not affixed to a package, the identity of the die including but not

limited to the model name or number, speed and "OPN" (or "SKU" or any

other identifying information);

(c) the number of die that are affixed to a package but never sent to a test facility;

(d) for each die/package combination that is never sent to a test facility, the date

of assembly, the identity of the package, and the identity of the die including

but not limited to the model name or number, speed and "OPN" (or "SKU" or

any other identifying information);

(e) for each die/package combination never sent to a test facility, the final disposition of the combination and the date of such disposition;

(e) the number of die that are affixed to a package and sent to a test facility;

(f) for each die/package combination that is sent to a test facility, the date of assembly, the date on which the combination is sent to a test facility, the identity of the package and the identity of the die including but not limited to the model name or number, speed and "OPN" (or "SKU" or any other identifying information);

13. For each facility in which AMD x86 microprocessors were tested at any point between 1996 and the present, for each x86 microprocessor die/package combination received by the facility:

(a) the dates(s) on which the combination was tested;

(b) whether combination was approved to be marked and packed;

(c) for each combination approved to be marked and packed, the date on which it was marked, the date on which it was packed, how the microprocessor is marked, including but not limited to the model name or number, speed and "OPN" (or "SKU" or any other identifying information);

(d) for each combination that was not approved to be marked, the final disposition of the combination and the date of such disposition;

(e) for each combination that is not approved to be packed, the final disposition of the combination and the date(s) of such disposition

14. For each microprocessor marked and packed by AMD between 1996 and the present, the identity of each facility to which that microprocessor was shipped until it

was sent to a customer, including but not limited to the length of time the microprocessor resided in each facility and the nature or description of each facility.

15. The data and methodology needed to replicate AMD's categorization of items as being part of WIP, die bank, FUM, or finished goods inventory.

16. The data and methodology needed to determine the number of wafer starts, wafer outs, assembly outs, net die per wafer, die to ship, other measures of yield and any metric maintained by AMD in the ordinary course of business regarding AMD's manufacturing, assembling, testing, inventorying or distributing of each of AMD's x86 microprocessor products.

17. AMD's purchase requirements for the tools and equipment necessary for AMD to manufacture its flash and logic products; the purchase details of these tools and equipment; the maintenance schedules and maintenance costs for these tools and equipment; and the purchase lead times for and the life spans of these tools and equipment.

18. The components purchased by AMD for the manufacture of its flash and logic products, including but not limited to wafers, chemicals, packages and package components; and the purchase lead times for and inventories maintained by AMD of these components.

19. The names and positions of AMD employees who would be knowledgeable of the matters listed above, and the departments, groups, or business units within AMD that are responsible or knowledgeable of the matters listed above.

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

CERTIFICATE OF SERVICE

I, W. Harding Drane, Jr., hereby certify that on April 13, 2009 the attached

document was hand delivered to the following persons and was electronically filed with

the Clerk of the Court using CM/ECF which will send notification of such filing(s) to the

following and the document is available for viewing and downloading from CM/ECF:

Jesse A. Finkelstein
Frederick L. Cottrell, III
Chad M. Shandler
Steven J. Fineman
Richards, Layton & Finger
One Rodney Square
920 North King Street
Wilmington, DE 19801

James L. Holzman
J. Clayton Athey
Prickett, Jones & Elliott, P.A.
1310 King Street
P.O. Box 1328
Wilmington, DE 19899

I hereby certify that on April 13, 2009, I have electronically mailed the documents

to the following non-registered participants:

Charles P. Diamond
Linda J. Smith
O'Melveny & Myers LLP
1999 Avenue of the Stars, 7th Floor
Los Angeles, CA 90067
cdiamond@omm.com
lsmith@omm.com

Salem M. Katsh
Laurin B. Grollman
Kasowitz, Benson, Torres & Friedman LLP
1633 Broadway, 22nd Floor
New York, New York 10019
skatsh@kasowitz.com
lgrollman@kasowitz.com

Mark A. Samuels
O'Melveny & Myers LLP
1999 Avenue of the Stars, 7th Floor
Los Angeles, CA 90067
msamuels@omm.com

Michael D. Hausfeld
Daniel A. Small
Brent W. Landau
Cohen, Milstein, Hausfeld & Toll, P.L.L.C.
1100 New York Avenue, N.W.
Suite 500, West Tower
Washington, DC 20005
mhausfeld@cmht.com
dsmall@cmht.com
blandau@cmht.com

Thomas P. Dove
Alex C. Turan
The Furth Firm LLP
225 Bush Street, 15th Floor
San Francisco, CA 94104
tdove@furth.com
aturan@furth.com

Guido Saveri
R. Alexander Saveri
Saveri & Saveri, Inc.
111 Pine Street, Suite 1700
San Francisco, CA 94111
guido@saveri.com
rick@saveri.com

Steve W. Berman
Anthony D. Shapiro
Hagens Berman Sobol Shapiro, LLP
1301 Fifth Avenue, Suite 2900
Seattel, WA 98101
steve@hbsslaw.com
tony@hbsslaw.com

Michael P. Lehman
Cohen, Milstein, Hausfeld & Toll, P.L.L.C.
One Embarcadero Center, Suite 526
San Francisco, CA 94111
mlehmann@cmht.com

By: /s/ W. Harding Drane, Jr.
      Richard L. Horwitz (#2246)
      W. Harding Drane, Jr. (#1023)
      POTTER ANDERSON & CORROON
      LLP
      Hercules Plaza, 6th Floor
      1313 N. Market Street
      P.O. Box 951
      Wilmington, DE 19899-0951
      (302) 984-6000
      rhorwitz@potteranderson.com
      wdrane@potteranderson.com