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Demo Sheet

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Demonstrations of the 48-core Research Prototype

Dec. 2, 2009 — Below are summary of demonstrations from Justin Rattner's presentation at the announcement of the 48 core "Single-chip Cloud Computer".

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Financial Analytics using Software-Coordinated Memory Technology
Black-Scholes is a standard application and method used to calculate the value of stock options by predicting their future performance. Wall Street financial advisors often run 1000s of Black-Scholes calculations in parallel to evaluate 1000s of possible market scenarios in order to make the best decisions for their client. In order to produce results quickly for the fast-paced market, many computers are required to be running in parallel. This is a key application for future many-core processors, both for the competitive financial services industry as well as amateur day-traders that want to manage their own investments. Intel researchers demonstrated the Black-Scholes running on the 48 core prototype and proved good results.

- All the cores act as if they share a single block of memory so that they can work together more effectively, thanks to the experimental, software-based memory sharing technology.
- Software coordinates data reads/writes between the all the memory caches across the chip – a technique called "cache coherence" that is done in hardware today, without the aide of software.
- Intel Labs believes this software based approach could increase the performance and energy-efficiency of future many-core chips by eliminating the need for this hardware memory management.
- The memory sharing technology enables programmers to pick how they want to program the chip – either the traditional, shared memory approach of processors today, or the cluster based message passing approach of data-centers. It can do either, or both – very flexible.

Programming for the 3D Internet: JavaScript Server Farm on a Chip
As Justin Rattner emphasized in his Supercomputing 2009 keynote in November, the Internet is poised to transition from flat, 2D experiences to more immersive 3D experiences. Bringing real world physics to 3D graphics is essential to making these emerging online interactions true-to-

life. For instance, realistic, physics-based cloth modeling could enable both virtual clothing design as well as virtual dressing rooms that allow you to "try out" clothes on your virtual body and see how they would actually fall on you and match your specific skin tone. Intel Labs have demonstrated JavaScript, the language used broadly to create interactive web pages, taken to new levels of capability. Although JavaScript is used in every browser, it's mainly used to operate very simple tasks like processing web forms and has performance problems running more complicated activities. JavaScript has been underutilized until now due to the lack of programming environment. Intel Labs have worked on a programming model that allows better utilization, takes better advantage of newer and future high-core count processors, and can be immediately deployed without requiring any modifications to the underlying infrastructure.

- By treating the prototype chip as a "server farm" the chip is able to divide the work involved in calculating the motion of interactive cloth.
- Researchers use the "Actor" model, commonly used in server farms, which treats each core as an independent worker to own and process one piece of the cloth.
- Leveraging the standard HTTP web protocol, the browser distributes pieces of the cloth across the actor server farm, allows them to calculate the location of their piece of the cloth at the next time step, collects the results, and displays the combined image.

Scalability through "Message Passing": Linear Algebra and Fluid Dynamics

"Message Passing" is the idea of sharing data by passing messages directly to other processors over a network rather than reading and writing to a pool of shared memory. As a programming model, it is a proven method to build reliable applications that scale to 100's or even 1000's of processors in clusters and datacenters today. We show how the message passing environment, created by Intel Labs, enables this kind of scalability on a many-core processor using standard workloads from the high-performance computing community which stress message passing: the solving of linear equations and the simulation of fluid dynamics.

- The message passing environment technique on this chip is exposed directly to an application developer, bypassing even the operating system for the most hard core programmer.
- Programmers can use this environment to maximize performance by moving messages across the network of cores with extremely low latencies and high bandwidths.
- Intel demonstrated three different communication patterns, proving the scalability available on the chip and the core functionality needed in a communication environment to upport a wide variety of higher level programming models and datacenter middleware packages.

Energy Efficiency with Real-time Advanced Power Management

The experimental chip was designed to operate from as high as 125W to as low as 25W by providing a variety of advanced capabilities to manage power consumption. Power use is largely determined by the cores' clock speeds and operating voltages. The chip has a unique ability to mix and match voltages and clock speeds for the different cores, or even to turn off entire regions of the chip when not needed. These capabilities can be controlled by software, allowing the application or operating system to intelligently manage power consumption, adapting in real time to use only the energy that is really needed. The demonstration displays how power levels for

different sections of the chip change in response to the needs of a series of tasks whose power requirements vary over time. The tasks of the application are modeled after parallel computations.

Cloud Programming on a Chip: Hadoop Web Search

One of the main benefits of the single chip cloud computer is to provide a prototype that runs highly parallel software on a chip using methods that have already been proven to work well for cloud computing and datacenters, requiring minimal work for programmers, a common challenge when going to a many-core model. Intel demonstrated Apache Hadoop running on the new experimental chip without any significant changes required by the developer.

- Hadoop is an open-source Java software framework based on Map/Reduce that enables applications to work with thousands of processors and petabytes of data.
- Hadoop can be used for indexing an array of web pages using Map/Reduce by first "mapping" the work into smaller tasks assigned to worker cores, then collecting the results of the worker and "reduce" them to a single result, indexing all of the related pages. Here it is shown grouping related objects using an approach that can automatically categorize text documents, such as web pages, as part of an indexing process.
- For example, search engines use this technique to divide the work of scouring the world and sorting web pages by different search terms.
- Searching web pages, an application that most people use every day, and "Map/Reduce," an algorithm used to index those web pages across clusters of distributed computers, have broader applications such as machine learning and natural language translation.

Microsoft Visual Studio + SCC Message Passing Environment

Bringing parallel programming to mainstream software developers is one of the main goals of Intel's Tera-scale research program. Microsoft Visual Studio is a widely popular software development environment that can also be used for developing parallel applications to run on the SCC many-core platform.

- Visual Studio 2008 is demonstrated working together with Intel's research SCC message passing environment.
- This allows programmers to directly take advantage of the cloud-like message passing architecture of SCC.
- Proves how easy it is for a programmer to setup a project, edit, compile and run applications that take advantage of the unique features of the experimental SCC.