Intel® Carrier Grade Server TIGI2U

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Date	Revision Number	Modifications
August 2005	1.0	Initial release.
November 2007	1.1	Corrected system board identification
January 2008	1.2	Corrected non-operating temperature value in Table 7 (page 36)

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1. Introduction

This document provides an overview of the Intel® Carrier Grade Server TIGI2U and includes information on chassis hardware, cables, connectors, Intel® server board SE7520JR2, system boards, power subsystem, and regulatory requirements.

1.1 Document Structure and Outline

This document is organized into the following chapters:

Chapter 1: Introduction
Provides an overview of this document.

Chapter 2: System Overview
Provides an overview of the Intel® Carrier Grade Server TIGI2U chassis hardware.

Chapter 3: Cables and Connectors
Describes the cables and connectors used to interconnect the system board set and the server system components.

Chapter 4: Front Panel/SCSI Backplane Board
Describes the specifications of the front panel/SCSI backplane board.

Chapter 5: CD-RW/DVD/SysCon Interface Board
Describes the specifications of the CD-RW/DVD/SysCon interface board.

Chapter 6: PCI-X Riser Board
Describes the specifications of the PCI-X riser board.

Chapter 7: DC Power Subsystem
Describes the specifications of the DC power subsystem.

Chapter 8: AC Power Subsystem
Describes the specifications of the AC power subsystem.

Chapter 9: Regulatory Specifications
Describes system compliance to regulatory specifications.

2. System Overview

This chapter describes the features of the Intel® Carrier Grade Server TIGI2U chassis.

2.1 System Features

Table 1 provides a list and brief description of the features of the TIGI2U Carrier Grade Server.

Table 1. Intel® Carrier Grade Server TIGI2U Feature List

Feature	Description	
Compact, high-density system	Rack-mount server with a height of 2U (3.5 inches) and a depth of 20.0 inches	
Configuration flexibility	1 or -2 way capability in low profile and cost/value effective packaging Stand-alone system 800 MHz Front Side Bus (FSB) Intel® Xeon™ processor support up to 3.2 GHz	
Serviceability	Back access to hot-swap power supplies Front access to hot-swap disk drives Front access to blind-mate CD-RW/DVD Carrier Module	
Availability	Two hot-swap 600 W power supplies in a redundant (1+1) configuration Zero Channel RAID ready (requires Intel SRCZCRX PCI adapter) to provide RAID 1 capability using two hot-swap SCSI disk drives. Memory online sparing and memory mirroring	
Manageability	Remote management Emergency management port (Serial and LAN) IPMI 1.5 compliant Remote diagnostics support	
Upgradeability and investment protection	Designed to support 800 MHz FSB Intel® Xeon™ processor family Multigenerational chassis Intel® Extended Memory 64 Technology (EM64T) support	
System-level scalability	16 GB DDR2-400 Registered SDRAM DIMM memory support Dual 800 MHz FSB Intel® Xeon™ processor support 3 Full Height Full Length 64-bit x 100/66 MHz PCI Slots 3 Low Profile / Half Length 64-bit x 100/66 MHz PCI Slots 2 internal hot-swap SCSI disk drives (SCA support) 1 Low Profile CD-RW/DVD drive	
Front panel	Power switch Reset switch NMI switch ID switch Main power LED HDD activity LED NIC activity LED ID LED	Hard Drive 1 Fault LED Hard Drive 2 Fault LED Telco power alarm fault LED/Relay Telco critical alarm fault LED/Relay Telco major alarm fault LED/Relay Telco minor alarm fault LED/Relay

2.2 Chapter Structure and Outline

This chapter is organized into the following sections. The content of each section is summarized as follows.

Section 2.3: Introduction
Provides an overview and block diagram of the TIGI2U Carrier Grade Server.

Section 2.4: External Chassis Features
Describes features of the Intel® Carrier Grade Server TIGI2U chassis in detail (buttons, switches, bezel, etc.).

Section 2.5: Internal Chassis Features
Provides an overview of the components of the Carrier Grade Server TIGI2U.

Section 2.6: Server Management
Describes the server management features of the Carrier Grade Server TIGI2U.

Section 2.7: Specifications
Summarizes the environmental and physical specifications of the Carrier Grade Server TIGI2U.

2.3 Introduction

The Carrier Grade Server TIGI2U is a compact, high-density, rack mount server system with support for one or two 800 MHz FSB Intel® Xeon™ processors and 16 GB DDR2-400 SDRAM DIMM memory. The TIGI2U supports high availability features such as hot-swap disk drives and hot-swap and redundant power supply modules. The scalable architecture of the TIGI2U supports symmetric multiprocessing (SMP) and a variety of operating systems (OS).

Figure 1 shows an isometric view of the system.

A. Power Supply	G. FPIO system board
B. PCI card bracket (full-length)	H. RJ45 COM2 and USB port
C. Riser card assembly (full and low profile)	I. Control Panel and Status Indicators
D. PCI card bracket (low-profile)	J. SCSI Hard Disk Drive Bays
E. Server board SE7520JR2	K. Peripheral Bay
F. System Fans	

Figure 2 shows the system with the top covers and the front bezel removed.

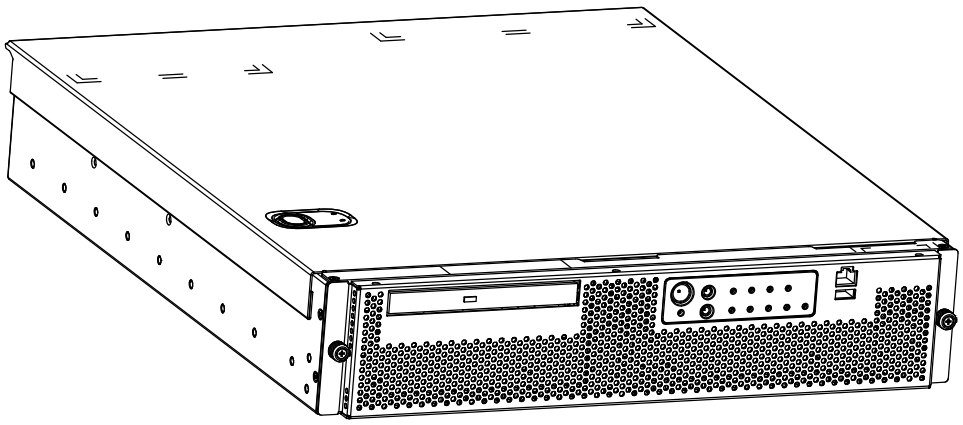
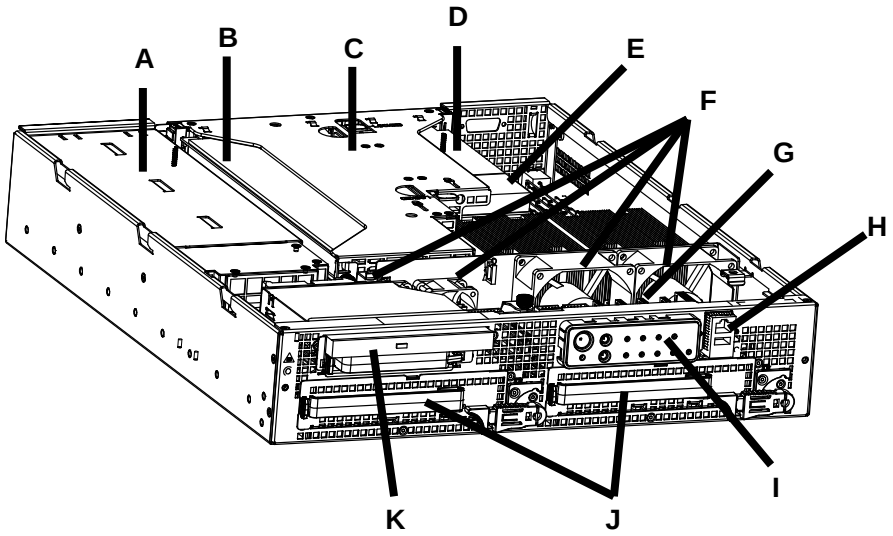


Figure 1. Intel® Carrier Grade Server TIGI2U

The Carrier Grade Server TIGI2U uses the Server board SE7520JR2, which contains dual processor slots for installing up to two 800 MHz FSB Intel® Xeon™ processors utilizing 604-pin zero insertion force (ZIF) processor sockets. The server board has 6 DIMM slots and supports up to 16 GB error checking and correcting (ECC) SDRAM memory. The Server board SE7520JR2 also contains 6 PCI slots (implemented via riser cards), input/output (I/O) ports and various controllers.



A. Power Supply	G. FPIO system board
B. PCI card bracket (full-length)	H. RJ45 COM2 and USB port
C. Riser card assembly (full and low profile)	I. Control Panel and Status Indicators
D. PCI card bracket (low-profile)	J. SCSI Hard Disk Drive Bays
E. Server board SE7520JR2	K. Peripheral Bay
F. System Fans	

Figure 2. Intel® Carrier Grade Server TIGI2U (shown with top cover and bezel removed)

The Carrier Grade Server TIGI2U server board SE7520JR2 is mounted horizontally toward the rear of the chassis behind the system fan array.

Up to two 1.0” Ultra-320* SCSI technology hard drives can be mounted in the hot-swap drive bays, which are located in the bottom front of the chassis. The front bezel must be removed to access the hot-swap drive bays. Figure 2 shows the location of the two hot-swap drive trays.

One peripheral drive can be mounted in the system using a blind-mate peripheral drive carrier inserted into the peripheral drive bay. The peripheral drive bay is located above the hard drive tray and to the left.

The Front Panel/SCSI I/O board (FPIO board) is located above the hard drive tray and provides user interface for the system front panel and for system management as well as SCSI backplane connectivity for the hot-swap drives.

The power supply modules (both AC-input and DC-input options are available) are installed at the left-rear of the chassis. Up to two hot-swap 600W DC or 600W AC power supply modules may be installed for a 1 + 1 redundant configuration. A filler module for the empty power supply location is supplied for systems without redundancy.

The system contains a fan array consisting of two 80 x 38mm fans and two 40 x 28mm fans to cool the server board SE7520JR2 and other components. The fans are installed directly behind the drive bays and are located in front of the server board. Individual fan connectors are located on the FPIO board. A fan failure is indicated by one of the fault light-emitting diodes (LED) located on the FPIO board.

The front bezel can be customized to meet OEM industrial design requirements. The bezel design allows adequate airflow to cool the system components. The front bezel is removed to access the drive tray. The front bezel also supports an air filter.

Figure 3 shows a block diagram of the TIGI2U Carrier Grade Server with interconnections.

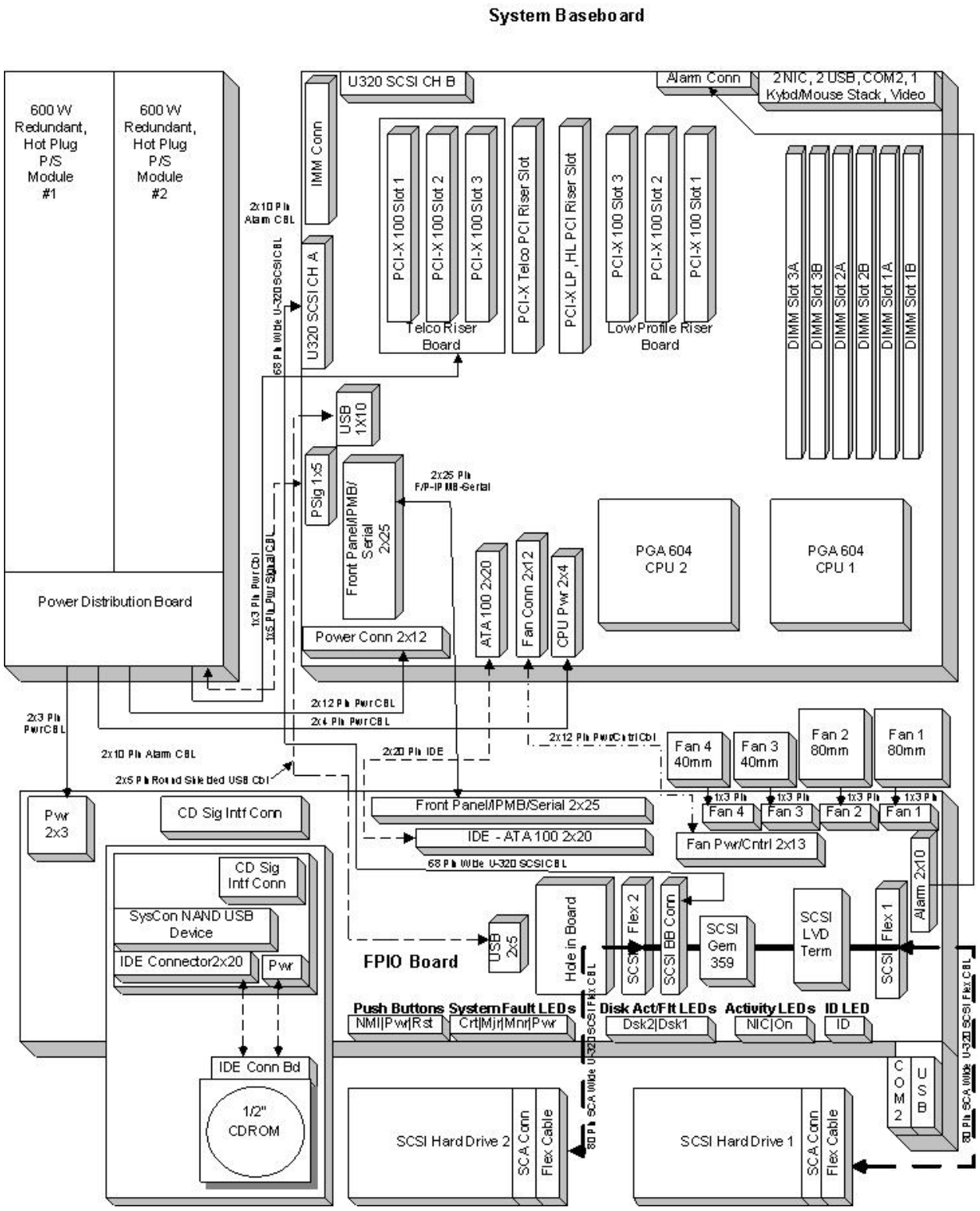


Figure 3. Carrier Grade Server TIGI2U Block Diagram

2.4 External Chassis Features

2.4.1 Front View of Chassis

Figure 4 shows the front view of the system. Figure 5 shows the front view of the system with the front bezel removed. Removing the front bezel provides access to the two hot-plug hard drive bays. Removing the front bezel also provides access to the peripheral bay.

Both areas are described in detail in the following sections.

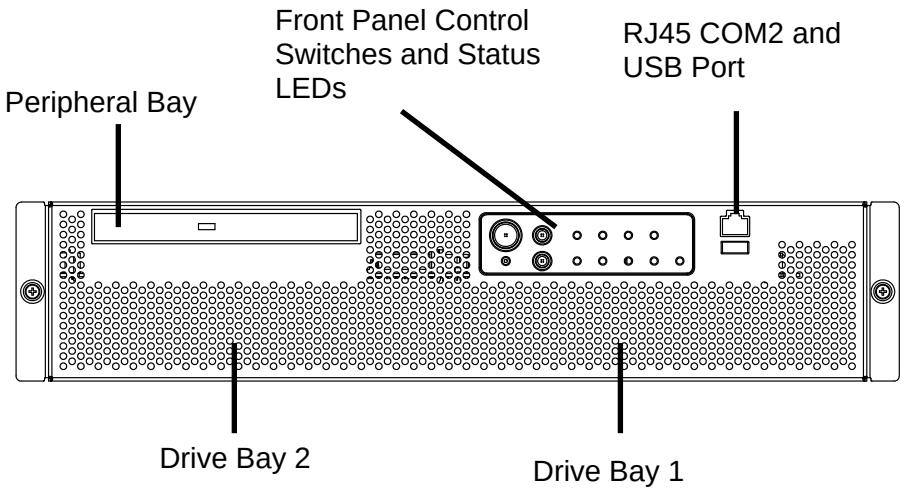


Figure 4. Front View of System

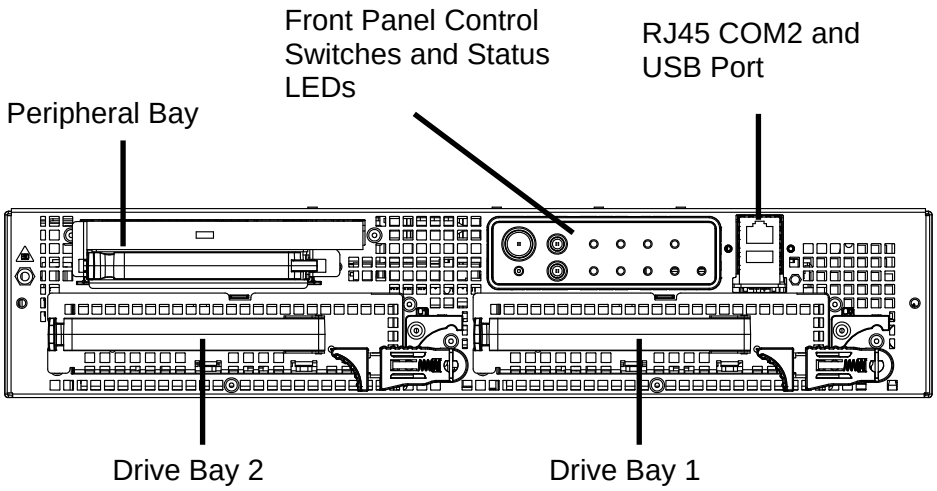


Figure 5. Front View of System (shown with bezel removed)

2.4.2 Front Panel

The front panel features are shown in Figure 6 and described in

Table 2. All front panel control switches and status LEDs are contained on the FPIO system board. Please refer to Section 4.4 for a detailed description of the control switches and status LEDs contained on the Front Panel.

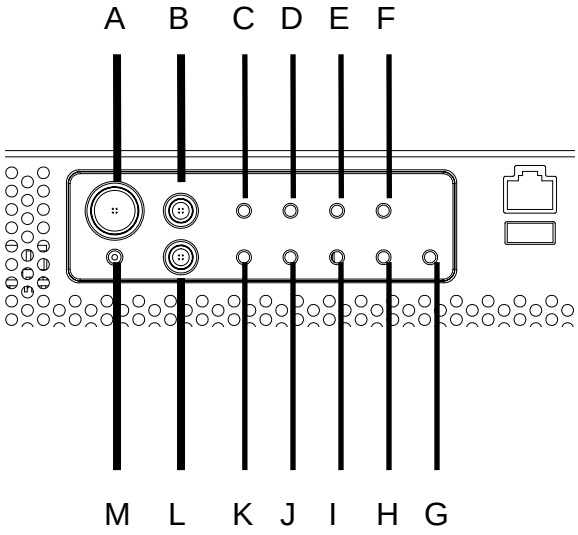


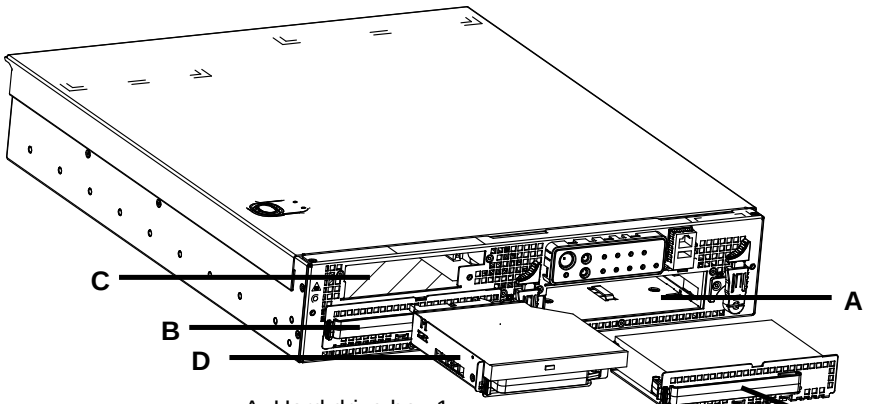
Figure 6. Front Panel Details

Table 2. Front Panel Features

Item	Feature	Description
Front Panel Switches		
A	Power switch	Toggles the system power
B	Reset switch	Resets the system
L	ID switch	Toggles system ID LED
M	NMI switch	Assert NMI to server board
Front Panel Alarm LEDs and Relays		
C	Critical (amber)	When continuously lit, indicates the presence of a Critical System Fault. A critical system fault is an error or event that is detected by the system with a fatal impact to the system. In this case, the system cannot continue to operate. An example could be the loss of a large section of memory, or other corruption, that renders the system not operational. The front panel critical alarm relay will be engaged.
D	Major (amber)	When continuously lit, indicates the presence of a Major System Fault. A major system fault is an error or event that is detected by the system that has discernable impact to system operation. In this case, the system can continue to operate but in a “degraded” fashion (reduced performance or loss of non-fatal feature reduction). An example could be the loss of one of two mirrored disks. The front panel major alarm relay will be engaged.
E	Minor (amber)	When continuously lit, indicates the presence of a Minor System Fault. A minor system fault is an error or event that is detected by the system but has little impact to actual system operation. An example would be a correctable ECC error. The front panel minor alarm relay will be engaged.
F	Power (amber)	When continuously lit, indicates the presence of a Power System Fault. The front panel power alarm relay will be engaged.
Front Panel Status LEDs		
G	Disk 1 Activity/Fault LED (green/amber)	Indicates disk 1 SCSI hard drive activity when green, or a disk 1 SCSI hard drive fault when amber
H	Disk 2 Activity/Fault LED (green/amber)	Indicates disk 2 SCSI hard drive activity when green, or a disk 2 SCSI hard drive fault when amber
I	Main power LED (green)	When continuously lit, indicates the presence of DC power in the server. The LED goes out when the power is turned off or the power source is disrupted.
J	NIC0/NIC1 activity LED (green)	Indicates activity on either NIC0 or NIC1
K	System ID LED (white)	Indicates any system SCSI hard drive activity

2.4.3 Chassis Peripheral Bay and Hard Drive Bays

The Carrier Grade Server TIGI2U chassis provides two hot-swap hard drive bays at the front of the chassis, along with a non hot-swap blind-mate peripheral bay that supports either a floppy drive carrier or a CD-RW/DVD drive carrier. Both hard drive bays may be populated with a tray-mounted 3.5” SCSI SCA hard disk drive.



A. Hard drive bay 1
B. Hard drive bay 2
C. Peripheral drive bay
D. CD-RW/DVD drive
E. Hard disk drive module

Figure 7: Chassis Peripheral Bay and Hard Drive Bays

2.4.3.1 Peripheral Drive Bay

The peripheral bay supports a CD-RW/DVD drive carrier assembly. The blind-mate CD-RW/DVD drive carrier assembly can be inserted or removed when the system power is off.

The CD-RW/DVD drive carrier assembly utilizes a 0.5” (12.7mm) slim-line CD-RW/DVD drive.

As shown in Figure 8, the CD-RW/DVD carrier assembly is installed in the system, and the handle is rotated closed in the direction indicated and snapped into place to lock the carrier into the chassis.

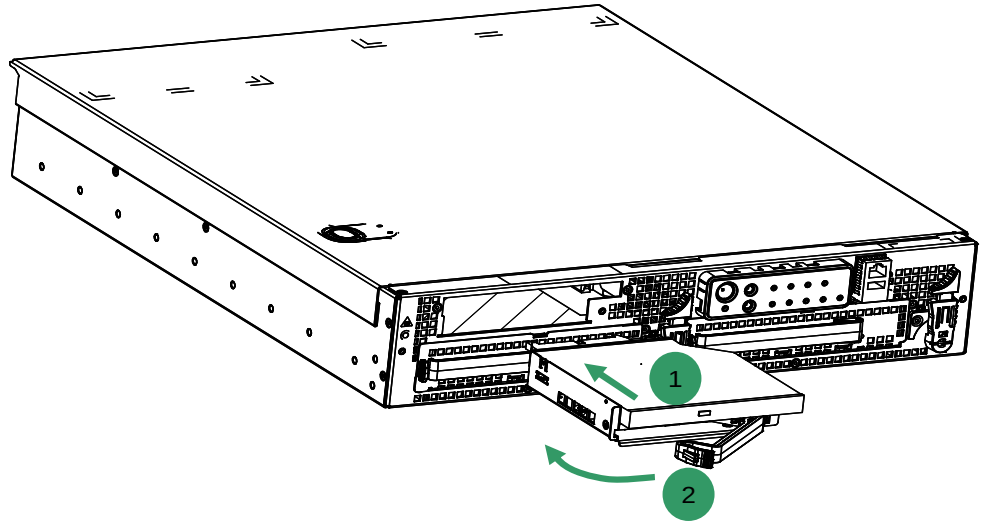
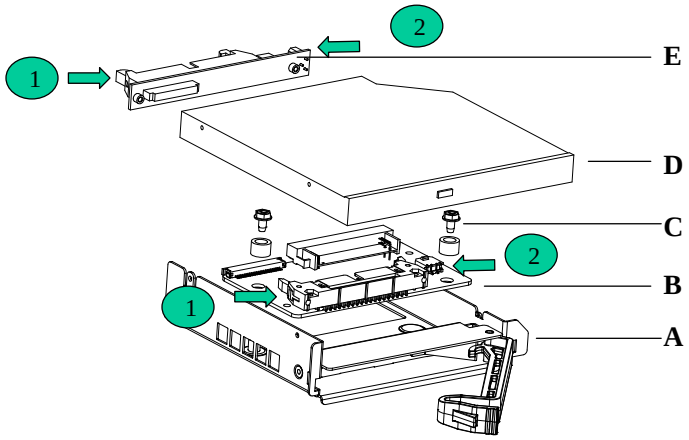


Figure 8: Peripheral Drive Bay

2.4.3.1.1 CD-RW/DVD Drive Carrier Assembly

The CD-RW/DVD drive is installed in a CD-RW/DVD drive carrier assembly before installing it into the system. An exploded view of the CD-RW/DVD drive carrier assembly is shown in the following figure.



A. CD-RW/DVD drive carrier metal housing
B. CD-RW/DVD drive carrier interface board with SysCon Device
C. Two screws to connect interface board to metal housing
D. CD-RW/DVD Drive
E. CD-RW/DVD interface board

Figure 9: CD-RW/DVD Drive Carrier Assembly

Two cables are required to connect between the CD-RW/DVD drive carrier interface board (B) and the CD-RW/DVD interface board (E). An IDE cable is used to connect between the 2x20 IDE connector on both of these interface boards as indicated in (1). A 1x2 power cable is used to connect between the power connector on both of these interface boards as indicated in (2).

The CD-RW/DVD drive carrier assembly inserts into the peripheral bay on the front of the system. The mating connectors on the CD-RW/DVD drive carrier assembly and the FPIO board are blind-mate style connectors, and will seat fully when the rotating handle on the CD-RW/DVD drive carrier assembly is snapped into place in the chassis.

2.4.3.2 Hard Drive Bays

There are two hard drive bays in the system (see (1) and (2) in the drawing below). Each hard drive bay supports a tray-mounted U320 SCSI disk drive with SCA (single connector attach) interconnect. The drive tray is installed into the front of the chassis in the hard drive bay, and then secured in place by pushing in the handle on the drive tray. A small lever on the front of the system is then rotated into the horizontal position to connect the SCA connector on the system flex circuit SCSI cable to the SCA connector on the drive. Ultra 320 SCSI technology (SCA interconnect) or slower hard disk drives can be installed in this hard drive tray. The hard drive bays are designed to accept 15,000 RPM (and below) hard drives that consume up to 18W of power.

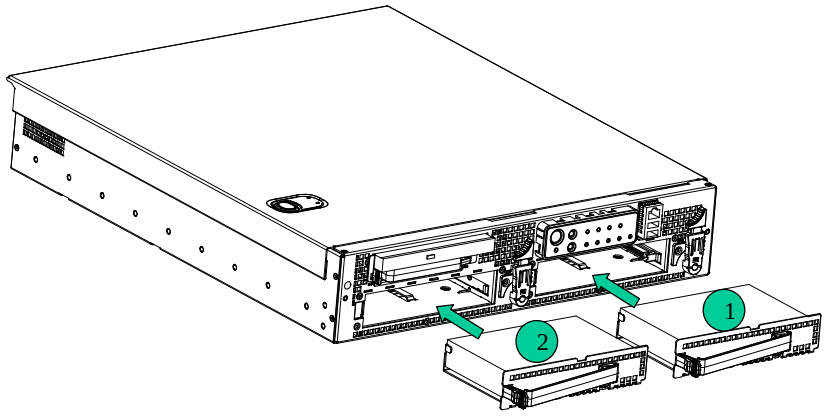


Figure 10: SCSI Hard Drive Bays

2.4.3.2.1 Hard Drive Tray

Each hard drive used in the system must be mounted to a drive tray using four screws inserted into the bottom of the drive as shown in the figure.

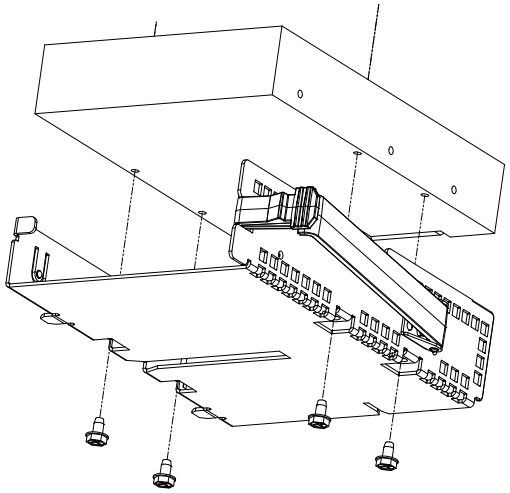


Figure 11: SCSI Hard Drive Tray

2.4.4 Rear View of Chassis

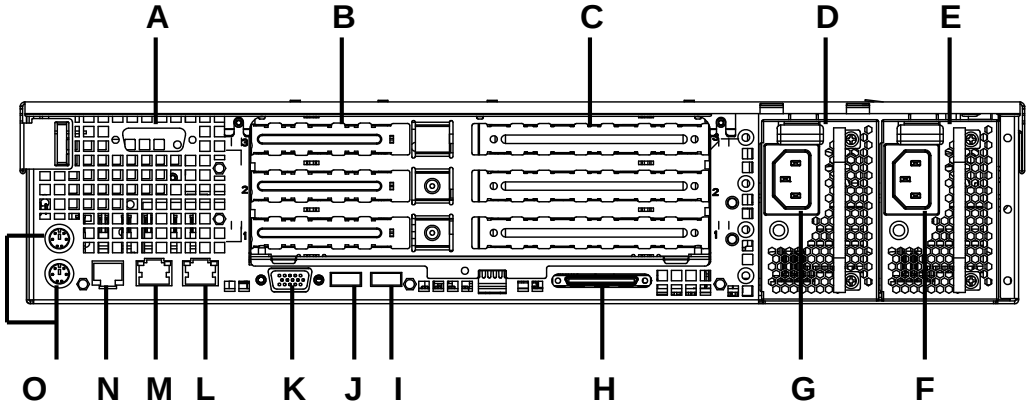


Figure 12. Rear View of System

Table 3. System Features - Rear

Item	Description
A	DB15 Alarm Connector
B	PCI card bracket (low profile)
C	PCI card bracket (full-height)
D	Power supply module, redundant (system accessory)
E	Power supply module, primary
F	AC power input (primary)
G	AC power input (redundant)
H	U320 SCSI connector
I	USB connector 0
J	USB connector 1
K	Video connector
L	RJ45 NIC 2 connector - Green Status LED / Yellow Status LED
M	RJ45 NIC 1 connector - Green Status LED / Yellow Status LED
N	RJ45 serial 2 port
O	PS/2 mouse/keyboard connectors

Note: AC configuration depicted. Items D-G may be configured for DC operation.

2.5 Internal Chassis Features

2.5.1 Carrier Grade Server board SE7520JR2

The Intel® Carrier Grade Server board SE7520JR2 is a monolithic printed circuit board that can accept one or two 800 MHz FSB Intel® Xeon™ processors using the 604-pin ZIF socket. The figure below shows the functional blocks of the Carrier Grade server board SE7520JR2 and the plug-in modules that it supports.

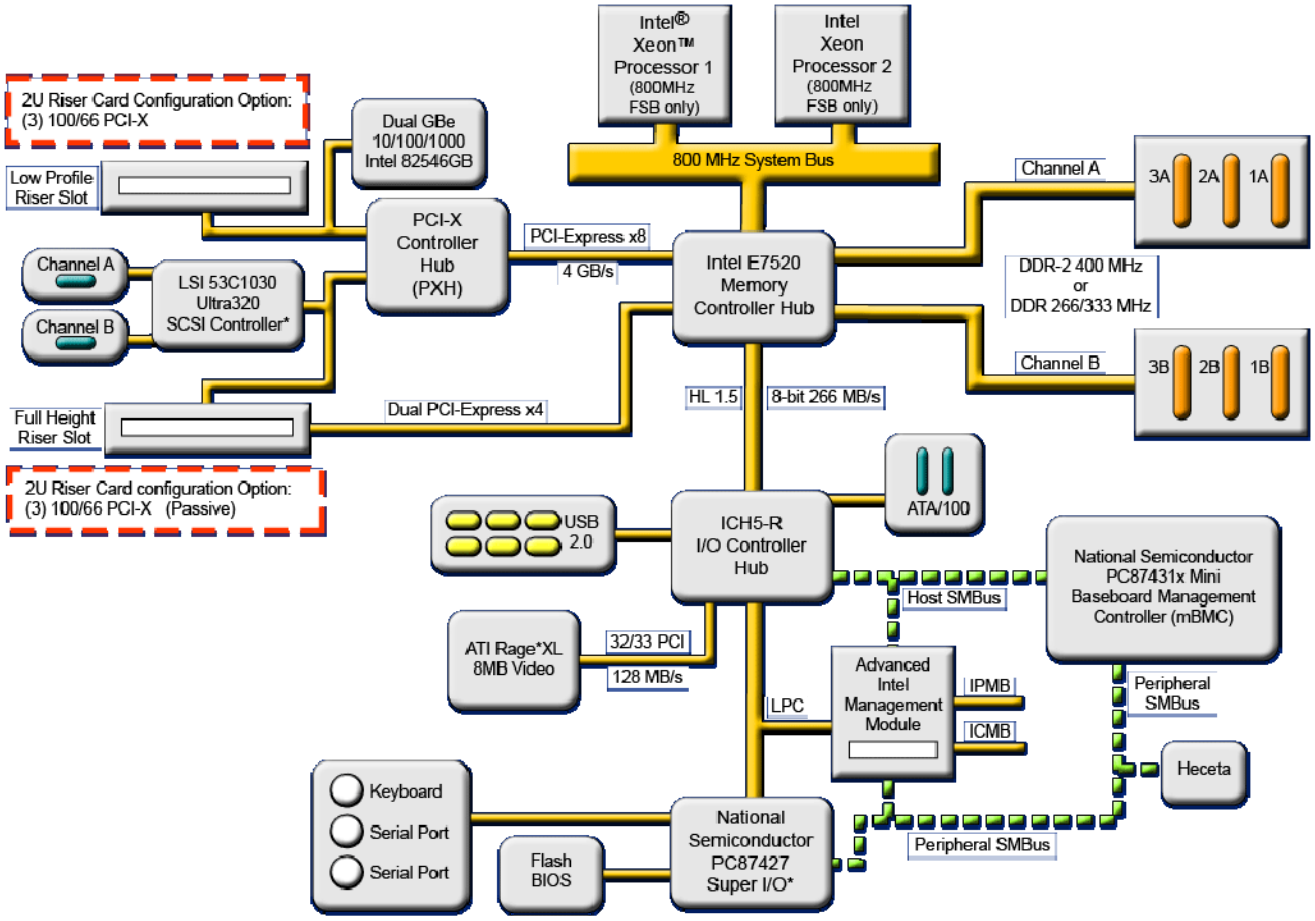


Figure 13. TIGI2U Carrier Grade Server Board SE7520JR2 Block Diagram

- Dual processor slots supporting 800MHz Front Side Bus (FSB) Intel® Xeon™ processors
- Intel E7520 Chipset (MCH, PXH, ICH-5R)
- Two PCI riser slots
  - Riser Slot 1: Supports low profile PCI-X 64 bit 100MHz PCI-X cards
  - Riser Slot 2: Supports full height PCI-X 64 bit 100MHz PCI-X cards
- Six DIMM slots supporting DDR2 – 400MHz memory
- Dual channel LSI* 53C1030 Ultra320 SCSI Controller with integrated RAID 0/1 support
- Dual Intel® 82546GB 10/100/1000 Network Interface Controllers (NICs)
- On board ATI* Rage XL video controller with 8MB SDRAM
- On-board platform instrumentation using Intel's Sahalee BMC
- External IO connectors
  - Stacked PS2 ports for keyboard and mouse
  - RJ45 Serial B Port
  - Two RJ45 NIC connectors
  - 15-pin video connector
  - Two USB 2.0 ports
  - U320 High density SCSI connector (Channel B)
- Dual Intel® 800 MHz Front Side Bus
- Intel® E7520 chipset
  - E7520 North Bridge
  - PXH I/O Bridge
  - ICH-5R S South Bridge

- Support for up to six DDR2-400MHz compliant registered ECC DIMMs providing up to 16 GB of memory, when 4G DIMMs become available and have been tested.
- Three separate and independent PCI buses:
  - Segment P32-A: 32-bit, 33 MHz, 5 V with the embedded device:
    - 2D/3D graphics controller: ATI Rage XL Video Controller with 8 MB of memory.
  - Segment P64-A: 64-bit, 100/66 MHz, 3.3 V, PCI-X supporting the following configuration:
    - One PCI I/O riser slot capable of supporting full length PCI add-in cards
    - Dual-channel LSI 53C1030 Ultra320 SCSI Controller with integrated RAIS 0/1 support

    Segment P64-B: 64-bit, 100/66 MHz, 3.3 V PCI-X supporting the following devices:
    - One PCI I/O riser slot capable of supporting low-profile PCI add-in cards
    - Dual-channel Intel® 10/100/1000 82546EB Gigabit Ethernet Controller
- LPC (Low Pin Count) bus segment with two embedded devices:
  - National Semiconductor* PC87431M mini-Baseboard Management Controller (mBMC) providing monitoring, alerting, and logging of critical system information obtained from embedded sensors on the server board

  - Super I/O controller chip providing all PC-compatible I/O (floppy, serial, keyboard, mouse)

- X-Bus segment with one embedded device:
  - Flash ROM device for system BIOS: Intel® 32-megabit 28F320C3 Flash ROM
- Two external Universal Serial Bus (USB) ports with an additional internal header providing two optional USB ports for front panel and SysCon support
- One external low-profile RJ45 serial port
- IDE connector for one CD-RW/DVD drive
- Support for up to four system fans
- Fault/Status LEDs throughout the server board
- Multiple server management headers providing on-board interconnects to server management features

Refer to the server board SE7520JR2 TPS for further details.

2.5.2 PCI Adapter Subsystem

A PCI adapter assembly that supports both the full-height PCI riser and the low profile riser and associated PCI adapters is installed in the PCI riser slots located in the middle of the server board SE7520JR2. This PCI adapter assembly is configured and installed as shown in the following figure. After the PCI adapter assembly is removed from the system, it is configured with PCI adapters by plugging the PCI adapters into the PCI connectors on the riser cards that are part of the PCI adapter assembly. The PCI adapter assembly is then installed into the system by plugging the riser cards into the riser card connectors on the Server board SE7520JR2. Refer to the Server board SE7520JR2 specification for electrical characteristics for this PCI adapter subsystem.

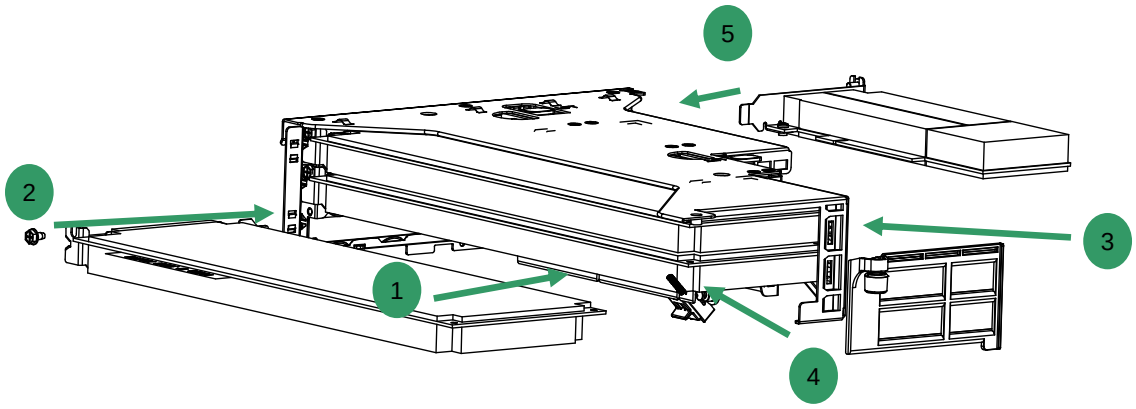


Figure 14: PCI Adapter Subsystem Assembly and Installation (A)

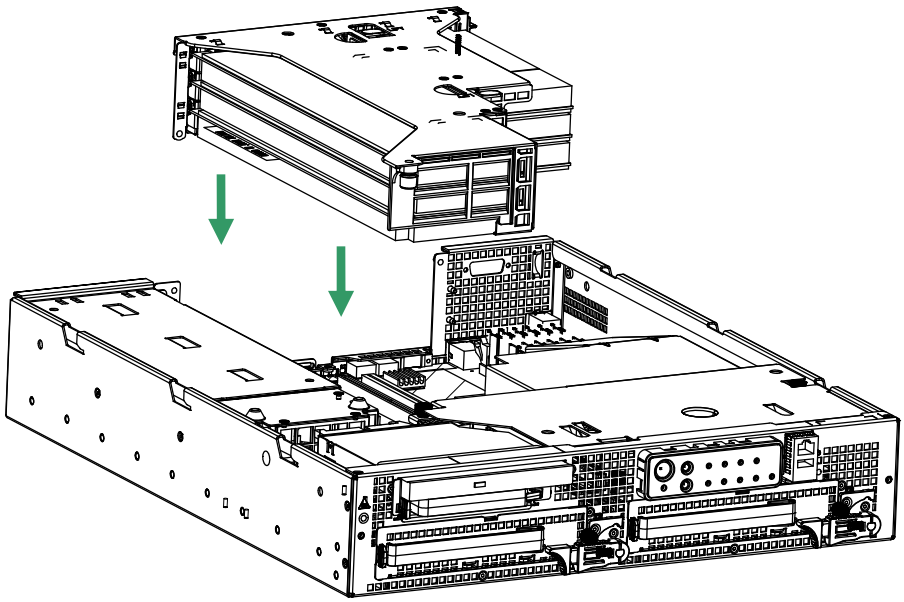


Figure 15: PCI Adapter Subsystem Assembly and Installation

The following table shows the maximum PCI bus speed achievable on full height PCI riser. Any slower PCI adapter installed in the PCI Adapter Subsystem will gate the speed. When populating add-in cards, the add-in cards must be installed starting with the slot furthest from the server board SE7520JR2 in order to maintain the signal integrity of the bus.

Table 4: Full Height PCI Bus Maximum Speed Table

Configuration	Bus B with Anvik Dual NIC and 3.3V Riser
0 Adapter Cards installed and on board device enabled	PCI-X 64/100
1 Adapter Cards installed and on board device enabled	PCI-X 64/100
2 Adapter Cards installed and on board device enabled	PCI-X 64/100
3 Adapter Cards installed and on board device enabled	PCI-X 64/66
1 Adapter Cards installed and on board device disabled	PCI-X 64/100
2 Adapter Cards installed and on board device disabled	PCI-X 64/100
3 Adapter Cards installed and on board device disabled	PCI-X 64/66

2.5.3 Power Subsystem

The Carrier Grade Server TIGI2U can be configured with either an AC-input power subsystem or a DC-input power subsystem. The power supply modules are located at the left rear of the chassis. Both the AC and DC-input power subsystems may contain up to two power supply modules and can be configured as follows:

- Two power supply modules installed, (1 + 1) power redundancy for maximally loaded system
- One power supply module installed[1], non-redundant for maximally loaded system

When the system is configured with two power supply modules, the hot-swap feature allows the user to replace a failed power supply module without interrupting system functionality. To ensure that all components remain within specification under all system environmental conditions, it is recommended that power supply module hot-swap operations not exceed two minutes in duration.

Power from the power subsystem is carried to internal system boards and peripheral devices via discrete cables from the Power Distribution Board. One power supply module is capable of handling the worst-case power requirements for a fully configured TIGI2U server system. This includes two 800 MHz FSB Intel® Xeon™ processors, 16 GB of memory, two hard drives at 18 W per drive (typical worst case 3.5-inch by 1.0-inch, 15k RPM drive), and a full complement of PCI adapters.

The total power requirement for the TIGI2U server system exceeds the 240 VA energy hazard limit, which defines an operator-accessible area. As a result, only qualified technical individuals should access the processor, memory, and I/O areas on the Server board SE7520JR2 while the system is energized.

Refer to *Section 7 DC Power Subsystem* or *Section 8 AC Power Subsystem* of this document for detailed power specifications.

[1] Proper power subsystem cooling by the power subsystem fan requires the population of both (power supply bay) receptacles either by a power supply module or a filler panel.

2.5.4 Cooling Subsystem

2.5.4.1 Description

All system components except the power supply cage are cooled by a set of fans mounted near the middle of the chassis and behind the hard drive bays. This is shown in Figure 16.

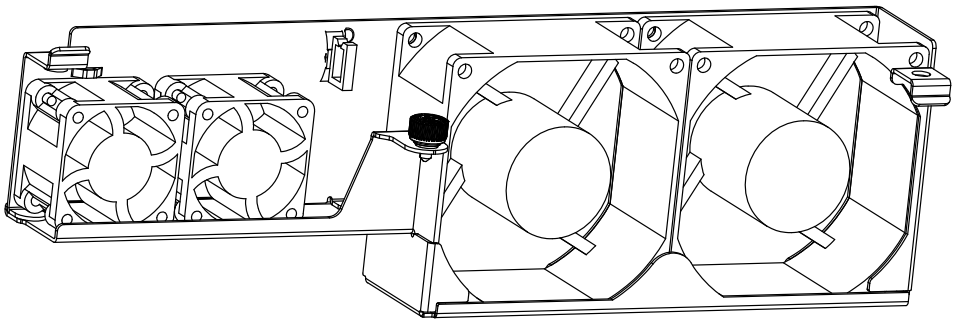


Figure 16. Fan Array with Four System Fans Installed

The TIGI2U system comes in a non-redundant, four-fan configuration that consists of two 80mm x 38mm fans and two 40mm x 28mm fans.

Air flows in through the front bezel over the peripheral bay and the hard drive bays, passes through the fans and over the server board, and exhausts through the rear of the chassis. Each fan provides tachometer signal output to the server board SE7520JR2 to indicate a fan failure.

2.5.4.2 Ambient Temperature Control

The server board SE7520JR2 contains two pulse-width-modulation (PWM) circuits, which cycle the 12 Vdc fan voltage to provide quiet operation when system ambient temperature is low and there are no fan failures. One PWM is connected to the two 80x38mm fans and the other to the two 40x28mm fans. Based on the ambient temperature, the fan speeds are set per the following table:

Table 5: Fan Speed Settings

	40mm	40mm	80mm	80mm
Temperature	**PWM %**	**VDC**	**PWM%**	**VDC**
20c	49% (31h)	5.47v	49% (31h)	5.26v
21c	49% (31h)	5.47v	49% (31h)	5.26v
22c	49% (31h)	5.47v	49% (31h)	5.26v
23c	51% (33h)	6.23v	49% (31h)	5.26v
24c	54% (36h)	6.23v	49% (31h)	5.26v
25c	57% (39h)	6.99v	49% (31h)	5.26v
26c	60% (3Ch)	6.99v	50% (32h)	5.99v
27c	63% (3Fh)	7.47v	51% (33h)	5.99v
28c	66% (42h)	7.47v	52% (34h)	5.99v
29c	69% (45h)	8.53v	54% (36h)	5.99v
30c	72% (48h)	8.53v	55% (37h)	5.99v
31c	76% (4Ch)	9.30v	58% (3Ah)	6.72v
32c	82% (52h)	10.07v	68% (44h)	7.45v
33c	90% (5Ah)	10.84v	74% (4Ah)	8.18v
34c	96% (60h)	11.59v	80% (50h)	8.91v
35c	100% (64h)	12.21v	86% (56h)	9.63v
36c			90% (5Ah)	10.37v
37c				
38c			96% (60h)	11.08v
39c				
40c			100% (64h)	11.79v

2.5.4.3 Cooling Summary

The four-fan cooling subsystem is sized to provide cooling for:

- Up to two processors
- 16 GB of SDRAM memory
- Two 15,000 RPM hard drives at a maximum of 18W per drive
- 6 PCI cards

The cooling subsystem is designed to meet acoustic and thermal requirements at the lower fan speed settings. At the higher fan speed settings, thermal requirements are met for the maximum ambient temperatures, but acoustic requirements are not met. The environmental specifications are summarized in 2.7.1.

2.6 Server Management

The Server Management sub-system provided by the TIGI2U server consists of a micro-controller, communication buses, sensors, system BIOS, and server management firmware. Standard On-Board Platform Instrumentation is based around the National Semiconductor* PC87431M mini-Baseboard Management Controller (mBMC) and the Intel® Management Module Advanced Edition, which is based on Intel's "Sahalee" BMC.

The following table summarizes the supported features:

Table 6: Server Management Features

Element	TIGI2U
IPMI Messaging, Commands, and Abstractions	Yes
Baseboard Management Controller (BMC)	Yes
Sensors	Yes
Sensor Data Records (SDRs) and SDR Repository	Yes
FRU Information	Yes
Autonomous Event Logging	Yes
System Event Log (SEL)	3276 Entries
BMC Watchdog Timer, covering BIOS and run-time software	Yes
IPMI Channels, and Sessions	Yes
EMP (Emergency Management Port) - IPMI Messaging over Serial/Modem. This feature is also referred to as DPC (Direct Platform Control) over serial/modem.	Yes
Serial/Modem Paging	Yes
Serial/Modem Alerting over PPP using the Platform Event Trap (PET) format	Yes
DPC (Direct Platform Control) - IPMI Messaging over LAN (available via both on-board network controllers)	Yes
LAN Alerting using PET	Yes
Platform Event Filtering (PEF)	Yes
ICMB (Intelligent Chassis Management Bus) - IPMI Messaging between chassis	Yes
PCI SMBus support	Yes
Fault Resilient Booting	Yes

Element	TIGI2U
BIOS logging of POST progress and POST errors	Yes
Integration with BIOS console redirection via IPMI v2.0 Serial Port Sharing	Yes
Access via web browser	Yes
SNMP access	Yes
Telnet access	Yes
DNS support	Yes
DHCP support (dedicated NIC only)	Yes
Memory Sparing/Mirroring sensor support	Yes
Alerting via Email	Yes
Keyboard, Video, Mouse (KVM) redirection via LAN	Yes
High speed access to dedicated NIC	Yes

2.7 Specifications

2.7.1 Environmental Specifications

The TIGI2U system will be tested to the environmental specifications as indicated in Table 7. All testing will be performed per procedures defined in Bellcore GR-63-CORE NEBS Physical Protection, Bellcore GR-3580 NEBS Criteria Levels, Bellcore GR-1089-CORE EMC and Electrical Safety – Generic Criteria for Network Telecommunications Equipment, and the *Intel Environmental Standards Handbook*.

Table 7. Environmental Specifications Summary

Environment	Specification
Temperature operating	5° C to 40° C (41° F to 104° F)
Temperature non-operating	-40° C to 70° C (-40° F to 158° F)
Altitude	0 to 1,800 m (0 to 5,905 ft)
Humidity non-operating	95%, non-condensing at temperatures of 23° C (73° F) to 40° C (104° F)
Vibration operating	Swept sine survey at an acceleration amplitude of 0.1 g from 5 to 100 Hz and back to 5 Hz at a rate of 0.1 octave/minute, 90 minutes per axis on all three axes as per Bellcore GR-63-CORE standards
Vibration non-operating	Swept sine survey at an acceleration amplitude of 0.5 g from 5 to 50 Hz at a rate of 0.1 octaves/minute, and an acceleration amplitude of 3.0 g from 50 to 500 Hz at a rate of 0.25 octaves/minute, on all three axes as per Bellcore GR-63-CORE standard. 2.2 Grms, 10 minutes per axis on all three axes as per the *Intel Environmental Standards Handbook*
Shock operating	Half-sine 2 G, 11 ms pulse, 100 pulses in each direction, on each of the three axes as per the *Intel Environmental Standards Handbook*
Shock non-operating	Trapezoidal, 25 G, 170 inches/sec delta V, three drops in each direction, on each of the three axes as per *Intel Environmental Standards Handbook*
Safety	UL 1950, CSA 950, IEC 950, TUV/GS EN60950
Emissions	Certified to FCC Class A; tested to CISPR 22 Class A, EN 55022 Class A, VCCI Class A ITE, AS/NZS 3548 Class A
Immunity	Verified to comply with EN 50082-1
Electrostatic discharge (ESD)	Tested to ESD levels up to 15 kilovolts (kV) air discharge and up to 8 kV contact discharge without physical damage as per *Intel Environmental*

Environment	Specification
	Standards Handbook
Acoustic	Sound pressure: < 55 dBA at ambient temperatures < 24°C measured at bystander positions in operating mode

2.7.2 Physical Specifications

Table 8 describes the physical specifications of the TIGI2U system.

Table 8. Physical Dimensions

Height	3.45 inches (87.6 mm)
Width	17.14 inches (435.3 mm)
Depth	20 inches (508 mm)
Front clearance	2 inches (76 mm)
Side clearance	1 inches (25 mm)
Rear clearance	3.6 inches (92 mm)

3. Cables and Connectors

This chapter describes interconnections between the various components of the TIGI2U server system. Also, this chapter includes an overview diagram of the TIGI2U server system interconnections, as well as tables describing the signals and pin-outs for the system connectors. Refer to the appropriate Server board SE7520JR2 section or system board sections in this document for other connector signal descriptions and pin-outs.

3.1 Chapter Structure and Outline

The information contained in this chapter is organized into four sections. The information is presented in a modular format, with numbered headings for each major topic and subtopic. The content of each section is summarized as follows:

Section 3.2: Interconnect Block Diagram
Provides an overview of system interconnects.

Section 3.3: Cable and System Interconnect Descriptions
Provides a list of all the connectors and cables in the system.

Section 3.4: User-accessible Interconnects
Describes the form-factor and pin-out of user-accessible interconnects.

Section 3.5: CD-RW/DVD Peripheral Adapter Boards and Connectors
Describes the form-factor and pin-out of peripheral adapter boards and connectors.

3.2 Interconnect Block Diagram

Figure 17 shows interconnections for all of the boards used in the TIGI2U server system.

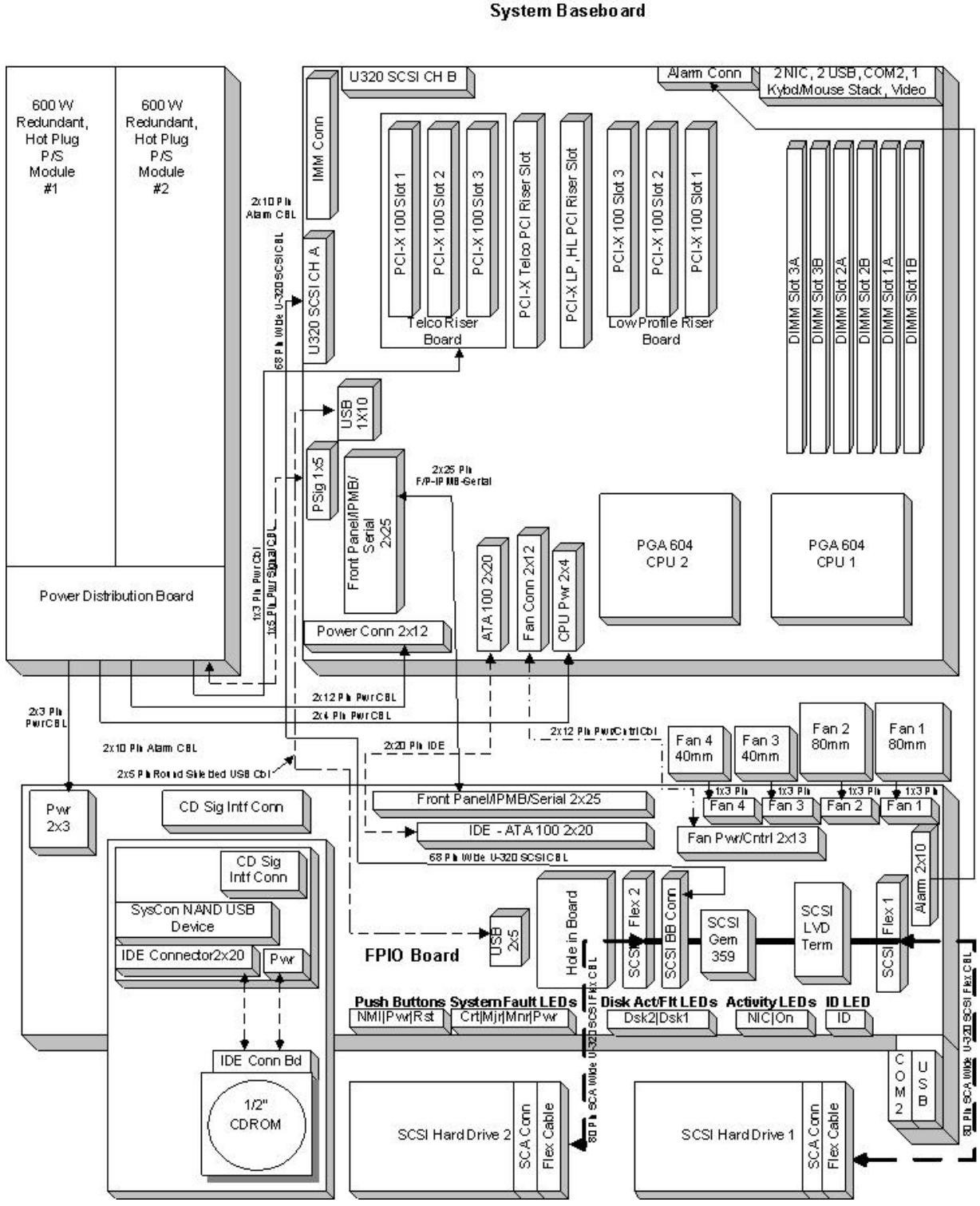


Figure 17. TIGI2U System Interconnect Block Diagram

3.3 User-accessible Interconnects

3.3.1 Keyboard and Mouse Ports

Two stacked PS/2 ports are provided to support both a keyboard and a mouse. Either port can support a mouse or keyboard. The following table details the pin-out of the PS/2 connector.

Table 9. Keyboard and Mouse Port

Pin	Signal
1	KEYDAT (keyboard data)
2	MSEDAT (mouse data)
3	GND (ground)
4	Fused VCC (+5 V)
5	KEYCLK (keyboard clock)
6	MSECLK (mouse clock)

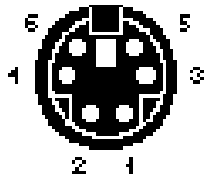


Figure 18. Keyboard, Mouse Connector

3.3.2 Serial Port

Two serial port connectors are provided, one on the front panel and one at the rear I/O using 8-pin RJ-45 connectors. Each port connects to COM2. The user may connect to either the front or the rear port, but never both. The front port is described in the FPIO board chapter, section 4.5.1.

Table 10. Serial Port Connector on rear I/O Port

Pin	Signal
1	RTS (request to send)
2	DTR (data terminal ready)
3	TXD (transmit data)
4	GND
5	RIA (ring indicator)
6	RXD (receive data)
7	DSR/DCD (date set ready / data carrier detect[2])
8	CTS (clear to send)

[2] Use the jumper on the server board SE7520JR2 to select.

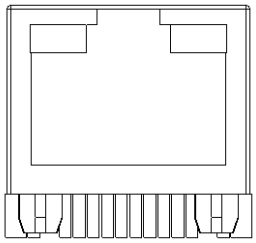


Figure 19. Serial Port Connector

3.3.3 Video Port

The video port interface is a standard VGA compatible, 15-pin connector. Onboard video is supplied by an ATI Rage XL video controller with 8 MB of onboard video SGRAM.

Table 11. Video Connector

Pin	Signal
1	Red (analog color signal R)
2	Green (analog color signal G)
3	Blue (analog color signal B)
4	No connection
5	GND
6	GND
7	GND
8	GND
9	Fused VCC (+5 V)
10	GND
11	No connection
12	DDCDAT
13	HSYNC (horizontal sync)
14	VSYNC (vertical sync)
15	DDCCLK

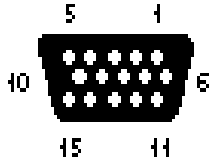


Figure 20. Video Connector

3.3.4 Universal Serial Bus (USB) Interface

The server board provides four USB ports. USB ports 0 and 1 are brought out the rear of the unit on the server board, and USB ports 2 and 3 are routed to the FPIO board. USB port 2 is brought to the front of the system and is accessible without removing the front bezel. USB port 3 is used internally for interfacing to the SysCon device. The built-in USB ports permit the direct connection of four USB peripherals without an external hub. If more devices are required, an external hub can be connected to any of the built-in ports.

Table 12. Single USB Connector

Pin	Signal
1	Fused VCC (+5 V w/over-current monitor of ports 0, 1, 2, and 3)
2	DATAL0 (differential data line paired with DATAH0)
3	DATAH0 (differential data line paired with DATAL0)
4	GND
5	GND
6	GND

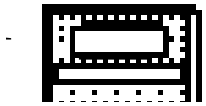


Figure 21. USB Connector

3.3.5 Ethernet Connector

The server board SE7520JR2 provides two NIC RJ45 connectors oriented side by side on the back edge of the board and accessible at the rear I/O panel. The pin-out of each connector is identical and is defined in the following table.

Table 13. Ethernet Connector

Pin	Signal Name	Pin	Signal Name
1		9	LAN_MID3N
2	LAN_MID0P	10	P2V5_NIC
3	LAN_MID0N	11	LAN_LINK_1000_L (LED)
4	LAN_MID1P	12	LAN_LINK_100_L_R (LED)
5	LAN_MID2P	13	LAN_ACT_L (LED)
6	LAN_MID2N	14	LAN_LINK_L_R (LED)
7	LAN_MID1N	15	GND
8	LAN_MID3P	16	GND

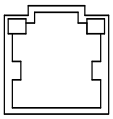


Figure 22. Ethernet Connector

3.3.6 Telco Alarms Connector

The system provides one Telco DB15 alarms connector on the rear bulkhead. Table 14 shows the pin-out for the Telco alarms connector, and Figure 23 shows the Telco alarms connector as viewed from the back of the server.

Table 14. Telco Alarms Connector

Pin	Description	Pin	Description
1	MinorReset +	9	MinorAlarm – NC
2	MinorReset -	10	MinorAlarm - COM
3	MajorReset +	11	MajorAlarm - NO
4	MajorReset -	12	MajorAlarm - NC
5	CriticalAlarm - NO	13	MajorAlarm - COM
6	CriticalAlarm - NC	14	PwrAlarm - NO
7	CriticalAlarm - COM	15	PwrAlarm - COM
8	MinorAlarm - NO		

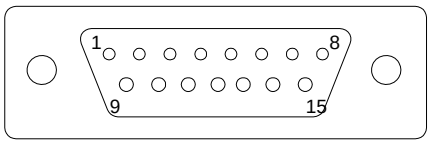


Figure 23. Telco Alarms Connector

3.3.7 Internal and External Ultra 320 SCSI Hard Disk Drive Connector

The server board SE7520JR2 provides an internal connection to Channel A of the LSI53C1030 Ultra 320 SCSI controller to the SCSI hard disk drives mounted in the hard drive bays. The SCSI bus on the server board SE7520JR2 is routed first to a SCSI bus on the FPIO board using a 68-pin LVD SCSI round cable, and then from the SCSI bus on the FPIO board to the SCSI disk drives using an 80-pin LVD SCSI flex circuit cable. The hot-plug circuitry resides on the FPIO board and not on the server board SE7520JR2.

In addition, the server system provides a shielded external VHDCI SCSI connection. This connection is on Channel B of the LSI53C1030 Ultra 320 SCSI controller.

Table 15. 68-pin SCSI Connectors on server board SE7520JR2

Connector Contact Number	Signal Name	Signal Name	Connector Contact Number
1	+DB(12)	-DB(12)	35
2	+DB(13)	-DB(13)	36
3	+DB(14)	-DB(14)	37
4	+DB(15)	-DB(15)	38
5	+DB(P1)	-DB(P1)	39
6	+DB(0)	-DB(0)	40
7	+DB(1)	-DB(1)	41
8	+DB(2)	-DB(2)	42
9	+DB(3)	-DB(3)	43
10	+DB(4)	-DB(4)	44
11	+DB(5)	-DB(5)	45
12	+DB(6)	-DB(6)	46
13	+DB(7)	-DB(7)	47
14	+DB(P)	-DB(P)	48
15	GROUND	GROUND	49
16	GROUND	GROUND	50
17	RESERVED	RESERVED	51
18	RESERVED	RESERVED	52
19	RESERVED	RESERVED	53
20	GROUND	GROUND	54
21	+ATN	-ATN	55
22	GROUND	GROUND	56
23	+BSY	-BSY	57
24	+ACK	-ACK	58
25	+RST	-RST	59
26	+MSG	-MSG	60
27	+SEL	-SEL	61
28	+C/D	-C/D	62
29	+REQ	-REQ	63
30	+I/O	-I/O	64
31	+DB(8)	-DB(8)	65
32	+DB(9)	-DB(9)	66
33	+DB(10)	-DB(10)	67
34	+DB(11)	-DB(11)	68

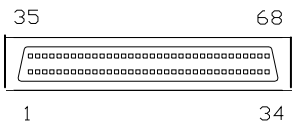


Figure 24. Internal Standard 68-pin SCSI Connector

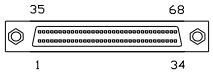


Figure 25. External VHDCI SCSI Connector

3.3.8 AC Power Input for AC-Input Power Supply Cage

A single IEC320-C13 receptacle is provided at the rear of each AC-input power module installed in the system. It is recommended to use an appropriately sized power cord and AC main. Please refer to *Section 8 AC Power Subsystem* of this document for system voltage, frequency, and current draw specifications.

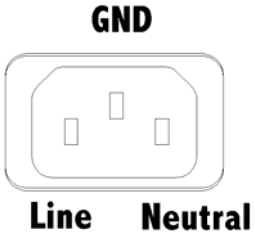


Figure 26. AC Power Input Connector

3.3.9 DC Power Input for DC-Input Power Supply Cage

A pluggable DC power terminal block is used to provide the DC-input power connection to each of the DC-input power supply modules that are configured in the DC power supply cage. It is recommended to use appropriately sized power wire and DC main. Please refer to *Section 7 DC Power Subsystem* of this document for system DC voltage, and current draw specifications.

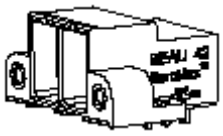


Figure 27. DC Power Input Connector

4. Front Panel IO (FPIO) System Board

This chapter describes the basic functions and interface requirements of the Front Panel IO (FPIO) system board that is designed for the TIGI2U server system.

4.1 Features

- Four switches to control power-on, reset, NMI, and the system ID LED
- One system ID LED that can be controlled remotely or by the system ID switch
- Two system activity LEDs that indicate power-on and NIC activity
- Two hard drive activity/fault LEDs that indicate activity/fault status for drives 0 and 1
- Four system fault LEDs that indicate critical, major, minor, and power system fault status
- Four system fault relays for external critical, major, minor, and power fault indicators
- One SCSI bus with hot-swap circuitry for controlling hot-swap SCSI disk drives 0 and 1
- IDE Bus from IDE Connector to blind-mate connector
- One blind-mate connector for interfacing to SysCon/CD-RW/DVD assembly
- Connectors for interfacing to the P/S, server board SE7520JR2, drive carrier assemblies, and hot plug disk drives 1 and 2

4.2 Chapter Structure and Outline

The information contained in this chapter is organized into eight sections. The information is presented in a modular format, with numbered headings for each major topic and subtopic. The content of each section is summarized as follows:

Section 4.3: Introduction
Provides an overview of the TIGI2U FPIO board, showing primary components and their relationships, and physical board layout diagrams.

Section 4.4: Functional Description of Front Panel Switches, LEDs, and Relays
Provides a functional description of the front panel switches, LEDs, and relays contained on the FPIO board.

Section 4.5: Connector Information
Provides information on all connectors contained on the FPIO board. Gives signal descriptions and the corresponding electrical parameters for each input and output of a given connector.

Section 4.6: IDE Bus
Provides information on the interconnection of the Server board SE7520JR2 IDE bus to the CD-RW/DVD assembly through the blind-mate connector on the FPIO board.

Section 4.7: SCSI Subsystem
Provides information on the SCSI subsystem on the FPIO board. The SCSI subsystem is designed to give the end user support for two SCSI hot-plug hard drives. The design enables easy use and replacement of the SCSI hard drives without powering down the system.

Section 4.8: Specifications
Describes the electrical, environmental and mechanical specifications.

4.3 Introduction

The FPIO system board provides the means of mounting and electrically connecting switches and indicators for system operation and status. These features are accessible and visible from the front of the chassis. In addition, it contains the blind-mate connector for interfacing to either the CD-RW/DVD drive carrier assembly that incorporates the SysCon device. It also contains the SCSI bus and hot-plug control circuitry necessary for the hot-plug SCSI disk drives. An alarms function is also provided. The FPIO system board is designed for use with SSI compliant telecom server board SE7520JR2.

4.4 Functional Description of Front Panel Switches, LEDs and Relays

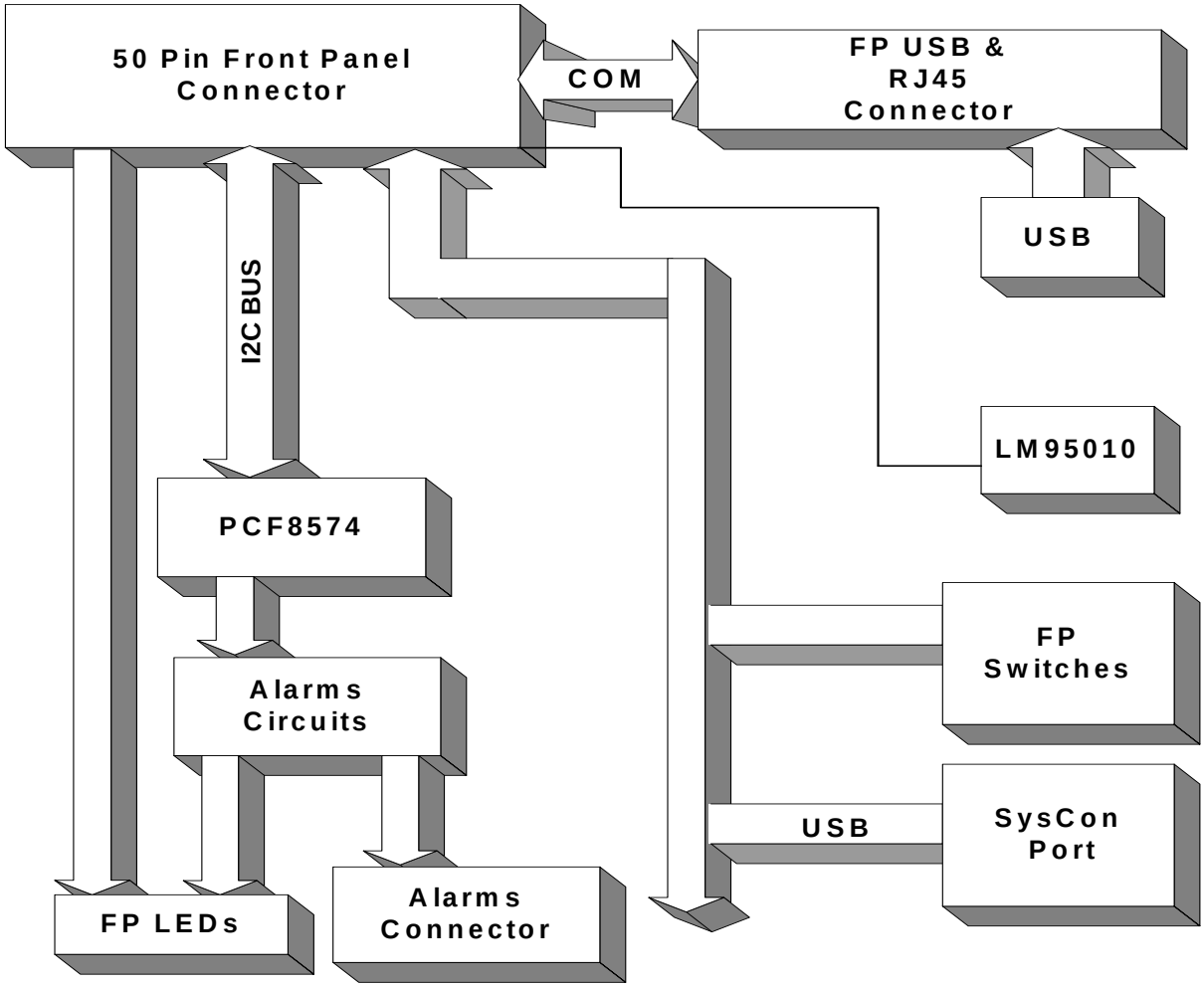


Figure 28. Block Diagram of Front Panel Switches, LEDs and Relays

4.4.1 Front Panel Switches

The front panel has a power switch, a reset switch, an NMI switch, and a system ID switch. The function of these switches is described in the following table.

Table 16. Front Panel Switch Description

Switch	Function
Power Switch	A momentary switch, APCI compliant, used to toggle system power on/off.
Reset Switch	A momentary switch used to reset the system when it is in the power-on state.
NMI Switch	A momentary switch used to instruct the processor to copy system memory to hard disk.
System ID Switch	A momentary switch used to instruct the processor to toggle the state of the system ID LED.

4.4.2 Front Panel LEDs

The following table lists the LED specifications.

Table 17. LED Specifications

LED Function	LED Color	Peak Wavelength (nm)	Luminous Intensity Typ(mcd)	Luminous Intensity Min(mcd)
ID	White	N/A	8.9	4.5
	Blue	470	1.1	0.5
	Red	640	8.6	4.3
	Green	525	2.0	1.0
NIC	Green	560	4.3	1.7
ON	Green	560	4.3	1.7
DRV 1/0 Activity	Green	568	6.8	4.5
DRV 1/0 Fault	Red	625	7.9	4.0
DRV 1/0 Fault	Yellow	597	10.4	6.0
CRT	Red	627	8.9	3.0
	Yellow	590	11.4	4.5
MJR	Red	627	8.9	3.0
	Yellow	590	11.4	4.5
MNR	Yellow	580	3.3	1.6
PWR	Yellow	580	3.3	1.6

4.4.3 System Status LEDs

There are five FPIO system board system status LEDs. The function of these system status LEDs is described in the following table.

Table 18. Front Panel System Status LED Description

Status LED	Function
Power	The green *Power LED* indicates that system power is on when it is illuminated continuously. When it is blinking green, it indicates that the system is in ACPI sleep mode.
NIC0/NIC1	The green *NIC activity LED* indicates network link presence and activity on either NIC0 or NIC1.
System ID	The white or blue *NIC activity LED* is used to identify a particular system. The LED can be toggled remotely or with the System ID Switch.
Disk 0	The *green/amber/red hard drive 1 activity/fault LED* displays activity or fault status for hard disk drive 1.
Disk 1	The *green/amber/red hard drive 2 activity/fault LED* displays activity or fault status for hard disk drive 2.

4.4.4 System Fault LEDs

There are four front panel system fault LEDs. The function of these system fault LEDs is described in the following table.

Table 19. Front Panel System Fault LED Description

Fault LED	Function
Critical	This amber or red LED alarm is illuminated via BMC private I^2C bus and may only be turned off via BMC private I^2C control. When continuously lit, it indicates the presence of a Critical System Fault. A critical system fault is an error or event that is detected by the system with a fatal impact to the system. In this case, the system cannot continue to operate. An example could be the loss of a large section of memory, or other corruption, that renders the system not operational. The front panel critical alarm relay will be engaged.
Major	This amber or red major alarm is illuminated via BMC private I^2C bus and may be turned off via BMC private I^2C control or alarm connector reset. When continuously lit, it indicates the presence of a Major System Fault. A major system fault is an error or event that is detected by the system that has discernable impact to system operation. In this case, the system can continue to operate, but in a "degraded" fashion (reduced performance or loss of non-fatal feature reduction). An example could be the loss of one of two mirrored disks. The front panel major alarm relay will be engaged.
Minor	This amber LED minor alarm is illuminated via BMC private I^2C bus and may be turned off via BMC private I^2C control or alarm connector reset. When continuously lit, it indicates the presence of a Minor System Fault. A minor system fault is an error or event that is detected by the system but has little impact to actual system operation. An example would be a correctable ECC error. The front panel minor alarm relay will be engaged.
Power	The amber power alarm is illuminated via BMC private I^2C bus or SYS_FLT_LED_L signal and may only be turned off via BMC private I^2C control. When continuously lit, it indicates the presence of a Power System Fault. The front panel power alarm relay will be engaged.

4.4.5 LED Color Selection

Colors of the ID, disk fault, major alarm and critical alarm are configurable using 2 position .1 inch shunts/jumpers on header J7D1. The ID LED may be configured as blue or white. A white ID LED needs shunts across pins 3-4 and 5-6.

Table 20. LED Color Selection

Shunt	Pins	ON	OFF
ID Blue	1-2	N/C	Blue
ID Green	3-4	Green	off
ID Red	5-6	Red	off
Critical Alarm	7-8	Red	Yellow
Disk 0 Fault	9-10	Yellow	Red
Disk 1 Fault	11-12	Yellow	Red
spare	13-14		
spare	15-16		

4.4.6 System Fault Relays

The front panel board contains four relays. These relays are for power, critical, major and minor alarms. The relays are controlled by the SMBUS. See Section 4.4.7 for programming information. Section 4.6.4 describes the relay outputs.

4.4.7 I²C Interfaces

This section describes the programming of front panel board.

A PFC8574 remote 8-bit I/O expander on the private I²C bus controls the front panel alarms. All signals are active low. All outputs power up high (inactive). PFC8574 I²C address is 40 hex (write) and 41 hex (read). On system reset, all ones should be written to PFC8574 since the part does not provide a reset input pin.

Table 21. Front Panel Board I²C Interface Input/Output Bit Description

Bit	I/O	Name	Description
0	O	Power alarm	Writing 0 turns on the power alarm relay and illuminates the POWER LED, writing 1 turns both off. The relay and LED may also be turned on by a FAN_FAIL_L signal.
1	O	Critical alarm	Writing 0 turns on the critical alarm relay and illuminates the CRITICAL LED, writing 1 turns both off.
2	O	Major alarm	Writing a 1 to 0 edge will turn on the flip-flip that enables major alarm relay. Writing a 1 will turn off the major alarm relay or a MAJOR_RESET signal input. MAJOR LED in on when output is 0, off when output is 1.[3]
3	O	Minor alarm	Writing a 1 to 0 edge will turn on the flip-flip that enables major alarm relay. Writing a 1 will turn off the major alarm relay or a MINOR_RESET signal input. MINOR LED in on when output is 0, off when output is 1.[3]
4	I	Major alarm sense	Senses the state of the major alarm relay. 0 relay is on, 1 relay is off. This allows software to detect if the MAJOR_RESET signal was activated. Always write 1 during write operations.
5	I	Minor alarm sense	Senses the state of the minor alarm relay. 0 relay is on, 1 relay is off. This allows software to detect if the MINOR_RESET signal was activated. Always write 1 during write operations.
6	I	Critical/Major color	Writing a 1 turns CRITICAL and MAJOR LEDs to yellow, writing 0 color is RED. Strapping J7D1 pins 7-8 forces LEDs to RED. Resets to yellow.
7	I	Not used	Reserved for future use, always write 1 during write operations.

4.4.7.1 Temperature Sensor

The FPIO system board provides an LM95010 Single wire Interface temperature sensor that can be read by the ICH5R chipset on the server board.

[3] Normally closed (NC) and normally open (NO) relay contacts are provided on the rear panel Telco alarms connector. To activate the relay, a 1 to 0 transition must be written.

4.5 RJ-45 COM2 Port and USB Ports

4.5.1 RJ-45 COM2 RS-232 Port

The FPIO Board has provision for an RS-232C port using an RJ-45 connector. This is available for use at the front of the chassis. Grounding EMP_INUSE_L disables the rear COM2 port and enables the front port.

Table 22. RJ-45 (RS232-C) Pin-out

Pin #	I/O	Signal Name	Description
1	O	SPB_EMP_RTS_L	Request To Send
2	O	SPB_EMP_DTR_L	Data Terminal Ready
3	O	SPB_EMP_SOUT	Serial Out
4	PWR	GND	GND
5	I	EMP_INUSE_L	In Use
6	I	SPB_EMP_SIN	Serial In
7	I	SPB_EMP_DSR_L	Data Set Ready
8	I	SPB_EMP_CTS_L	Clear To Send

4.5.2 USB Port

The FPIO Board has provision for USB 1.1 for use at the front of the chassis. A single vertical stacked connector is used for connections.

Table 23. USB Pin-out

Pin #	I/O	Signal Name	Description
B1	PWR	VREG_FP_USBPWR	USB_PWR_2
B2	I/O	USB_DM4_FP	USB_BCK3_L
B3	I/O	USB_DP4_FP	USB_BCK3
B4	GND	VSS (GND)	VSS (GND)

4.6 Connector Information

The following table shows all the connectors on the FPIO system board, the interconnect used for each connector, and the destination for the interconnect. In addition, the first column references the location on the following figure of the connector location.

Table 24. FPIO Board Connections

FPIO Board Connections				
Loc	**Ref Des**	**Function**	**Interconnect**	**Connects to**
A	J5A2	IDE Connector	C91146	Baseboard J3K1
B	J2A1	Removable Media Connector	NA	CD-RW/DVD/Syscon I/F Board J1
C	J7A1	Fan Control Connector	C91147	Baseboard J3K6
D	J5B1	SCSI Connector	C91145	Baseboard J1E1
E	J9A2	Telco Alarms Connector	C91143	System rear panel
F	J1A1	Power Input Connector	NA	PDB harness P5
G	J7A2	Fan 4 Connector	NA	Fan 4 40mm
H	J8A1	Fan 3 Connector	NA	Fan 3 40mm
I	J8A2	Fan 2 Connector	NA	Fan 2 80mm
J	J9A2	Fan 1 Connector	NA	Fan 1 80mm
K	J9C1	SCSI Disk Drive 0 Connector	C12721	SCSI Disk 0
L	J5C1	SCSI Disk Drive 1 Connector	C12722	SCSI Disk 1
M	J4B1	USB Connector	C91148	Baseboard J1F1
O	J5A1	Front Panel Connector	C91144	Baseboard J1J1
P	J9D1	Stacked Serial/USB External Connector	NA	External devices

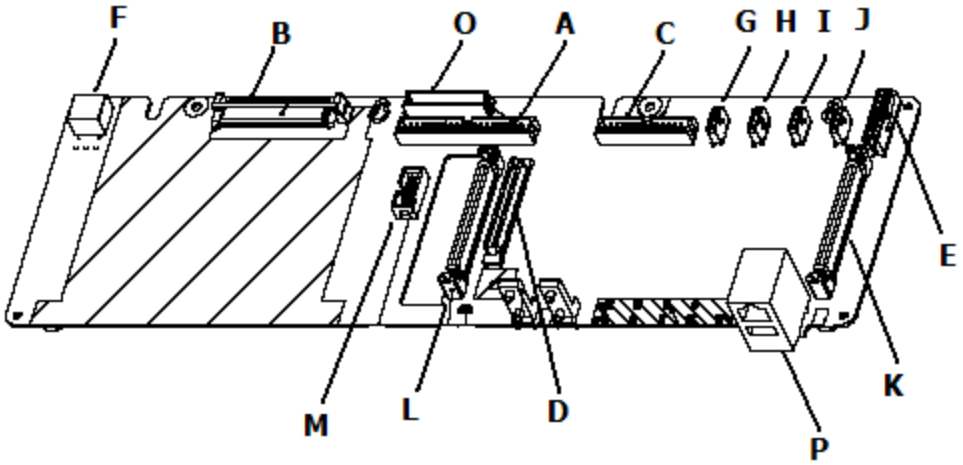


Figure 29: FPIO Connector Location

The IDE, SCSI, and USB connector pin-outs are industry standard and will not be given in this document. The 2x3 power connector pin-out is shown in the power supply section of this document and will not be shown here. The 2x34 pin blind-mate, the 2x13 fan, the 2x8 alarm, the 1x3 fan, and the 2x25 front panel connector pin-outs are shown in the following tables.

4.6.1 FPIO Board Front Panel Connector Pin-out

The following table details the pin-out of the front panel connector to the server board SE7520JR2.

Table 25. Front Panel J5A1 Connector

Pin	Front Panel Signal	Pin	Front Panel Signal
1	V_IO_RED_CONN_FP	2	GND
3	V_IO_GREEN_CONN_FP	4	GND
5	V_IO_BLUE_CONN_FP	6	GND
7	V_IO_HSYNC_BUFF_FP_L	8	GND
9	V_IO_VSYNC_BUFF_FP_L	10	GND
11	VIDEO_IN_USE	12	TEMP_PWM_R
13	SPB_DTR_L	14	SPB_DCD_L
15	SPB_RTS_L	16	SPB_CTS_L
17	SPB_SIN	18	SPB_SOUT
19	SPB_DSR_L	20	SPB_EN_L
21	FP_NMI_BTN_L	22	GND
23	LAN_ACT_A_L	24	LAN_LINKA_R
25	NC	26	FP_CHASSIS_INTRU
27	FP_ID_BTN_L	28	PS_I2C_5VSB_SCL
29	GND	30	PS_I2C_5VSB_SDA
31	FP_RST_BTN_L	32	LAN_ACT_B_L
33	FP_HDD_FLT_LED_R	34	LAN_LINKB_R
35	FP_PWR_BTN_L	36	FP_ID_LED_R
37	IPMB_I2C_5VSB_SCL	38	GND
39	IPMB_I2C_5VSB_SDA	40	P3V3
41	FP_PWR_LED_R	42	P5V_STBY
43	P5V_STBY	44	FP_STATUS_LED2_R
45	RST_IDE_L	46	FP_STATUS_LED1_R
47	HDD_LED_ACT_R	48	P5V
49	P5V_STBY	50	P5V_STBY

4.6.2 Fan 1x3 Connector Pin-out

The four fans all have the same wire harness, and the connector pin-out is shown in the following table.

Table 26. Fan 1x3 Connector

Pin	Signal
1	GND
2	Fan Speed Control
3	Fan Tachometer Signal

4.6.3 Fan 2x13 Connector Pin-out

One cable brings the fan speed control voltage to the FPIO board from the server board, and returns the fan tachometer signal from the FPIO board to the server board. This fan 2x13 connector pin-out is shown in the following table.

Table 27. Fan 2x13 Connector

Pin	Fan Signal	Pin	Fan Signal
1	BB_LED_FAN4_R	2	BB_LED_FAN2_R
3	BB_LED_FAN3_R	4	BB_LED_FAN1_R
5	ZZ_FANCON8	6	ZZ_FANCON4
7	ZZ_FANCON7	8	ZZ_FANCON3
9	ZZ_FANCON6	10	ZZ_FANCON2
11	ZZ_FANCON5	12	ZZ_FANCON4
13	GND	14	GND
15	GND	16	GND
17	FAN_SPEED_CNTL2	18	FAN_SPEED_CNTL1
19	FAN_SPEED_CNTL2	20	FAN_SPEED_CNTL2
21	BB_LED_FAN7_R	22	BB_LED_FAN5_R
23	BB_LED_FAN8_R	24	BB_LED_FAN6_R
25	NC	26	NC

4.6.4 Alarms Port Pin-out

The alarms port interface is a standard DB15-pin connector. Each alarm (major, minor, critical and power) is the output of a STDT relay contacts. A common contact with normally open and normally closed connections is included. Power alarm has only common and normally open contact outputs. The major and minor alarms contain external reset circuits.

Table 28. Alarms Connector

Pin	Signal
1	Minor reset positive
2	Minor reset negative
3	Major reset positive
4	Major reset negative
5	Critical alarm normally open
6	Critical alarm normally closed
7	Critical alarm common
8	Minor alarm normally open
9	Minor alarm normally closed
10	Minor alarm common
11	Major alarm normally open
12	Major alarm normally closed
13	Major alarm common
14	Power alarm normally open
15	Power alarm common

4.6.5 FPIO Board Blind-Mate 2x34 Connector Pin-out

The following table details the pin-out of the 2x34 blind-mate connector that is used to interface to the CD-RW/DVD/SysCon drive carrier assembly.

Table 29. 2x34 Blind-Mate Connector

Pin	Blind-Mate Signal	Pin	Blind-Mate Signal
1	NC_INDEX_L	35	+5V
2	NC_DS0_L	36	+5V
3	NC_DSKCHG_L	37	+5V
4	GND	38	NC_RDY_L
5	NC_MTR_L	39	GND
6	NC_WDATA_L	40	USB_P3
7	NC_WGATE_L	41	USB_P3_L
8	GND	42	GND
9	NC_TRK0_L	43	GND
10	NC_RDATA_L	44	FD_DENSEL0_L
11	NC_HDSEL_L	45	FD_DENSEL1_L
12	GND	46	BM_SPARE
13	IDE_RST_L	47	GND
14	IDE_PDD7	48	IDE_PDD8
15	IDE_PDD6	49	IDE_PDD9
16	GND	50	IDE_PDD10
17	IDE_PDD5	51	GND
18	IDE_PDD4	52	IDE_PDD11
19	IDE_PDD3	53	IDE_PDD12
20	GND	54	IDE_PDD13
21	IDE_PDD2	55	GND
22	IDE_PDD1	56	IDE_PDD14
23	IDE_PDD0	57	IDE_PDD15
24	GND	58	GND
25	IDE_PDDREQ	59	IDE_CSEL_P
26	GND	60	IDE_PDIOR_L
27	IDE_PDIOW_L	61	GND
28	GND	62	IDE_PIORDY
29	IDE_PIRQ_P	63	GND
30	IDE_PDA1	64	IDE_PDDACK_L
31	IDE_PDA0	65	IDE_CBL_DET
32	GND	66	IDE_PDA2
33	IDE_PDCS0_L	67	GND
34	IDE_PRI_HD_ACL_L	68	IDE_PDCS1_L

4.7 IDE Bus

There is an IDE connector on the FPIO system board for interfacing to the IDE bus on the server board SE7520JR2. The IDE bus on the FPIO system board is routed from this connector to the 2x34 blind-mate connector for interfacing to the CD-RW/DVD/SysCon carrier assembly. Pin definitions for the 2x34 blind-mate connector are shown in Table 29 above. The IDE bus is ULTRA DMA mode two (DMA33) capable.

4.8 SCSI Subsystem

The SCSI subsystem on the FPIO board is designed to give the end user support for two SCSI hot-plug hard drives. The design enables easy use and replacement of the SCSI hard drives without powering down the system. The following block diagram and functional description will give a general idea of how the FPIO SCSI subsystem works.

4.8.1 FPIO Board SCSI Subsystem Block Diagram

The block diagram in Figure 30 illustrates the general architecture of the FPIO SCSI subsystem. The physical and functional blocks of the FPIO SCSI subsystem are shown, with arrows representing buses and signals, and the blocks representing the functional parts of the SCSI subsystem.

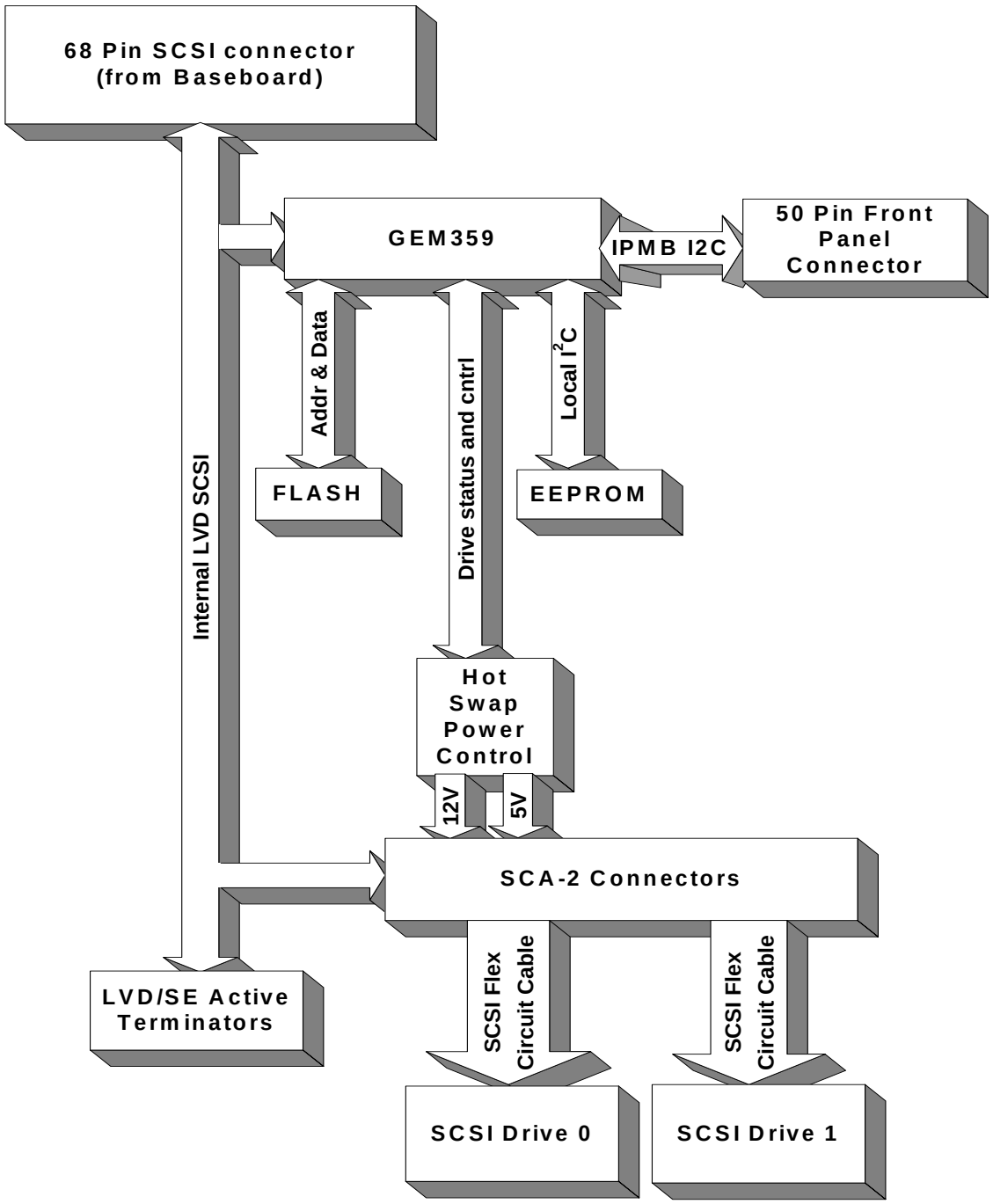


Figure 30: FPIO Board SCSI Subsystem Block Diagram

4.8.2 SCSI Bus

The FPIO SCSI subsystem passes the SCSI bus from the server board SE7520JR2 to the internal SCSI drives. The SCSI bus is Ultra 320 (SPI-4) capable. SE drives are not supported. SE drives should not be installed as the behavior of the drives is unpredictable and data corruption could result. The bus is comprised of 68 signals. The bus clock is 80 MHz. The 320 Mbytes data rate results from double transition (DT) data transfers on a two byte wide bus. The SCSI bus attaches to the server board SE7520JR2 via a 68-pin SCSI connector.

320 Mbytes/s = 2 byte bus * 80 MHz clock * double transitions.

NOTE: The SCSI drives and SCSI controller on the server board SE7520JR2 determine actual SCSI bus data rate.

4.8.3 FPIO SCSI Drive Power Control

SCSI Power Control is provided by the FPIO SCSI subsystem. SCSI Power Control includes SCSI drive power switching, over-current protection, system status notification, and SCSI drive status LEDS.

If a SCSI drive is detected, the system will be notified. Then the system will instruct the FPIO SCSI subsystem to apply power to the internal SCSI drive. Status LEDs will provide the user with visual indicators for the internal SCSI drive.

Once the system is powered up, the user can request the system to remove power to a SCSI drive. The system will instruct the FPIO SCSI subsystem to remove power from the internal SCSI drive. The user can then safely remove the internal SCSI drive. Upon reinserting an internal SCSI drive, the user must notify the system. The system will then instruct the FPIO SCSI subsystem to apply power to the specified drive.

4.8.4 Internal SCSI Drive Power Switching

Each SCSI drive is supplied with +12 V and +5 V. Separate MOSFET switches apply and remove the +12 V and +5 V to each internal SCSI drive.

4.8.5 Initial Soft Power-On

When power is first applied to a SCSI drive there is a large initial current surge (up to 20 Amps). At turn-on, the gate of each external N-Channel MOSFET is charged with a 10μA current source. Capacitors on each gate create a programmable ramp (soft turn-on) to control inrush currents.

4.8.6 Over-current Protection

If either of the drive's power rails exceeds 5 amps, the MOSFET switch for the problematic rail will be turned off. Removing power will protect the MOSFET and system from damage in the event of a short on one of the power rails. After one third of a second the MOSFET will be turned on to see if the short has been removed. Turning on and checking for a short every one third of a second will continue until the system instructs the FPIO SCSI subsystem to remove power or the fault disappears.

When the MOSFET is first enabled, the over current condition is not detected for the first 640 nS period. This no OCP period allows the initial current surge produced by many SCSI drives. The 640 nS period is short enough not allowing damage to occur to the MOSFETS or the system.

4.8.7 Power Control Inter-Lock

The power control inter-lock prevents drives from powering on at the same time. Since only one drive can power on at once the board power requirements can be kept lower. After one drive starts the next drive will start one third of a second later.

4.8.8 System Status Notification

Internal SCSI drive status information is collected by the micro-controller. The micro-controller passes the information to the Server Management via the global I^2C bus and Enclosure Management via the SCSI bus.

4.8.9 FPIO SCSI Subsystem Status LEDs

The status LEDs give the user a visual indication of the drives' condition. There is a single LED for each drive. The LEDs are bi-colored and use a combination of color and blinking frequency to indicate multiple conditions. The LEDs are mounted on the FPIO board, and the light is directed to the front panel through the use of a light pipe assembly. See Table 30 for LED activity definitions. See the Firmware EPS for definitions of the different blink rates.

Table 30. LED Activity Definitions

LED State	Drive Active	Fault Condition
Solid Green		
Blinking Green	X	
Blinking Yellow/Green		X
Blinking Yellow/Blank		X
Blank		

4.8.10 FPIO SCSI Subsystem Enclosure Management

SCSI Enclosure Management allows the FPIO SCSI subsystem to report on SCSI drive status via the SCSI bus. Normally a RAID controller will interface with Enclosure Management. The SCSI Enclosure Management subsystem consists of a Qlogic* GEM359 controller, Flash, and Programmable Logic Device (PLD).

4.8.10.1 Qlogic* GEM359 Enclosure Management Controller

The GEM359 sends acquired board information to the SCSI bus and IPMB bus. The GEM359 also acts on requests from both the SCSI bus and IPMB bus. GEM359 GPIOs send LED and drive power control. Please see the GEM359 firmware EPS for further information.

4.8.10.2 4 Meg Flash

The GEM359's code is stored in a 4 Meg FLASH (512K x 8). The FLASH boot block is stored in the top block. The boot block is normally protected. Non-protected FLASH can be updated via the IPMB bus.

4.8.11 Server Management Interface

The FPIO SCSI subsystem will support the following Server Management features:

Local I²C Interface

- SCSI subsystem Field Replaceable Unit (FRU)
- Micro-controller interface

System I²C Interface

- Micro-controller IPMB interface

4.8.11.1 Local I²C Bus

The local I²C bus has an Atmel* AT24C02N (or equivalent) serial EEPROM to the micro-controller.

4.8.11.2 Global I²C Bus (IPMB)

The global I²C bus connects the micro-controller to the system. The micro-controller is isolated from the system until the system PWRGRD signal is asserted.

4.8.11.3 I²C Addresses

Three I²C devices and their addresses are listed in Table 31 and Table 32. There are two I²C devices that can be addressed on or through the FPIO SCSI subsystem.

- Hot-swap Micro Controller
- FPIO SCSI subsystem FRU EEPROM

Table 31. I²C Local Bus Addresses

Device	Address	Bus/Location	Description
AT24C02	0xA0	Legacy I²C/ SCSI backplane	Private SCSI backplane FRU EEPROM

Table 32. I²C Global Bus Addresses (IPMB Bus)

Device	Address	Bus/Location	Description
GEM359	0xC0-0xCF	Legacy I²C/ SCSI backplane	Micro controller public IPMB bus

4.8.12 Power Good Circuit

Power Good are positive logic signals reflecting the status of various power rails.

4.8.12.1 Power Good Outputs

On board Power Good circuits monitor both the 12-V and 5-V rails. When the +5-V rail is within +/-5% of +5 V, the 5-volt Power Good signal is asserted. When the 12-V signal is greater than 12 V –5%, the 12-volt Power Good signal is asserted. Both detection circuits have built in hysteresis to prevent chatter. The 5-V and 12-V Power Good signals are ANDED together (via the PLD) to generate the SCSI_V_GOOD output signal.

4.8.12.2 Power Good Inputs

The Power Good input tells the FPIO SCSI subsystem that the system power supply is powered up and working within specifications.

4.8.13 Reset Control

The Reset signal resets the GEM micro-controller only on power up.

4.8.14 SCA2 Connector Interlocks

The SCA2 connectors on the FPIO SCSI subsystem have interlocks. Interlock is used by the FPIO SCSI subsystem to determine if a SCSI device is present. Drive presence is used by enclosure management.

4.8.15 Clock Generation

A single 10MHz clock on the FPIO supplies clock input to the GEM359.

4.8.16 Programmable Devices

There are two programmable devices on the FPIO SCSI subsystem. These are described below.

4.8.16.1 FLASH

Flash contains program code to be run by the onboard micro-controller.

Memory configuration: 512 K x 8

4.8.16.2 Field Replaceable Unit (FRU)

The FRU is programmed during manufacture during In Circuit Test (ICT).

Memory Configuration: 2 k serial

4.8.17 Signal Descriptions

The following notations are used to describe the signal type, from the perspective of the FPIO SCSI subsystem:

I	Input pin to the SCSI subsystem
O	Output pin from the SCSI subsystem
I/O	Bi-directional (input/output) pin
PWR	Power Supply pin

The signal description also includes the type of buffer used for the particular signal:

LVD	Low Voltage Differential SCSI
SE	Standard Single Ended SCSI
TTL	5V TTL signals
CMOS	5V CMOS signals
3.3V CMOS	3.3V CMOS signals
Analog	Typically a voltage reference or specialty power supply

4.8.17.1 LVD SCSI Connectors

The LVD connector carries signals between the FPIO SCSI bus and internal SCSI drives through the SCSI flex circuit cables. The LVD SCSI bus's signals are driven by either the server board SCSI controller, the LVD/SE transceiver, or the internal SCSI drives. Table 33 provides a description of each signal on the SCSI connectors.

Table 33. LVD SCSI Bus Signals – J9D1, J5D1, J5B1

Signal	Type	Driver	Name and Description
DB_[15..0][P, N]	I/O	LVD/ SE	**SCSI Data Bus.** These pins, with the DBP[1/0][P/N] pins form the bi-directional SCSI data bus.
DB_P0[P, N] DB_P1[P, N]	I/O	LVD/ SE	**SCSI Data Parity.** These pins support parity on the SCSI bus. DBP0[P/N] supports parity for data [7..0] DBP1[P/N] supports parity for data [15..8]
DIFFSENSE	I	Analog	**Differential Sense.** This pin monitors the DIFFSENSE signal from the terminator. The voltage level determines the operating mode of the target devices on the SCSI bus. If the voltage on the DIFFSENSE signal is from –0.35 V to +0.5 V the mode will be SE. If it is from +0.7 V to 1.9 V the mode will be LVD.
ATN_[P, N]	I/O	LVD/ SE	**SCSI Bus Attention.** These pins are asserted by a SCSI device in initiator mode to alert the target that the initiator has a message to transfer.
BSY_[P, N]	I/O	LVD/ SE	**SCSI Bus Busy.** In SE mode, these pins are bi-directional and are asserted to gain use of the SCSI bus and to indicate that that SCSI bus is in use.
ACK_[P, N]	I/O	LVD/ SE	**SCSI Bus Acknowledge.** These pins are asserted by a SCSI device in initiator mode to acknowledge the target's request for a data transfer.
RST_[P, N]	I/O	LVD/ SE	**SCSI Bus Reset.** In SE mode, these pins are bi-directional and are asserted when all the SCSI devices attached to the SCSI bus need to be reset.
MSG_[P, N]	I/O	LVD/ SE	**SCSI Bus Message Phase.** These pins are asserted by a SCSI device in target mode to indicate the Message In or Message Out phase.
SEL_[P, N]	I/O	LVD/ SE	**SCSI Bus Select.** In SE mode, these pins are bi-directional and are asserted by the controller when attempting to select or reselect a SCSI device.
CD_[P, N]	I/O	LVD/ SE	**SCSI Bus Control/Data Phase.** These pins are asserted or de-asserted by a SCSI device in target mode to indicate that control or data information is being transferred over the SCSI bus

Signal	Type	Driver	Name and Description
REQ_[P, N]	I/O	LVD/ SE	**SCSI Bus Request.** These pins are asserted by a SCSI device in target mode to indicate that the target is requesting a data transfer over the SCSI bus.
IO_[P, N]	I/O	LVD/ SE	**SCSI Bus I/O Phase.** These pins are asserted by a SCSI device in target mode to indicate the direction of data movement on the SCSI bus between the target and the initiator.
SCSI_ID	O	GND/OPEN	**SCSI ID.** Sets internal SCSI ID depending on slot. Drive 0 has SCSI address 0. Drive 1 has SCSI address 1.
MATED [1,2]	I/O	TTL	**SCSI MATED.** Pins are used to determine if SCSI is present and has proper contact. See T10/1302D Annex C for additional information.
GND	I/O	PWR	**Ground. These pins provide Secondary Ground reference.**
P12V	O	PWR	**+12-V supply.** Max 1 amp of continuous current. Max 6 amps peak current.
P5V	O	PWR	**+5-V supply.** Max 1.4 amps of continuous current. Max 6 amps peak current.

4.8.18 Internal Logic Signals

Table 34 is a summary of the signals that route between logic that is contained in the FPIO SCSI subsystem.

Table 34. Internal Logic Signals

	Signal	Type	Driver	Name and Description
Clks	CLK_20MHZ	O	CMOS	**20-MHz Clock.** This signal is the 20-MHz clock used by the GEM359 and PLD.
GEM359 Logic Contrl	ADDR<16..0>	O	CMOS	**Address/Bus.** These pins are used as address bus for the FLASH.
	PROM_VPP_L	O	CMOS	**FLASH PROGRAM VOLTAGE ENABLE.** This pin in driven by the S870BN4 SCSI backplane GEM359 to all FLASH to be programmed.
	PROM_OE_L	O	CMOS	**FLASH Output Enable.** This pin is driven by the S870BN4 SCSI backplane GEM359 to enable the Flash for writing data on the bus.
	PROM_WE_L	I	CMOS	**FLASH Chip Enable.** This pin is driven by the S870BN4 SCSI backplane GEM359 to enable the Flash to be written to.
Misc. Logic	5V_RST_N	O	TTL	**5-V reset.** This signal is driven by micro controller reset chip. Output is asserted low for 150 ms after +5 V returns to an in-tolerance condition (+/- 5%).
	POWER_GD	O	TTL	**Power Good.** Asserted high when 5-V supply is with in tolerance and system power good is asserted.

4.9 Specifications

4.9.1 Electrical Specifications

DC specifications for the TIGI2U front panel board power connectors are summarized in this section excluding disk drive power. All power rails must operate within +/- 5% voltage range.

Table 35. Maximum Power Requirements (mA)

12V	5V	3.3V	+5V_STBY
20(mA)	186(mA)	384(mA)	184(mA)

Maximum current on +5V_STBY with all LEDs illuminated and relays energized, is 320 mA. The typical current with no LEDs illuminated or relay energized is 150 mA. Note: Software limits 2 alarms active at once power fault and one of major, minor or critical alarms.

Alarms connector relay contacts are rated at 1 A with a maximum rating of 30 W (DC) / 60 VA (AC).

Alarms connector external alarm (major and/or minor) reset is an optoisolated input that is reverse voltage protected. A voltage of 3.3 V to 48 V input with a pulse width of at least 200 ms is required to activate the alarm-reset function. Maximum current is 12 mA.

4.9.2 Mechanical Specifications

The following figure shows the mechanical specifications of the TIGI2U front panel board. All dimensions are given in inches.

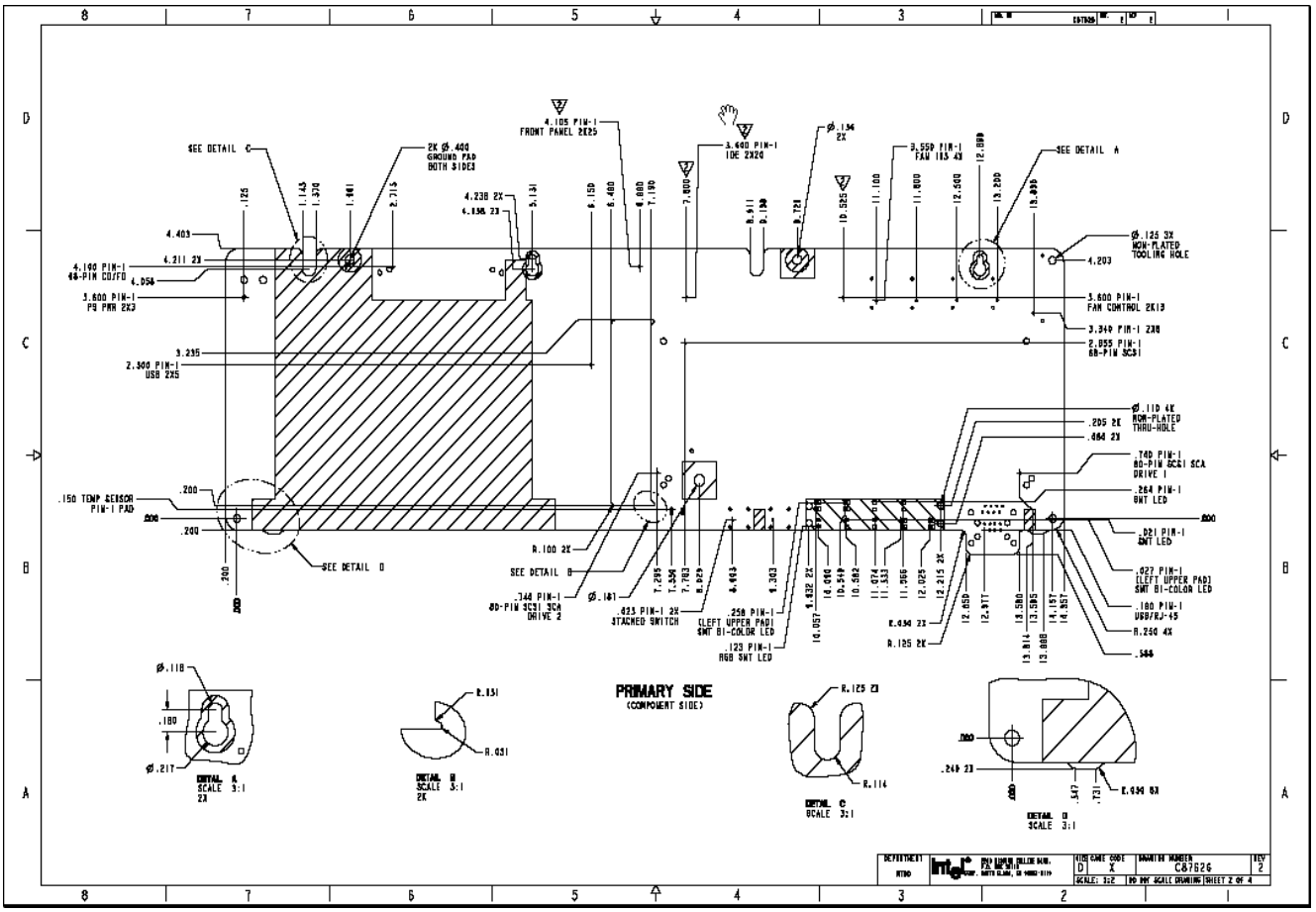


Figure 31. Front Panel Board Mechanical Specifications

5. Interconnect System Board (with SysCon Device)

This chapter describes the basic functions and interface requirements of the interconnect system board that is designed for the TIGI2U server system.

5.1 Features

- Used for CD-RW/DVD connections to Main System Board, (IDE Controller)
- Blind-mate connector for connection to FPIO system board
- IDE connector and power connector for interfacing with the CD-RW/DVD Drive
- Embedded USB Flash Memory Controller with up to 128 Mbyte, (2 Devices)

5.2 Chapter Structure and Outline

The information contained in this chapter is organized into four sections. The information is presented in a modular format, with numbered headings for each major topic and subtopic. The content of each section is summarized as follows:

Section 5.3: Functional Description of Interface Board
Provides an overview of the TIGI2U FPIO board and a physical board layout diagram.

Section 5.4: Connector Descriptions
Provides connector descriptions for all connectors on the interface board.

5.3 Functional Description of Interface Board

The interface board is used in both the CD-RW/DVD drive carrier assembly as the signal and power interface between the CD-RW/DVD drive and the FPIO system board. The interface board has standard IDE and power connectors for interfacing to the CD-RW/DVD drive, and has a high-density blind-mate connector for interfacing to the FPIO system board. These connectors are identified in Figure 32 Description of Interface Board. All IDE bus signals, +5v, and GND are routed from the FPIO board through the blind-mate connector to the appropriate connector on the interface board. Additionally, the USB signals required for the SysCon device are also routed through the blind-mate connector.

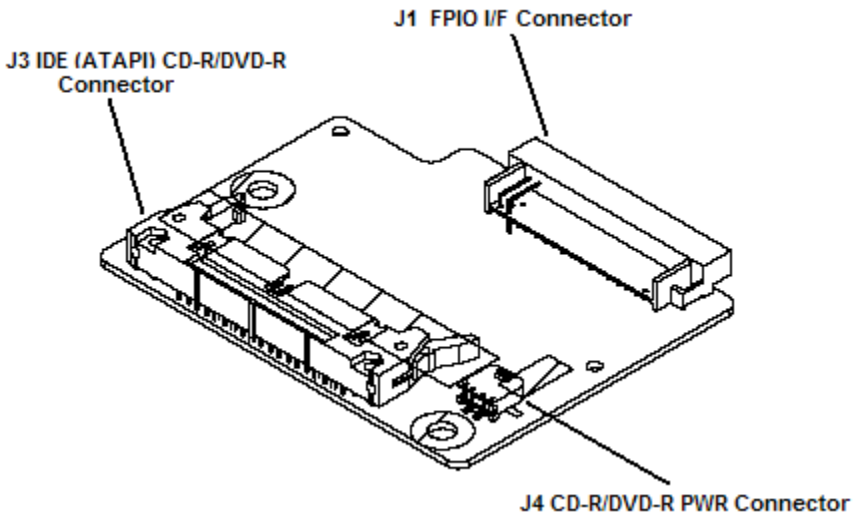


Figure 32 Description of Interface Board

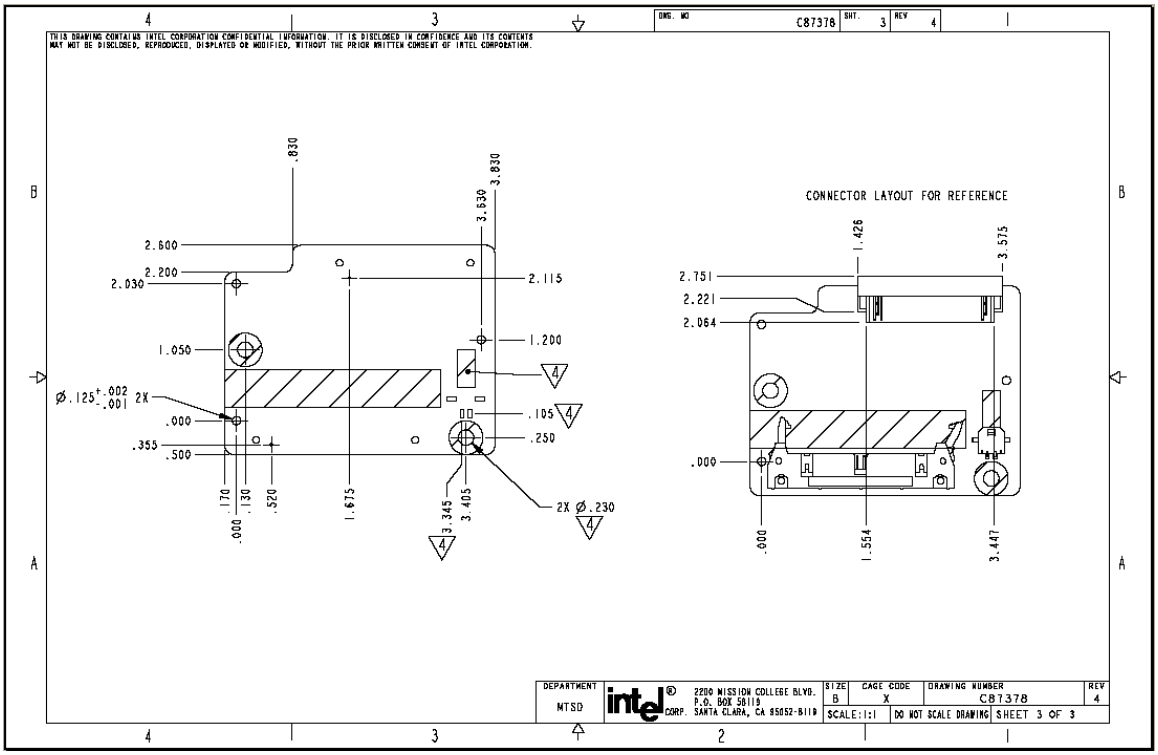


Figure 33 Dimensions of Interface Board

5.4 Connector Description

5.4.1 Interface Board Blind-Mate 2x34 Connector Pin-out

The following table details the pin-out of the 2x34 blind-mate connector that is used to interface to the FPIO Board.

Table 36. 2x34 Blind-Mate Connector

Pin	Blind-Mate Signal	Pin	Blind-Mate Signal
1	NC_J1_1	35	+5V
2	NC_J1_2	36	+5V
3	NC_J1_3	37	+5V
4	GND	38	NC_J1_38
5	NC_J1_5	39	GND
6	NC_J1_6	40	USB_P
7	NC_J1_7	41	USB_M
8	GND	42	GND
9	NC_J1_9	43	GND
10	NC_J1_10	44	NC_J1_44
11	NC_J1_11	45	NC_J1_45
12	GND	46	NC_J1_46
13	IDE_RST_L	47	GND
14	IDE_PDD7	48	IDE_PDD8
15	IDE_PDD6	49	IDE_PDD9
16	GND	50	IDE_PDD10
17	IDE_PDD5	51	GND
18	IDE_PDD4	52	IDE_PDD11
19	IDE_PDD3	53	IDE_PDD12
20	GND	54	IDE_PDD13
21	IDE_PDD2	55	GND
22	IDE_PDD1	56	IDE_PDD14
23	IDE_PDD0	57	IDE_PDD15
24	GND	58	GND
25	IDE_PDDREQ	59	IDE_CSEL_P
26	GND	60	IDE_PDIOR_L
27	IDE_PDIOW_L	61	GND
28	GND	62	IDE_PIORDY
29	IDE_PIRQ_P	63	GND
30	IDE_PDA1	64	IDE_PDDACK_L
31	IDE_PDA0	65	IDE_CBL_DET
32	GND	66	IDE_PDA2
33	IDE_PDCS0_L	67	GND
34	IDE_DASP_L	68	IDE_PDCS1_L

5.4.2 Interface Board CD-RW/DVD 1x2 Power Connector Pin-out

The following table details the pin-out of the 1x2 power connector that is used to interface to the CD-RW/DVD interface board.

Table 37. J4 1x2 CD-RW/DVD Power Connector

Pin	Power Signal	Pin	Power Signal
1	GND	2	+5V

5.4.3 Interface Board CD-RW/DVD 2x20 IDE Connector Pin-out

The following table details the pin-out of the CD-RW/DVD 2x20 IDE connector that is used to interface the IDE signals to the CD-RW/DVD drive interface board.

Table 38. J3 2x20 IDE Connector Pin-out

Pin	IDE Signal	Pin	IDE Signal
1	IDE_RST_L	2	GND
3	IDE_DD7	4	IDE_DD8
5	IDE_DD6	6	IDE_DD9
7	IDE_DD5	8	IDE_DD10
9	IDE_DD4	10	IDE_DD11
11	IDE_DD3	12	IDE_DD12
13	IDE_DD2	14	IDE_DD13
15	IDE_DD1	16	IDE_DD14
17	IDE_DD0	18	IDE_DD15
19	GND	20	KEY – Pin Pulled
21	IDE_PDDREQ	22	GND
23	IDE_PDIOW_L	24	GND
25	IDE_PDIOR_L	26	GND
27	IDE_PIORDY	28	GND
29	IDE_PDDACK_L	30	GND
31	IDE_PIRQ_L	32	TP
33	IDE_PDA1	34	IDE_CBL_DET_P
35	IDE_PDA0	36	IDE_PDA2
37	IDE_PDCS0_L	38	IDE_PDCS1_L
39	IDE_DASP_L	40	GND

5.5 CD-RW/DVD Connectors

The ½" slim line CD-RW/DVD uses a 50-pin JAE signal/power interface connector. The pin-out is listed in the following table.

Table 39. CD-RW/DVD JAE Signal / Power Connector Pin-out

Pin	Signal	Signal	Pin
1	Audio L-Ch	Audio R-Ch	2
3	Audio GND	GND	4
5	RESET-	DD8	6
7	DD7	DD9	8
9	DD6	DD10	10
11	DD5	DD11	12
13	DD4	DD12	14
15	DD3	DD13	16
17	DD2	DD14	18
19	DD1	DD15	20
21	DD0	DMARQ	22
23	GND	/DIOR	24
25	DIOW-	GND	26
27	IORDY	/DMACK	28
29	INTRQ	/IOCS16	30
31	DA1	/PDIAG	32
33	DA0	DA2	34
35	/CS1FX	/CS3FX	36
37	/DASP	+5V	38
39	+5V	+5V	40
41	+5V	+5V	42
43	GND	GND	44
45	GND	GND	46
47	CSEL	GND	48
49	RESERV	RESERV	50

A small interface board is connected to the 50-pin JAE signal/power interface connector on the CD-RW/DVD. This small interface board has three connectors: 1) The mating 50-pin JAE signal/power interface connector to the one on the CD-RW/DVD drive, 2) A 2x20 IDE connector for interfacing via a standard IDE cable to the 2x20 IDE connector contained on the interconnect board, and 3) a 1x2 power connector for interfacing via a two wire power cable to the 1x2 power connector on the interconnect board.

5.6 Embedded Flash Memory Function (SysCon Device)

The USB97C242 is a USB 2.0 Bulk Only Mass Storage Class Peripheral Controller intended for supporting SmartMedia* (SM) and NAND* flash memory devices. It provides a single chip solution for the SM and NAND flash devices in the market.

The device consists of a USB 2.0 PHY and SIE, buffers, Fast 8051 microprocessor with expanded scratchpad, and program SRAM, 48KB program ROM and SM controller and provides 64MB of flash memory.

Provisions for optional external Flash Memory up to 64K bytes for program storage is provided.

12K bytes of scratchpad SRAM and 768 Bytes of program SRAM are also provided.

Seven GPIO pins are for the 100-pin device. Provisions are made to allow dynamic attach and re-attach to the USB bus to allow hot swap of flash media to be implemented.

Datasheet

Product Features

- 2.5 Volt, Low Power Core Operation
- 3.3 Volt I/O with 5V input tolerance
- Complete USB Specification 2.0 Compatibility
  - Includes USB 2.0 Transceiver
  - A Bi-directional Control and a Bi-directional Bulk Endpoint are provided.
- Complete System Solution for interfacing SmartMedia (SM), and NAND flash devices to USB 2.0 bus
  - Supports USB Bulk Only Mass Storage Compliant Bootable BIOS
  - Support for the following devices:
    - SM: 2M –15MB/sec
    - NAND Flash: 2M – 15MB/sec
  - Built-in hardware 1-bit ECC support.
- 8051 8 bit microprocessor
  - Provides low speed control functions
  - 30 Mhz execution speed at 4 cycles per instruction average
  - 12K Bytes of internal SRAM for general purpose scratchpad
  - 768 Bytes of internal SRAM for general purpose scratchpad or program execution with external flash
- Double Buffered Bulk Endpoint
  - Bi-directional 512 Byte Buffer for Bulk Endpoint
  - 64 Byte RX Control Endpoint Buffer
  - 64 Byte TX Control Endpoint Buffer
- Internal or External Program Memory Interface
  - 48K Byte Internal Code Space or optional 64K Byte External Code Space using Flash, SRAM, or EPROM memory.
- On Board 12Mhz Crystal Driver Circuit
- Internal PLL for 480Mhz USB2.0 Sampling, 30Mhz MCU clock
- Supports firmware upgrade via USB bus if sector-erasable Flash program memory is used
- 7 GPIOs for special function use: LED indicators, button inputs, power control to memory devices, etc.
  - Inputs capable of generating interrupts with either edge sensitivity
- 100 Pin TQFP (12x12x1.4 body) package

6. PCI-X Riser Board

This chapter describes the design and external interface of the TIGI2U PCI-X riser board. Features of the PCI-X riser board include:

- Three 3.3 V 64-bit PCI slots

6.1 Chapter Structure and Outline

The information contained in this chapter is organized into four sections. The information is presented in a modular format, with numbered headings for each major topic and subtopic. The content of each section is summarized as follows:

Section 6.2: Introduction:
Provides an overview of the TIGI2U PCI-X riser board, showing primary components and their relationships, and physical board layout diagrams.

Section 6.3: Functional Description:
Provides a functional description of the PCI-X riser board.

Section 6.4: Connector Interface:
Gives signal descriptions and the corresponding electrical parameters for each input and output of a given connector.

Section 6.5: Specifications:
Describes the electrical, environmental and mechanical specifications.

6.2 Introduction

The PCI-X riser card supports three 3.3 V 64-bit slots. The bus speed varies from 66MHz to 100MHz depending on the type and number of PCI adapters configured in the PCI-X riser card. This is described in the Server board SE7520JR2 specification.

Figure 34 is a drawing of the riser board.

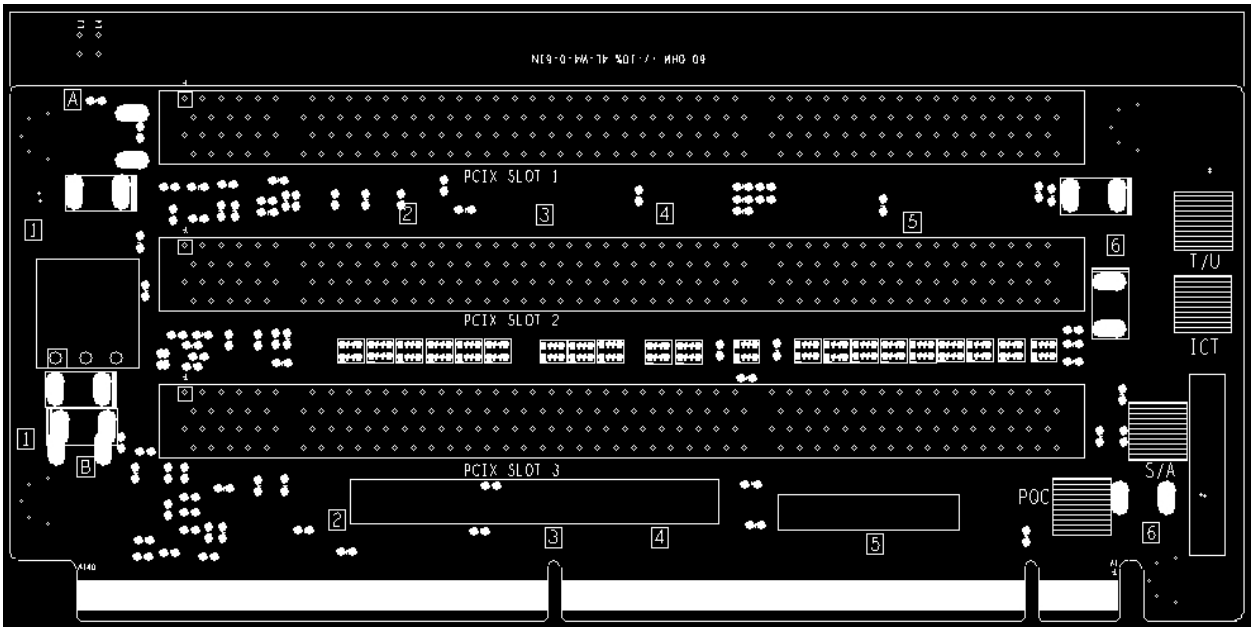


Figure 34. PCI-X Riser Board Layout

6.3 Functional Description

The PCI-X riser card has three 64-bit slots with a maximum bus speed of 100MHz.

IDSELs are AD24 for slot 1, AD25 for slot 2 and AD26 for slot 3.

6.4 Connector Interface

Table 40 describes the common signals between the edge fingers and all of the slots.

Table 40. Riser Card Slot Pin-out Common Signals

Pin-Side B	PCI Spec Signal	Description	Pin-Side A	PCI Spec Signal	Description
140	12V		140	12V	
139	12V		139	12V	
138	Ground		138	GND	
137	-12V		137	3.3VAux	375ma per slot and 3 slots
136	12V		136	Wake#	
135	GND		135	12V	Two slots = 4 amps
134	REFCLK2+	FL-3GIO Slot 2/PXH - DIF5P	134	3.3V	
133	REFCLK2+	FL-3GIO Slot 2/PXH - DIF5N	133	PERST_N	
132	GND		132	GND	1 amp per pin

Pin-Side B	PCI Spec Signal	Description	Pin-Side A	PCI Spec Signal	Description
131	GND		131	REFCLK1 +	FL-3GIO Slot 1 – DIF4P
130	HSOp(0)		130	REFCLK1 +	FL-3GIO Slot 1 – DIF4N
129	HSOn(0)		129	GND	
128	GND		128	HSIp(0)	
127	GND		127	HSIn(0)	
126	HSOp(1)		126	GND	
125	HSOn(1)		125	GND	
124	GND		124	HSIp(1)	
123	GND		123	HSIn(1)	
122	HSOp(2)		122	GND	
121	HSOn(2)		121	GND	
120	GND		120	HSIp(2)	
119	GND		119	HSIn(2)	
118	HSOp(3)		118	GND	
117	HSOn(3)		117	GND	
116	GND		116	HSIp(3)	
115	GND		115	HSIn(3)	
114	HSOp(4)		114	GND	
113	HSOn(4)		113	GND	
112	GND		112	HSIp(4)	
111	GND		111	HSIn(4)	
110	HSOp(5)		110	GND	
109	HSOn(6)		109	GND	
108	GND		108	HSIp(5)	
107	GND		107	HSIn(5)	
106	HSOp(6)		106	GND	
105	HSOn(6)		105	GND	
104	GND		104	HSIp(6)	
103	GND		103	HSIn(6)	
102	HSOp(7)		102	GND	
101	HSOn(7)		101	GND	
100	GND		100	HSIp(7)	
99	+5V		99	HSIn(7)	
98	INTB#	This pin will be connected on the 2U riser to INT_B# of the bottom PCI slot, INT_A# of the middle slot and INT_D# of the top slot.	98	GND	
97	INTD#	This pin will be used by 1U/2U riser to bring the INT_B# interrupt from the top and INT_C# from the middle PCI slot down to the baseboard.	97	ZCR_PRSNT_L	From TDI of lowest slot only
96	+5V		96	+5V	

Pin-Side B	PCI Spec Signal	Description	Pin-Side A	PCI Spec Signal	Description
95	Reserved	SLOT_ID_FL, not required as the risers are unique.	95	+5V	
94	+5V		94	ZCR_MSKID_L	From TMS of lowest slot only
93	IOP INTA	SCSI Interrupt A to ZCR. This pin will be used by 1U/2U riser to bring the INT_C# interrupt on the bottom PCI slot down to the baseboard	93	+5V	
92	IOP INTB	SCSI Interrupt B to ZCR. This pin will be used by 1U/2U riser to bring the INT_D# interrupt on the bottom PCI slot down to the baseboard	92	INTA#	This pin will be connected on the 2U riser to INT_A# of the bottom PCI slot, INT_D# of the middle slot and INT_C# of the top slot.
91	GND		91	INTC#	This pin will be used by 1U/2U riser to bring the INT_A# interrupt from the top and INT_B# from the middle PCI slot down to the baseboard.
90	CLK3	Highest PCI Slot (SLOT3)	90	GND	
89	GND		89	REQ3#	Highest PCI Slot (SLOT3)
88	CLK2	Middle PCI Slot (SLOT2)	88	GND	
87	GND		87	GNT3#	Highest PCI Slot (SLOT3)
86	REQ2#	Middle PCI Slot (SLOT2)	86	GND	
85	GND		85	RST#	
84	Reserved		84	GND	
83	GND		83	Reserved	
	KEY			KEY	
	KEY	End of x16 PCI-Express connector		KEY	
82	Reserved		82	+5V	Was Vio 3.3V or 1.5V
81	GND		81	Reserved	
80	CLK1	Lowest PCI slot (SLOT1)	80	GND	
79	Ground		79	GNT2#	Middle PCI Slot (SLOT2)
78	REQ1#	Lowest PCI slot (SLOT1)	78	+3.3V	Was Vio 3.3V or 1.5V
77	+3.3V	Was Vio 3.3V or 1.5V	77	GNT1#	Lowest PCI slot (SLOT1)
76	PME2#	active riser only, PME needed per PCI segment, reserved for passive riser	76	Ground	
75	AD[31]		75	PME1#	for passive slots on both passive and active riser
74	AD[29]		74	PME3#	active riser only, PME needed per PCI segment reserved for passive riser
73	Ground		73	AD[30]	AD[31]
72	AD[27]		72	+3.3V	
71	AD[25]		71	AD[28]	
70	+3.3V		70	AD[26]	
69	C/BE[3]#		69	Ground	

Pin-Side B	PCI Spec Signal	Description	Pin-Side A	PCI Spec Signal	Description
68	AD[23]		68	AD[24]	
67	Ground		67	RSVRD	Reserved
66	AD[21]		66	+3.3V	
65	AD[19]		65	AD[22]	
64	+3.3V		64	AD[20]	
63	AD[17]		63	Ground	
62	C/BE[2]#		62	AD[18]	
61	Ground		61	AD[16]	
60	IRDY#		60	+3.3V	
59	+3.3V		59	FRAME#	
58	DEVSEL#		58	Ground	
57	PCI-XCAP		57	TRDY#	
56	LOCK#		56	Ground	
55	PERR#		55	STOP#	
54	+3.3V		54	+3.3V	
53	SERR#		53	SMBD	Daisy chain to all slots
52	+3.3V		52	SMBCLK	Daisy chain to all slots
51	C/BE[1]#		51	Ground	
50	AD[14]		50	PAR	
49	Ground		49	AD[15]	
48	AD[12]		48	+3.3V	
47	AD[10]		47	AD[13]	
46	M66EN		46	AD[11]	
45	Ground		45	Ground	
44	Ground		44	AD[09]	
43	AD[08]		43	C/BE[0]#	
42	AD[07]		42	+3.3V	
41	+3.3V		41	AD[06]	
40	AD[05]		40	AD[04]	
39	AD[03]		39	Ground	
38	Ground		38	AD[02]	
37	AD[01]		37	AD[00]	
36	+3.3V	Was Vio 3.3V or 1.5V	36	+3.3V	Was VIO 3.3V or 1.5V
35	ACK64#		35	REQ64#	
34	+5V		34	+5V	
33	+5V		33	+5V	
32	Reserved		32	+5V	Was GND
31	Ground		31	C/BE[7]#	
30	C/BE[6]#		30	C/BE[5]#	
29	C/BE[4]#		29	Ground	Was VIO
28	Ground		28	PAR64	
27	AD[63]		27	AD[62]	
26	AD[61]		26	3.3V	Was GND
25	3.3V		25	AD[60]	

Pin-Side B	PCI Spec Signal	Description	Pin-Side A	PCI Spec Signal	Description
24	AD[59]		24	AD[58]	
23	AD[57]		23	Ground	
22	Ground		22	AD[56]	
21	AD[55]		21	AD[54]	
20	AD[53]		20	3.3V	
19	Ground		19	AD[52]	
18	AD[51]		18	AD[50]	
17	AD[49]		17	Ground	
16	3.3V		16	AD[48]	
15	AD[47]		15	AD[46]	
14	AD[45]		14	Ground	
13	Ground		13	AD[44]	
12	AD[43]		12	AD[42]	
KEY		Reversed PCI-Express	KEY		
KEY		Reversed PCI-Express	KEY		
11	AD[41]		11	3.3V	V
10	Ground		10	AD[40]	
9	AD[39]		9	AD[38]	
8	AD[37]		8	Ground	
7	3.3V		7	AD[36]	
6	AD[35]		6	AD[34]	
5	AD[33]		5	Ground	
4	Ground		4	AD[32]	
3	Type1	Type(1:0) (1U)00 = PCI-Express, (1U)01 = PCI (1U)10 = N/A (1U)11 = N/A	3	PXH_RST_N	Input to reset the PXH on the active Riser
2	Type0	(2U)00=2xPCI-Express+PCI (2U)01=3x PCI (2U)10=PXH 3 PCI-X-D (2U)11=No Riser	2	Ground	
1	Size	0=1U, 1 = 2U	1	PXH_PWROK	Input to indicate to PXH on active riser that baseboard power is OK

.

6.5 Electrical Specification

The maximum power per slot is 25 W. This maximum power per slot conforms to *PCI Specification 2.2*.

7. DC Power Subsystem

This chapter defines the features and functionality of the DC-input switching power subsystem. The DC power subsystem comprises up to two DC power supply modules capable of operating in redundant mode and a power distribution board (PDB). The subsystem will be NEBS hardened, so NEBS certification of the TIGI2U server system will be performed with the TIGI2U server system configured with a DC power subsystem.

7.1 Features

- 600W power module output capability in full DC input voltage range
- 580 W subsystem output capability in full DC input voltage range
- Power good indication LEDs
- Predictive failure warning
- Internal cooling fans with multi-speed capability
- Remote sense of 3.3 V, 5 V, and 12 Vdc (on the PDB) outputs
- DC_OK circuitry for brown out protection and recovery
- Built-in load sharing capability
- Built-in overloading protection capability
- Onboard field replaceable unit (FRU) information
- I^2C interface for server management functions
- Integral handle for insertion/extraction

7.2 Chapter Structure and Outline

The information contained in this chapter is organized into two sections. The information is presented in a modular format, with numbered headings for each major topic and subtopic. The content of each section is summarized as follows:

Section 7.3: DC-input Power Supply Module
Provides an overview of the TIGI2U DC-input power supply module.

Section 7.4: DC-input Power Distribution Board
Provides an overview of the TIGI2U power distribution board.

7.3 DC-input Power Supply Module

7.3.1 Power Supply Module Enclosure

A mechanical drawing for the power supply module is shown in Figure 35.

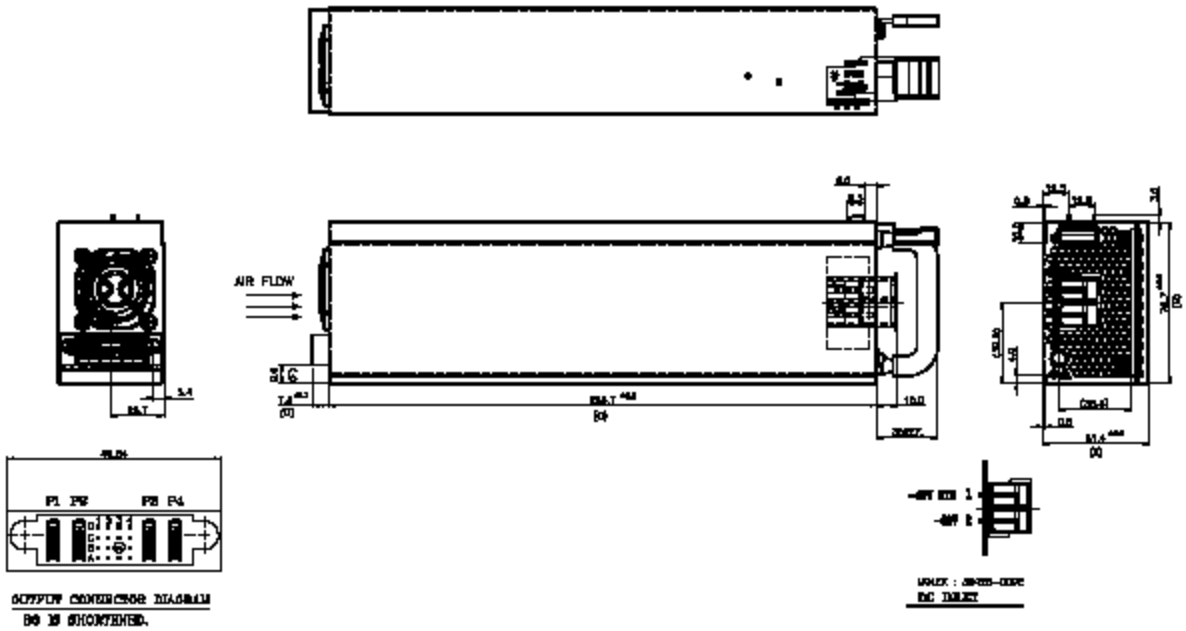


Figure 35. Power Supply module Mechanical Drawing

7.3.2 Power Supply Module to Cage Interconnect

The power supply provides a pluggable terminal block, which mates to a connector located at the PDB. This is a blind mating type connector that connects the power module's output voltages and signals.

The power supply module shall be provided with a reliable protective earth ground. All secondary circuits shall be connected to protective earth ground. Resistance of the ground returns to chassis shall not exceed 1.0 mΩ. This path may be used to carry DC current.

7.3.3 Power Supply Module Input Connector Pin Assignment

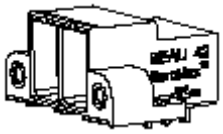
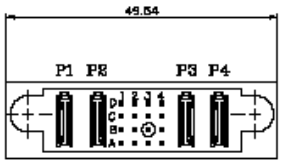


Figure 36. Supply Module Input Connector Pin Assignment

7.3.4 Power Supply Module Output Connector Pin Assignment



OUTPUT CONNECTOR DIAGRAM
B3 IS SHORTENED.

OUTPUT CONNECTOR : FCI 51939-136
PIN ASSIGNMENT:

Signal Pins				
POSITION	1	2	3	4
D	+12VRS	-12V	+5VSB	15VCC
C	PWOK	RS RTN	+5VSB	A0
B	+12VLS	RESERVE	PS KILL	A1
A	PS ON#	SDA	SCL	PS ALERT#
Power Blades				
P1	P2	P3	P4	
+12V	+12V	RTN	RTN	

Figure 37. Supply Module Input Connector Pin Assignment

7.3.5 Output Current Requirements

The power supply module provides three main outputs; +12V, -12V, and 5V standby, along with the 15 VBIAS voltage. The combined maximum output power of all outputs is 600 W (680 W peak). Each output has a maximum and minimum current rating as shown in the following table.

Table 41. Power Supply Module 600W Load Ratings

	+12V	+5Vsb	-12V
MAX Load	49.0A	2.0A	0.5A
MIN DYNAMIC Load	2.5A	0.1A	0A
MIN STATIC Load	0.5A	0.1A	0A
PEAK Load (12 seconds min)	56.0A	2.5A	N/A
Max Output Power (continuous), see note	12V x 49A = 588W max	5V x 2A = 10W max	-12V x 0.5A = 6W max
Peak Output Power (for 12s min), see note	12V x 56A = 672W pk	5V x 2.5A = 12.5W pk	N/A

Note:
At max and peak loads the 12V output voltage is allowed to sag to –4%(11.52V)

7.3.6 Power Supply Module LED Indicator

The power supply module provides a single external bi-color LED to indicate the status of the power supply. When DC is applied to the PSU and standby voltages are available, the LED will blink green.

The LED will be solid on green when all the power outputs are available.

The LED will be solid on amber when the power supply module has failed: shutdown due to over current, shutdown due to over current or shutdown due to over temperature. Refer to the following table for conditions of the LED.

Table 42. LED Indicators

Power Supply Condition	Bi-Color LED
No DC power to all power supplies	OFF
No DC power to this PSU only (for 1+1 configuration) or Power supply **critical event** causing a shutdown: failure, fuse blown (1+1 only), OCP(12V), OVP(12V), Fan Failed	AMBER
Power supply **warning events** where the power supply **continues to operate**: high temp, high power/high current, slow fan.	1Hz Blink AMBER
DC present / Only 5Vsb on (PS Off)	1Hz Blink GREEN
Output ON and OK	GREEN

7.3.7 Air Flow

The power supply shall incorporate fans for self cooling. The fans provide no less than **TBD CFM** airflow through the power supply when installed in the system and operating at maximum fan speed. The cooling air will enter the power module from the PDB side (pre-heated air from the system). Variable fans speed is based on output load and ambient temperature. Under standby mode, the fans run at minimum RPM.

7.3.8 Thermal Protection

The power supply module incorporates thermal protection that causes a shut down if airflow through the power supply module is insufficient. Thermal protection activates shutdown before the temperature of any power supply module component passes the maximum rated temperature. This shutdown takes place prior to over-temperature induced damage to the power supply module.

7.4 Power Distribution Board

The DC-power subsystem incorporates the PDB identical to the AC-power subsystem (see sec.8.3).

7.5 Output Current Requirements

This describes the +12V output power requirements from the power distribution board with a single or two ERP700W power supply plugged into the input of the power distribution board.

Table 43. +12V Outputs Load Ratings

	+12V1	+12V2	+12V3	+12V4
MAX Load	16A	16A	16A	16A
MIN Static / Dynamic Load	0.75A	0.75A	0.5A	0.5A
Peak load (12 seconds)	18A	18A	18A	18A
Max Output Power	12V x 16A =192W	12V x 16A =192W	12V x 16A =192W	12V x 16A =192W

Note:

- The combined total power limit for all outputs is 580 W max.
- +12V1/2/3/4 combined output limit = 40A / 56A pk max

The following table defines power and current ratings of the two DC/DC converters located on the PDB, each powered from +12V rail. The converters must meet both static and dynamic voltage regulation requirements for the minimum and maximum loading conditions.

Table 44. DC/DC Converters Load Ratings

	+12VDC Input DC/DC Converters	
	+3.3V Converter	+5V Converter
MAX Load	20A	26A
MIN Static / Dynamic Load	0.5A	0.5A
Max Output Power	3.3V x20A =66W	5V x26A =130W

Note:
3.3V / 5V combined power limit: 150W Max.

7.6 Hot-swapping Power Modules

Hot swapping a power supply module is the process of extracting and inserting a power supply module from an operating system. The DC-input power subsystem is capable of supporting hot swapping of power supply modules in a 1+1 configuration.

7.7 Intelligent Cage Functions

The power supply module and power distribution board (PDB) combination shall provide a monitoring interface to the system over a server management bus. Device should be compatible with both SMBus 2.0 'high power' and I^2C V_{dd} based power and drive. This bus may operate inside the power supply module and PDB at 5V (powered from stand-by voltage) but, looking from the system server management into the power supply module and PDB combination, it shall be compatible with the 3.3V bus. A bi-directional I2C voltage translator IC, such as GTL2002 or similar, may be employed on the PDB. The SMBus pull-ups are located on the server board.

The power distribution board's I2C serial bus will have a dual function: to provide the power supply module and PDB monitoring features and to convey the stored FRU data in the power supply module and PDB EEPROM.

7.8 FRU Data

The power subsystem contains a 2 KB EEPROM device that contains FRU data for the subsystem according to the IPMI spec. Each separate output is given a different number for identification purposes.

8. AC Power Subsystem

This chapter defines the features and functionality of the AC-input switching power subsystem. The AC power supply will not be NEBS hardened, so NEBS certification of a TIGI2U server system configured with an AC power subsystem will not be possible.

8.1 Features

- 600 W output capability in full AC input voltage range
- Power good indication LEDs
- Predictive failure warning
- External cooling fans with multi-speed capability
- Remote sense of 3.3 V, 5 V, and 12 Vdc outputs
- Brown out protection and recovery
- Built-in overloading protection capability
- Onboard field replaceable unit (FRU) information
- I^2C interface for server management functions
- Integral handle for insertion/extraction

8.2 Chapter Structure and Outline

The information contained in this chapter is organized into two sections. The information is presented in a modular format, with numbered headings for each major topic and subtopic. The content of each section is summarized as follows:

Section 8.3: AC-input Power Supply Cage
Provides an overview of the TIGI2U AC-input power cage.

Section 8.4: AC-input Power Supply Module
Provides an overview of the TIGI2U AC-input power supply module.

8.3 Power Distribution Cage

8.3.1 AC-input Power Distribution Cage Mechanical Specification

The AC-input power distribution cage can support up to two 600W SSI TPS power supply modules in a 1+1 configuration or a 1+0 configuration. A mechanical drawing for the power supply cage is shown below.

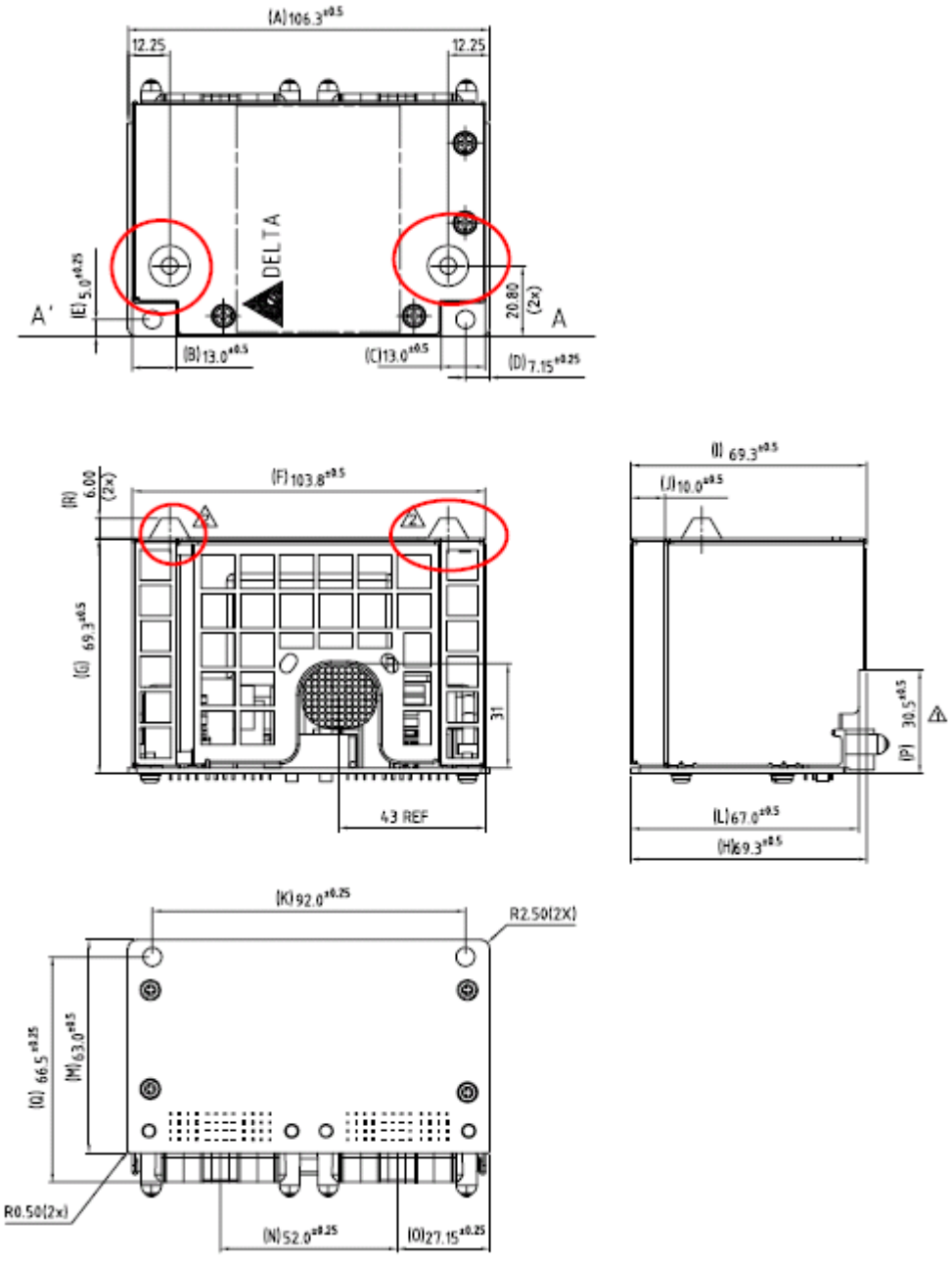
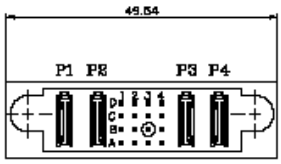


Figure 38. Power Distribution Cage Mechanical Drawing



OUTPUT CONNECTOR DIAGRAM
B3 IS SHORTENED.

OUTPUT CONNECTOR : FCI 51939-136
PIN ASSIGNMENT:

Signal Pins				
POSITION	1	2	3	4
D	+12VRS	-12V	+5VSB	15VCC
C	PWOK	RS RTN	+5VSB	A0
B	+12VLS	RESERVE	PS KILL	A1
A	PS ON#	SDA	SCL	PS ALERT#
Power Blades				
P1	P2	P3	P4	
+12V	+12V	RTN	RTN	

Figure 39. Power Supply Cage Input Connector Drawing and Pin-out

8.3.2 Power Supply Cage Wire Harness

The power distribution board connects to the system via a wire harness. The harness size, connectors, and pin outs are shown below. Listed or recognized component appliance wiring material (AVLV2), VW-1 flame rating, rated 105°C Min, 300Vdc Min shall be used for all output wiring.

Table 45. Cable Lengths

From	Length mm	To connector #	No of pins	Description
Backplane cover exit hole	96, turn 90°	P1	2x12	Baseboard Power Connector
Backplane cover exit hole	252	P2	2x4	Processor Power Connector
Backplane cover exit hole	247	P3	1x5	Power Signal Connector
Backplane cover exit hole	392	P4	1x3	PCI-X Riser Power Connector
Backplane cover exit hole	85	P5	1x6	FPIO Board Power Connector

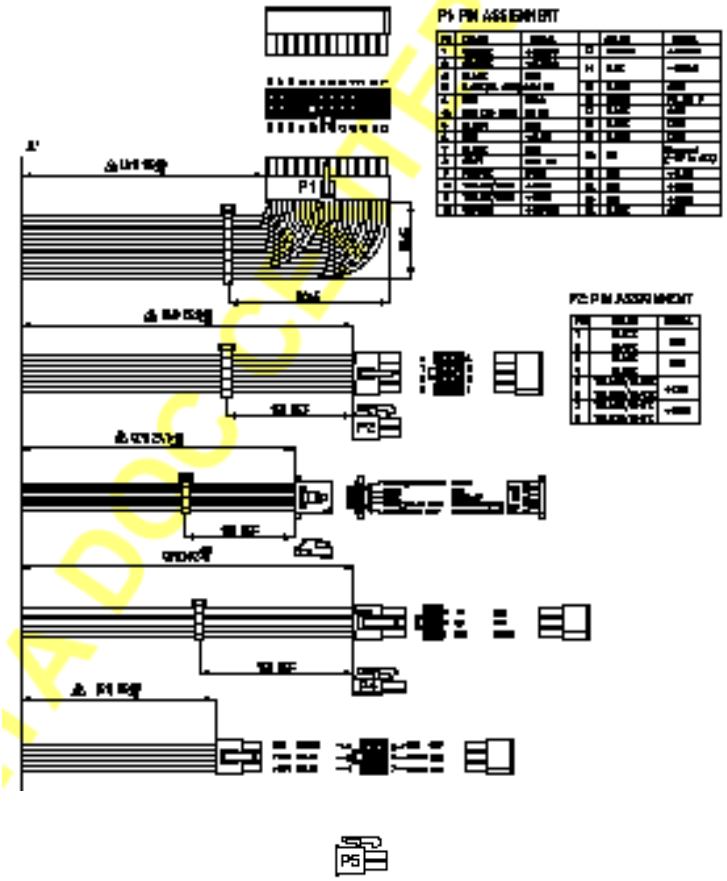


Figure 40. Output Wire Harness Detail

8.3.3 P1 Server Board Power Connector

A 24-pin Molex* 39-01-2245 (or equivalent) connector and harness from the power supply cage provides the server board SE7520JR2 with the required voltages and interface signals. The following table provides the connector pin-out.

Table 46. 24-pin Server Board Power Connector Pin-out

PIN	SIGNALS	18 AWG COLOR	PIN	SIGNAL	18 AWG COLORS
1	+3.3 VDC	Orange	12	+3.3 VDC	Orange
2	+3.3 VDC	Orange	13	+3.3 VDC	Orange
3*	COM (GND)	Black	14	-12 VDC	Blue
	COM	Black (24 AWG)	15	COM	Black
4*	5 VDC	Red	16	PS_ON#	Green
	5V RS	Red (24 AWG)	17	COM	Black
5	COM	Black	18	COM	Black
6	+5 VDC	Red	19	COM	Black
7	COM	Black	20	*Reserved (-5V in ATX)*	*NC*
8	PWR OK	Gray	21	+5 VDC	Red
9	5VSB	Purple	22	+5 VDC	Red
10	+12 V3	Yellow/Blue Stripe	23	+5 VDC	Red
11	+12 V3	Yellow/Blue Stripe	24	COM	Black

Note:
* Remote Sense wire double crimped.

8.3.4 P2 Processor Power Connector

An 8-pin Molex 39-01-2085 (or equivalent) connector and harness from the power supply cage provides the server board SE7520JR2 with the required +12V power required for the processors. The following table provides the connector pin-out.

Table 47. P2 Processor Power Connector Pin-out

PIN	SIGNAL	18 AWG COLOR	PIN	SIGNAL	18 AWG COLOR
1	COM	Black	5	+12 V1	Yellow/Black Stripe
2	COM	Black	6	+12 V1	Yellow/Black Stripe
3	COM	Black	7	+12 V2	Yellow/White Stripe
4	COM	Black	8	+12 V2	Yellow/White Stripe

Note:
The 12V remote sense should be connected just before the 240VA current sense resistors on the PDB.

8.3.5 P3 Power Signal Cable

A 5-wire cable with a Molex 50-57-9705 (or equivalent) female housing connector is used to direct power management signals to the server board SE7520JR2. The following table shows the pin-out.

Table 48. P3 Power Signal Cable Pin-out

Pin	Signal	24 AWG Colors	Description
1	SMBus Clock (SCL)	White/Green Stripe	Serial Clock.
2	SMBus Data (SDL)	White/Yellow Stripe	Serial Data. Information from the power supply.
3	SMBAlert#	White	Indicates power supply is operating beyond its limits and has failed or may fail soon.
4	COM	Black	Return remote sense
5	3.3RS	Orange/White Stripe	3.3V sense

Notes:

- It is recommended to use gold plated signal connector contacts on both the PDB connector and the server board header.
- If the server signal connector is unplugged, the PS/PDB-combo shall not shut down or go into an OVP condition.

8.3.6 P4 PCI-X Riser Power Connector

A 3-wire cable with a Molex Mini-Fit Jr. PN# 39-01-4031 connector is used to provide power to the PCI-X Riser.

Table 49. P4 PCI-X Riser Power Connector Pin-out

Pin	Signal	22 AWG COLOR
1	COM	Black
2	5V	Red
3	5V	Red

8.3.7 P5 Hard Drive Interface Board Power Connector

A 3-wire cable with a Molex Mini-Fit Jr. PN# 39-01-2065 connector is used to provide power to the FPIO system board for system logic power, for peripheral drive power, and for disk drive power.

Table 50. P5 Hard Drive Interface Board Power Connector Pin-out

PIN	SIGNAL	18 AWG Colors
1	COM	Black
2	COM	Black
3	5V	Red
4	12V4	Yellow
5	12V4	Yellow
6	3.3V	Orange

8.3.8 Output Current Requirements

This describes the +12V output power requirements from the power distribution board with a single or two ERP700W power supply plugged into the input of the power distribution board.

Table 51. +12V Outputs Load Ratings

	+12V1	+12V2	+12V3	+12V4
MAX Load	16A	16A	16A	16A
MIN Static / Dynamic Load	0.75A	0.75A	0.5A	0.5A
Peak load (12 seconds)	18A	18A	18A	18A
Max Output Power	12V x16A =192W	12V x16A =192W	12V x16A =192W	12V x16A =192W

Notes:
The combined total power limit for ALL outputs is 580W max.
+12V1/2/3/4 combined output limit = 40A / 56A pk max.

The following table defines power and current ratings of 2 DC/DC converters located on the PDB, each powered from +12V rail. The 3 converters must meet both static and dynamic voltage regulation requirements for the minimum and maximum loading conditions.

Table 52. DC/DC Converters Load Ratings

	+12VDC Input DC/DC Converters	
	+3.3V Converter	**+5V Converter**
MAX Load	20A	26A
MIN Static / Dynamic Load	0.5A	0.5A
Max Output Power, see note 1	3.3V x20A =66W	5V x26A =130W

Note:
3.3V / 5V combined power limit: 150W max.

8.3.9 Hot-swapping Power Modules

The AC-input power supply cage is capable of supporting hot swapping of power supply modules in a 1+1 configuration. Hot swapping a power supply module is the process of extracting and inserting a power supply module from an operating system.

8.3.10 Intelligent Cage Functions

The power supply module and power distribution board (PDB) combination shall provide a monitoring interface to the system over a server management bus. Devices should be compatible with both SMBus 2.0 'high power' and I^2C V_{dd} based power and drive. This bus may operate inside the power supply module and PDB at 5V (powered from stand-by voltage) but, looking from the system server management into the power supply module and PDB combination, it shall be compatible with the 3.3V bus. A bi-directional I2C voltage translator IC, such as GTL2002 or similar, may be employed on the PDB. The SMBus pull-ups are located on the server board.

The power distribution board's I2C serial bus will have a dual function: to provide power supply module and PDB monitoring features and to convey the stored FRU data in the power supply module and PDB EEPROM.

8.3.11 FRU Data

The power supply cage contains a 2 KB EEPROM device that contains FRU data for the cage according to the IPMI spec. Each separate output is given a different number for identification purposes.

8.4 AC-input Power Supply Module

8.4.1 AC-input Power Supply Module Mechanical Specification

The AC-input power system supports one 600W SSI TPS (Thin Power Supply) module for a non redundant configuration, or two in a 1+1 redundant configuration.

8.4.1.1 Power Supply Module Mechanical Drawing

The power supply module contains one 40mm fan. The module provides a handle to assist in insertion and extraction and can be inserted and extracted without the assistance of tools.

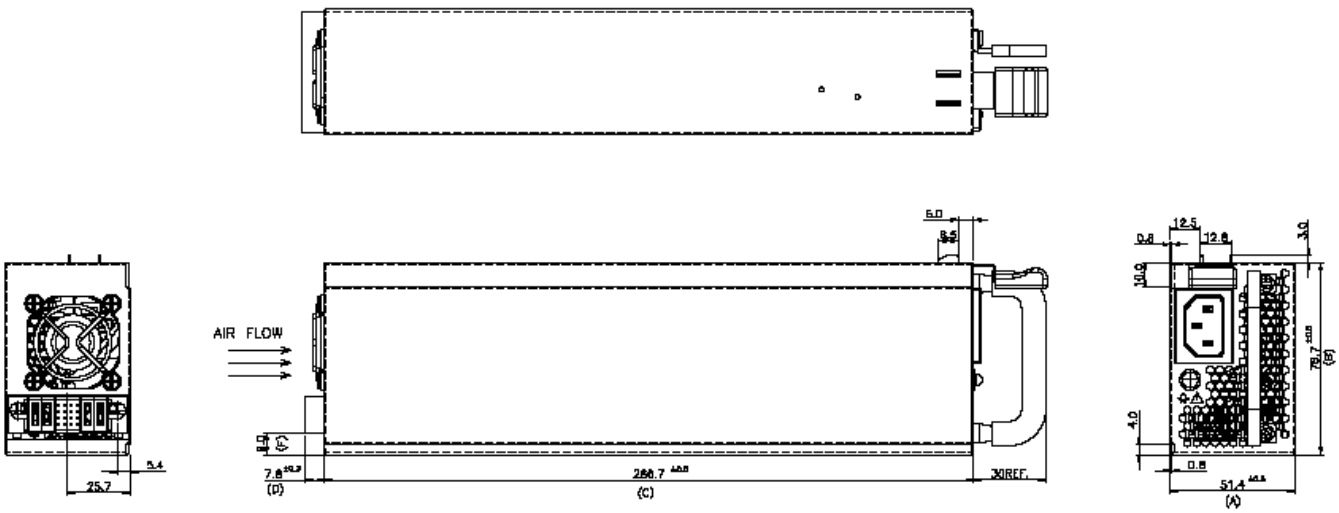
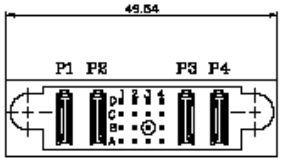


Figure 41. Power Supply Module Mechanical Drawing

8.4.2 Power Supply Module to Cage Interconnect

The power supply provides pluggable terminal block, which mate to a connector located at the PDB. This is a blind mating type connector that connects the power supply's output voltages and signals.

The power supply shall be provided with a reliable protective earth ground. All secondary circuits shall be connected to protective earth ground. Resistance of the ground returns to chassis shall not exceed 1.0 mΩ. This path may be used to carry DC current.



OUTPUT CONNECTOR DIAGRAM
B3 IS SHORTENED.

OUTPUT CONNECTOR : FCI 61939-136
PIN ASSIGNMENT:

Signal Pins				
POSITION	1	2	3	4
D	+12VRS	-12V	+5VSB	15VCC
C	PWOK	RS_RTN	+5VSB	A0
B	+12VLS	RESERVE	PS_KILL	A1
A	PS_ON#	SDA	SCL	PS_ALERT#
Power Blades				
P1	P2	P3	P4	
+12V	+12V	RTN	RTN	

Figure 42. Power Supply Module Output Connector and Pin-out Drawing

8.4.3 Output Current Requirements

The power supply module provides three main outputs; +12V, -12V, and 5V standby, along with the 15VBIAS voltage. Two DC-to-DC converters located in the cage provide the 3.3V and 5V rails from the 12V provided by the power supply module.

The combined maximum output power of all outputs is 600 W (680 W peak). Each output has a maximum and minimum current rating as shown in the following table.

Table 53. Power Supply Module 600W Load Ratings

	+12V	+5Vsb	-12V
MAX Load	49.0A	2.0A	0.5A
MIN DYNAMIC Load	2.5A	0.1A	0A
MIN STATIC Load	0.5A	0.1A	0A
PEAK Load (12 seconds min)	56.0A	2.5A	N/A
Max Output Power (continuous), see note 1	12V x 49A = 588W max	5V x 2A = 10W max	-12V x 0.5A = 6W max
Peak Output Power (for 10s min), see note 2	12V x 56A = 672W pk	5V x 2.5A = 12.5W pk	N/A

Notes:

1. At max load the 12V output voltage is allowed to sag to –4%, which is 11.52V; so the actual max power will then be: 11.52V x 49A = 564.5 W, and the same applies for 5VSB: 4.80Vx2A=9.6W; so total max continuous Power = 564.5+9.6=574.1W .
2. At peak load the 12V output voltage is allowed to sag to –4%, which is 11.52V; so the actual peak power will then be: 11.52V x 56A = 645W; and the same applies to 5VSB: 4.80Vx2.5A=12W. The total peak power = 657 W pk.

8.4.4 Power Supply Module LED Indicator

The power supply module provides a single external bi-color LED to indicate the status of the power supply. When AC is applied to the PSU and standby voltages are available, the LED will blink green.

The LED will be solid on green when all the power outputs are available.

The LED will be solid on amber when the power supply has failed - shutdown due to over current, shutdown due to over current or shutdown due to over temperature. Refer to the following table for conditions of the LED.

Table 54. LED Indicators

Power Supply Condition	Bi-color LED
No AC power to all power supplies	OFF
No AC power to this PSU only (for 1+1 configuration) or Power supply **critical event** causing a shutdown: failure, fuse blown (1+1 only), OCP(12V), OVP(12V), Fan Failed	AMBER
Power supply **warning events** where the power supply **continues to operate**: high temp, high power/high current, slow fan.	1Hz Blink AMBER
AC present / Only 5Vsb on (PS Off)	1Hz Blink GREEN
Output ON and OK	GREEN
No AC power to all power supplies	OFF

8.4.5 Air Flow

The power supply shall incorporate **one 40mm fan** for self cooling and also used for partial system cooling. The fans will provide no less than **10 CFM** airflow through the power supply when installed in the system and operating at maximum fan speed. The cooling air will enter the power module from the PDB side (pre-heated air from the system). Variable fans speed is based on output load and ambient temperature. Under standby mode, the fans must run minimum RPM.

8.4.6 Thermal Protection

The power supply incorporates thermal protection that causes a shut down if airflow through the power supply is insufficient. Thermal protection activates shutdown before the temperature of any power supply component the maximum rated temperature. This shutdown takes place prior to over-temperature induced damage to the power supply.

9. Regulatory Specifications

The TIGI2U server system meets the specifications and regulations for safety and EMC defined in this chapter.

9.1 Safety Compliance

USA/Canada	UL 60950-1, 1st Edition/CSA 22.2
Europe	Low Voltage Directive, 73/23/EEC TUV/GS to EN60950-1, 1st Edition
International	CB Certificate and Report to IEC60950-1, 1St Edition and all international deviations

9.2 Electromagnetic Compatibility

USA	FCC 47 CFR Parts 2 and 15, Verified Class A Limit
Canada	IC ICES-003 Class A Limit
Europe	EMC Directive, 89/336/EEC EN55022, Class A Limit, Radiated & Conducted Emissions EN55024 Immunity Characteristics for ITE EN61000-4-2 ESD Immunity (level 2 contact discharge, level 3 air discharge) EN61000-4-3 Radiated Immunity (level 2) EN61000-4-4 Electrical Fast Transient (level 2) EN61000-4-5 Surge EN61000-4-6 Conducted RF EN61000-4-8 Power Frequency Magnetic Fields EN61000-4-11 Voltage Fluctuations and Short Interrupts EN61000-3-2 Harmonic Currents EN61000-3-3 Voltage Flicker
Australia/New Zealand	AS/NZS 3548, Class A Limit
Japan	VCCI Class A ITE (CISPR 22, Class A Limit) IEC 1000-3-2; Harmonic Currents
Taiwan	BSMI Approval, CNS 13438, Class A and CNS13436 Safety
Korea	RRL Approval, Class A
China	CCC Approval, Class A (EMC and Safety)
Russia	Gost Approval (EMC and safety)
International	CISPR 22, Class A Limit

9.3 CE Mark

The CE marking on this product indicates that it is in compliance with the European Union's EMC Directive 89/336/EEC, and Low Voltage Directive, 73/23/EEC.

9.4 NEBS Compliance (DC Input Only)

The TIGI2U system with DC input is compliant with the following NEBS specifications:

- NEBS GR-63-CORE, Issue 2 – Physical Protection
- NEBS GR-1089-CORE, Issue 3 – Electromagnetic Compatibility and Electrical Safety

9.5 ETSI Standards Compliance (DC Input Only)

The TIGI2U system with DC input is compliant with the following ETSI specifications:

- ETSI EN 300 386 EMC requirements for Telecom Equip.
- ETS 300-019-2-1 Storage Tests, Class T1.2
- ETS 300-019-2-2 Transportation Tests, Class T2.3
- ETS 300-019-2-3 Operational Tests, Class T3.2
- ETS 753 Acoustic Noise.

Appendix A: Glossary

This appendix contains important acronyms and terms used in the preceding chapters.

Term	Definition
A, Amp	Ampere
A/µs	Amps per microsecond
AC	Alternating current
ACPI	Advanced Configuration and Power Interface
ANSI	American National Standards Institute
APIC	Advanced Programmable Interrupt Controller
ASIC	Application specific integrated circuit
AWG	American wire gauge
BIOS	Basic input/output system
BMC	Bus management controller
Bridge	Circuitry that connects one computer bus to another
Byte	8-bit quantity
C	Centigrade
CE	Community European
CFM	Cubic feet per minute
CISPR	International Special Committee on Radio Interference
CSA	Canadian Standards Organization
CTS	Clear to send
DAT	Digital audio tape
dB	Decibel
dBA	Acoustic decibel
DC	Direct current
DIMM	Dual inline memory module
DMI	Desktop management interface
DOS	Disk operating system
DRAM	Dynamic random access memory
DSR	Data set ready
DTR	Data terminal ready
DWORD	Double word - 32-bit quantity
ECC	Error checking and correcting
EEPROM	Electrically erasable programmable read-only memory
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
EMP	Emergency management port
EN	European Standard (Norme Européenne or Europäische Norm)
EPS	External product specification
ESCD	Extended system configuration data
ESD	Electrostatic discharge
ESR	Equivalent series resistance
F	Fahrenheit

Term	Definition
FCC	Federal Communications Commission
FFC	Flexible flat connector
Flash ROM	EEPROM
FPC	Front panel controller
FRB	Fault resilient booting
FRU	Field replaceable unit
G	Acceleration in gravity units, 1G = 980665 m/s^2
GB	Gigabyte - 1024 MB
GND	Ground
GPIO	General purpose input/output
Grms	Root mean square of acceleration in gravity units
GUI	Graphical user interface
HDD	Hard disk drive
HPIB	Hot-plug indicator board
HSC	Hot-swap controller
Hz	Hertz – 1 cycle/second
I/O	Input/output
I^2C*	Inter-integrated circuit bus
ICMB	Intelligent Chassis Management Bus
IDE	Integrated drive electronics
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IFLASH	Utility to update Flash EEPROM
IMB	Intelligent management bus
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Initiative
IRQ	Interrupt request line
ITE	Information technology equipment
ITP	In-target probe
JAE	Japan Aviation Electronics
KB	Kilobyte - 1024 bytes
kV	Killivolt – 1,000 volts
L2	Second-level cache
LAN	Local area network
LED	Light-emitting diode
LVDS	Low voltage differential SCSI
mA	Milliamp
MB	Megabyte - 1024 KB
MEC	Memory expansion card
mm	Millimeter
MPS	Multiprocessor specification
MTTR	Mean time to repair
mΩ	Milliohm
NEMKO	Norges Elektriske Materiellkontroll (Norwegian Board of Testing and Approval of Electrical Equipment)

Term	Definition
NIC	Network interface card
NMI	Nonmaskable interrupt
NWPA	NetWare* Peripheral Architecture
ODI	Open data-link interface
OEM	Original equipment manufacturer
OPROM	Option ROM (expansion BIOS for a peripheral)
OS	Operating system
OTP	Over-temperature protection
OVP	Over-voltage protection
PC-100	Collection of specifications for 100 MHz memory modules
PCB	Printed circuit board
PCI	Peripheral component interconnect
PHP	PCI hot-plug
PID	Programmable interrupt device
PIRQ	PCI interrupt request line
PMM	POST memory manager
PnP	Plug and play
POST	Power-on Self Test
PSU	Power supply unit
PVC	Polyvinyl chloride
PWM	Pulse width modulation
RAS	Reliability, availability, and serviceability
RIA	Ring indicator
RPM	Revolutions per minute
RTS	Request to send
SAF-TE	SCSI Accessed Fault-Tolerant Enclosures
SCA	Single connector attachment
SCL	Serial clock
SCSI	Small Computer Systems Interface
SDR	Sensor data records
SDRAM	Synchronous dynamic RAM
SEC	Single edge connector
SEL	System event log
SELV	Safety extra low voltage
SEMKO	Sverge Elektriske Materiellkontroll (Swedish Board of Testing and Approval of Electrical Equipment)
SGRAM	Synchronous graphics RAM
SM	Server management
SMBIOS	System management BIOS
SMBus	Subset of I^2C bus/protocol (developed by Intel)
SMI	System management interrupt
SMM	Server management mode
SMP	Symmetric multiprocessing
SMRAM	System management RAM
SMS	Server management software

Term	Definition
SPD	Serial presence detect
SSI	Server system infrastructure
TUV	Technischer Uberwachungs-Verein (A safety testing laboratory with headquarters in Germany)
UL	Underwriters Laboratories, Inc.
USB	Universal Serial Bus
UV	Under-voltage
V	Volt
VA	Volt-amps (volts multiplied by amps)
Vac	Volts alternating current
VCCI	Voluntary Control Council for Interference
Vdc	Volts direct current
VDE	Verband Deutscher Electrotechniker (German Institute of Electrical Engineers)
VGA	Video graphics array
VRM	Voltage regulator module
VSB	Voltage standby
W	Watt
WfM	Wired for Management
Word	A 16-bit quantity
Ω	Ohm
μF	Microfarad
μs	Microsecond

Appendix B: Reference Documents

Refer to the following documents for additional information:

ACPI

- *Advanced Configuration And Power Interface Specification*, Revision 1.0b, http://www.teleport.com/~acpi/.

Boot

- *BIOS Boot Specification*, Version 1.01, http://www.ptltd.com/techs/specs.html.
- *El Torito CD-RW/DVD Boot Specification*, Version1.0, http://www.ptltd.com/techs/specs.html.

DMI

- *Desktop Management Interface (DMI) Specification*, Version 2.0s, Desktop Management Task Force, Inc., http://www.dmtf.org/spec/dmis.html.

ESCD

- *Extended System Configuration Data Specification*, Version 1.02a, http://www.microsoft.com/hwdev/respec/PNPSPECS.HTM.

Ethernet

- *Intel 82559 Fast Ethernet Multifunction PCI/Cardbus Controller Datasheet*, Intel Corporation, http://developer.intel.com/design/network/datashts/738259.htm.

Flash

- *Intel 5 VOLT FlashFile™ Memory (28F008SA x8) Datasheet*, December 1998, Intel Corporation, Number 290429-008, http://developer.intel.com/design/flcomp/datashts/290429.htm.

I_2O

- *Intelligent Input/Output (I_2O) Architecture Specification*, Revision 1.0, I_2O Special Interest Group, http://www.Intelligent-IO.com

MPS

- *MultiProcessor Specification*, Version 1.4, Intel Corporation, http://www-techdoc.intel.com/design/intarch/manuals/242016.htm.

PC133 SDRAM

- *PC SDRAM Registered DIMM Specification*, Revision 1.2, Intel Corporation, http://developer.intel.com/technology/memory/.

- *PC SDRAM Specification*, Revision 1.63, Intel Corporation, http://developer.intel.com/technology/memory/.
- *PC SDRAM Serial Presence Detect (SPD) Specification*, Revision 1.2A, Intel Corporation, http://developer.intel.com/technology/memory/.

PCI

- *PCI Bus Power Management Interface Specification*, Revision 1.1, PCI Special Interest Group, http://www.pcisig.com/.
- *PCI Local Bus Specification*, Revision 2.1, PCI Special Interest Group, http://www.pcisig.com/.
- *PCI Hot-plug Specification*, Revision 1.0, PCI Special Interest Group, http://www.pcisig.com/.
- *PCI Hot-plug Application and Design*, Alan Goodrum, ISBN 0-929392-60-4.
- *Compaq* PCI Hot-Plug Megacell Specification.*

PID

- *Programmable Interrupt Device External Product Specification*, Revision 1.1, Intel Corporation, Document number OR4-680777.

Plug and Play

- *Plug and Play BIOS Specification*, Version 1.0a, http://www.microsoft.com/hwdev/respec/PNPSPECS.HTM.
- *Clarification to Plug and Play BIOS Specification*, Version 1.0a, http://www.microsoft.com/hwdev/respec/PNPSPECS.HTM.
- *Plug and Play ISA Specification*, Version 1.0a, http://www.microsoft.com/hwdev/respec/PNPSPECS.HTM.
- *Clarification to Plug and Play ISA Specification*, Version 1.0a, http://www.microsoft.com/hwdev/respec/PNPSPECS.HTM.

PMM

- *POST Memory Manager Specification*, Version 1.01, http://www.ptltd.com/techs/specs.html.

Power Supply

- *TIGI2U AC Power Supply Module Specification*, Revision 1.0, Intel Corporation.
- *TIGI2U DC Power Supply Module Specification*, Revision 1.0, Intel Corporation.
- *TIGI2U AC / DC Power Supply Power Distribution Board Specification*, Revision 1.0, Intel Corporation.

Regulatory

- *CISPR 22: Limits and Methods of Measurement of Radio Interference Characteristics of Information Technology Equipment*, 2nd Edition.
- *CFR 47: Federal Communications Commission (FCC) Compliance with the Class A Limits for Computing Devices (FCC Mark)*, Part 2 & 15.
- *ANSI C63.4: American National Standard for Methods of Measurement of Radio-Noise Emissions from Low Voltage Electronic Equipment in the Range of 9kHz to 40GHz for EMI Testing*, 1992.
- *CISPR 24: Information Technology Equipment - Immunity Characteristics Limits and Methods of Measurement*, 1st Edition.
- *ICES-003: Canadian Radio Interference Regulations for Digital Apparatus*.
- *EN 61000-3-2: Electromagnetic Compatibility (EMC) Part 3: Limits - Section 2: Limits for Harmonic Current Emissions.*
- *JEIDA MITI Guideline for Suppression of High Harmonics in Appliances and General-Use Equipment*.

SCSI

- *SCSI Accessed Fault-Tolerant Enclosures (SAF-TE) Specification*.

Server Management

- *Emergency Management Port v1.0 Interface External Product Specification*, Revision 0.83, Intel Corporation.
- *Intelligent Platform Management Interface (IPMI) Specification*, Version 1.0, Revision 1.1, Intel Corporation, http://developer.intel.com/design/servers/ipmi/spec.htm.

SMBIOS

- *System Management BIOS Reference Specification*, Version 2.3, http://www.ptltd.com/techs/specs.html.

Super I/O

- *National PC97317 SuperI/O Plug and Play Compatible Chip with ACPI-Compliant Controller/Extender*, http://www.national.com/pf/PC/PC97317.html.

USB

- *Universal Serial Bus Specification*, Revision 1.0, http://www.usb.org/developers.

VGA

- *ATI RAGE IIC Technical Reference Manual*.
- *ATI-264 VT4 Graphics Controller Technical Reference Manual*.

Wired for Management

- *Wired for Management (WfM) Baseline Specifications*, Version 2.0, Intel Corporation, http://developer.intel.com/ial/wfm/wfmspecs.htm.

Windows

- *Hardware Design Guide for Microsoft Windows NT Server*, Version 2.0, http://www.microsoft.com/HWDEV/serverdg.htm.

Miscellaneous

- *Intel Environmental Standards Handbook,* June 1999, Intel Document No. 662394-04.
- *VRM 8.3 DC-DC Converter Specification.*
- VRM 8.4 DC-DC Converter Specification.