Intel® Server System SC5400RA

Technical Product Specification

Revision 1.0

November 2006

Enterprise Platforms and Services Division - Marketing

Revision History

Date	Revision Number	Modifications
November 2006	1.0	Document released

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Intel order number: D78185-001

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1.   Introduction

This Technical Product Specification (TPS) provides information about the features, functionality, and high-level architecture of the Intel® Server System SC5400RA. See the *Intel® S5000 Server Board Family Datasheet* for details about board sub-systems, including the chipset, BIOS, and server management.

This specification details the chassis features that are specific to the Intel® Server System SC5400RA. The chassis is similar to the Intel® Server Chassis SC5400 BRP.

This document describes the differences between Intel® Server Chassis SC5400BRP and the server chassis that is used with the Intel® Server System SC5400RA. The features of the Intel® Server System SC5400RA that are common with the Intel® Server Chassis SC5400BRP are described in the *Intel® Server Chassis SC5400 Technical Product Specification*.

1.1   Chapter Outline

This document is divided into the following chapters

Chapter 1 – Introduction
Chapter 2 – Server Board Overview
Chapter 3 – Functional Architecture
Chapter 4 – Platform Management
Chapter 5 – Connector and Header Location and Pin-out
Chapter 6 – Configuration Jumpers
Chapter 7 – Light-Guided Diagnostics
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Appendix B – BMC Sensor Tables
Appendix C – POST Code Diagnostic LED Decoder
Appendix D – POST Code Errors
Appendix E – Supported Intel® Server Chassis

1.2   Server Board Use Disclaimer

Intel Corporation server boards support add-in peripherals and contain a number of high-density VLSI and power delivery components that need adequate airflow to cool. Intel ensures through its own chassis development and testing that when Intel server building blocks are used together, the fully integrated system will meet the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel-developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of air flow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside any of their published operating or non-operating limits.

2.   Server System Overview

The Intel® Server System SC5400RA has a monolithic printed circuit board with features that support the pedestal server markets.

2.1   Intel® Server System SC5400RA Chassis Design Features

The Intel® Server System SC5400RA makes extensive use of tool-less hardware features and, dependent upon configuration, provides redundant power supply capability.

Table 1. Intel® Server Chassis SC5400BRP and Intel® Server System SC5400RA Chassis Features

Feature	Intel® Server Chassis SC5400 BRP	Intel® Server System SC5400RA
Power Delivery	Includes one of two redundant 830 W PFC power supply units. This is an Intel-validated power supply unit. Each power supply unit includes an integrated cooling fan. Each redundant power supply includes one AC line input.	Includes one of two redundant 830W PFC power supply units. This is an Intel-validated power supply unit. Each power supply unit includes an integrated cooling fan. Each redundant power supply includes one AC line input.
Memory Riser	N/A.	Includes two memory risers and a memory riser cage.
System Cooling	Two fixed, non-redundant chassis fans: one 120 mm and one 92 mm.	Two fixed, non-redundant chassis fans: one 120 mm and one 92 mm.
Peripheral Bays	Three tool-less, multi-mount 5.25-inch peripheral bays	Three tool-less, multi-mount 5.25-inch peripheral bays
Drive Bays (6+4) Bay Layout	One tool-less fixed drive bay for up to six drives. Supports up to ten drives.	One tool-less fixed drive bay for up to six drives. Supports up to six drives.
PCI Slots	Seven full-length PCI slots.	Seven full-length PCI slots.
Form Factor	5U pedestal, can be a rack-mounted.	5U pedestal, can be rack-mounted.
Front Panel	LEDs for NIC1, NIC2, System ID, HDD activity and system status. Power button, chassis ID button, reset button, NMI button. Optical side cover intrusion switch and connection for bezel intrusion switch. Integrated temperature sensor for fan speed management.	LEDs for NIC1, NIC2, System ID, HDD activity and system status. Power button, chassis ID button, reset button, NMI button. Optical side cover intrusion switch and connection for bezel intrusion switch. Integrated temperature sensor for fan speed management.
External	Two front USB ports and one optional front or rear mounted serial port.	Two front USB ports and one optional front or rear mounted serial port.
Color	Black	Black
Construction	1.0 mm, zinc-plated sheet metal, meets Intel cosmetic specification C25432.	1.0 mm, zinc-plated sheet metal, meets Intel cosmetic specification C25432.

Feature	Intel® Server Chassis SC5400 BRP	Intel® Server System SC5400RA
Chassis ABS	Fire retardant, non- brominated PC-ABS	Fire retardant, non- brominated PC-ABS
Dimensions (Rack)	8.6-inch x 16.6-inch x 27.4-inch	8.6-inch x 16.6-inch x 27.4-inch
Dimensions (Pedestal)	17.0-inch x 8.6-inch x 28.4-inch	17.0-inch x 8.6-inch x 28.4-inch
Weight	24.5 kg	28.12 kg
Optional Accessories	Rack conversion kit Rack cable management arm Intel® Remote Management Module Redundant power supply Four-drive fixed drive bay Six-drive hot-swap SAS/SATA backplane Six-drive hot-swap SAS/SATA expander backplane Four-drive hot-swap SAS/SATA backplane Four-drive hot-swap SAS/SATA expander backplane Redundant cooling upgrade kit 10-pack branding / customization panels Unpainted rack top cover Slimline CD-ROM / USB floppy kit	Rack conversion kit Rack cable management arm Intel® Remote Management Module Redundant power supply Six-drive hot-swap SAS/SATA backplane Six-drive hot-swap SAS/SATA expander backplane 10-pack branding / customization panels Unpainted rack top cover Slimline CD-ROM / USB floppy kit

Table 2. Intel® Server System SC5400RA Dimensions and Weights

	Pedestal Configuration	Rack Configuration
Height	17 inches (43.2 cm)	8.6 inches (21.8 cm)
Weight	62 pounds (28.12 kg)	62 pounds (28.12 kg)
Width	8.6 inches (21.8 cm)	16.6 inches (42.2 cm)
Depth	28.4 inches (70.9 cm)	27.4 inches (69.6 cm)
Clearance front	Ten inches (25.4 cm)	N/A
Clearance rear	Five inches (12.7 cm)	N/A
Clearance side	3 inches (7.6 cm)	N/A

Notes:

Shipping weights include packaging.

The weight varies due to installed accessories and hard drives.

2.2 Server Board Feature Set

Table 3. Server Board Features

Feature	Description
Processors	Socket J (771-pin LGA sockets) supporting one or two Dual-Core Intel® Xeon® processors 5000, 5100 and 5300 sequence with system bus speeds of 667 MHz, 1066 MHz, and 1333 MHz.
Memory	Sixteen DIMM sockets on two DIMM risers, with eight DIMM sockets on each riser, supporting fully buffered DIMM technology (FBDIMM) memory. 240-pin DDR2-533 and DDR2-677 FBDIMMs can be used.
Chipset	Intel® 5000P Memory Controller Hub Intel® ESB2-E I/O Controller
On-board Connectors / Headers	▪ Stacked PS/2* ports for keyboard and mouse ▪ Stacked video / DB9 serial port A connector ▪ Two RJ45 / 2xUSB connectors for 10 / 100 / 1000 Mb and USB 2.0 support ▪ One USB 2x5 pin header, which supports two USB ports ▪ One USB port Type A connector ▪ One DH10 serial port B header ▪ Six SATA-2 connectors with integrated RAID 0, 1, and 10 support ▪ Software RAID 5 support through an optional SATA RAID KEY ▪ One ATA100 40-pin connector ▪ One RMM connector to support the optional Intel® Remote Management Module ▪ One I/O connector supporting an optional Intel® RMM NIC I/O module ▪ SSI-compliant front panel header ▪ SSI-compliant 24-pin main power connector, supporting the ATX-12 V standard on the first 20 pins
Add-in PCI, PCI-X*, PCI Express* Cards	▪ One full-length / full-height PCI-X* 64-bit slot with up to 100 MHz support ▪ One full-length / full-height PCI-X 64-bit slot with up to 133-MHz support when only one PCI-X slot is populated ▪ One full-length / full-height PCI Express* x8 ▪ One half-length / full-height PCI Express x4 slot ▪ Two full-length / full-height PCI Express x8 slots
Video	On-board ATI* ES1000 video controller with 16-MB DDR SDRAM
Hard Drive	Support for six SATA-2 hard drives
LAN	Two 10 / 100 / 1000 Intel® 82563EB PHYs supporting Intel® I/O Acceleration Technology
Fans	Support for ▪ Two processor fans ▪ Four front hot-swap fans ▪ Two rear system fans
Server Management	Support for Intel® System Management Software

2.3   Intel® Server System SC5400RA Layout
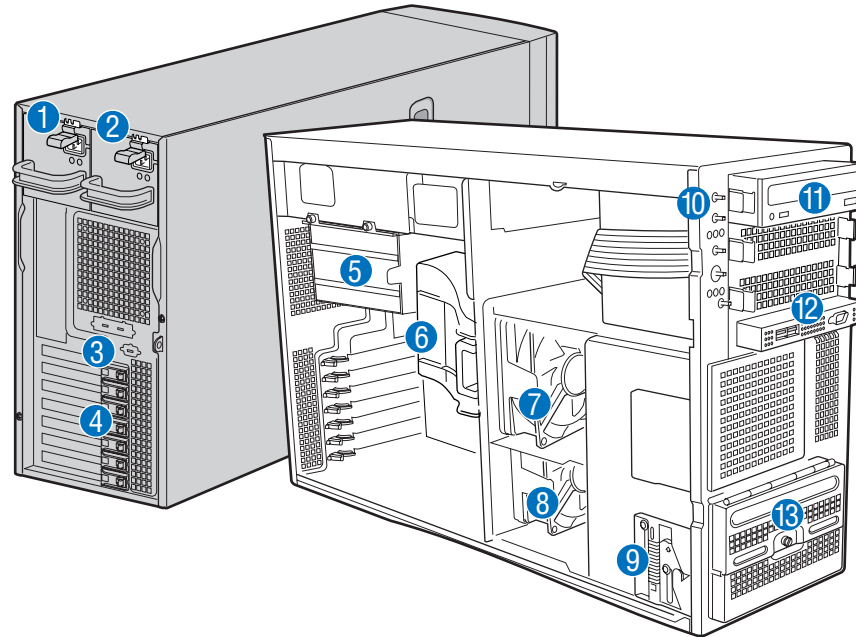
1. Hot-swap power supply	8. Fixed fan – 92 mm
2. Hot-swap power supply (optional)	9. Hard drive cage release mechanism
3. Rear serial B connector	10. Front panel controls
4. PCI add-in card panel	11. 5.25-inch device bays (three)
5. Memory riser cage	12. Front panel USB / Serial B connectors
6. Processor air duct	13. Six-drive fixed drive cage
7. Fixed fan – 120 mm	

Figure 1. Intel® Server System SC5400RA

2.4   Server Board Connector and Component Layout

Figure 2. Major Board Components
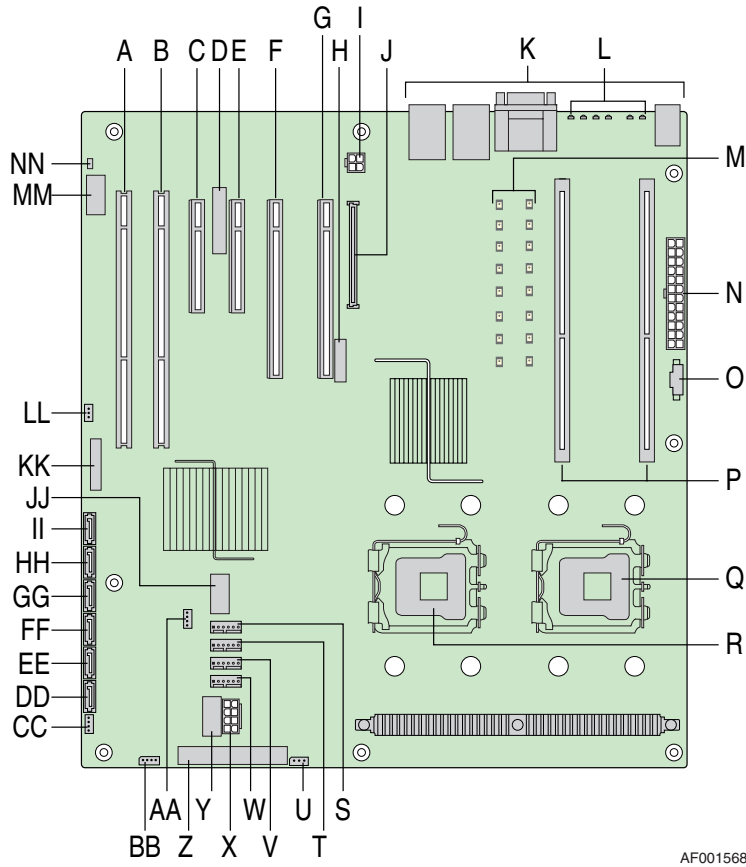
A. PCI-X 64-bit, 100-MHz slot 1	O. Auxiliary power signal connector	BB. Intel® Local Control Panel header
B. PCI-X 64-bit, 133-/100-MHz slot 2	P. DIMM riser sockets	CC. Hot-swap backplane A header
C. PCI Express* x8 slot 3	Q. Processor 1 socket	DD. SATA 0
D. Intel® RMM NIC connector	R. Processor 2 socket	EE. SATA 1
E. PCI Express* x8 slot 4	S. System fan 4 header	FF. SATA 2
F. PCI Express x8 slot 5	T. System fan 3 header	GG. SATA 3
G. PCI Express x8 slot 6	U. IPMB connector	HH. SATA 4
H. CMOS battery	V. System fan 2 header	II. SATA 5
I. P12V4 connector	W. System fan 1 header	JJ. USB port
J. Intel® Remote Management Module (RMM) connector	X. Processor power connector	KK. Front control panel header
K. Back panel I/O ports	Y. USB header	LL. SATA RAID 5 key connector
L. Diagnostic and identify LEDs	Z. IDE connector	MM. Serial B / emergency management port header
M. DIMM LEDs	AA. Enclosure management SATA SGPIO header	NN. Chassis intrusion header
N. Main power connector		

2.4.1   Server Board Mechanical Drawings
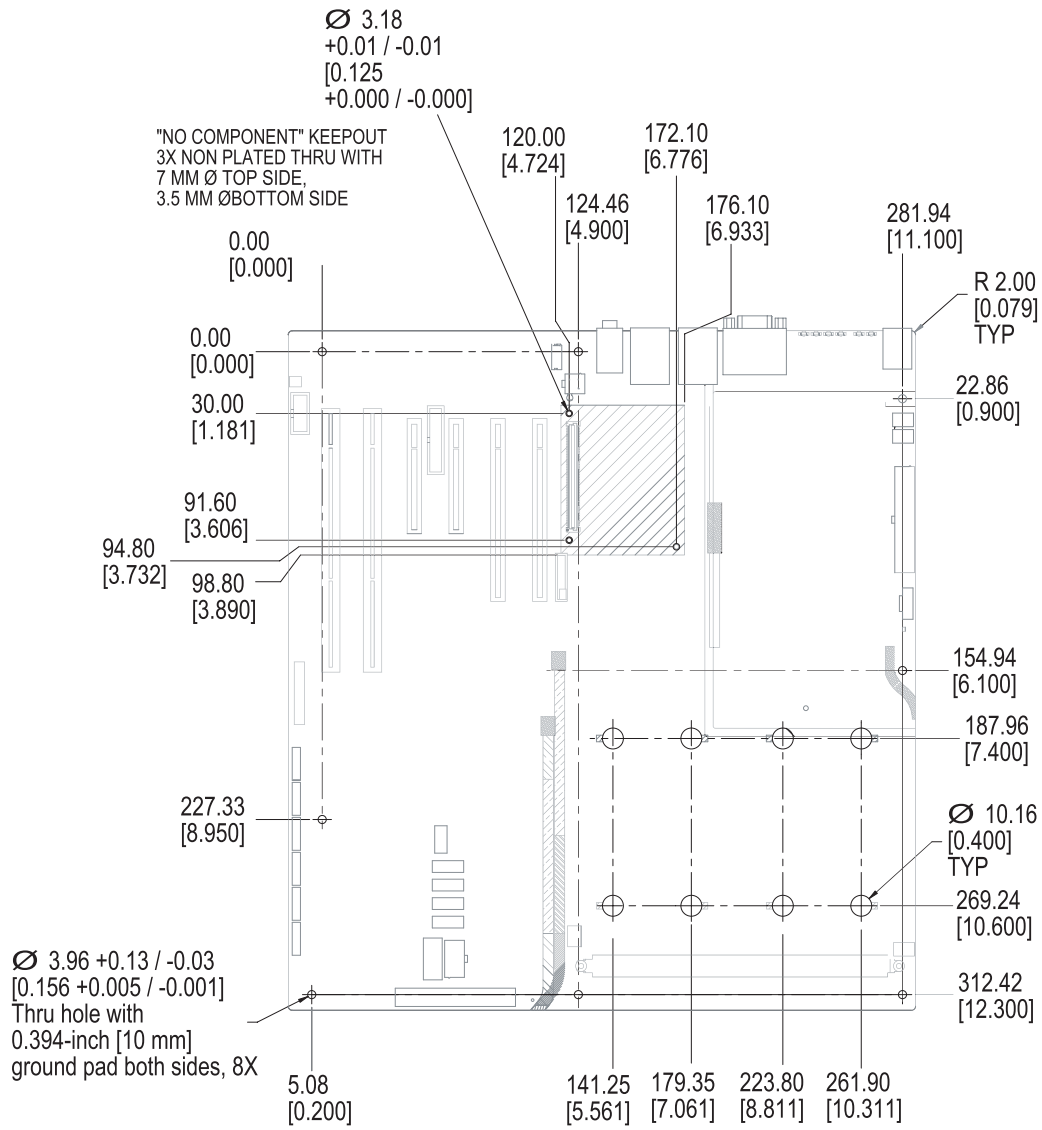
Figure 3. Mounting Hole Positions
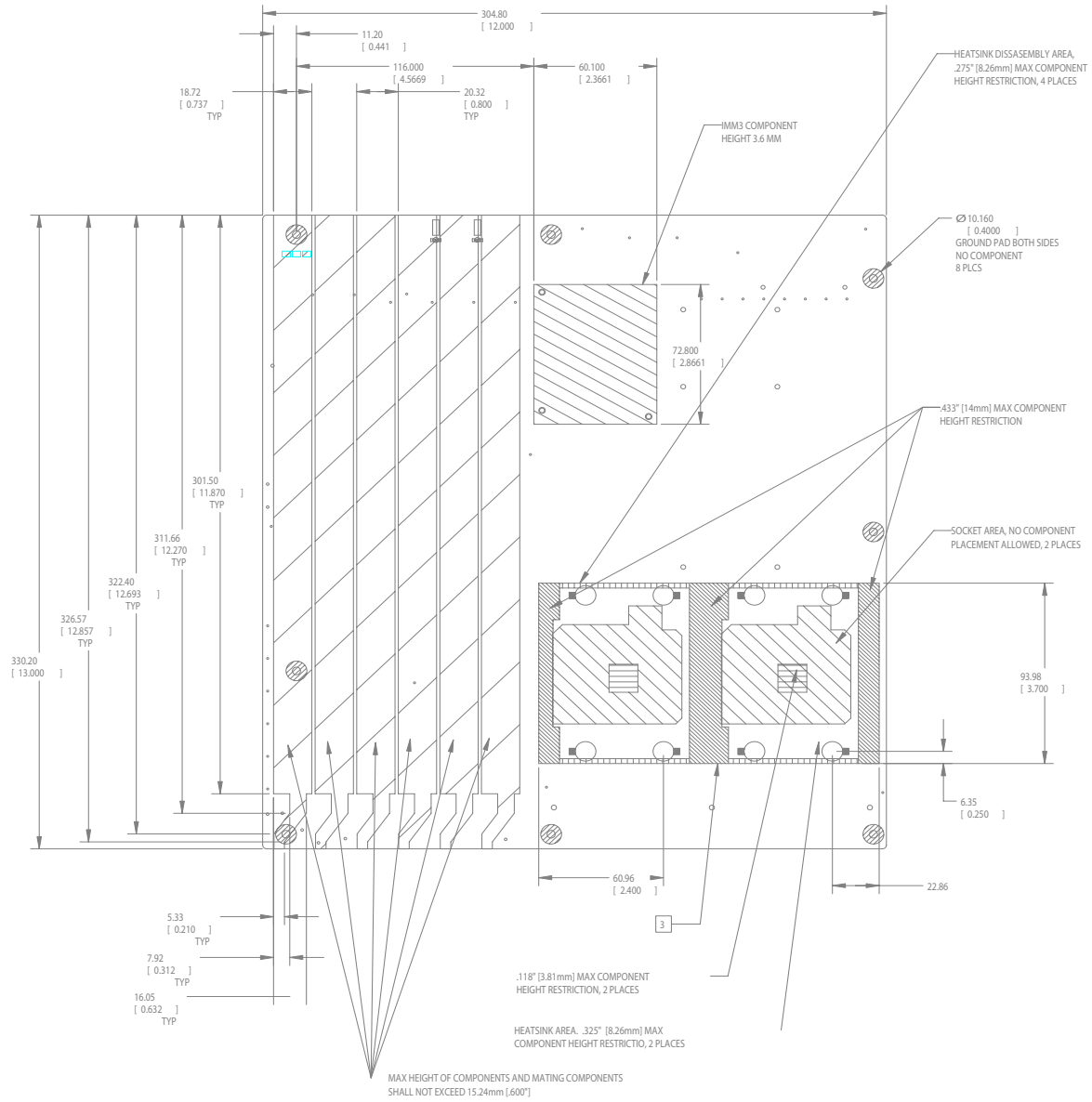
Figure 4. Restricted Areas on Side 1
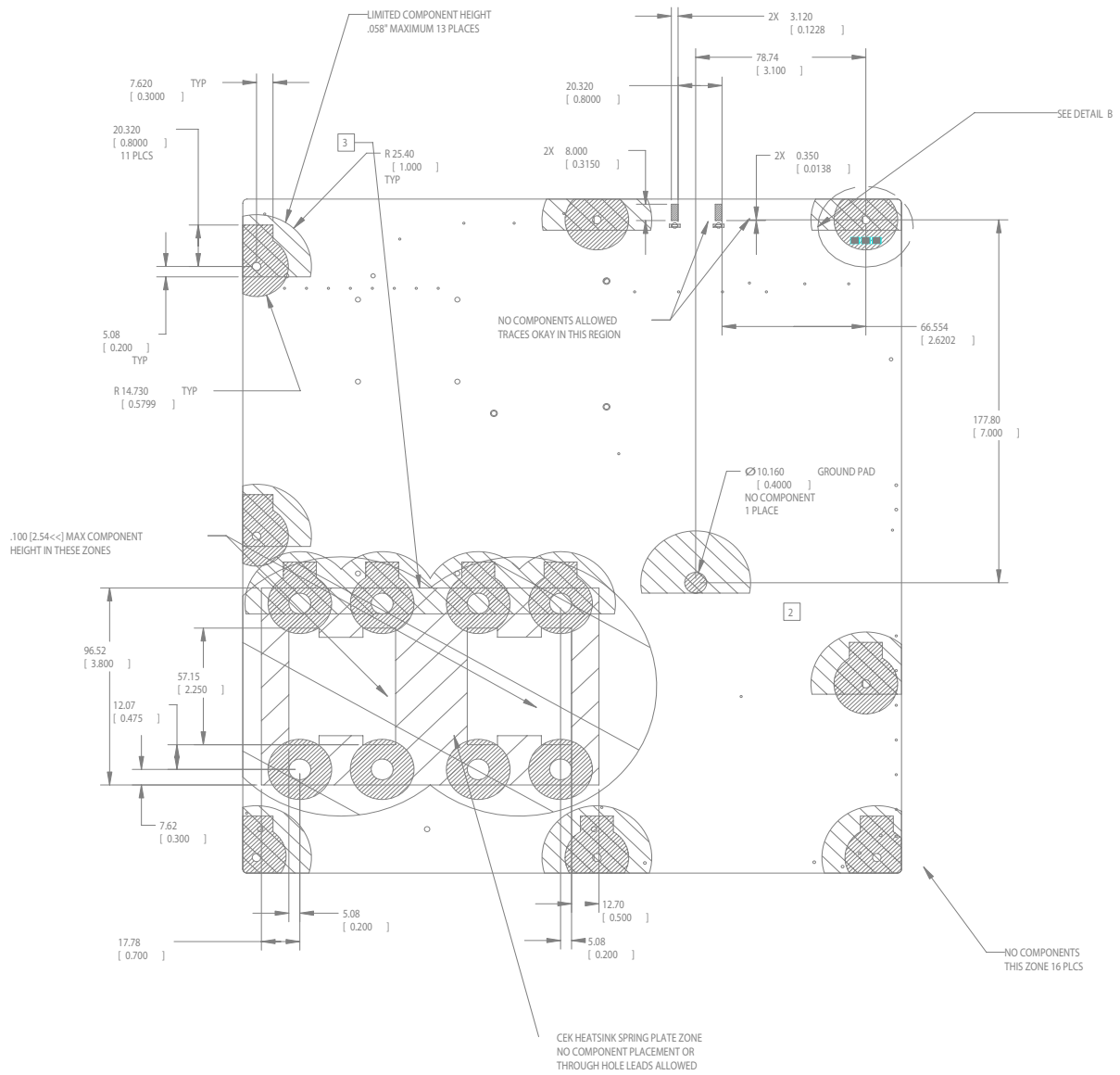
Figure 5. Restricted Areas on Side 2
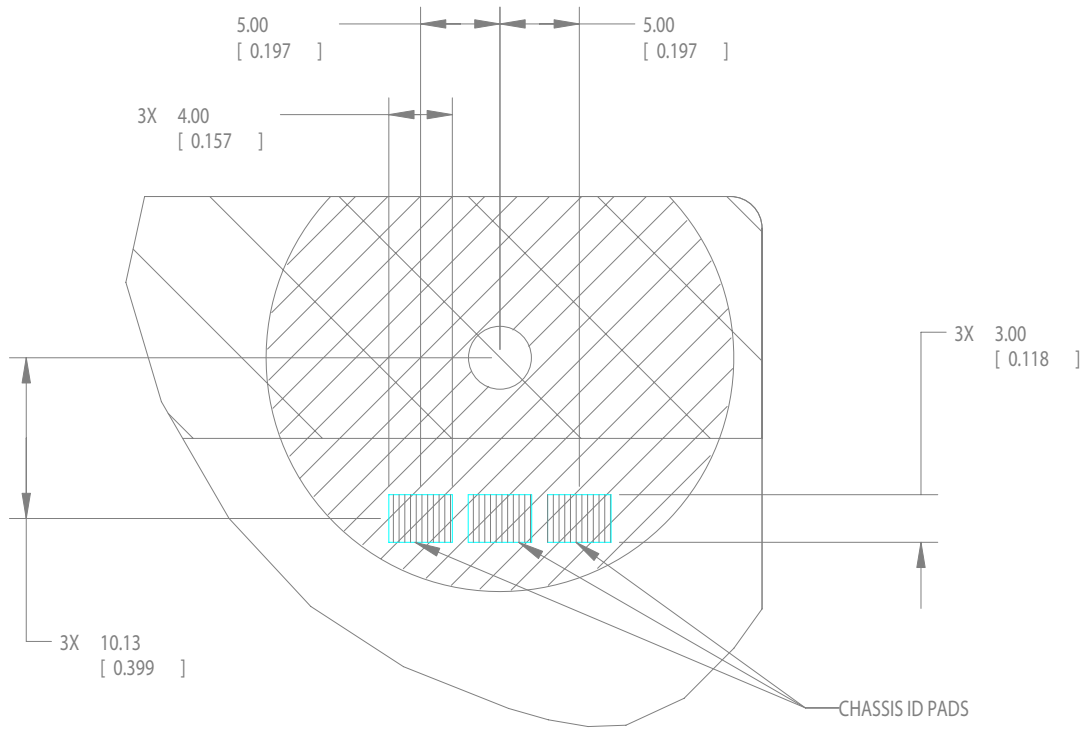
Figure 6. Restricted Areas on Side 2, "Detail B"
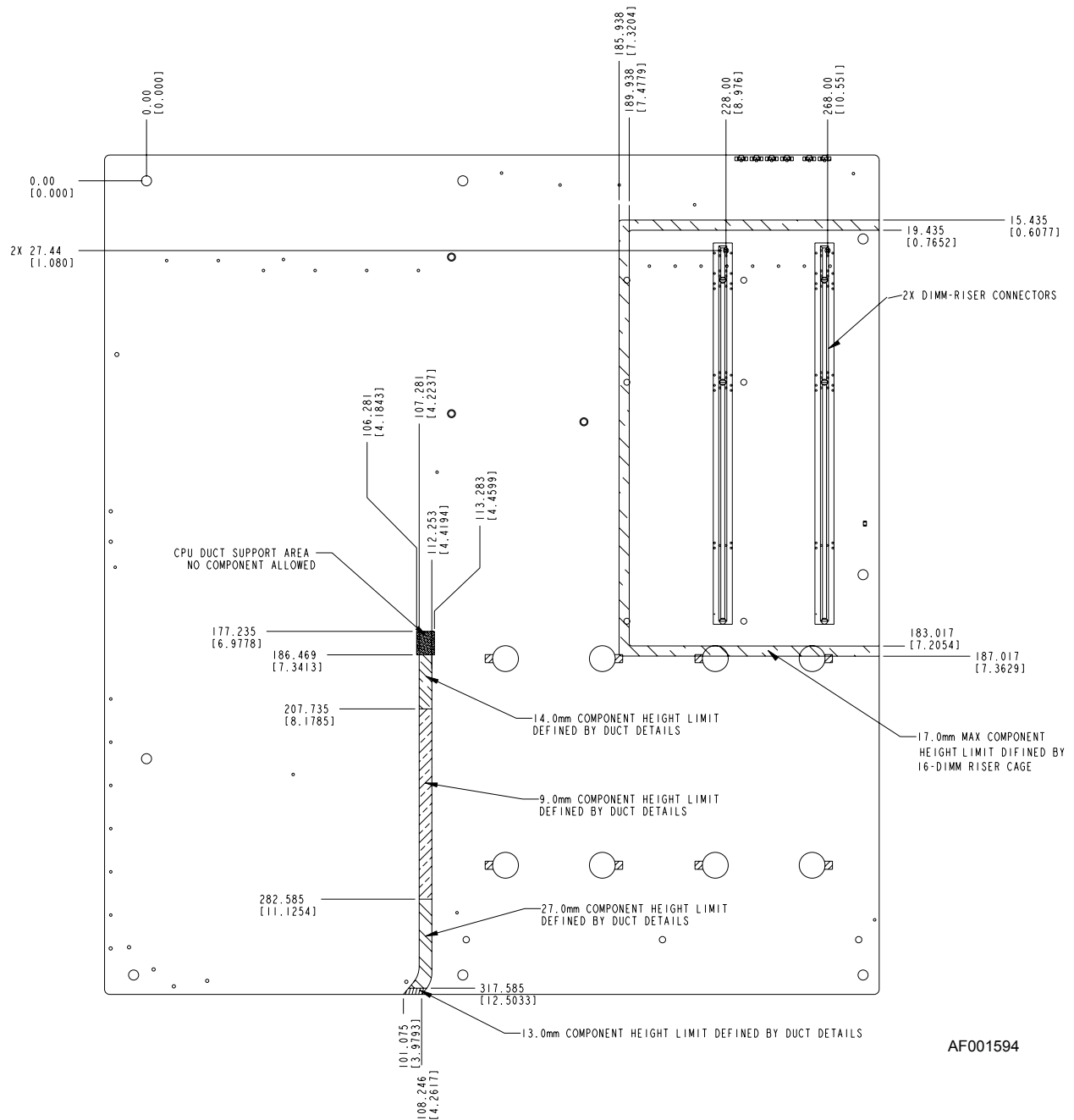
Figure 7. CPU and Memory Duct Keepout

2.4.2   Rear I/O Component Layout
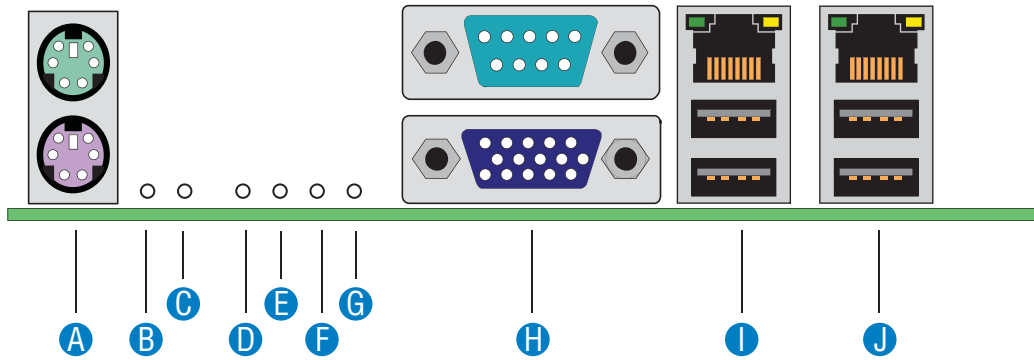
AF000421

A. PS/2 mouse (top), keyboard (bottom)	F. Bit 1 LED (POST LED)
B. Status LED	G. LSB LED (POST LED)
C. ID LED	H. Serial A (top), video (bottom)
D. MSB LED (POST LED)	I. NIC1 (top), two USB ports (bottom)
E. Bit 2 LED (POST LED)	J. NIC 2 (top), two USB ports (bottom)

Figure 8. Rear I/O Component Layout

3.   Functional Architecture

3.1   Drive Installation Options

The server system includes one fixed bay that supports six cabled drives. An optional six-drive hot-swap drive bay is available to replace the six-drive fixed drive bay. No tools are required to replace the fixed drive bay.

Note: *The four-drive bay for cabled (fixed) drives and the four-drive hot-swap bay are not supported in the Intel® Server System SC5400RA.*

Three 5.25-inch half-height peripheral bays are available for installing a floppy, CD-ROM drive or other accessories.

3.2   System Cooling

The cooling for the Intel® Server System SC5400RA chassis consists of two fixed fans: one 92 mm fan and one 120 mm fan. These fans provide cooling for the processors, hard drives, and add-in cards. The fans draw in air through the rear of each hard drive bay. The fans maintain proper system cooling even if one of the fans fails. An air duct and the riser cage are necessary to maintain a proper airflow within the system.

A power supply fan provides cooling for the power supply.

The circled area in the figure shows the location of the two fixed fans.

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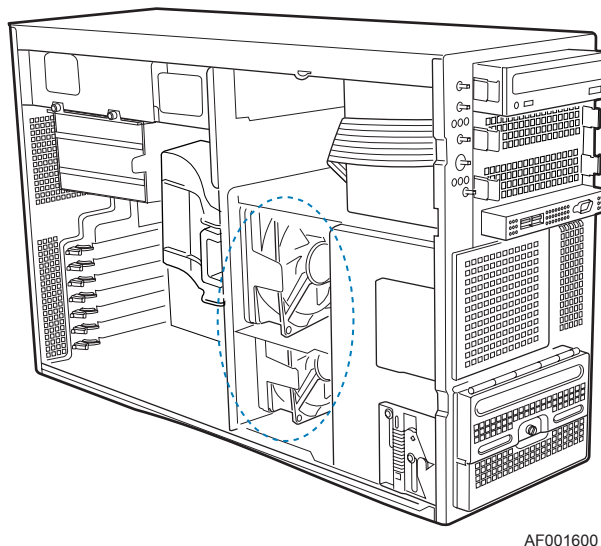
Figure 9. Fixed Fan Location

3.2.1 Processor Air Duct and Heat Sinks

Both of the passive tower heat sinks that are included with the server system must be installed at all times to maintain a proper air flow, even if only one processor is installed. The processor air duct shown below works with the heat sinks and must be installed at all times to maintain a proper air flow.
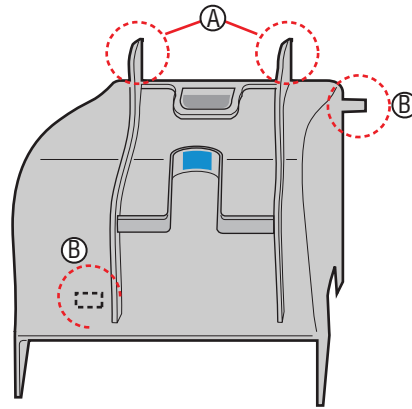
AF001601

A.   These two tabs slide into matching slots in the top edge of the chassis center wall
B.   These two tabs slide into matching hooks in the chassis wall

Figure 10. Processor Air Duct
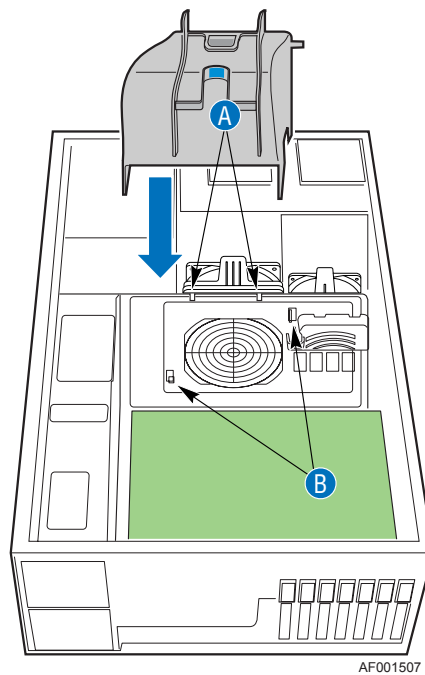
AF001507

Figure 11. Processor Air Duct Installation

The figure below shows the airflow characteristics through the server system.
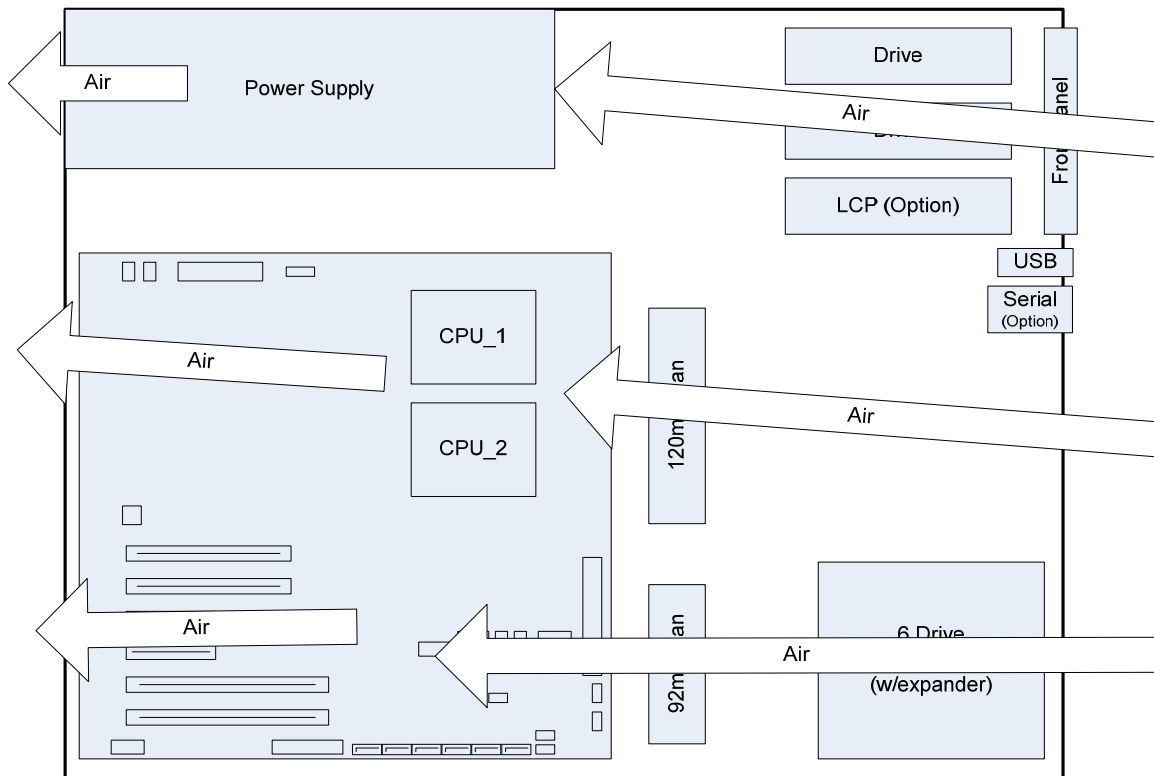
Figure 12. Redundant Chassis Airflow

3.3   Power Sub-system

The server system supports the redundant power capability of the Intel® Server Chassis SC5400 LX configuration and the fixed fan features of the Intel® Server Chassis SC5400 BASE configuration.

The Intel® Server System SC5400RA includes one 830-watt PFC power supply module. Two tachometer output fans are mounted in front of the server board and a second 830-watt power supply module can be added to provide redundancy.

The Intel® Server System SC5400RA chassis power supply is server system infrastructure (SSI) compliant. The 830-watt power distribution board has power supply wire harness cable lengths to reach peripheral bays and server board.

The 830 watt power supply replaceable module 12 V and 5 VSB outputs. The input is power factor corrected. An IEC connector on the external face provides for AC input to the power supply. The power supply contains one cooling fan.

Note: The SSI specifications are at www.ssifourm.org.

3.4   Server Board / Chassis Interconnections
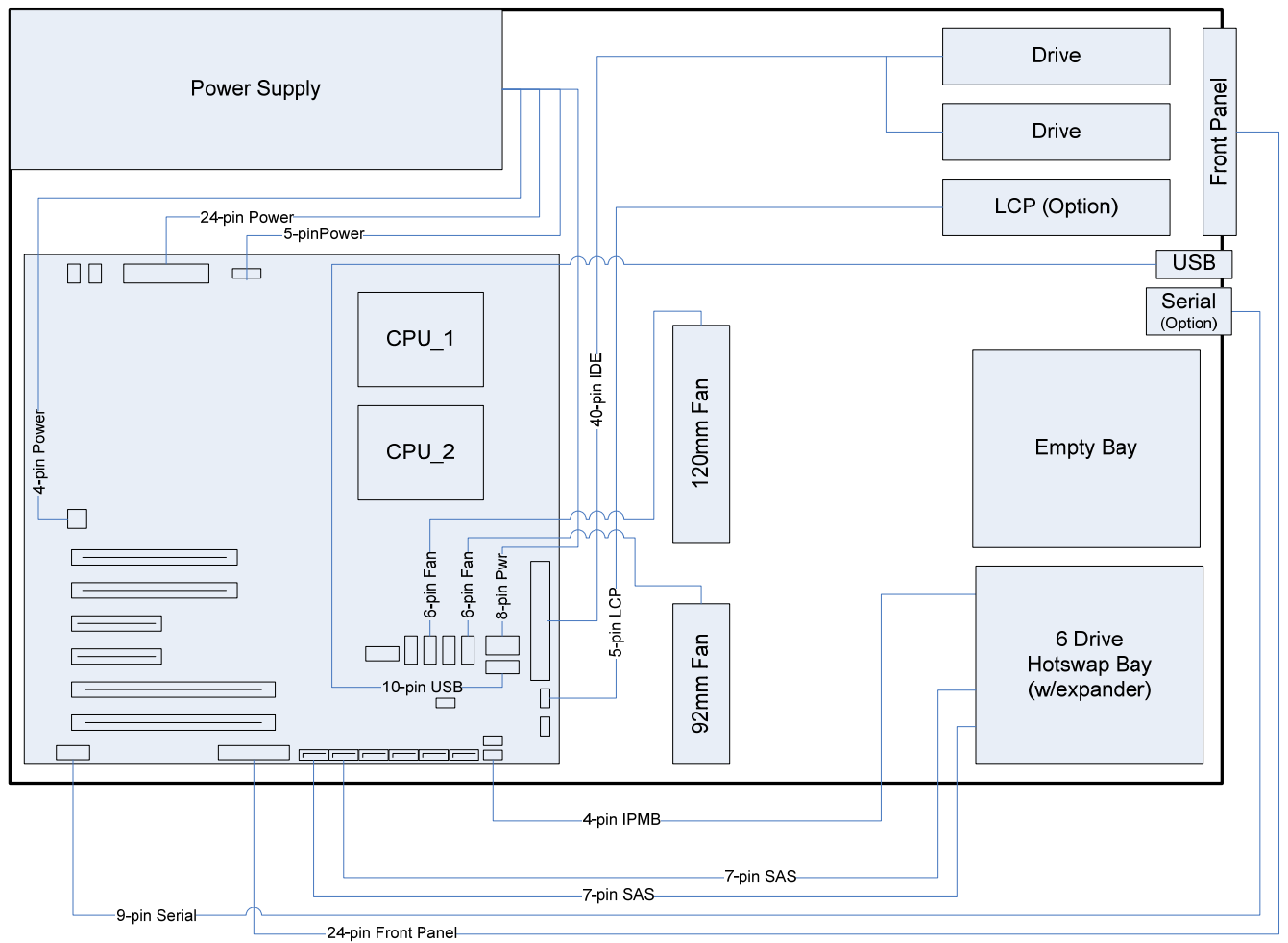
Figure 13. Chassis Interconnect Diagram with Expander Backplane
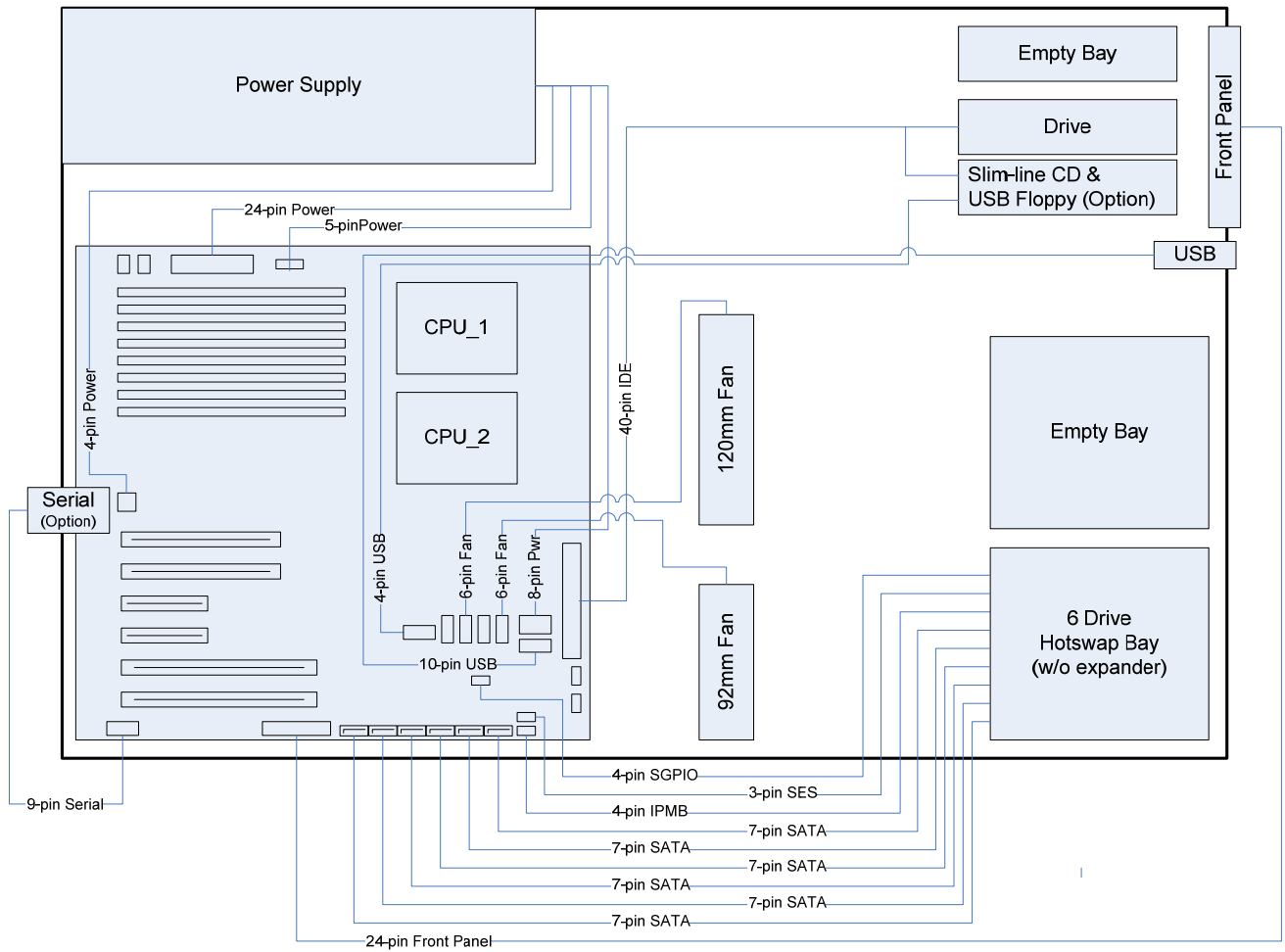
Figure 14. Chassis Interconnect Diagram with Non-Expander Backplane

3.5   Chassis Internal Cables

The following cables are provided as part of the chassis kit and accessories.

Table 4. Internal Cables

Cable Description	Source
Front panel cable 24-pin	Server System
ATA 100 (IDE) cable	Server System
SAS/SATA data cables for hot-swap drive bays	AXX6DRV3G, AXX6DRV3GEXP Accessory. See Appendix E.
SES 3-pin cable	AXX6DRV3G Accessory. See Appendix E.
IPMB 4-pin cable	AXX6DRV3G, AXX6DRV3GEXP Accessory. See Appendix E.
SATA cables for fixed drives	Server System
Local Control Panel (LCP) I^{2}C cable	Accessory. See Appendix E.
USB cable	Server System
Serial COM cable	Server System
Intrusion switch cable	Server System

3.6   Server Board Architecture

The architecture and design of the Intel® Server Board SC5400RA is based on the Intel® S5000P chipset. This chipset is used in systems that use the Dual-Core Intel® Xeon® processor 5000, 5100 or 5300 sequence with system bus speeds of 667 MHz, 1066 MHz, and 1333 MHz.

The chipset contains two main components: the Memory Controller Hub (MCH) for the host bridge and the I/O controller hub for the I/O sub-system. The chipset uses the Enterprise South Bridge (ESB2-E) for the I/O controller hub.

For more information about the functional architecture blocks, see the *Intel® S5000 Server Board Family Datasheet.*
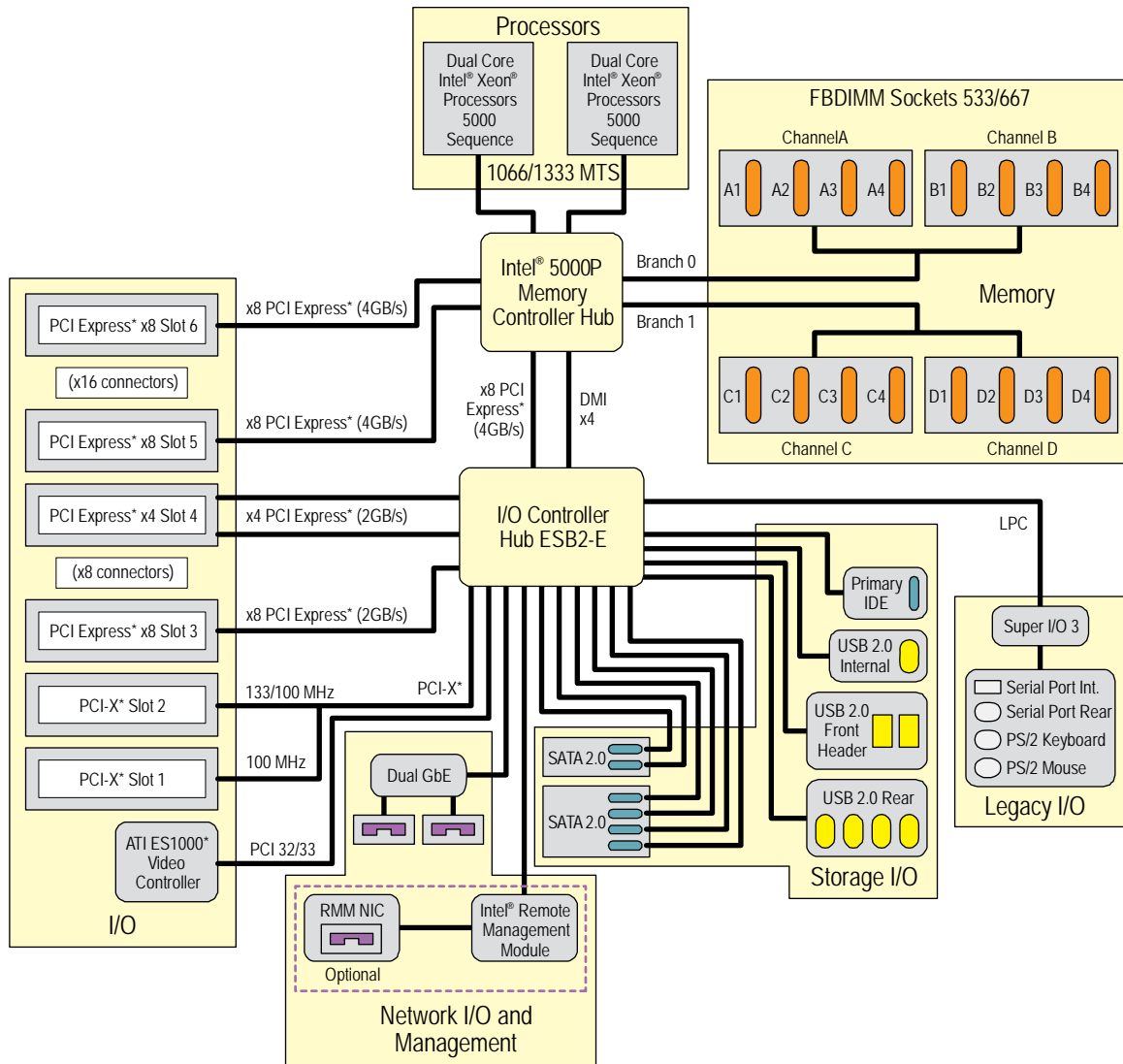
Figure 15. Functional Block Diagram

3.7   Intel® 5000P Memory Controller Hub (MCH)

The Memory Controller Hub (MCH) is a single 1432-pin FCBGA package that includes the following core platform functions:

- System bus interface for the processor sub-system
- Memory controller
- PCI-Express* ports including the Enterprise South Bridge Interface (ESI)
- FBD thermal management
- SMBUS interface

This section provides a high-level overview of some of these core functions as they pertain to this server system. Additional information can be obtained from the *Intel S5000 Server Board Family Datasheet* and the *Intel 5000 Series Chipset Memory Controller Hub Datasheet.*

3.7.1   System Bus Interface

The MCH is configured for symmetric multi-processing across two independent front side bus interfaces that connect to the processors. Each front side bus on the MCH uses a 64-bit wide 667, 1066, or 1333 MHz data bus. The 1333 MHz data bus can transfer data at up to 10.66 GB/s. The MCH supports a 36-bit wide address bus that can address up to 64 GB of memory. The MCH is the priority agent for both front side bus interfaces, and is optimized for one processor on each bus.

3.7.2   Processor Support

The server system supports one or two Dual-Core Intel® Xeon® processors 5000, 5100 or 5300 sequence with system bus speeds of 667 MHz, 1066 MHz, or 1333 MHz, and core frequencies starting at 3.73 GHz. Previous generations of the Intel® Xeon® processor are not supported.

Table 5. Supported Processors

Processor Family	System Bus Speed	Core Frequency	Cache	Watts	Support
Dual-Core Intel® Xeon® Processor 5030	667MHz	2.67 GHz	2x 2 MB	95	Yes
Dual-Core Intel® Xeon® Processor 5050	667 MHz	3.0 GHz	2x 2 MB	95	Yes
Dual-Core Intel® Xeon® Processor 5060	1066 MHz	3.2 GHz	2x 2 MB	130	Yes
Dual-Core Intel® Xeon® Processor 5063	1066 MHz	3.2 GHz	2x 2 MB	95	Yes
Dual-Core Intel® Xeon® Processor 5080	1066 MHz	3.73 GHz	2x 2 MB	130	Yes
Dual-Core Intel® Xeon® Processor 5110	1066 MHz	1.60 GHz	4 MB	65	Yes
Dual-Core Intel® Xeon® Processor 5120	1066 MHz	1.86 GHz	4 MB	65	Yes

Processor Family	System Bus Speed	Core Frequency	Cache	Watts	Support
Dual-Core Intel® Xeon® Processor 5130	1333 MHz	2.00 GHz	4 MB	65	Yes
Dual-Core Intel® Xeon® Processor 5140	1333 MHz	2.33 GHz	4 MB	65	Yes
Dual-Core Intel® Xeon® Processor 5148	1333 MHz	2.33 GHz	4 MB	35	Yes
Dual-Core Intel® Xeon® Processor 5150	1333 MHz	2.66 GHz	4 MB	65	Yes
Dual-Core Intel® Xeon® Processor 5160	1333 MHz	3.00 GHz	4 MB	80	Yes
Quad-Core Intel® Xeon® Processor L5310	1066 MHz	1.60 GHz	8 MB	50	Yes
Quad-Core Intel® Xeon® Processor E5310	1066 MHz	1.60 GHz	8 MB	80	Yes
Quad-Core Intel® Xeon® Processor E5320	1066 MHz	1.86 MHz	8 MB	80	Yes
Quad-Core Intel® Xeon® Processor E5345	1333 MHz	2.33 MHz	8 MB	80	Yes
Quad-Core Intel® Xeon® Processor X5355	1333 MHz	2.66 MHz	8 MB	120	Yes

3.7.2.1 Processor Population Rules

When two processors are installed, both must have identical revisions, core voltages, and bus/core speeds. When only one processor is installed, it must be in the socket labeled CPU1. A processor terminator should not be installed.

The board provides up to 130 A of current per processor. Processors with higher current requirements are not supported.

3.7.2.2 Common Enabling Kit (CEK) Design Support

The server system complies with Intel's common enabling kit (CEK) processor mounting and heat sink retention solution. The server system ships with a CEK spring snapped onto the underside of the server board, beneath each processor socket. The heat sink attaches to the CEK on the top of the processor and the thermal interface material (TIM). See the figure below.

The CEK spring is removable, allowing for the use of non-Intel heatsink retention solutions.

Note: The processor heat sink and CEK spring shown in the following diagram are for reference only. The processor heat sink and CEK might look different.

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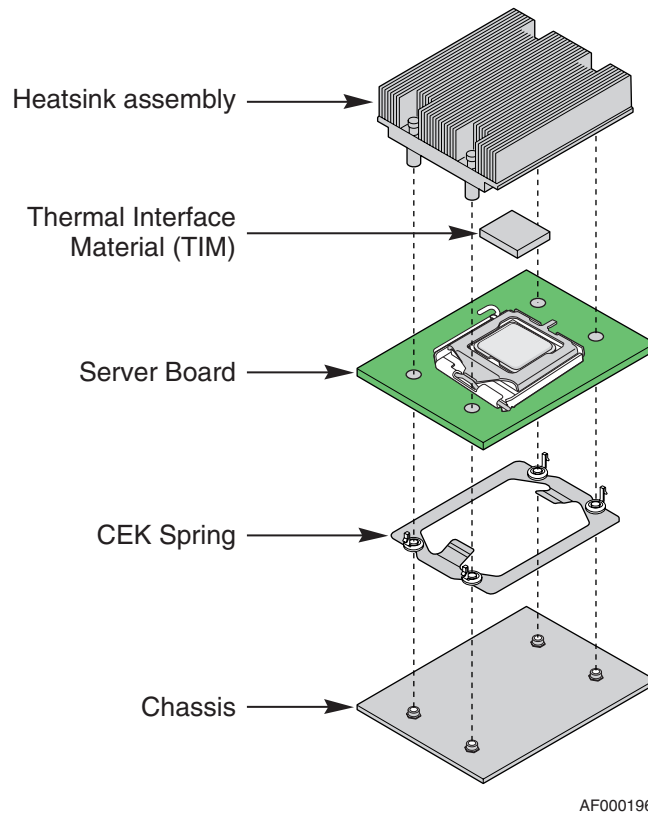
Figure 16. CEK Processor Mounting

3.7.3   Memory Sub-system

The MCH masters four fully-buffered DIMM (FBD) memory channels. FBD memory utilizes a narrow high-speed, frame-oriented interface, referred to as a channel. The four FBD channels are organized into two branches, with two channels on each branch. Each branch is supported by a separate memory controller. The two channels on each branch operate in lock-step to increase FBD bandwidth.

The four channels are routed to sixteen DIMM sockets and support registered DDR2-533 and DDR2-667 FBDIMM memory (stacked or unstacked). The read bandwidth of each FBDIMM channel is 4.25 GB/s for DDR2-533 FBDIMM memory, which gives a total read bandwidth of 17 GB/s for four DIMM channels. The read bandwidth of each FBDIMM channel is 5.35 GB/s for DDR2-667 FBDIMM memory, which gives a total read bandwidth of 21.4 GB/s for four DIMM channels.

The server system supports two DIMM riser cards. Each DIMM riser card supports eight DIMM sockets, for total of sixteen DIMM sockets.

FBD memory channels are organized into two branches for support of RAID 1 (mirroring). A pair of channels becomes a branch in which Branch 0 consists of channels A and B, and Branch 1 consists of channels C and D. Branch 0 is routed to DIMM riser card 1 and Branch 1 is routed to DIMM riser card 2 (closest to the edge of the server board).

To boot the system, the system BIOS on the server board uses a dedicated I^{2}C bus to retrieve DIMM information to program the MCH memory registers. The following figure and table provides the I^{2}C addresses for each DIMM socket and identifies the channels on each DIMM riser card.

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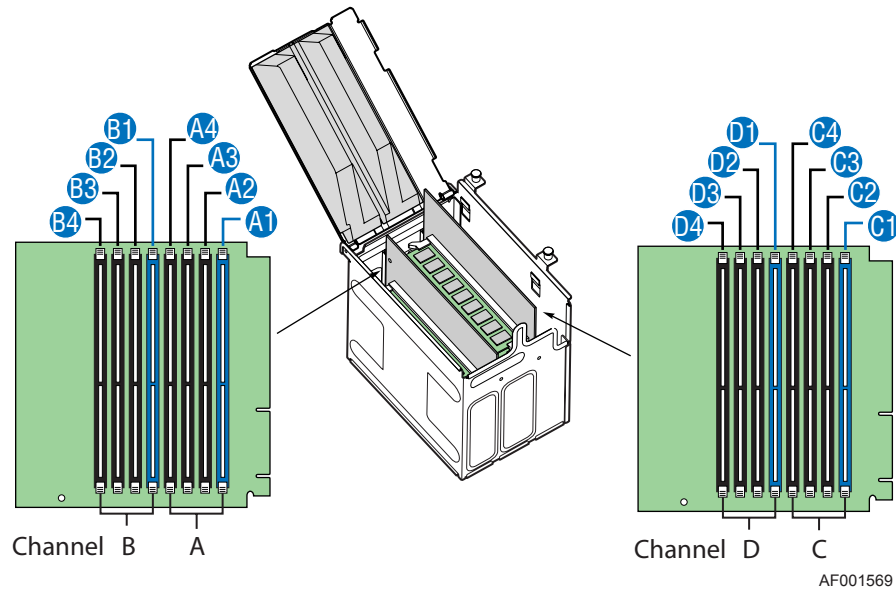
Table 6. I^{2}C Addresses for Memory Module SMB

Riser Card 1		Riser Card 2	
Device	**Address**	**Device**	**Address**
DIMM A1	0xA0	DIMM C1	0xA0
DIMM A2	0xA2	DIMM C2	0xA2
DIMM A3	0xA4	DIMM C3	0xA4
DIMM A4	0xA6	DIMM C4	0xA6
DIMM B1	0xA0	DIMM D1	0xA0
DIMM B2	0xA2	DIMM D2	0xA2
DIMM B3	0xA4	DIMM D3	0xA4
DIMM B4	0xA6	DIMM D4	0xA6

3.7.3.1   Memory RASUM Features

The MCH supports memory RASUM (reliability, availability, serviceability, usability, and manageability) features. These features include the Intel® x4 Single Device Data Correction (Intel® x4 SDDC) for the following:

- Memory error detection and correction
- Memory scrubbing
- Retry on correctable errors
- Memory built-in self-test

- DIMM sparing
- Memory mirroring

See the *Intel® S5000 Server Board Family Datasheet*.

3.7.3.2   Supported Memory

The server system supports up to sixteen DDR2-533 or DDR2-667 fully-buffered DIMMs (FBD memory). The following tables show the maximum memory configurations supported with the specified memory technology.

Table 7. Maximum Sixteen-DIMM System Memory Configruation – x8 Single Rank

DRAM Technology x8 Single Rank	Maximum Capacity Mirrored Mode	Maximum Capacity Non-mirrored Mode
512 Mb	4 GB	8 GB
1024 Mb	8 GB	16 GB

Table 8. Maximum Sixteen-DIMM System Memory Configuration – x4 Dual Rank

DRAM Technology x4 Dual Rank	Maximum Capacity Mirrored Mode	Maximum Capacity Non-mirrored Mode
1024 Mb	16 GB	32 GB
2048 Mb	32 GB	64 GB

Note: Only fully buffered DDR2 DIMMs (FBDIMMs) are supported on this server system. See the Intel® Server System SC5400RA Tested Memory List *for a list of supported memory for this server system.*

3.7.3.3   DIMM Population Rules and Supported DIMM Configurations

The DIMM population rules depend on the operating mode of the memory controller, which is determined by the number of DIMMs installed. DIMMs must be populated in multiples of four. DIMMs are populated in the following DIMM slot order: A1, B1, C1, D1; A2, B2, C2, D2, and so on.

DIMMs within a given multiple of four must be identical with respect to size, speed, and organization. However, DIMM capacities can be different between different DIMM multiple of four. For example, a valid mixed DIMM configuration may have 512 MB DIMMs installed in DIMM sockets A1, B1, C1, and D1, and 1 GB DIMMs installed in DIMM slots A2, B2, C2, and D2.

Supported DIMM configurations are shown in the following table. In the table, the following codes are used:

- VP: Validated configuration and the slot is populated
- SP: Supported, but not validated configuration, and the slot is populated
- NP: Slot is not populated

Branch 0								Branch 1								Mirroring Possible	Sparing Possible
Channel A				Channel B				Channel C				Channel D					
A1	A2	A3	A4	B1	B2	B3	B4	C1	C2	C3	C4	D1	D2	D3	D4		
VP	NP	NP	NP	VP	NP	NP	NP	VP	NP	NP	NP	VP	NP	NP	NP	VP. Yes	No
SP	SP	NP	NP	SP	SP	NP	NP	SP	NP	NP	NP	SP	NP	NP	NP		No
VP	VP	NP	NP	VP	VP	NP	NP	VP	SP	NP	NP	VP	VP	NP	NP	VP. Yes	VP. Yes
SP	SP	SP	NP	SP	SP	SP	NP	SP	VP	NP	NP	SP	SP	NP	NP		SP. Yes
VP	VP	VP	NP	VP	VP	VP	NP	VP	SP	VP	NP	VP	VP	VP	NP	VP. Yes	VP. Yes
SP	SP	SP	SP	SP	SP	SP	SP	SP	SP	SP	NP	SP	SP	SP	NP		SP. Yes
VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP. Yes	VP. Yes

Notes:

- The supported memory configurations must meet population rules defined above.
- For best performance, the number of DIMMs installed should be balanced across both memory branches. For example: a eight-DIMM configuration performs better than a four-DIMM configuration, with DIMMs installed in DIMM slots A1, B1, C1, and D1, and A2, B2, C2, and D2. A 12-DIMM configuration performs better then an 8-DIMM configuration.
- Although mixed DIMM capacities between channels are supported, Intel does not validate DIMMs in a mixed DIMM configuration.

3.7.3.3.1   *Minimum Non-Mirrored Mode Configuration*

At least four DIMMs must be installed. The following diagram shows the recommended minimum DIMM memory configuration. The populated DIMM slots are shown in blue.
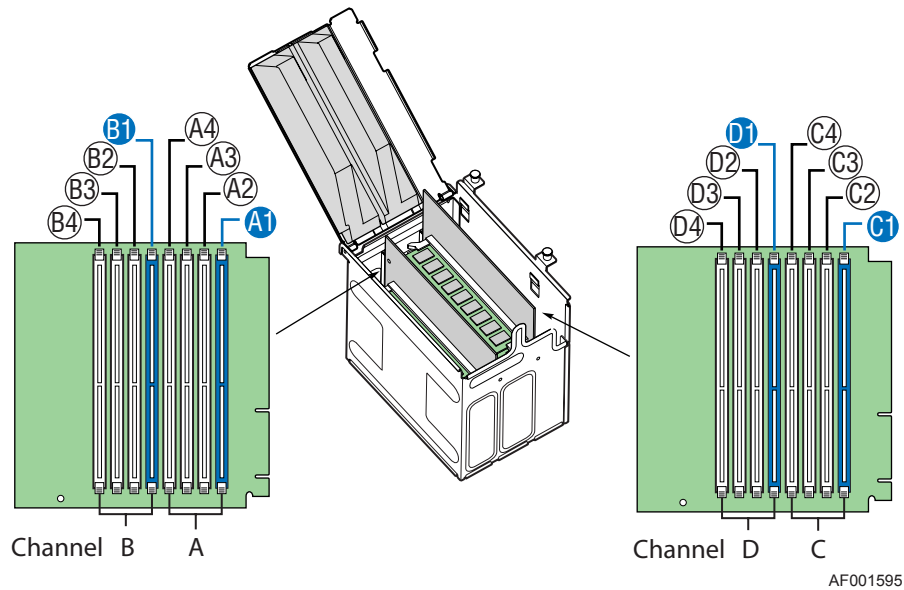
Figure 17. Minimum Four DIMM Memory Configuration

3.7.3.4   Non-mirrored Mode Memory Upgrades

The minimum memory upgrade increment is four DIMMs. The DIMMs must cover the same slot position on all four channels. DIMMs must be identical with respect to size, speed, and organization. DIMMs that cover adjacent slot positions do not need to be identical.

When adding four DIMMs to the configuration shown in Figure 17 (above), the second set of DIMMs should be populated in DIMM sockets A2, B2, C2 and D2 as shown in the following diagram. The set of four DIMMs that must be populated second are shown in grey.
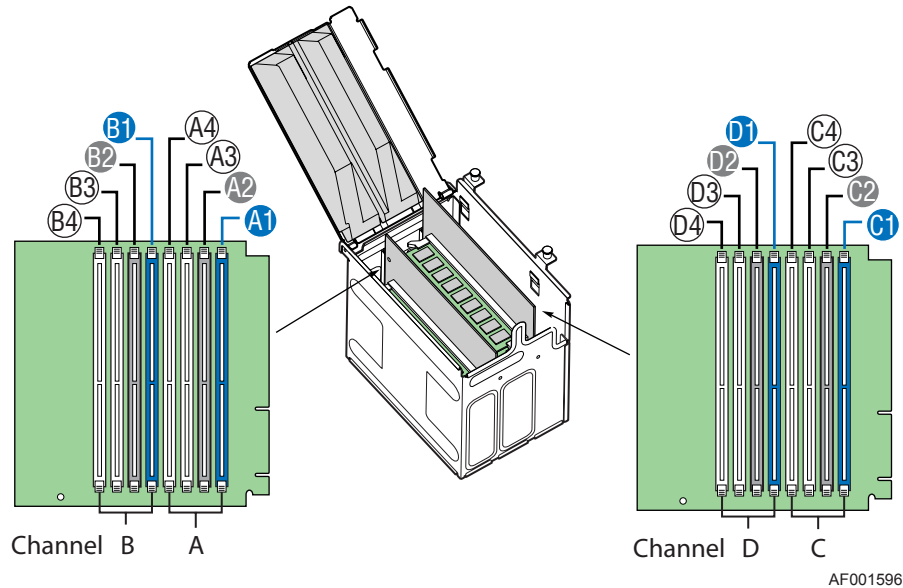
Figure 18. Recommended Eight DIMM Configuration

3.7.3.4.1   Mirrored Mode Memory Configuration

In mirrored mode, both branches operate in lock-step. Branch 1 contains a replicate copy of the data in branch 0. At least four DIMMs must be installed for support memory mirroring. All four DIMMs must be identical with respect to size, speed, and organization.

To upgrade a four-DIMM mirrored memory configuration, a second set four DIMMs must be installed. The second set of four DIMMs must be identical to the first set, except for speed. The MCH adjusts to the lowest speed DIMM.

3.7.3.4.2   Sparing Mode Memory Configuration

The MCH provides memory sparing capabilities. Sparing is a RAS feature that involves configuring a DIMM to be placed in reserve so it can be use to replace a DIMM that fails. DIMM sparing occurs within a given bank of memory and is not supported across branches. There are two supported memory sparing configurations.

- Single-branch mode sparing
- Dual-branch mode sparing

3.7.3.4.2.1   Single-branch Mode Sparing
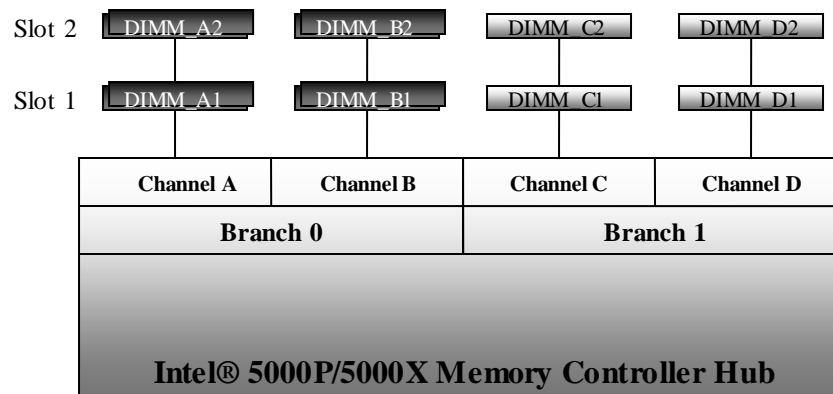
Figure 19. Single-branch Mode Sparing DIMM Configuration

- DIMM_A1, DIMM_B1, DIMM_C1, and DIMM_D1 must be identical in organization, size and speed.
- DIMM_A2, DIMM_B2, DIMM_C2, and DIMM_D2 must be identical in organization, size and speed.
- DIMM_A3, DIMM_B3, DIMM_C3, and DIMM_D3 must be identical in organization, size and speed.
- DIMM_A4, DIMM_B4, DIMM_C4, and DIMM_D4 must be identical in organization, size and speed.

- DIMMs across sets of four can be different in organization, size and speed. For example, the set of DIMMs that consists of A2, B2, C2, and D2 can be different from the set of DIMMs that consists of A1, B1, C1, and D1.

- Sparing should be enabled in BIOS setup.

- The BIOS configures rank sparing mode.

- The larger of the pairs {DIMM_A1, DIMM_B1, DIMM_ A3, DIMM_B3} and {DIMM_A2, DIMM_B2, DIMM_A4, DIMM_B4} will be selected as the spare pair unit.

3.7.3.4.2.2   *Dual-branch Mode Sparing*

Dual-branch mode sparing requires that all eight DIMM sockets be populated and must comply with the following population rules.

- DIMM_A1, DIMM_B1, DIMM_C1, and DIMM_D1 must be identical in organization, size and speed.

- DIMM_A2, DIMM_B2, DIMM_C2, and DIMM_D2 must be identical in organization, size and speed.

- DIMM_A3, DIMM_B3, DIMM_C3, and DIMM_D3 must be identical in organization, size and speed.

- DIMM_A4, DIMM_B4, DIMM_C4, and DIMM_D4 must be identical in organization, size and speed.

- DIMMs across sets of four need can be different in size and speed. For example, the set of DIMMs that consists of A2, B2, C2, and D2 can be different from the set of DIMMs that consists of A1, B1, C1, and D1.

- Sparing should be enabled in BIOS setup.

- The BIOS configures rank sparing mode.

- The larger of the pairs {DIMM_A1, DIMM_B1}, {DIMM_A2, DIMM_B2}, {DIMM_C1, DIMM_D1}, and {DIMM_C2, DIMM_D2} are selected as the spare pair units.

3.8   Enterprise South Bridge (ESB2-E)

The ESB2-E is a multi-function device that provides four functions: an I/O controller, a PCI-X* bridge, a GB Ethernet controller, and a baseboard management controller (BMC). Each function has its own set of configuration registers. Once configured, each appears to the system as a distinct hardware controller.

The ESB2-E provides the gateway to all PC-compatible I/O devices and features. The server system uses the following ESB2-E features:

- PCI-X bus interface

- Six-channel SATA interface with SATA busy LED control

- Dual GbE MAC

- Baseboard management controller (BMC)

- Single ATA interface, with Ultra DMA 100 capability

- Universal Serial Bus 2.0 (USB) interface

- Removable media drives

- LPC bus interface
- PC-compatible timer/counter and DMA controllers
- APIC and 8259 interrupt controller
- Power management
- System RTC
- General purpose I/O

For more detailed information, see the *Intel S5000 Server Board Family Datasheet* or the *Intel 631xESB/632xESB I/O Controller Hub Datasheet.*

3.8.1   PCI Sub-system

The primary I/O buses for the server system are PCI, PCI Express*, and PCI-X,* with six independent PCI bus segments. The PCI buses comply with the *PCI Local Bus Specification*, Revision 2.3. The table below lists the characteristics of the PCI bus segments. Details about each bus segment follow the table.

Table 9. PCI Bus Segment Characteristics

PCI Bus Segment	Voltage	Width	Speed	Type	PCI I/O Card Slots
PCI 32 ESB2-E	3.3 V	32 bit	33 MHz	PCI	None. Used internally for video controller
PXA ESB2-E	3.3 V / 5.0 V	64 bit	100 MHz	PCI-X*	PCI-X Slot 1
PXA ESB2-E	3.3 V / 5.0 V	64 bit	133 MHz	PCI-X*	PCI-X Slot 2
PE0 ESB2-E PCI Express* Port0	3.3 V	X4	10 Gb/S	PCI Express*	X4 PCI Express* Slot 4
PE1, PE2 ESB2-E PCI Express* Port1	3.3 V	X8	20 Gb/S	PCI Express	X8 PCI Express* Slot 3 (x8 is created by combining PE2 with PE1)
PE4, PE5 BNB PCI Express* Ports 4, 5	3.3 V	X8	20 Gb/S	PCI Express	X8 PCI Express* Slot 5
PE6, PE7 BNB PCI Express* Ports 6, 7	3.3 V	X8	20 Gb/S	PCI Express	X8 PCI Express* Slot 6

3.8.1.1   PCI32: 32-bit, 33-MHz PCI Sub-system

All 32-bit, 33-MHz PCI I/O is directed through the ESB2-E ICH6. The 32-bit, 33-MHz PCI segment created by the ESB2-E-ICH6 is known as the PCI32 segment. The PCI32 segment supports the embedded ATI* ES1000 2D graphics accelerator.

3.8.1.2   PXA: 64-bit, 133-MHz PCI Sub-system

One 64-bit PCI-X* bus segment is directed through the ESB2-E ICH6. This PCI-X segment, PXA, is routed to PCI-X slots 1 and 2. When a PCI-X adapter is installed in slot 2 and slot 1 is empty, PCI-X slot 2 supports a speed of 133 MHz. When both slot 1 and slot 2 are populated, slot 2 supports a speed of 100 MHz. PCI-X Slot 1 always supports a maximum speed of 100 MHz.

3.8.1.3   PE0: One x4 PCI Express* Bus Segment

One x4 PCI Express* bus segment, PE0, is directed through the ESB2-E to PCI Express* Slot 4.

3.8.1.4   PE1, PE2: Two x4 PCI Express* Bus Segment

Two x4 PCI Express* bus segments, PE1 and PE2, are directed through the ESB2-E to PCI Express* slot 3.

3.8.1.5   PE4, PE5: Two x4 PCI Express* Bus Segments

Two x4 PCI Express* bus segments, PE4 and PE5, are directed through the MCH to PCI Express* slot 5.

3.8.1.6   PE6, PE7: Two x4 PCI Express* Bus Segments

Two x4 PCI Express* bus segments, PE6 and PE7, are directed through the MCH to PCI Express* slot 6.

3.8.2   Serial ATA Support

The ESB2-E has an integrated Serial ATA (SATA) controller that supports independent DMA operation on six ports and supports data transfer rates of up to 3.0 Gb/s. The six SATA ports are numbered SATA-0 thru SATA-5. The SATA ports can be enabled, disabled, or configured in the BIOS Setup utility.

3.8.2.1   Intel® Embedded Server RAID Technology II Support

The onboard storage capability includes support for Intel® Embedded Server RAID Technology, which provides three standard software RAID levels: data stripping (RAID Level 0), data mirroring (RAID Level 1), and data stripping with mirroring (RAID Level 10). For higher performance, data stripping can be used to alleviate disk bottlenecks by taking advantage of the dual independent DMA engines that each SATA port offers.

Data mirroring provides data security. If a disk fails, a mirrored copy of the failed drive is brought on-line. There is no loss of PCI resources (request/grant pair) or add-in card slots.

If the optional Intel RAID Activation Key is installed, Intel® Embedded Server RAID Technology can provide fault-tolerant data stripping (software RAID Level 5), such that if a SATA hard drive fails, the lost data can be restored on a replacement drive from the other drives that make up the RAID 5 pack.

See Figure 2 for the location of Intel® RAID Activation Key connector location.

Intel® Embedded Server RAID Technology functionality requires the following items:

- Intel® ESB-2 I/O Controller Hub
- Intel® Embedded Server RAID Technology Option ROM
- Intel® Application Accelerator RAID Edition drivers, most recent revision
- At least two SATA hard disk drives (three or more drives are required for RAID 5)

Intel® Embedded Server RAID Technology is not available in the following configurations:

- The SATA controller is in compatible mode
- Intel® Embedded Server RAID Technology is disabled

3.8.2.2 Intel® Embedded Server RAID Technology Option ROM

The Intel® Embedded Server RAID Technology for SATA Option ROM provides a pre-OS user interface for the Intel® Embedded Server RAID Technology implementation and provides the ability for an Intel® Embedded Server RAID Technology volume to be used as a boot disk as well as to detect any faults in the Intel® Embedded Server RAID Technology volume(s) attached to the Intel® RAID controller.

3.8.3 Parallel ATA (PATA) Support

The integrated IDE controller of the ESB2-E ICH6 provides one IDE channel. It redefines signals on the IDE cable to allow both host and target throttling of data and transfer rates of up to 100 MB/s. For this server system, the IDE channel was designed to provide optical drive support to the platform. The BIOS initializes and supports ATAPI devices such as LS-120/240, CD-ROM, CD-RW and DVD-ROM. The IDE channel is accessed through a single standard 40-pin IDE connector (J2J2) that provides the I/O signals. The ATA channel can be configured and enabled or disabled by accessing the BIOS Setup utility during POST.

3.8.4   USB 2.0 Support

The USB controller functionality that is integrated into ESB2-E provides the server system with the interface for up to eight USB 2.0 ports. Four external connectors are located on the back of the server system. One internal 2x5 header (J3J1) is provided, capable of supporting two optional USB 2.0 ports. One USB port Type A connector (J3G1) is provided to support the installation of a USB device inside the server chassis. An additional USB port is dedicated to the Intel® Remote Management Module (Intel® RMM) connector.

3.9   Video Support

The server system provides an ATI* ES1000 PCI graphics accelerator, along with 16 MB of video DDR SDRAM and support circuitry for an embedded SVGA video sub-system. The ATI ES1000 chip contains an SVGA video controller, clock generator, 2D engine, and RAMDAC in a 359-pin BGA. One 4 M x 16 x 4-bank DDR SDRAM chip provides 16 MB of video memory.

The SVGA sub-system supports modes up to 1024 x 768 resolution in 8 / 16 / 32 bpp modes under 2D. It also supports both CRT and LCD monitors up to a 100 Hz vertical refresh rate.

A standard 15-pin VGA connector is on the back of the server system. The on-board video controller can be disabled through the BIOS Setup utility or when an add-in video card is installed. The system BIOS provides the option for dual-video operation when an add-in video card is installed.

3.9.1   Video Modes

The ATI* ES1000 chip supports all standard IBM* VGA modes. The following table shows the 2D modes supported for both CRT and LCD.

Table 10. Video Modes

2D Mode	Refresh Rate (Hz)	2D Video Mode Support		
		8 bpp	16 bpp	32 bpp
640 x 480	60, 72, 75, 85, 90, 100, 120, 160, 200	Supported	Supported	Supported
800 x 600	60, 70, 72, 75, 85, 90, 100, 120,160	Supported	Supported	Supported
1024 x 768	60, 70, 72, 75, 85, 90, 100	Supported	Supported	Supported
1152 x 864	43, 47, 60, 70, 75, 80, 85	Supported	Supported	Supported
1280 x 1024	60, 70, 74, 75	Supported	Supported	Supported
1600 x 1200	52	Supported	Supported	Supported

3.9.2   Video Memory Interface

The memory controller sub-system of the ES1000 arbitrates requests from the direct memory interface, the VGA graphics controller, the drawing co-processor, the display controller, the video scalar, and the hardware cursor. Requests are serviced in a manner that ensures display integrity and maximum CPU/co-processor drawing performance.

The server system supports a 16 MB (4 Meg x 16-bit x 4 banks) DDR SDRAM device for video memory.

3.9.3   Dual-video Mode Support

The BIOS supports single- and dual-video modes. Dual-video mode is enabled by default.

- In single mode (Dual Monitor Video = disabled), the on-board video controller is disabled when an add-in video card is detected.
- In dual mode (On-board Video = enabled, Dual Monitor Video = enabled), the on-board video controller is enabled and will be the primary video device. The external video card is allocated resources and is considered the secondary video device. The BIOS Setup utility provides options to configure the feature as follows.

On-board Video	**Enabled**	
	Disabled	
Dual Monitor Video	**Enabled**	Shaded if on-board video is set to "Disabled"
	Disabled	

3.10 Network Interface Controller (NIC)

Network interface support is provided from the built in Dual GbE MAC features of the ESB2 in conjunction with the Intel® 82563EB compact Physical Layer Transceiver (PHY). Together, they provide the server system with support for dual LAN ports designed for 10/100/1000 Mbps operation.

The 82563EB device is based upon proven PHY technology integrated into Intel's gigabit Ethernet controllers. The physical layer circuitry provides a standard IEEE 802.3 Ethernet interface for 1000BASE-T, 100BASE-TX, and 10BASE-T applications (802.3, 802.3u, and 802.3ab). The 82563EB device is capable of transmitting and receiving data at rates of 1000 Mbps, 100 Mbps, or 10 Mbps.

Each network interface controller (NIC) drives two LEDs on each network interface connector.

Table 11. NIC2 Status LED

LED Color	LED State	NIC State
Green / amber (Left – Speed LED)	Off	10 Mbps
	Green	100 Mbps
	Amber	1000 Mbps
Green (Right – Link / Actvity LED)	On	Active Connection
	Blinking	Transmit / Receive activity

3.10.1　　　Intel® I/O Acceleration Technolgy

Intel® I/O Acceleration Technology moves network data efficiently through Dual-Core Intel® Xeon® processor 5000, 5100 or 5300 sequence-based servers. Intel® I/OAT improves network application responsiveness by unleashing the power of these processors through efficient network data movement and reduced system overhead.

Intel multi-port network adapters with Intel® I/OAT provide high-performance I/O for server consolidation and virtualization via stateless network acceleration that seamlessly scales across multiple ports and virtual machines. Intel® I/OAT provides safe and flexible network acceleration through tight integration into popular operating systems and virtual machine monitors, avoiding the support risks of third-party network stacks and preserving existing network requirements such as teaming and failover.

3.10.2　　　MAC Address Definition

Each Intel® Server System SC5400RA has four MAC addresses assigned to it at the Intel factory. Each server board has a white MAC address label on it to display the MAC address in both bar code and alpha-numeric formats. The printed MAC address is assigned to NIC 1. NIC 2 is assigned the NIC 1 MAC address + 1.

Two additional MAC addresses are assigned to the baseboard management controller (BMC) embedded in the ESB-2. These MAC addresses are used by the BMC's embedded network stack to enable IPMI remote management over LAN. BMC LAN Channel 1 is assigned the NIC1 MAC address + 2, and BMC LAN Channel 2 is assigned the NIC1 MAC address + 3.

3.11 Super I/O

Legacy I/O support is provided by a National Semiconductor* PC87427 Super I/O device. This chip contains all of the necessary circuitry to support the following functions:
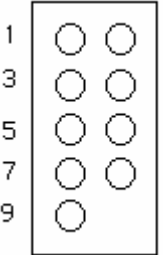
- GPIOs
- Two serial ports
- Keyboard and mouse support
- Wake up control
- System health support

3.11.1   Serial Ports

The system has two serial ports: an external DB9 serial port and an internal DH10 serial header. The rear DB9 serial A port is a fully-functional port that can support any standard serial device.

Serial B is an optional port that is accessed through a 9-pin internal DH-10 header. A standard DH10 to DB9 cable can be used to direct serial B to the rear of a chassis. The serial B interface follows the standard RS232 pin-out as defined in the following table.

Table 12. Serial B Header Pin-out

Pin	Signal Name	Serial Port B Header Pin-out
1	DCD	
2	DSR	
3	RX	
4	RTS	
5	TX	
6	CTS	
7	DTR	
8	RI	
9	GND	

3.11.2   Floppy Disk Controller

The server system does not support a floppy disk controller interface, but the system BIOS recognizes USB floppy devices.

3.11.3   Keyboard and Mouse Support

Dual-stacked PS/2* ports are on the back of the server system for keyboard and mouse support. Either port can support a mouse or keyboard. Neither port supports hot plugging.

3.11.4   Wake-up Control

Super I/O functionality allows events to power on and power off the system.

3.11.5   System Health Support

The super I/O provides an interface via GPIOs for BIOS and system management firmware to activate the diagnostic LEDs, the FRU fault indicator LEDs for processors, FBDIMMS, fans and the system status LED. See section 7 for the location of the LEDs.

The super I/O provides PMW fan control to the system fans, monitors tach and presence signals for the system fans and monitors server board and front panel temperature.

4. Platform Management

The platform management sub-system is based on the integrated baseboard management controller features of the ESB2-E. The on-board platform management sub-system consists of communication buses, sensors, system BIOS, and server management firmware. The following diagram provides an overview of the Server Management Bus (SMBUS) architecture used on this server system.

See Appendix B for on-board sensor data.

For more detailed platform management information, see the *Intel® S5000 Server Board Family Datasheet.*
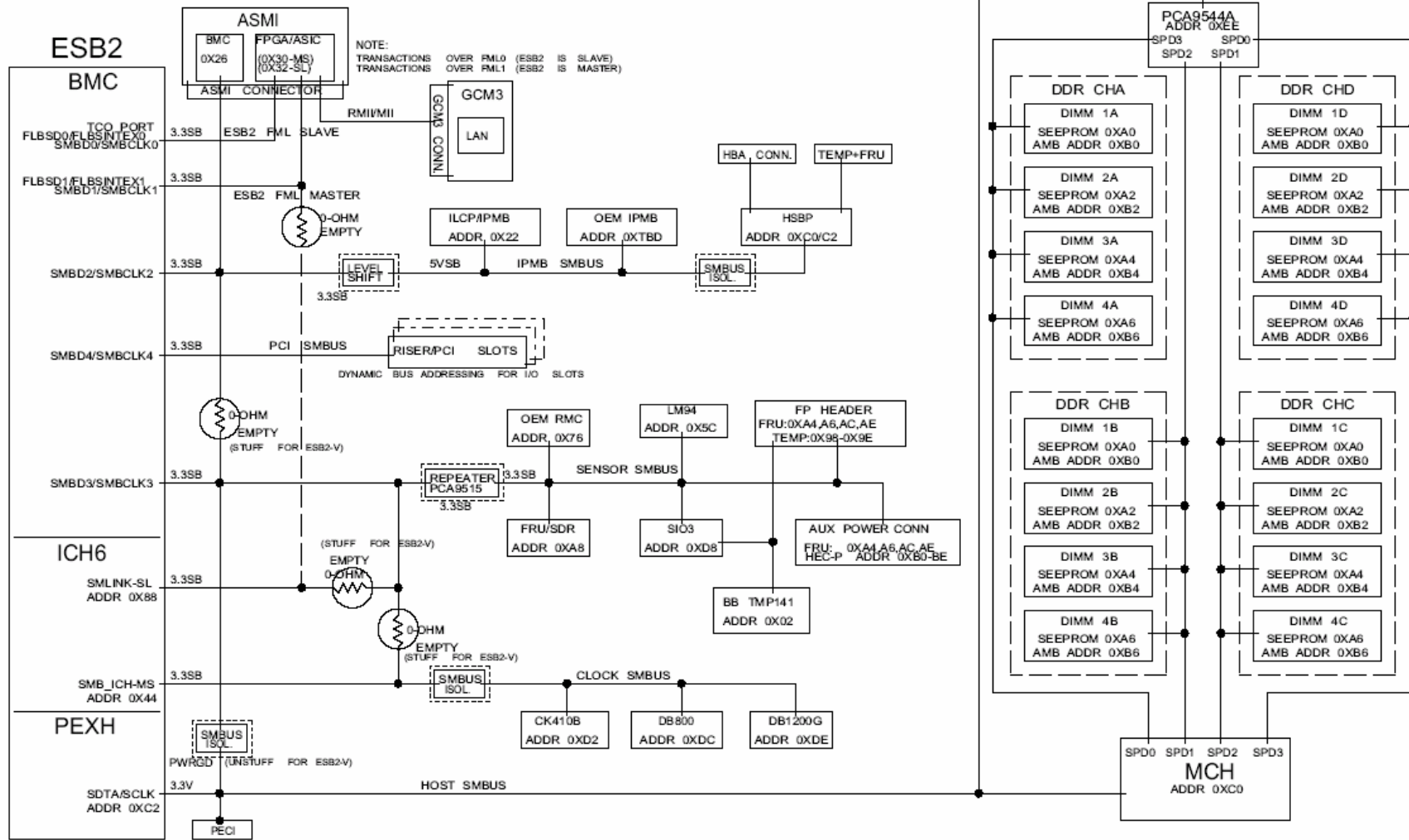
Figure 20. SMBUS Block Diagram

5.   Connector / Header Locations and Pin-outs

5.1   Board Connectors

Table 13. Board Connector Matrix

Connector	Quantity	Siklscreen Designator	Connector Type	Pin Count
Power supply	4	J9B5	Main power	24
		J3J2	CPU power	8
		J9D1	P/S aux / IPMB	5
		J5A2	P12V4 power	4
CPU	2	J8G1, J5G1	CPU sockets	771
DIMM Riser	2	J8B1, J9B6	Card edge	280
PCI-X	2	J1B2, J2B1	Card edge	
PCI Express* x8	2	J2B2, J3B1	Card edge	
PCI Express* x16	2	J4B2, J4B1	Card edge	
Intel® RMM	1	J5B1	Mezzanine	120
RMM NIC	1	J3B2	Mezzanine	40
RAID Key	1	J1E1	Key holder	3
IDE	1	J2J2	Shrouded header	40
System fans	4	J3H1, J3H2, J3H3, J3H4	Header	6
System fans	2	J9B3, J9B4	Header	4
CPU fans	2	J9J1, J5J1	Header	4
Battery	1	XBT4D1	Battery holder	3
Keyboard / mouse	1	J9A1	PS2, stacked	12
Stacked RJ45 / 2xUSB	2	JA6A1, JA6A2	External LAN built-in magnetic and dual USB	22
Stacked video / verial port A	1	J7A1	External DSub / DB9	24
Serial port B	1	J1B1	Header	10
Front panel	1	J1E4	Header	24
Internal USB	1	J3J1	Header	10
Internal USB	1	J3G1	Type A connector	4
Chassis Intrusion	1	J1A1	Header	2
Serial ATA / SAS	6	J1G1, J1F2, J1H1, J1G2, J1J1, J1H2	Header	7
HSBP / SGPIO	3	J1J2, J1J7, J2H1	Header	4
LCP/AUX IPMB	1	J2J1	Header	4
IPMB	1	J4J1	Header	3
HDD Activity	1	J2J3	Header	2
Configuration jumpers	4	J1D2 (Password Clear), J1D1 (CMOS Clear), J1C3 (BIOS Bank Select), J1E3 (BMC Force Update)	Jumper	3

5.2   Power Connectors

The main power supply connection uses an SSI-compliant 2x12 pin connector (J9B5). There are three additional power related connectors:

- One SSI-compliant 2x4 pin power connector (J3J2) provides 12V power to the CPU voltage regulators.
- One SSI-compliant 1x5 pin connector (J9D1) provides I^{2}C monitoring of the power supply along with 3.3V sense.
- One SSI-compliant 2x2 pin connector (J5A2) provides additional 12V power to the server board.

Table 14. Power Connector Pin-out (J9B5)

Pin	Signal	Color	Pin	Signal	Color
1	+3.3 Vdc	Orange	13	+3.3 Vdc	Orange
2	+3.3 Vdc	Orange	14	-12 Vdc	Blue
3	GND	Black	15	GND	Black
4	+5 Vdc	Red	16	PS_ON#	Green
5	GND	Black	17	GND	Black
6	+5 Vdc	Red	18	GND	Black
7	GND	Black	19	GND	Black
8	PWR_OK	Gray	20	RSVD_(-5 V)	White
9	5 VSB	Purple	21	+5 Vdc	Red
10	+12 Vdc	Yellow	22	+5 Vdc	Red
11	+12 Vdc	Yellow	23	+5 Vdc	Red
12	+3.3 Vdc	Orange	24	GND	Black

Table 15. 12 V Power Connector Pin-out (J3J2)

Pin	Signal	Color
1	GND	Black
2	GND	Black
3	GND	Black
4	GND	Black
5	+12 Vdc	Yellow / black
6	+12 Vdc	Yellow / black
7	+12 Vdc	Yellow / black
8	+12 Vdc	Yellow / black

Table 16. Power Supply Signal Connector Pin-out (J9D1)

Pin	Signal	Color
1	SMB_CLK_ESB_FP_PWR_R	Orange
2	SMB_DAT_ESB_FP_PWR_R	Black
3	SMB_ALRT_3_ESB_R	Red
4	3.3 V SENSE-	Yellow
5	3.3 V SENSE+	Green

Table 17. P12V4 Power Connector Pin-out (J5A2)

Pin	Signal	Color
1	GND	Black
2	GND	Black
3	+12 Vdc	Yellow / black
4	+12 Vdc	Yellow / black

5.3   System Management Headers

5.3.1   Intel® Remote Management Module (Intel® RMM) Connector

A 120-pin Intel® RMM connector (J5B1) is included supports the optional Intel® Remote Management Module. There is no support for third-party ASMI cards.

Note: This connector is not compatible with the Intel® Server Management Module Professional Edition (Product Code AXXIMMPRO) or the Intel® Server Management Module Advanced Edition (Product Code AXXIMMADV).

Table 18. Intel® RMM Connector Pin-out (J5B1)

Pin	Signal Name	Pin	Signal Name
1	Reserved - NC	2	GND
3	ESB_PLT_RST_G1_N	4	Reserved - NC
5	GND	6	Reserved - NC
7	Reserved - NC	8	GND
9	Reserved - NC	10	GND
11	GND	12	Reserved - NC
13	GND	14	IRQ_SERIAL_R
15	USB_ESB_P7P	16	GND
17	USB_ESB_P7N	18	GND
19	GND	20	Reserved - NC
21	P3V3	22	Reserved - NC
23	LPC_LAD<0>	24	GND
25	LPC_LAD<1>	26	LPC_FRAME_N
27	P3V3	28	LPC_LAD<2>
29	LPC_LCLK	30	LPC_LAD<3>
31	P3V3	32	P3V3
33	SMB_1_3V3SB_MS_DAT	34	SMB_IPMB_3V3SB_DAT
35	SMB_1_3V3SB_SL_DAT	36	SMB_IPMB_3V3SB_CLK
37	SMB_1_3V3SB_MS_CLK	38	SMB_0_3V3SB_MS_CLK
39	SMB_1_3V3SB_INT	40	SMB_0_3V3SB_INT
41	P3V3_AUX	42	SMB_0_3V3SB_MS_DAT
43	SPB_IMM_DSR_N	44	SMB_0_3V3SB_SL_DAT
45	SPB_IMM_RTS_N	46	P3V3_AUX
47	SPB_IMM_CTS_N	48	FM_IMM_PRESENT_N
49	SPB_IMM_DCD_N	50	SPB_IMM_DTR_N
51	SPB_RI_N	52	SPB_IMM_SIN
53	SPB_IMM_SOUT	54	P3V3_AUX
55	P3V3_AUX	56	V_LCDDATA7
57	V_LCDCNTL3	56	V_LCDDATA6
59	P3V3_AUX	60	V_LCDDATA5
61	Reserved - NC	62	V_LCDDATA4

Pin	Signal Name	Pin	Signal Name
63	Reserved - NC	64	V_LCDDATA3
65	GND	66	V_LCDCNTL1
67	V_LCDCNTL0	68	GND
69	Reserved - NC	70	V_LCDDATA15
71	GND	72	V_LCDDATA714
73	V_LCDDATA23	74	V_LCDDATA13
75	V_LCDDATA22	76	V_LCDDATA12
77	V_LCDDATA21	78	V_LCDDATA11
79	V_LCDDATA20	80	GND
81	V_LCDDATA19	82	V_LCDCNTL2
83	GND	84	V_DVO_DDC_SDA
85	FM_MAN_LAN_TYPE1	86	V_DVO_DDC_SCL
87	FM_MAN_LAN_TYPE2	88	RST_PS_PWRGD
89	Reserved - NC	90	Reserved - NC
91	Reserved - NC	92	Reserved - NC
93	MII_MDC_RMII_SPARE	94	Reserved - NC
95	MII_COL_RMIIB_RXER	96	GND
97	GND	98	MII_CRS_RMIIB_CRS
99	MII_TXER_RMIIB_TXEN	100	MII_TXCLK_RMIIB_RXCLK
101	MII_MDIO_RMIIB_PRESENT	102	GND
103	GND	104	MII_TXD3_RMIIB_TXD1
105	MII_RXD3_RMIIB_RXD1	106	MII_TXD2_RMIIB_TXD0
107	MII_RXD2_RMIIB_RXD0	108	GND
109	GND	110	MII_TXD1_RMIIA_TXD1
111	MII_RXD1_RMIIA_RXD1	112	MII_TXD0_RMIIA_TXD0
113	MII_RXD0_RMIIA_RXD0	114	GND
115	GND	116	MII_TXEN_RMIIA_TXEN
117	MII_RXCLK	118	MII_RXER_RMIIA_TXER
119	MII_RXDV_RMIIA_CRS	120	GND

5.3.2   LCP / AUX IPMB Header

Table 19. LPC / AUX IPMB Header Pin-out (J2J1)

Pin	Signal Name	Description
1	SMB_IPMB_5VSB_DAT	BMC IMB 5V standby data line
2	GND	Ground
3	SMB_IPMB_5VSB_CLK	BMC IMB 5V standby clock line
4	P5V_STBY	+5 V standby power

5.3.3 IPMB Header

Table 20. IPMB Header Pin-out (J4J1)

Pin	Signal Name	Description
1	SMB_IPMB_5VSB_DAT	BMC IMB 5V Standby Data Line
2	GND	Ground
3	SMB_IPMB_5VSB_CLK	BMC IMB 5V Standby Clock Line

5.3.4 HSBP Header

Table 21. HSBP Header Pin-out (J1J7, J1J2)

Pin	Signal Name	Description
1	SMB_IPMB_5V_DAT	BMC IMB 5V Data Line
2	GND	Ground
3	SMB_IPMB_5V_CLK	BMC IMB 5V Clock Line
4	GND – HSBP_A P5V – HSBP_B	Ground for HSBP A +5V for HSBP B

5.3.5 SGPIO Header

Table 22. SGPIO Header Pin-out (J2H1)

Pin	Signal Name	Description
1	SGPIO_CLOCK	SGPIO Clock Signal
2	SGPIO_LOAD	SGPIO Load Signal
3	SGPIO_DATAOUT	SGPIO Data Out
4	SGPIO_DATAIN	SGPIO Data In

5.3.6 HDD Activity LED Header

Table 23. HDD Activity LED Header Pin-out (J2J3)

Pin	Signal Name	Description
1	LED_SCSI_CONN_N	HDD Activity LED Input
2	GND	Ground

5.4 Front Panel Connector

Table 24. Front Panel SSI Standard 24-pin Connector Pin-out (J1E4)

Pin	Signal Name	Pin	Signal Name
1	P3V3_STBY	2	P3V3_STBY
3	Key	4	P5V_STBY
5	FP_PWR_LED_N	6	FP_ID_LED_BUF_N
7	P3V3	8	FP_LED_STATUS_GREEN_N
9	LED_HDD_ACTIVITY_N	10	FP_LED_STATUS_A MBER_N
11	FP_PWR_BTN_N	12	NIC1_ACT_LED_N
13	GND	14	NIC1_LINK_LED_N
15	BMC_RST_BTN_N	16	SMB_SENSOR_3V3STB_DATA
17	GND	18	SMB_SENSOR_3V3STB_CLK
19	FP_ID_BTN_N	20	FP_CHASSIS_INTRU
21	FM_SIO_TEMP_SENSOR	22	NIC2_ACT_LED_N
23	FP_NMI_BTN_N	24	NIC2_LINK_LED_N

5.5 I/O Connectors

5.5.1 VGA Connector

Table 25. VGA Connector Pin-out (J7A1)

Pin	Signal Name	Description
1	V_IO_R_CONN	Red (analog color signal R)
2	V_IO_G_CONN	Green (analog color signal G)
3	V_IO_B_CONN	Blue (analog color signal B)
4	TP_VID_CONN_B4	No connection
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	TP_VID_CONN_B9	No connection
10	GND	Ground
11	TP_VID_CONN_B11	No connection
12	V_IO_DDCDAT	DDCDAT
13	V_IO_HSYNC_CONN	HSYNC (horizontal sync)
14	V_IO_VSYNC_CONN	VSYNC (vertical sync)
15	V_IO_DDCCLK	DDCCLK

5.5.2 NIC Connectors

The server system provides two stacked RJ45 / 2xUSB connectors side-by-side on the back edge of the server board (JA6A1, JA6A2). The pin-out for NIC connectors are identical.

Table 26. RJ-45 10/100/1000 NIC Connector Pin-out (JA6A1, JA6A2)

Pin	Signal Name
1	GND
2	P1V8_NIC
3	NIC_A_MDI3P
4	NIC_A_MDI3N
5	NIC_A_MDI2P
6	NIC_A_MDI2N
7	NIC_A_MDI1P
8	NIC_A_MDI1N
9	NIC_A_MDI0P
10	NIC_A_MDI0N
11 (D1)	NIC_LINKA_1000_N (LED
12 (D2)	NIC_LINKA_100_N (LED)
13 (D3)	NIC_ACT_LED_N
14	NIC_LINK_LED_N
15	GND
16	GND

5.5.3 Legacy IDE ATA100 Connector

Table 27. IDE 40-pin Connector Pin-out (J2J2)

Pin	Signal Name	Pin	Signal Name
1	ESB_PLT_RST_IDE_N	2	GND
3	RIDE_DD_7	4	RIDE_DD_8
5	RIDE_DD_6	6	RIDE_DD_9
7	RIDE_DD_5	8	RIDE_DD_10
9	RIDE_DD_4	10	RIDE_DD_11
11	RIDE_DD_3	12	RIDE_DD_12
13	RIDE_DD_2	14	RIDE_DD_13
15	RIDE_DD_1	16	RIDE_DD_14
17	RIDE_DD_0	18	RIDE_DD_15
19	GND	20	KEY
21	RIDE_DDREQ	22	GND
23	RIDE_DIOW_N	24	GND
25	RIDE_DIOR_N	26	GND

Pin	Signal Name	Pin	Signal Name
27	RIDE_PIORDY	28	GND
29	RIDE_DDACK_N	30	GND
31	IRQ_IDE	32	TP_PIDE_32
33	RIDE_DA1	34	IDE_PRI_CBLSNS
35	RIDE_DA0	36	RIDE_DA2
37	RIDE_DCS1_N	38	RIDE_DCS3_N
39	LED_IDE_N	40	GND

5.5.4 Intel® Remote Management Module NIC Connector

The server system provides an internal 40-pin connector (J3B2) to accommodate a proprietary form factor Intel® Remote Management Module NIC module.

Table 28. 40-pin RMM NIC Module Connector Pin-out (J3B2)

Pin	Signal Name	Pin	Signal Name
1	FM_MAN_LAN_TYPE2	2	FM_MAN_LAN_TYPE1
3	P3V3_AUX	4	MII_MDIO_RMIIB_PRESENT
5	P3V3_AUX	6	MII_MDC_RMII_SPARE
7	GND	8	MII_RXD3_RMIIB_RXD1
9	GND	10	MII_RXD2_RMIIB_RXD0
11	GND	12	MII_RXD1_RMIIA_RXD1
13	GND	14	MII_RXD0_RMIIA_RXD0
15	GND	16	MII_RXDV_RMIIA_CRS
17	GND	18	MII_RXCLK
19	GND	20	MII_RXER_RMIIA_RXER
21	GND	22	KEY
23	GND	24	MII_TXCLK_RMIIB_RXCLK
25	GND	26	MII_TXEN_RMIIA_TXEN
27	GND	28	MII_TXD0_RMIIA_TXD0
29	GND	30	MII_TXD1_RMIIA_TXD1
31	GND	32	MII_TXD2_RMIIB_TXD0
33	GND	34	MII_TXD3_RMIIB_TXD1
35	P3V3_AUX	36	MII_COL_RMIIB_RXER
37	P3V3_AUX	38	MII_CRS_RMIIB_CRS
39	P3V3_AUX	40	MII_TXER_RMIIB_TXEN

5.5.5   SATA Connectors

The server system provides up to six SATA connectors:

- SATA-0 (J1J1)
- SATA-1 (J1H2)
- SATA-2 (J1H1)
- SATA-3 (J1G2)
- SATA-4 (J1G1)
- SATA-5 (J1F2)

The pin configuration for each connector is identical.

Table 29. SATA Connector Pin-out (J1J1, J1H2, J1H1, J1G2, J1G1, J1F2)

Pin	Signal Name	Description
1	GND	Ground
2	SATA_TX_P_C	Positive side of transmit differential pair
3	SATA_TX_N_C	Negative side of transmit differential pair
4	GND	Ground
5	SATA_RX_N_C	Negative side of receive differential pair
6	SATA_RX_P_C	Positive side of receive differential pair
7	GND	Ground

5.5.6   Serial Port Connectors

Table 30. External DB9 Serial A Port Pin-out (J7A1)

Pin	Signal Name	Description
1	SPA_DCD	DCD (carrier detect)
2	SPA_SIN_L	RXD (receive data)
3	SPA_SOUT_N	TXD (Transmit data)
4	SPA_DTR	DTR (Data terminal ready)
5	GND	Ground
6	SPA_DSR	DSR (data set ready)
7	SPA_RTS	RTS (request to send)
8	SPA_CTS	CTS (clear to send)
9	SPA_RI	RI (Ring Indicate)

Table 31. Internal 9-pin Serial B Header Pin-out (J1B1)

Pin	Signal Name	Description
1	SPB_DCD	DCD (carrier detect)
2	SPB_DSR	DSR (data set ready)
3	SPB_SIN_L	RXD (receive data)
4	SPB_RTS	RTS (request to send)
5	SPB_SOUT_N	TXD (Transmit data)
6	SPB_CTS	CTS (clear to send)
7	SPB_DTR	DTR (Data terminal ready)
8	SPB_RI	RI (Ring indicate)
9	SPB_EN_N	Enable

5.5.7   Keyboard and Mouse Connector

Two stacked PS/2* ports (J9A1) support a keyboard and a mouse. Either PS/2 port can support a mouse or keyboard.

Table 32. Stacked PS/2 Keyboard and Mouse Port Pin-out (J9A1)

Pin	Signal Name	Description
1	KB_DATA_F	Keyboard data
2	TP_PS2_2	Test point – keyboard
3	GND	Ground
4	P5V_KB_F	Keyboard / mouse power
5	KB_CLK_F	Keyboard clock
6	TP_PS2_6	Test point – keyboard / mouse
7	MS_DAT_F	Mouse data
8	TP_PS2_8	Test point – keyboard / mouse
9	GND	Ground
10	P5V_KB_F	Keyboard / mouse power
11	MS_CLK_F	Mouse clock
12	TP_PS2_12	Test point – keyboard / mouse
13	GND	Ground
14	GND	Ground
15	GND	Ground
16	GND	Ground
17	GND	Ground

5.5.8   USB Connector

Table 33. External USB Connector Pin-out (JA6A1, JA6A2)

Pin	Signal Name	Description
1	USB_OC	USB_PWR
2	USB_PN	DATAL0 (Differential data line paired with DATAH0)
3	USB_PP	DATAH0 (Differential data line paired with DATAL0)
4	GND	Ground

One 2x5 connector at location J3J1 on the server board provides an option to support an additional two USB ports. The pin-out of the connector is detailed in the following table.

Table 34. Internal USB Connector Pin-out (J3J1)

Pin	Signal Name	Description
1	USB2_VBUS5	USB power (port 5)
2	USB2_VBUS4	USB power (port 4)
3	USB_ESB_P5N_CONN	USB port 5 negative signal
4	USB_ESB_P4N_CONN	USB port 4 negative signal
5	USB_ESB_P5P_CONN	USB port 5 positive signal
6	USB_ESB_P4P_CONN	USB port 4 positive signal
7	Ground	Ground
8	Ground	Ground
9	Key	No pin
10	TP_USB_ESB_NC	Test point

5.6   Fan Headers

Four SSI-compliant 4-pin and four SSI-compliant 6-pin fan headers are provide as CPU and I/O cooling fans. 3-pin fans are supported on all fan headers. 6-pin fans are supported on header J3H4, J3H3, J3H2, and J3H1. 4-pin fans are supported on header J9J1, J5J1, J3H4, J3H3, J9B4, and J9B3.

4-pin fans are not supported on header J3H2 and J3H1 because these headers are tied to the CPU1 PWM. These fan headers should not be used for CPU cooling fans. The pin configuration for each of the 4-pin and 6-pin fan headers is identical and is defined in the following tables.

- Four 6-pin fan headers are designated as hot-swap system fans:
  - Hot-swap system fan 1 (J3H4)
  - Hot-swap system fan 2 (J3H3)
  - Hot-swap system fan 3 (J3H2)
  - Hot-swap system fan 4 (J3H1)
- Two 4-pin fan headers are designated as rear system fans:
  - System fan 5 (J9B4)
  - System fan 6 (J9B3)

Table 35. SSI 4-pin Fan Header Pin-out (J9J1, J5J1, J9B3, J9B4)

Pin	Signal Name	Type	Description
1	Ground	GND	Ground is the power supply ground
2	12V	Power	Power supply 12 V
3	Fan Tach	In	FAN_TACH signal is connected to the BMC to monitor the fan speed
4	Fan PWM	Out	FAN_PWM signal to control fan speed

Table 36. SSI 6-pin Fan Header Pin-out (J3H1, J3H2, J3H3, J3H4)

Pin	Signal Name	Type	Description
1	Ground	GND	Ground is the power supply ground
2	12V	Power	Power supply 12 V
3	Fan Tach	In	FAN_TACH signal is connected to the BMC to monitor the fan speed
4	Fan PWM	Out	FAN_PWM signal to control fan speed
5	Fan Presence	In	Indicates the fan is present
6	Fan Fault LED	Out	Lights the fan fault LED

Note: *Intel Corporation server boards support peripheral components and contain a number of high-density VLSI and power delivery components that need adequate airflow to cool. Intel's own chassis are designed and tested to meet the intended thermal requirements of these components when the fully integrated system is used together. It is the responsibility of the system integrator that chooses not to use Intel developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of air flow required for their specific application and environmental conditions. Intel Corporation can not be held responsible if components fail or the server board does not operate correctly when used outside any of their published operating or non-operating limits.*

6.   Jumper Blocks

3-pin jumper blocks can be used to recover the password or CMOS, force a BMC update or select the BIOS bank. Pin 1 on each jumper block is noted on the silkscreen by ▼.
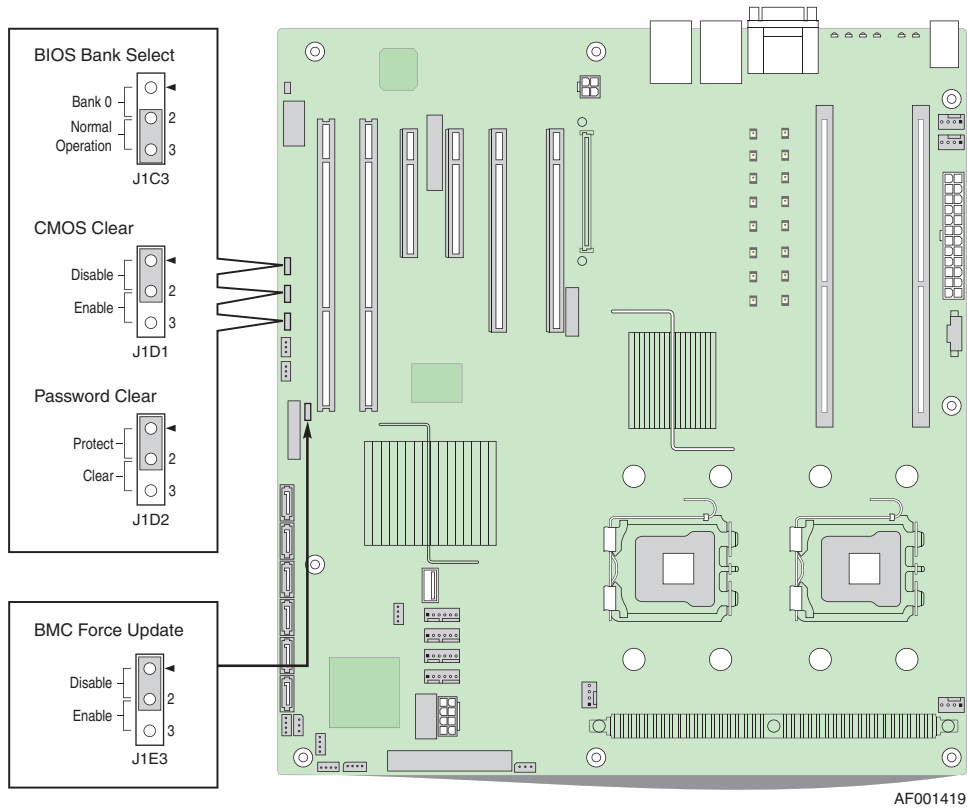
Figure 21. Jumper Blocks (J1C3, J1D1, J1D2, J1E32)

Table 37. Server Board Jumpers (J1C3, J1D1, J1D2, J1E3)

Jumper Name	Pins	System Results
J1C3: BIOS Bank Select	1-2	If these pins are jumper the system boots from an alternate BIOS image.
	2-3	System is configured for normal operation. **(Default)**
J1D1: CMOS Clear	1-2	These pins should have a jumper in place for normal system operation. **(Default)**
	2-3	If these pins are jumpered, the CMOS settings are cleared immediately. These pins should not be jumpered for normal operation
J1D2: Password Clear	1-2	These pins should have a jumper in place for normal system operation. **(Default)**
	2-3	If these pins are jumpered, administrator and user passwords are cleared immediately. These pins should not be jumpered for normal operation.
J1E3: BMC Force Update	1-2	BMC Firmware Force Update Mode – Disabled **(Default)**
	2-3	BMC Firmware Force Update Mode – Enabled

6.1   CMOS Clear and Password Reset Usage Procedure

The CMOS Clear (J1D1) and Password Reset (J1D2) recovery features can be achieved with minimal system down time. The procedure for these two features has changed from previous generation Intel server boards. The new usage model is as follows.

1. Power down the server, but do not unplug the power cord.

2. Open the server chassis.

3. Move jumper from the default operating position, covering pins 1 and 2, to the reset / clear position, covering pins 2 and 3.

4. Wait 5 seconds.

5. Move the jumper back to default position, covering pins 1 and 2.

6. Close the server chassis.

7. Power up the server.

The password and/or CMOS is now cleared and can be reset by going into BIOS setup.

Note: Removing AC Power before performing the CMOS Clear operation will cause the system to automatically power up and immediately power down, after the procedure is followed and AC power is re-applied. If this happens, remove the AC power cord again, wait 30 seconds, and re-install the AC power cord. Power up system and proceed to the <F2> BIOS Setup Utility to reset the desired settings.

6.2   BMC Force Update Procedure

When performing a standard BMC firmware update procedure, the update utility places the BMC into an update mode, allowing the firmware to load safely onto the flash device. If the BMC firmware update process fails because the BMC is not in the proper update state, the server board provides a BMC Force Update jumper (J1E3) that forces the BMC into the correct state. The procedure described below should be followed if the standard BMC firmware update process fails.

1. Power down and remove the AC power cord.

2. Open the server chassis.

3. Move jumper from the default operating position, covering pins1 and 2, to the enabled position, covering pins 2 and 3.

4. Close the server chassis.

5. Reconnect the AC cord and power up the server.

6. Perform the BMC firmware update procedure as documented in the README.TXT file that is included in the given BMC firmware update package. After a successful completion of the firmware update process, the firmware update utility may generate an error stating that the BMC is still in update mode.

7. Power down and remove the AC power cord.

8. Open the server chassis.

9. Move jumper from the enabled position, covering pins 2 and 3 to the disabled position, covering pins 1 and 2.

10. Close the server chassis.

11. Reconnect the AC cord and power up the server.

Note: *Normal BMC functionality is disabled with the Force BMC Update jumper is set to the enabled position. The server should never be run with the BMC Force Update jumper set in this position. This jumper setting should only be used when the standard firmware update process fails. This jumper should remain in the default / disabled position when the server is running normally.*

6.3   BIOS Select Jumper

The jumper block at J1C3 is used to determine which BIOS image the system will boot. This jumper should only be moved if you want to force the BIOS to boot to the secondary bank, which may hold a different version of BIOS.

The rolling BIOS feature of the server board will automatically alternate the boot BIOS to the secondary bank if the BIOS image in the primary bank is corrupted and cannot boot.

7.   Intel® Light-Guided Diagnostics

The server board has on-board diagnostic LEDs to assist in troubleshooting board-level issues. For a more information about what drives the diagnostic LED operation, see the *Intel® S5000 Server Board Family Datasheet.*

7.1   5 Volt Standby LED

Several server management features require that a 5 volt stand-by voltage be supplied from the power supply. Features and components that require this voltage when the system is off include the BMC within the ESB2-E, onboard NICs, and optional RMM connector with Intel RMM installed.

The LED is at the right of the CMOS battery in the center of the server board. The LED is labeled "5VSB_LED" and is illuminated when AC power is applied to the platform and 5 volt standby voltage is supplied by the power supply.

AF001570
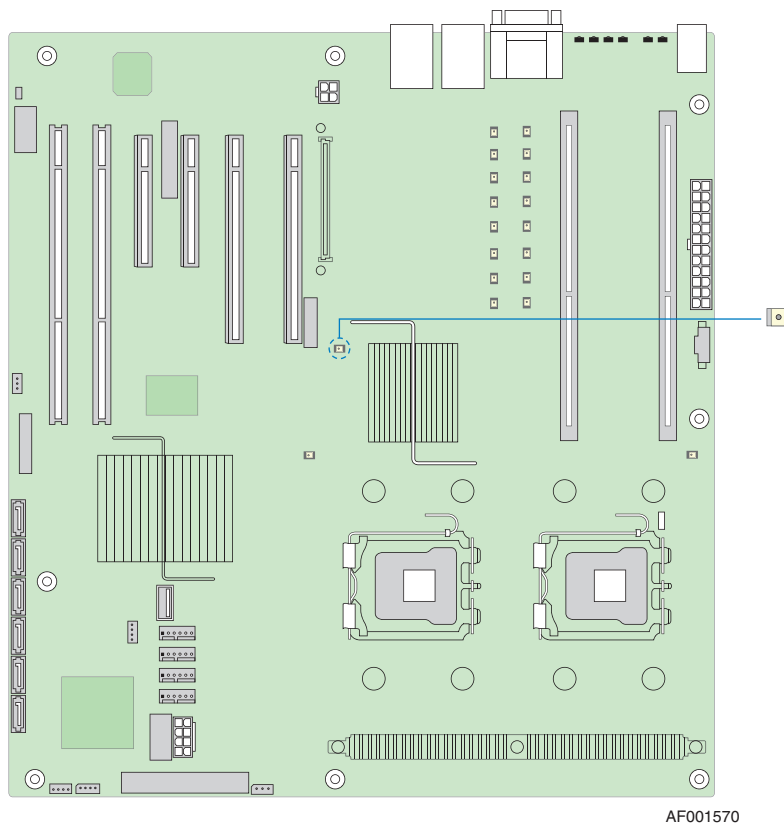
Figure 22. 5 Volt Standby Status LED Location

7.2   Fan Fault LEDs

Fan fault LEDs are present for the two CPU fans and the two rear system fans. The two CPU fan fault LEDs are located next to each CPU fan header. The two rear system fan fault LEDs are located next to each rear system fan header and are shown in the following figure.
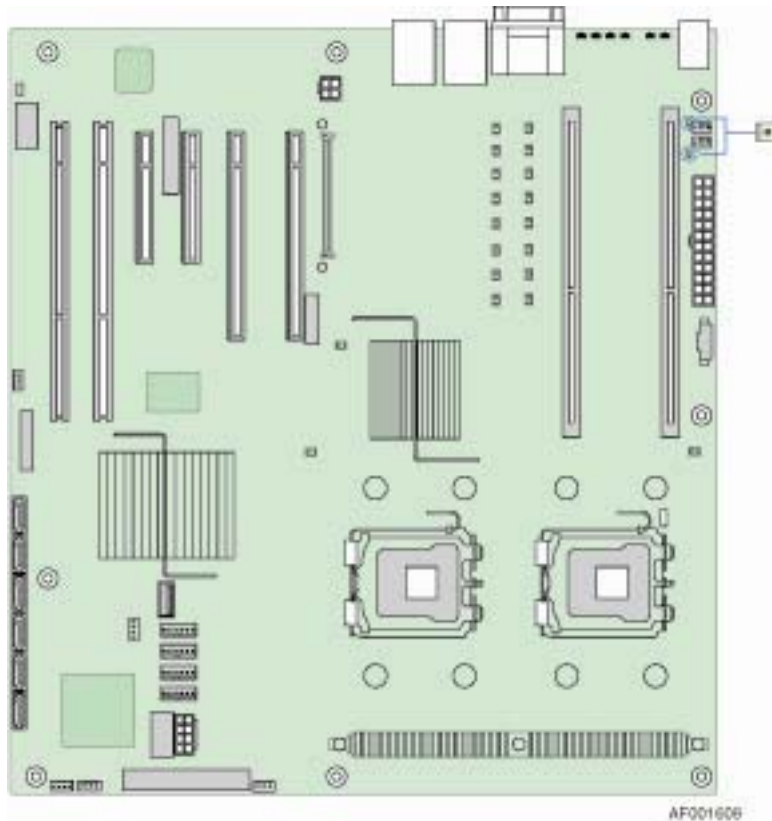
Figure 23. Fan Fault LED Locations

7.3   System ID LED and System Status LED

LEDs are available for both system ID and system status. These LEDs are in the rear I/O area between the PS/2* mouse / keyboard stacked connectors and the video / serial stacked connectors.

AF001571
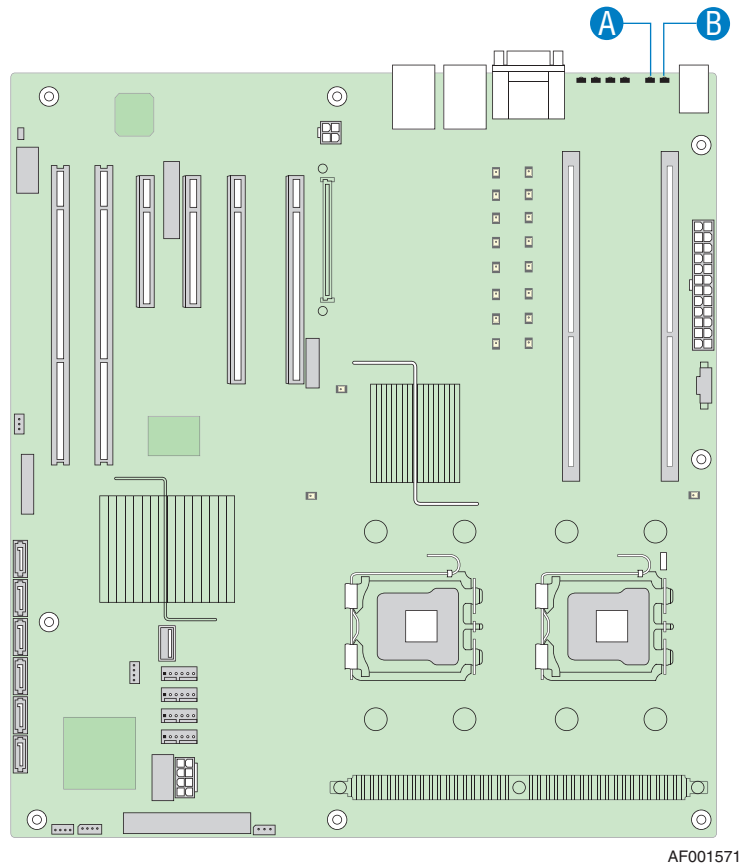
A. System ID LED
B. System Status LED

Figure 24. System ID LED and System Status LED Locations

The blue system ID LED can be illuminated in two ways.

- By pressing the system ID button on front panel. The ID LED displays in blue until the button is pressed again.
- By issuing the appropriate hex IPMI Chassis Identify value, the ID LED either blinks blue for 15 seconds and turns off or blinks indefinitely until the appropriate hex IPMI Chassis Identify value is issued to turn it off.

Table 38. System Status LED Operation

Color	State	Criticality	Description
Off	N/A	Not ready	AC power off
Green / Amber	Alternating Blink	Not ready	Pre DC Power On – 20-30 second BMC Initialization when AC is applied to the server. Control Panel buttons are disabled until BMC initialization is complete.
Green	Solid on	System OK	System booted and ready.
Green	Blink	Degraded	System degraded ▪ Unable to use all of the installed memory (more than one DIMM installed). ▪ Correctable errors over a threshold of 10 and migrating to a spare DIMM (memory sparing). This indicates that the user no longer has spared DIMMs indicating a redundancy lost condition. Corresponding DIMM LED should light up. ▪ In mirrored configuration, when memory mirroring takes place and system loses memory redundancy. ▪ Redundancy loss such as power-supply or fan. This does not apply to non-redundant sub-systems. ▪ PCI-e link errors ▪ CPU failure / disabled – if there are two processors and one of them fails ▪ Fan alarm – Fan failure. Number of operational fans should be more than minimum number needed to cool the system ▪ Non-critical threshold crossed – Temperature and voltage
Amber	Blink	Non-critical	Non-fatal alarm – system is likely to fail ▪ Critical voltage threshold crossed ▪ VRD hot asserted ▪ Minimum number of fans to cool the system not present or failed ▪ In non-sparing and non-mirroring mode if the threshold of ten correctable errors is crossed within the window
Amber	Solid on	Critical, non-recoverable	Fatal alarm – system has failed or shutdown ▪ DIMM failure when there is one DIMM present, no good memory present ▪ Run-time memory uncorrectable error in non-redundant mode ▪ IERR signal asserted ▪ Processor 1 missing ▪ Temperature (CPU ThermTrip, memory TempHi, critical threshold crossed) ▪ No power good – power fault ▪ Processor configuration error (for instance, processor stepping mismatch)

7.3.1   System Status LED – BMC Initialization

When the AC power is first applied and 5 V-STBY is present, the BMC requires 20-30 seconds to initialize. During this time, the system status LED blinks amber and green, and the power button is disabled. After BMC initialization is complete, the status LED stops blinking and the power button functionality is restored.

7.4   DIMM Fault LEDs

A memory fault LED is provided for each DIMM socket. Though the DIMM sockets are on the DIMM riser cards, the LEDs are located on the server board. The fault LEDs are arranged in two columns: the column at the left is for the DIMMs on DIMM riser card 1; the column at the right is for the DIMMs on DIMM riser card 2.

AF001597
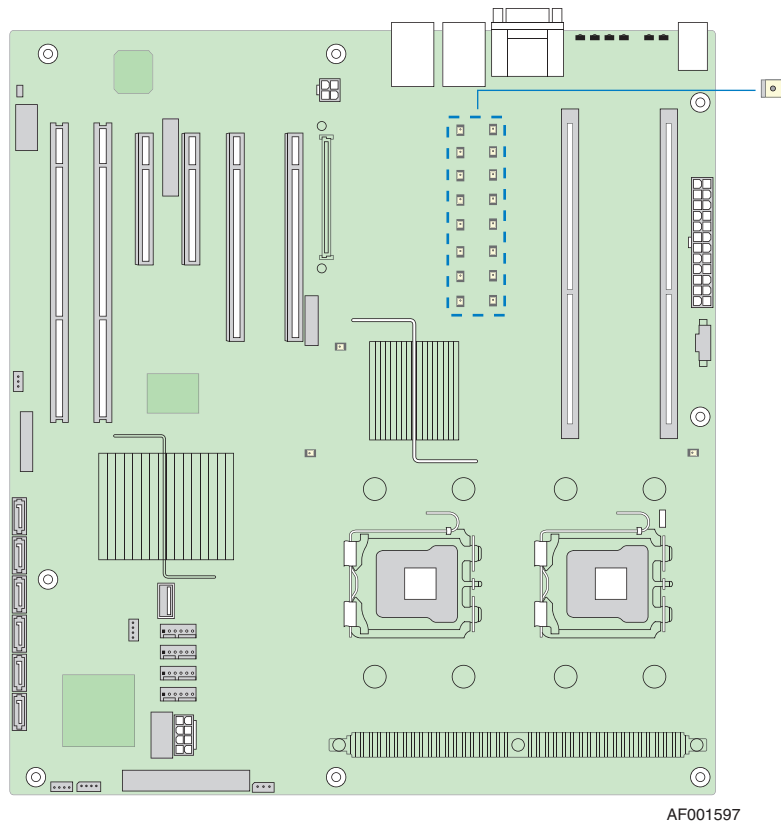
Figure 25. DIMM Fault LED Locations

7.5   Processor Fault LEDs

A fault LED is available for each processor socket. These LEDs are located near the processor sockets.
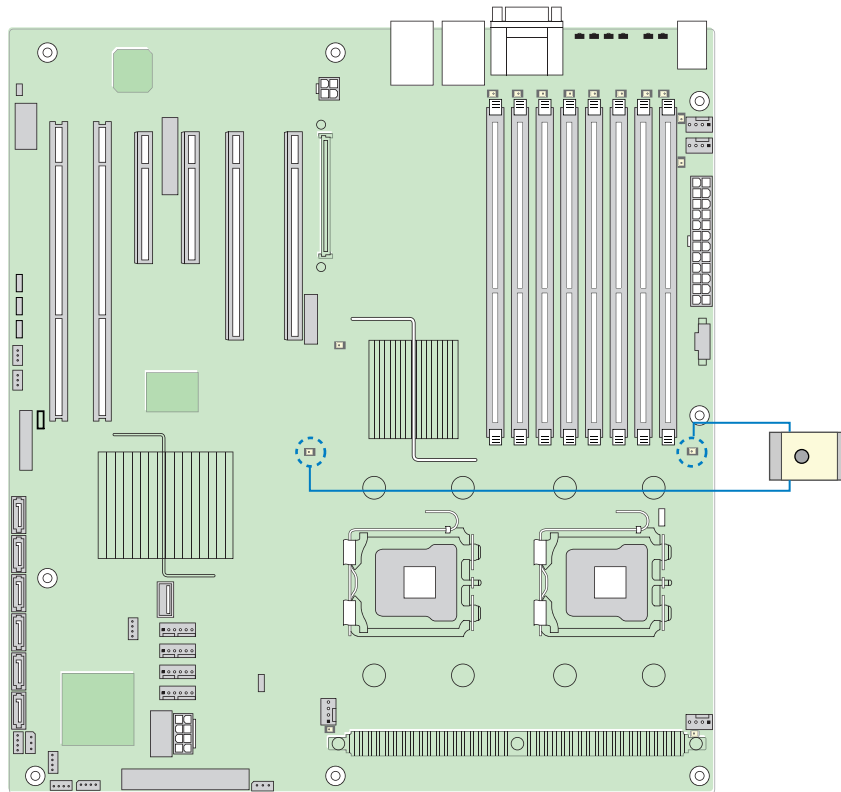
AF000206

Figure 26. Processor Fault LED Locations

7.6   Post Code Diagnostic LEDs

POST code diagnostic LEDs are in the rear I/O area between the PS/2 mouse / keyboard stacked connectors and the video / serial stacked connectors.

During the boot process, the BIOS executes a platform configuration processes. Each of these has a hex POST code number. As each configuration routine is started, the BIOS displays the POST code to the POST code diagnostic LEDs. If needed, the diagnostic LEDs identify the last POST process executed. See Appendix C for a description of how these LEDs are read and for a list of POST codes.
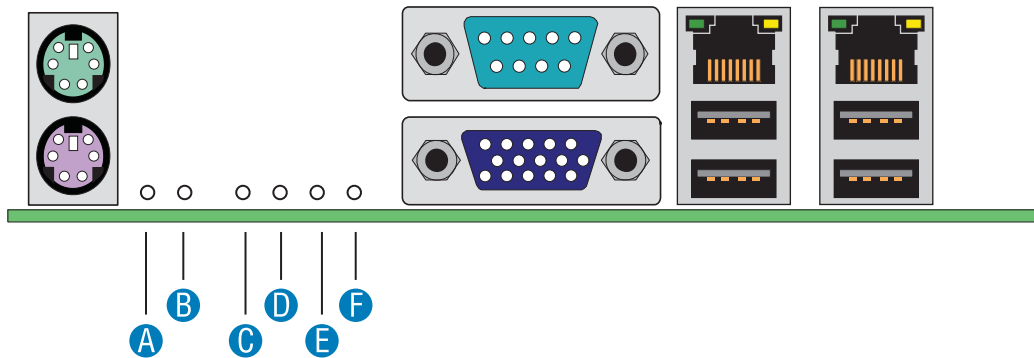
AF000541

A. Status LED	D. Bit 2 LED (POST LED)
B. ID LED	E. Bit 1 LED (POST LED)
C. MSB LED (POST LED)	F. LSB LED (POST LED)

Figure 27. POST Code Diagnostic LED Location

8.   Design and Environmental Specifications

8.1   Server System SC5400RA Design Specifications

The operation of server systems at conditions beyond those shown in the following table can cause permanent damage. Exposure to absolute maximum rating conditions for extended periods can affect reliability.

Table 39. Design Specifications

Operating Temperature	0º C to 55º C [1] (32º F to 131º F)
Non-Operating Temperature	-40º C to 70º C (-40º F to 158º F)
DC Voltage	± 5% of all nominal voltages
Shock (Unpackaged)	Trapezoidal, 50 G, 170 inches / sec
Shock (Packaged) <20 pounds 20 to <40 pounds 40 to <80 pounds 80 to <100 pounds 100 to <120 pounds 120 pounds	 36 inches 30 inches 24 inches 18 inches 12 inches 9 inches
Vibration (Unpackaged)	5 Hz to 500 Hz 3.13 g RMS random

Note:

[1] **Chassis design must provide proper airflow to avoid exceeding the processor's maximum case temperature**.

Disclaimer Note: Intel Corporation server boards contain a number of high-density VLSI and power delivery components that need adequate airflow to cool. Intel ensures through its own chassis development and testing that when Intel server building blocks are used together, the fully integrated system will meet the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of air flow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible, if components fail or the server board does not operate correctly when used outside any of their published operating or non-operating limits.

8.2 Power Requirements

This section provides power supply design guidelines, including voltage and current specifications, and power supply on/off sequencing characteristics.

Figure 28. Power Distribution Block Diagram

8.2.1 Processor Power Support

The server board supports the thermal design point (TDP) guideline for Dual-Core Intel® Xeon® processors and Quad-Core Intel® Xeon® processors. The flexible motherboard guidelines (FMB) have also been followed to help determine the suggested thermal and current design values for anticipating future processor needs. The following table provides maximum values for Icc, TDP power and T_{CASE} for the Dual-Core Intel® Xeon® processor 5000, 5100 or 5300 sequence.

Table 40. Processor Thermal Design Point Guidelines

TDP Power	Max TCASE	Icc MAX
130 W	70º C	150 A

Note: *These values are for reference only. The datasheets for the processors contain the actual specifications for the processor. If the values found in the datasheet are different than those published here, the datasheet values supersede these, and should be used.*

8.3 Power Supply Output Requirements

This section is for reference purposes only. It provides guidance to system designers to determine a power supply for use with this server board. This section specifies the power supply requirements Intel used to develop a power supply for its 5U server system.

The combined power of all outputs shall not exceed the rated output power of the power supply. The power supply must meet both static and dynamic voltage regulation requirements for the minimum loading conditions.

Table 41. 650 Watt Load Ratings

Voltage	Minimum Continuous	Maximum Continuous	Peak
+3.3 V	1.5 A	24 A	
+5 V	1.0 A	30 A	
+12 V1	0.8 A	16 A	18 A
+12 V2	0.8 A	16 A	18 A
+12 V3	0.5 A	16 A	18 A
+12 V4	1.0 A	16 A	18 A
-12 V	0 A	0.5 A	
+5 VSB	0.1 A	3.0 A	3.5 A

1. Maximum continuous total DC output power should not exceed 650 W.
2. Maximum continuous combined load on +3.3 VDC and +5 VDC outputs shall not exceed 170W.
3. Maximum peak total DC output power should not exceed 730W.
4. Peak power and current loading shall be supported for a minimum of 12 seconds.
5. Maximum combined current for the 12 V outputs shall be 52 A.
6. Peak current for the combined 12 V outputs shall be 58A.
7. Minimum of 30 A of +5 V is recommended.

8.3.1   Grounding

The grounds of the pins on the power supply output connector provide the power return path. The output connector ground pins are connected to a safety ground (power supply enclosure). This grounding ensures passing the maximum allowed common mode noise levels.

8.3.2   Standby Outputs

The 5 VSB output is present when an AC input greater than the power supply turn on voltage is applied.

8.3.3   Remote Sense

The power supply has remote sense return to regulate out ground drops for all output voltages: +3.3 V, +5 V, +12 V1, +12 V2, +12 V3, -12 V, and 5 VSB. The power supply uses remote sense (3.3 VS) to regulate out drops in the system for the +3.3 V output.

The +5 V, +12 V1, +12 V2, +12 V3, –12 V and 5 VSB outputs only use remote sense referenced to the remote sense return signal. The remote sense input impedance to the power supply must be greater than 200   on 3.3 VS and 5 VS. This is the value of the resistor connecting the remote sense to the output voltage internal to the power supply.

Remote sense must be able to regulate out a minimum of a 200 mV drop on the +3.3 V output. The remote sense return must be able to regulate out a minimum of a 200 mV drop in the power ground return. The current in any remote sense line shall be less than 5 mA to prevent voltage sensing errors.

The power supply must operate within specification over the full range of voltage drops from the power supply's output connector to the remote sense points.

8.3.4 Voltage Regulation

The power supply output voltages must stay within the following voltage limits when operating at steady state and dynamic loading conditions. These limits include the peak-peak ripple / noise.

Table 42. Voltage Regulation Limits

Parameter	Tolerance	Minimum	Nominal	Maximum	Units
+3.3V	- 5% / +5%	+3.14	+3.30	+3.46	V_{rms}
+5V	- 5% / +5%	+4.75	+5.00	+5.25	V_{rms}
+12 V1	- 5% / +5%	+11.40	+12.00	+12.60	V_{rms}
+12 V2	- 5% / +5%	+11.40	+12.00	+12.60	V_{rms}
+12 V3	- 5% / +5%	+11.40	+12.00	+12.60	V_{rms}
+12 V4	- 5% / +5%	+11.40	+12.00	+12.60	V_{rms}
- 12V	- 5% / +9%	- 11.40	-12.00	-13.08	V_{rms}
+5VSB	- 5% / +5%	+4.75	+5.00	+5.25	V_{rms}

8.3.5 Dynamic Loading

The output voltages remain within limits for the step loading and capacitive loading specified in the table. The load transient repetition rate is tested between 50 Hz and 5 kHz at duty cycles ranging from 10% to 90%. The load transient repetition rate is only a test specification. The step load may occur anywhere within the minimum load to the maximum load conditions.

Table 43. Transient Load Requirements

Output	Step Load Size [1]	Load Slew Rate	Test Capacitive Load
+3.3V	7.0A	0.25 A/ sec	4700 F
+5V	7.0A	0.25 A/ sec	1000 F
+12V	25A	0.25 A/ sec	4700 F
+5VSB	0.5A	0.25 A/ sec	20 F

1. Step loads on each 12V output may happen simultaneously.

8.3.6   Capacitive Loading

The power supply is stable and meets all requirements with the following capacitive loading ranges.

Table 44. Capacitive Loading Conditions

Output	Minimum	Maximum	Units
+3.3 V	250	6800	F
+5 V	400	4700	F
+12 V1,2,3,4	500 each	11,000	F
-12 V	1	350	F
+5 VSB	20	350	F

8.3.7   Ripple / Noise

The maximum ripple/noise output of the power supply is measured over a bandwidth of 0 Hz to 20 MHz at the power supply output connectors. A 10 F tantalum capacitor in parallel with a 0.1 F ceramic capacitor is placed at the point of measurement.

Table 45. Maximum Ripple and Noise

+3.3 V	+5 V	+12 V1,2,3,4	-12 V	+5 VSB
50mVp-p	50mVp-p	120mVp-p	120mVp-p	50mVp-p

8.3.8   Timing Requirements

The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 5 to 70 ms. 5 VSB is allowed to rise from 1.0 to 25 ms. All outputs rise monotonically. Each output voltage reaches regulation within 50 ms (T_{vout_on}) of each other during turn on of the power supply. Each output voltage falls out of regulation within 400 msec (T_{vout_off}) of each other during turn off.

The following tables and diagrams show the timing requirements for the power supply being turned on and off via the AC input with PSON held low, and the PSON signal with the AC input applied.

Table 46. Output Voltage Timing

Item	Description	Minimum	Maximum	Units
T_{vout_rise}	Output voltage rise time from each main output.	5.0 1	70 [1]	ms
T_{vout_on}	All main outputs must be within regulation of each other within this time.		50	ms
T_{vout_off}	All main outputs must leave regulation within this time.		400	ms

1. The 5VSB output voltage rise time is from 1.0 ms to 25 ms
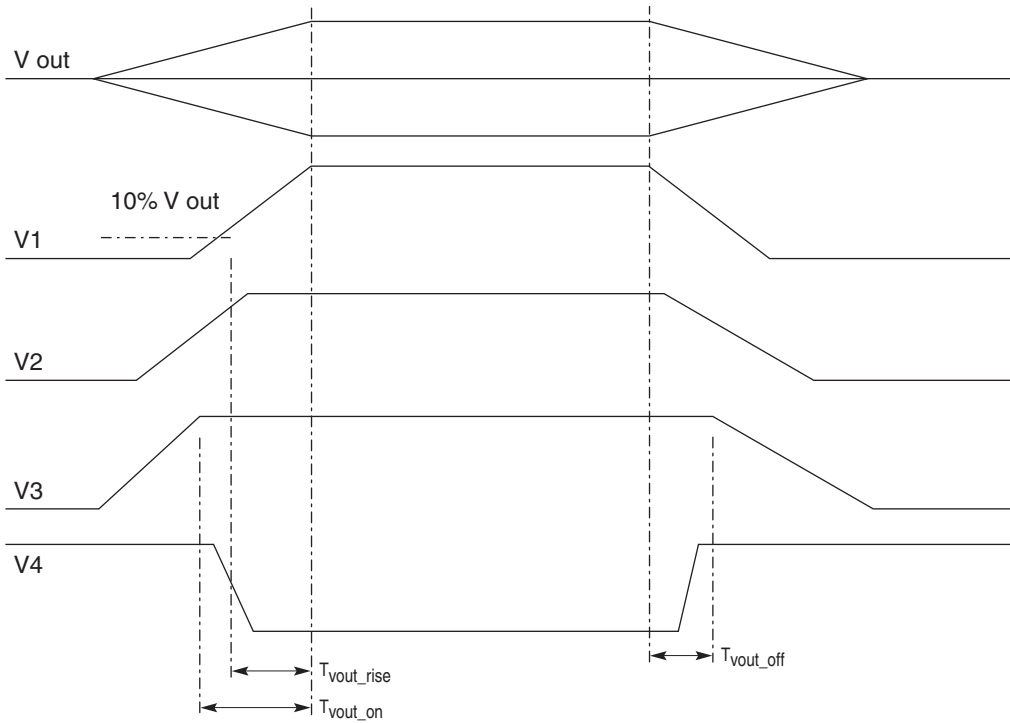
Figure 29. Output Voltage Timing

Table 47. Turn On/Off Timing

Item	Description	Minimum	Maximum	Units
$T_{sb\_on\_delay}$	Delay from AC being applied to 5VSB being within regulation.		1500	ms
$T_{ac\_on\_delay}$	Delay from AC being applied to all output voltages being within regulation.		2500	ms
T_{vout_holdup}	Time all output voltages stay within regulation after loss of AC.	21		ms
T_{pwok_holdup}	Delay from loss of AC to de-assertion of PWOK	20		ms
$T_{pson\_on\_delay}$	Delay from PSON# active to output voltages within regulation limits.	5	400	ms
T_{pson_pwok}	Delay from PSON# deactivate to PWOK being de-asserted.		50	ms
T_{pwok_on}	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	500	ms
T_{pwok_off}	Delay from PWOK de-asserted to output voltages (3.3V, 5V, 12V, -12V) dropping out of regulation limits.	1		ms
T_{pwok_low}	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal.	100		ms
T_{sb_vout}	Delay from 5VSB being in regulation to O/Ps being in regulation at AC turn on.	50	1000	ms
T_{5VSB_holdup}	Time the 5VSB output voltage stays within regulation after loss of AC.	70		ms
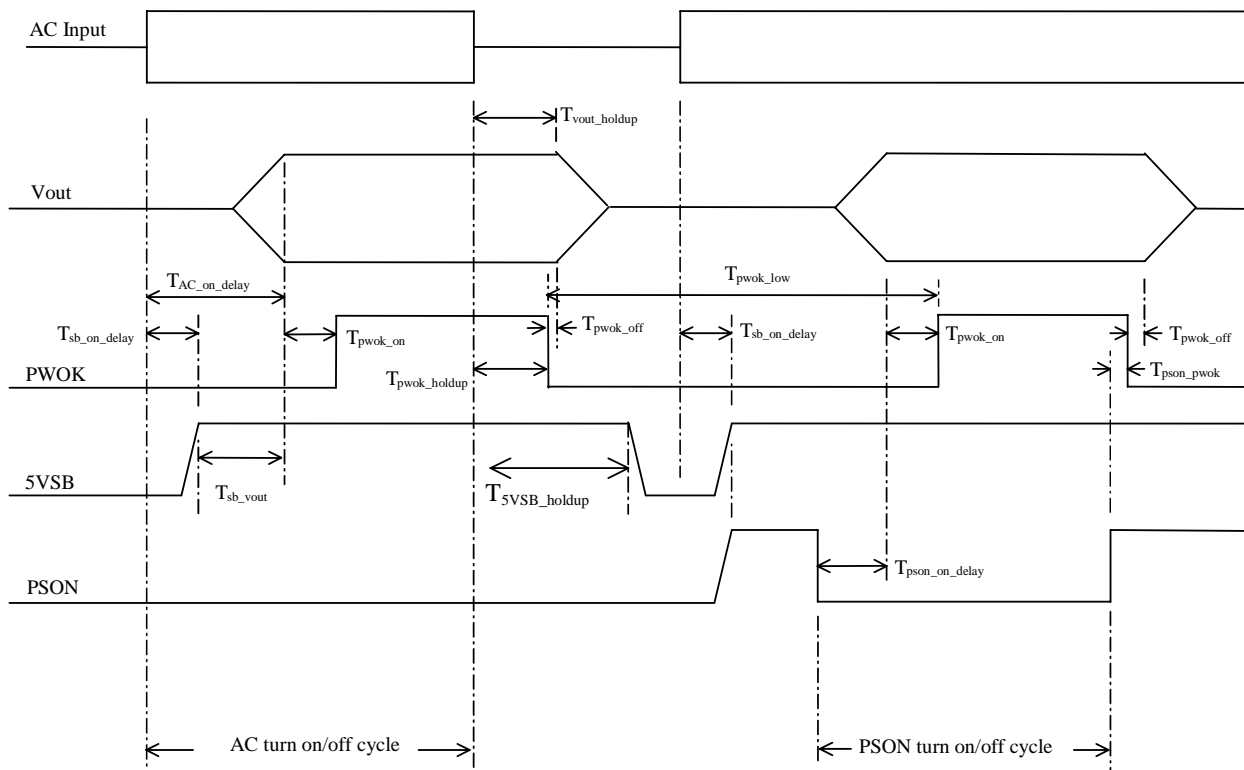
Figure 30. Turn On/Off Timing (Power Supply Signals)

8.3.9   Residual Voltage Immunity in Standby Mode

The power supply is immune to residual voltage placed on its outputs (typically, a leakage voltage through the system from standby output) up to 500 mV. No additional heat is generated, nor are internal components stressed with this voltage applied to any individual output, and all outputs simultaneously. It does not trip the power supply protection circuits during turn on.

Residual voltage at the power supply outputs for a no load condition do not exceed 100 mV when AC voltage is applied and the PSON# signal is de-asserted.

Appendix A: Integration and Usage Tips

- When adding or removing components or peripherals from the server board, AC power must be removed. 5-volt standby is as present whenever AC power is applied to the system.

- Processors must be installed in order. CPU 1 is located near the edge of the server board and must be populated.

- Four diagnostic LEDs on the back of the server board display a sequence of red, green, or amber POST codes during the boot process. If the server board hangs during POST, the LEDs display the last POST event run before the hang.

- Only fully-buffered DIMMs (FBDIMMs) are supported. For a list of supported memory for this server board, see the *Intel® S5000PSL / S5000XSL Tested Memory Report*.

- For a list of Intel supported operating systems, add-in cards, and peripherals, see the *Intel® S5000PSL, S5000XSL and S5000XVN Tested Hardware and OS List.*

- Only Dual-Core Intel® Xeon® processors 5000, 5100 or 5300 sequence with system bus speeds of 667, 1066, or 1333 MHz are supported. Previous generation Intel® Xeon® processors are not supported.

- For the best performance, the number of FBDIMMs installed should be balanced across memory branches. Example: an eight-DIMM configuration perform better than a four DIMM configuration. A sixteen-DIMM configuration perform better then a twelve DIMM configuration.

- The Intel® Remote Management Module connector is not compatible with the Intel® Server Management Module Professional Edition (Product Code AXXIMMPRO) or with the Intel® Server Management Module Advanced Edition (Product Code AXXIMMADV)

- Removing AC power before performing the CMOS Clear operation causes the system to power up and immediately power down after the CMOS Clear procedure is followed and AC power is re-applied. If this happens, remove the AC power cord, wait 30 seconds, and then re-connect the power cord. Power up the system and enter the BIOS Setup utility to reset the settings.

- Normal BMC functionality is disabled with the force BMC update jumper set to the enabled position (pins 2-3). This jumper should remain in the default (disabled) position (pins 1-2) when the server is running normally. The enabled position should only be used if the standard firmware update process fails.

- When performing a BIOS update, the BIOS select jumper must be in the default position (pins 2-3).

Appendix B: BMC Sensor Tables

This appendix lists the sensor identification numbers and information about the sensor type, name, supported thresholds, assertion and de-assertion information, and a brief description of the sensor purpose. See the *Intelligent Platform Management Interface Specification, Version 1.5*, for sensor and event/reading-type table information.

- **Sensor Type**

  The Sensor Type is the values enumerated in the *Sensor Type Codes* table in the IPMI specification. The Sensor Type provides the context in which to interpret the sensor, such as the physical entity or characteristic that is represented by this sensor.

- **Event / Reading Type**

  The Event/Reading Type values are from the *Event/Reading Type Code Ranges* and *Generic Event/Reading Type Codes* tables in the IPMI specification. Digital sensors are a specific type of discrete sensor, which have only two states.

- **Event Offset/Triggers**

  Event Thresholds are event-generating thresholds for threshold types of sensors.

  - [u,l][nr,c,nc]: upper nonrecoverable, upper critical, upper noncritical, lower nonrecoverable, lower critical, lower noncritical
  - uc, lc: upper critical, lower critical

  Event Triggers are supported event-generating offsets for discrete type sensors. The offsets can be found in the *Generic Event/Reading Type Codes* or *Sensor Type Codes* tables in the IPMI specification, depending on whether the sensor event/reading type is generic or a sensor-specific response.

- **Assertion / De-assertion Enables**

  Assertion and de-assertion indicators reveal the type of events the sensor generates:

  - As: Assertions
  - De: De-assertion

- **Readable Value / Offsets**

  - Readable Value indicates the type of value returned for threshold and other non-discrete type sensors.
  - Readable Offsets indicate the offsets for discrete sensors that are readable with the *Get Sensor Reading* command. Unless otherwise indicated, all event triggers are readable; Readable Offsets consist of the reading type offsets that do not generate events.

- **Event Data**

  Event data is the data that is included in an event message generated by the sensor. For threshold-based sensors, the following abbreviations are used:

  - R: Reading value
  - T: Threshold value

- **Rearm Sensors**

    The rearm is a request for the event status for a sensor to be rechecked and updated upon a transition between good and bad states. Rearming the sensors can be done manually or automatically. This column indicates the type supported by the sensor. The following abbreviations are used in the comment column to describe a sensor:

    - A: Auto-rearm
    - M: Manual rearm

- **Default Hysteresis**

    The hysteresis setting applies to all thresholds of the sensor. This column provides the count of hysterisis for the sensor, which can be 1 or 2 (positive or negative hysteresis).

- **Criticality**

    Criticality is a classification of the severity and nature of the condition. It also controls the behavior of the Control Panel Status LED

- **Standby**

    Some sensors operate on standby power. These sensors may be accessed and / or generate events when the main (system) power is off, but AC power is present.

Table 48. BMC Sensors

Sensor Name	Sensor Number	System Applica-bility	Sensor Type	Event / Reading Type	Event Offset Triggers	Criticality	Assert / De-assert	Readable Value / Offsets	Event Data	Rearm	Standby
Power Unit Status	01h	All	Power Unit 09h	Sensor Specific 6Fh	Power down Power cycle A/C lost	OK	As	–	Trig Offset	A	X
					Soft power control failure Power unit failure	Crit					
					Predictive failure	Non-Crit					
Power Unit Redun-dancy	02h	Chassis-specific	Power Unit 09h	Generic 0Bh	Redundancy regained Non-red: suff res from redund	OK	As	–	Trig Offset	A	X
					Redundancy lost Redundancy degraded	Degraded					
					Non-red: suff from insuff	OK					
					Non-red: insufficient	Critical					
					Redun degrade from full Redun degrade from non-redundant	OK					

Sensor Name	Sensor Number	System Applica-bility	Sensor Type	Event / Reading Type	Event Offset Triggers	Criticality	Assert / De-assert	Readable Value / Offsets	Event Data	Rearm	Standby
Watchdog	03h	All	Watchdog 2 23h	Sensor Specific 6Fh	Timer expired, status only Hard reset Power down Power cycle Timer interrupt	OK	As	–	Trig Offset	A	X
Platform Security Violation	04h	All	Platform Security Violation Attempt 06h	Sensor Specific 6Fh	Secure mode violation attempt Out-of-band access password violation	OK	As	–	Trig Offset	A	X
Physical Security	05h	Chassis Intrusion is chassis-specific	Physical Security 05h	Sensor Specific 6Fh	Chassis intrusion LAN leash lost 1	OK	As and De	–	Trig Offset	A	X
FP Diag Interrupt (NMI)	07h	All	Critical Interrupt 13h	Sensor Specific 6Fh	Front panel NMI / diagnostic interrupt Bus uncorrectable error	OK	As	–	Trig Offset	A	–
System Event Log	09h	All	Event Logging Disabled 10h	Sensor Specific 6Fh	Log area reset / cleared	OK	As	–	Trig Offset	A	X
Session Audit	0Ah	All	Session Audit 2Ah	Sensor Specific 6Fh	00h – Session activation 01h – Session deactivation	OK	As	–	As defined by IPMI	A	X
System Event ('System Event')	0Bh	All	System Event 12h	Sensor Specific 6Fh	00 – System reconfigured 04 – PEF action	OK	As	–	Trig Offset	A	X

Sensor Name	Sensor Number	System Applica-bility	Sensor Type	Event / Reading Type	Event Offset Triggers	Criticality	Assert / De-assert	Readable Value / Offsets	Event Data	Rearm	Standby
BB +1.2V Vtt	10h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	Threshold defined	As and De	Analog	R, T	A	–
BB+1.9V NIC Core	11h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	Threshold defined	As and De	Analog	R, T	A	X
BB +1.5V AUX	12h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	Threshold defined	As and De	Analog	R, T	A	–
BB +1.5V	13h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	Threshold defined	As and De	Analog	R, T	A	–
BB +1.8V	14h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	Threshold defined	As and De	Analog	R, T	A	–
BB +3.3V	15h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	Threshold defined	As and De	Analog	R, T	A	–
BB +3.3V STB	16h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	Threshold defined	As and De	Analog	R, T	A	X
BB +1.5V ESB	17h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	Threshold defined	As and De	Analog	R, T	A	X
BB +5V	18h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	Threshold defined	As and De	Analog	R, T	A	–
BB +1.2V NIC	19h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	Threshold defined	As and De	Analog	R, T	A	–
BB +12V AUX	1Ah	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	Threshold defined	As and De	Analog	R, T	A	–
BB 0.9V	1Bh	All except SC5400RA	Voltage 02h	Threshold 01h	[u,l] [c,nc]	Threshold defined	As and De	Analog	R, T	A	–
BB2 +1.8V	1Ch	SC5400RA	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-Fatal	As and De	Analog	R, T	A,I	–
BB Vbat	1Eh	All	Voltage 02h	Digital Discrete 05h	01h – Limit exceeded	Critical	As and De	–	R, T	A	X

Sensor Name	Sensor Number	System Applica-bility	Sensor Type	Event / Reading Type	Event Offset Triggers	Criticality	Assert / De-assert	Readable Value / Offsets	Event Data	Rearm	Standby
BB Temp	30h	All	Temperature 01h	Threshold 01h	[u,l] [c,nc]	Threshold defined	As and De	Analog	R, T	A	X
Front Panel Temp	32h	All	Temperature 01h	Threshold 01h	[u,l] [c,nc]	Threshold defined	As and De	Analog	R, T	A	X
BNB Temp	33h	All	Temperature 01h	Threshold 01h	[u,l] [c,nc]	Threshold defined	As and De	Analog	R, T	A	–
CPU 1 FAN	50h	Chassis-specific	Fan 04h	Threshold 01h	[l] [c,nc]	Threshold defined	As and De	Analog	R, T	M	–
CPU 2 FAN	51h	Chassis-specific	Fan 04h	Threshold 01h	[l] [c,nc]	Threshold defined	As and De	Analog	R, T	M	–
SYS FAN 1 TACH	52h	Chassis-specific	Fan 04h	Threshold 01h	[l] [c,nc]	Threshold defined	As and De	Analog	R, T	M	–
SYS FAN 2 TACH	53h	Chassis-specific	Fan 04h	Threshold 01h	[l] [c,nc]	Threshold defined	As and De	Analog	R, T	M	–
SYS FAN 3 TACH'	54h	Chassis-specific	Fan 04h	Threshold 01h	[l] [c,nc]	Threshold defined	As and De	Analog	R, T	M	–
SYS FAN 4 TACH	55h	Chassis-specific	Fan 04h	Threshold 01h	[l] [c,nc]	Threshold defined	As and De	Analog	R, T	M	–
SYS FAN 5 TACH'	56h	Chassis-specific	Fan 04h	Threshold 01h	[l] [c,nc]	Threshold defined	As and De	Analog	R, T	M	–
SYS FAN 6 TACH	57h	Chassis-specific	Fan 04h	Threshold 01h	[l] [c,nc]	Threshold defined	As and De	Analog	R, T	M	–
Tach Fan (Not used on this server)	58h	Chassis-specific	Fan 04h	Threshold 01h	[l] [c,nc]	Threshold defined	As and De	Analog	R, T	M	–
Tach Fan (Not used on this server)	59h	Chassis-specific	Fan 04h	Threshold 01h	[l] [c,nc]	Threshold defined	As and De	Analog	R, T	M	–

Sensor Name	Sensor Number	System Applica-bility	Sensor Type	Event / Reading Type	Event Offset Triggers	Criticality	Assert / De-assert	Readable Value / Offsets	Event Data	Rearm	Standby
Fan 1 Present	60h	Chassis-specific	Fan 04h	Generic 08h	Device present	OK	As and De	–	T	A	–
Fan 2 Present	61h	Chassis-specific	Fan 04h	Generic 08h	Device present	OK	As and De	–	T	A	–
Fan 3 Present	62h	Chassis-specific	Fan 04h	Generic 08h	Device present	OK	As and De	–	T	A	–
Fan 4 Present	63h	Chassis-specific	Fan 04h	Generic 08h	Device present	OK	As and De	–	T	A	–
Fan 5 Present	64h	Chassis-specific	Fan 04h	Generic 08h	Device present	OK	As and De	–	T	A	–
Fan 6 Present	65h	Chassis-specific	Fan 04h	Generic 08h	Device present	OK	As and De	–	T	A	–
Fan 7 Present	66h	Chassis-specific	Fan 04h	Generic 08h	Device present	OK	As and De	–	T	A	–
Fan 8 Present	67h	Chassis-specific	Fan 04h	Generic 08h	Device present	OK	As and De	–	T	A	–
Fan 9 Present	68h	Chassis-specific	Fan 04h	Generic 08h	Device present	OK	As and De	–	T	A	–
Fan 10 Present	69h	Chassis-specific	Fan 04h	Generic 08h	Device present	OK	As and De	–	T	A	–
Fan Redun-dancy	6Fh	Chassis-specific	Fan 04h	Generic 0Bh	Redundancy regained	OK	As	–	Trig Offset	A	X
					Redundancy lost Redundancy degraded	Degraded						
					Non-red: suff res from redund Non-red: suff from insuff	OK						
					Non-red: insufficient	Critical						

Sensor Name	Sensor Number	System Applica-bility	Sensor Type	Event / Reading Type	Event Offset Triggers	Criticality	Assert / De-assert	Readable Value / Offsets	Event Data	Rearm	Standby
					Redun degrade from full	OK					
					Redun degrade from non-redundant						
Power Supply Status 1	70h	Chassis-specific	Power Supply 08h	Sensor Specific 6Fh	Presence	OK	As and De	–	Trig Offset	A	X
					Failure	Critical					
					Predictive fail	Non-Crit					
					A/C lost	Critical					
					Configuration error	Non-Crit					
Power Supply Status 2	71h	Chassis-specific	Power Supply 08h	Sensor Specific 6Fh	Presence	OK	As and De	–	Trig Offset	A	X
					Failure	Critical					
					Predictive fail	Non-Crit					
					A/C lost	Critical					
					Configuration error	Non-Crit					
Power Nozzle Power Supply 1	78h	Chassis-specific	Current 03h	Threshold 01h	[u] [c,nc]	Threshold defined	As and De	Analog	R, T	A	–
Power Nozzle Power Supply 2	79h	Chassis-specific	Current 03h	Threshold 01h	[u] [c,nc]	Threshold defined	As and De	Analog	R, T	A	–
Power Gauge V1 rail (+12v) Power Supply 1	7Ah	Chassis-specific	Current 03h	Threshold 01h	[u] [c,nc]	Threshold defined	As and De	Analog	R, T	A	–

Sensor Name	Sensor Number	System Applica-bility	Sensor Type	Event / Reading Type	Event Offset Triggers	Criticality	Assert / De-assert	Readable Value / Offsets	Event Data	Rearm	Standby
Power Gauge V1 rail (+12v) Power Supply 2	7Bh	Chassis-specific	Current 03h	Threshold 01h	[u] [c,nc]	Threshold defined	As and De	Analog	R, T	A	–
Power Gauge (aggre-gate power) Power Supply 1	7Ch	Chassis-specific	Other Units 0Bh	Threshold 01h	[u] [c,nc]	Threshold defined	As and De	Analog	R, T	A	–
Power Gauge (aggregate power) Power Supply 2	7Dh	Chassis-specific	Other Units 0Bh	Threshold 01h	[u] [c,nc]	Threshold defined	As and De	Analog	R, T	A	–
System ACPI Power State	82h	All	System ACPI Power State 22h	Sensor Specific 6Fh	S0 / G0 S1 S3 S4 S5 / G2 G3 mechanical off	OK	As	–	Trig Offset	A	X
Button	84h	All	Button 14h	Sensor Specific 6Fh	Power button Reset button	OK	As	–	Trig Offset	A	X
SMI Timeout	85h	All	SMI Timeout F3h	Digital Discrete 03h	01h – State asserted	Critical	As and De	–	Trig Offset	A	–

Sensor Name	Sensor Number	System Applica-bility	Sensor Type	Event / Reading Type	Event Offset Triggers	Criticality	Assert / De-assert	Readable Value / Offsets	Event Data	Rearm	Standby
Sensor Failure	86h	All	Sensor Failure F6h	OEM Sensor Specific 73h	I^{2}C device not found I^{2}C device error detected I^{2}C bus timeout	OK	As	–	Trig Offset	A	X
NMI Signal State	87h	All	OEM C0h	Digital Discrete 03h	01h – State asserted	OK	–	01h	–	–	–
SMI Signal State	88h	All	OEM C0h	Digital Discrete 03h	01h – State asserted	OK	–	01h	–	–	–
Proc 1 Status	90h	All	Processor 07h	Sensor Specific 6Fh	IERR	Critical	As and De	–	Trig Offset	M	X
					Thermal trip	Non-rec					
					Config error	Critical					
					Presence	OK					
					Disabled	Degraded					
Proc 2 Status	91h	All	Processor 07h	Sensor Specific 6Fh	IERR	Critical	As and De	–	Trig Offset	M	X
					Thermal trip	Non-rec					
					Config error	Critical					
					Presence	OK					
					Disabled	Degraded					
Proc 1 Temp	98h	All	Temperature 01h	Threshold 01h	[u,l] [c,nc]	Threshold defined	As and De	Analog	R, T	A	–
Proc 2 Temp	9Ah	All	Temperature 01h	Threshold 01h	[u,l] [c,nc]	Threshold defined	As and De	Analog	R, T	A	–
PCIe Link0	A0h	Critical Interrupt 13F	Sensor Specific 6Fh	PCIe Link0	Bus correctable error	OK	As	–	See the BIOS EPS	A	–
					Bus uncorrectable error	Degraded					

Sensor Name	Sensor Number	System Applica-bility	Sensor Type	Event / Reading Type	Event Offset Triggers	Criticality	Assert / De-assert	Readable Value / Offsets	Event Data	Rearm	Standby
PCIe Link1	A1h	Critical Interrupt 13F	Sensor Specific 6Fh	PCIe Link1	Bus correctable error	OK	As	–	See the BIOS EPS	A	–
					Bus uncorrectable error	Degraded					
PCIe Link2	A2h	Critical Interrupt 13F	Sensor Specific 6Fh	PCIe Link2	Bus correctable error	OK	As	–	See the BIOS EPS	A	–
					Bus uncorrectable error	Degraded					
PCIe Link3	A3h	Critical Interrupt 13F	Sensor Specific 6Fh	PCIe Link3	Bus correctable error	OK	As	–	See the BIOS EPS	A	–
					Bus uncorrectable error	Degraded					
PCIe Link4	A4h	Critical Interrupt 13F	Sensor Specific 6Fh	PCIe Link4	Bus correctable error	OK	As	–	See the BIOS EPS	A	–
					Bus uncorrectable error	Degraded					
PCIe Link5	A5h	Critical Interrupt 13F	Sensor Specific 6Fh	PCIe Link5	Bus correctable error	OK	As	–	See the BIOS EPS	A	–
					Bus uncorrectable error	Degraded					
PCIe Link6	A6h	Critical Interrupt 13F	Sensor Specific 6Fh	PCIe Link6	Bus correctable error	OK	As	–	See the BIOS EPS	A	–
					Bus uncorrectable error	Degraded					
PCIe Link7	A7h	Critical Interrupt 13F	Sensor Specific 6Fh	PCIe Link7	Bus correctable error	OK	As	–	See the BIOS EPS	A	–
					Bus uncorrectable error	Degraded					

Sensor Name	Sensor Number	System Applica-bility	Sensor Type	Event / Reading Type	Event Offset Triggers	Criticality	Assert / De-assert	Readable Value / Offsets	Event Data	Rearm	Standby
PCIe Link8	A8h	Critical Interrupt 13F	Sensor Specific 6Fh	PCIe Link8	Bus correctable error	OK	As	–	See the BIOS EPS	A	–
					Bus uncorrectable error	Degraded					
PCIe Link9	A9h	Critical Interrupt 13F	Sensor Specific 6Fh	PCIe Link9	Bus correctable error	OK	As	–	See the BIOS EPS	A	–
					Bus uncorrectable error	Degraded					
PCIe Link10	AAh	Critical Interrupt 13F	Sensor Specific 6Fh	PCIe Link10	Bus correctable error	OK	As	–	See the BIOS EPS	A	–
					Bus uncorrectable error	Degraded					
PCIe Link11	ABh	Critical Interrupt 13F	Sensor Specific 6Fh	PCIe Link11	Bus correctable error	OK	As	–	See the BIOS EPS	A	–
					Bus uncorrectable error	Degraded					
PCIe Link12	ACh	Critical Interrupt 13F	Sensor Specific 6Fh	PCIe Link12	Bus correctable error	OK	As	–	See the BIOS EPS	A	–
					Bus uncorrectable error	Degraded					
PCIe Link13	ADh	Critical Interrupt 13F	Sensor Specific 6Fh	PCIe Link13	Bus correctable error	OK	As	–	See the BIOS EPS	A	–
					Bus uncorrectable error	Degraded					
Proc 1 Thermal Control	C0h	All	Temperature 01h	Threshold 01h	[u] [c,nc]	Threshold defined	As and De	Analog	Trig Offset	M	–

Sensor Name	Sensor Number	System Applica-bility	Sensor Type	Event / Reading Type	Event Offset Triggers	Criticality	Assert / De-assert	Readable Value / Offsets	Event Data	Rearm	Standby
Proc 2 Thermal Control	C1h	All	Temperature 01h	Threshold 01h	[u] [c,nc]	Threshold defined	As and De	Analog	Trig Offset	M	–
Proc 1 VRD Over Temp	C8h	All	Temperature 01h	Digital Discrete 05h	01h – Limit exceeded	Non-Critical	As and De	–	Trig Offset	M	–
Proc 2 VRD Over Temp	C9h	All	Temperature 01h	Digital Discrete 05h	01h – Limit exceeded	Non-Critical	As and De	–	Trig Offset	M	–
Proc 1 Vcc	D0h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	Threshold defined	As and De	Analog	R, T	A	–
Proc 2 Vcc	D1h	All	Voltage 02h	Threshold 01h	[u,l] [c,nc]	Threshold defined	As and De	Analog	R, T	A	–
Proc 1 Vcc Out-of-Range	D2h	All	Voltage 02h	Digital Discrete 05h	01h – Limit exceeded	Non-Critical	As and De	Discrete	R, T	A	–
Proc 2 Vcc Out-of-Range	D3h	All	Voltage 02h	Digital Discrete 05h	01h – Limit exceeded	Non-Critical	As and De	Discrete	R, T	A	–
CPU Population Error	D8h	All	Processor 07h	Generic 03h	01h –- State asserted	Critical	As and De	–	R, T	A	–
DIMM 1- 8	E0h – E7h	All	Slot Connector 21h	Sensor Specific 6Fh	Fault status asserted	Situation dependent[5]	As and De	–	Trig Offset	A	–
					Device installed	OK					
					Disabled	Situation dependent[5]					
					Sparing	OK					
DIMM 9-16	F7h – FEh	SC5400RA	Slot Connector 21h	Sensor Specific 6Fh	Fault status asserted	Situation dependent[5]	As and De	–	Trig Offset	A	–
					Device installed	OK					

Sensor Name	Sensor Number	System Applica-bility	Sensor Type	Event / Reading Type	Event Offset Triggers	Criticality	Assert / De-assert	Readable Value / Offsets	Event Data	Rearm	Standby
					Disabled	Situation dependent[5]					
					Sparing	OK					
Memory Error A - D	ECh - EFh	All	Memory 0Ch	Sensor Specific 6Fh	Uncorrectable ECC	OK[6]	As and De	–	Trig Offset	A	–
B0 DIMM Sparing Enabled	F0h	All	Entity Presence 25h	Sensor Specific 6Fh	Entity present	OK	As	–	Trig Offset	A	–
B0 DIMM Sparing Redun-dancy	F1h	All	Memory 0Ch	Discrete 0Bh	Fully redundant	OK	As	–	Trig Offset	A	–
					Non-red: suff res from redund	Degraded					
					Non-red: suff res from insuff res						
					Non-red: Insuff res	Crtical					
B1 DIMM Sparing Enabled	F2h	All	Entity Presence 25h	Sensor Specific 6Fh	Entity present	OK	As	–	Trig Offset	A	–
B1 DIMM Sparing Redun-dancy	F3h	All	Memory 0Ch	Discrete 0Bh	Fully redundant	OK	As	–	Trig Offset	A	–
					Non-red: suff res from redund	Degraded					
					Non-red: suff res from insuff res						
					Non-red: insuff res	Crtical					
B01 DIMM Mirroring Enabled	F4h	All	Entity Presence 25h	Sensor Specific 6Fh	Entity present	OK	As	–	Trig Offset	A	–
B01 DIMM	F5h	All	Memory	Discrete	Fully redundant	OK	As	–	Trig Offset	A	–

Sensor Name	Sensor Number	System Applica-bility	Sensor Type	Event / Reading Type	Event Offset Triggers	Criticality	Assert / De-assert	Readable Value / Offsets	Event Data	Rearm	Standby
Mirroring Redun- dancy			0Ch	0Bh	Non-red:suff res from redund	Degraded					
					Non-red:suff res from insuff res						
					Non-red: insuff res	Crtical					

Note 1: Not supported except for ESB2 embedded NICs

Appendix C: POST Code Diagnostic LED Decoder

During the boot process, the BIOS executes platform configuration processes, each of which is assigned a hex POST code number. At the start of each configuration routine, the BIOS displays the POST code to the POST code diagnostic LEDs. If the system hangs during POST, the diagnostic LEDs can be used to identify the last POST process.

Each POST code is represented by a combination of colors from the four POST LEDs. The LEDs display green, red, and amber. The POST codes are divided into an upper nibble and a lower nibble. Each bit in the upper nibble is represented by a red LED and each bit in the lower nibble is represented by a green LED. If both bits are set, then both the red and green LEDs are lit, resulting in amber. If both bits are clear, then the LED is off.
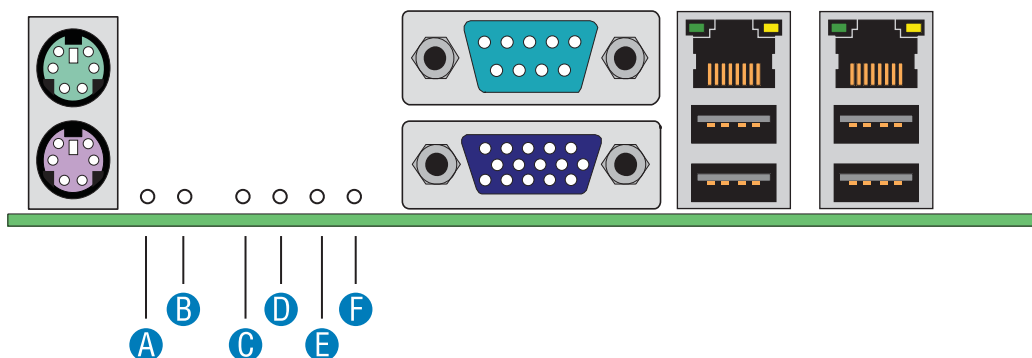
AF000541

A. Status LED	D. Bit 2 LED (POST LED)
B. ID LED	E. Bit 1 LED (POST LED)
C. MSB LED (POST LED)	F. LSB LED (POST LED)

Figure 31. Diagnostic LED Placement Diagram

Example: The BIOS sends a value of ACh to the diagnostic LED decoder. The LEDs are decoded as follows:

- Red bits = 1010b = Ah
- Green bits = 1100b = Ch

The red bits correspond to the upper nibble and the green bits correspond to the lower nibble. The two are concatenated as ACh.

Table 49. POST Progress Code LED Example

	8h		4h		2h		1h	
LEDs	**Red**	**Green**	**Red**	**Green**	**Red**	**Green**	**Red**	**Green**
ACh	1	1	0	1	1	0	0	0
Result	Amber		Green		Red		Off	
	MSB		Bit 2		Bit 1		LSB	

Table 50. Diagnostic LED POST Code Decoder

Checkpoint	Diagnostic LED Decoder G=Green, R=Red, A=Amber				Description
	MSB	Bit 2	Bit 1	LSB	
Host Processor					
0x10h	Off	Off	Off	R	Power-on initialization of the host processor (bootstrap processor)
0x11h	Off	Off	Off	A	Host processor cache initialization (including AP)
0x12h	Off	Off	G	R	Starting application processor initialization
0x13h	Off	Off	G	A	SMM initialization
Chipset					
0x21h	Off	Off	R	G	Initializing a chipset component
Memory					
0x22h	Off	Off	A	Off	Reading configuration data from memory (SPD on DIMM)
0x23h	Off	Off	A	G	Detecting presence of memory
0x24h	Off	G	R	Off	Programming timing parameters in the memory controller
0x25h	Off	G	R	G	Configuring memory parameters in the memory controller
0x26h	Off	G	A	Off	Optimizing memory controller settings
0x27h	Off	G	A	G	Initializing memory, such as ECC init
0x28h	G	Off	R	Off	Testing memory
PCI Bus					
0x50h	Off	R	Off	R	Enumerating PCI busses
0x51h	Off	R	Off	A	Allocating resources to PCI busses
0x52h	Off	R	G	R	Hot Plug PCI controller initialization
0x53h	Off	R	G	A	Reserved for PCI bus
0x54h	Off	A	Off	R	Reserved for PCI bus
0x55h	Off	A	Off	A	Reserved for PCI bus
0x56h	Off	A	G	R	Reserved for PCI bus
0x57h	Off	A	G	A	Reserved for PCI bus
USB					
0x58h	G	R	Off	R	Resetting USB bus
0x59h	G	R	Off	A	Reserved for USB devices
ATA / ATAPI / SATA					
0x5Ah	G	R	G	R	Resetting PATA / SATA bus and all devices
0x5Bh	G	R	G	A	Reserved for ATA
SMBUS					
0x5Ch	G	A	Off	R	Resetting SMBUS
0x5Dh	G	A	Off	A	Reserved for SMBUS
Local Console					
0x70h	Off	R	R	R	Resetting the video controller (VGA)
0x71h	Off	R	R	A	Disabling the video controller (VGA)
0x72h	Off	R	A	R	Enabling the video controller (VGA)
Remote Console					

Checkpoint	Diagnostic LED Decoder				Description
	G=Green, R=Red, A=Amber				
	MSB	Bit 2	Bit 1	LSB	
0x78h	G	R	R	R	Resetting the console controller
0x79h	G	R	R	A	Disabling the console controller
0x7Ah	G	R	A	R	Enabling the console controller
Keyboard (PS2 or USB)					
0x90h	R	Off	Off	R	Resetting the keyboard
0x91h	R	Off	Off	A	Disabling the keyboard
0x92h	R	Off	G	R	Detecting the presence of the keyboard
0x93h	R	Off	G	A	Enabling the keyboard
0x94h	R	G	Off	R	Clearing keyboard input buffer
0x95h	R	G	Off	A	Instructing keyboard controller to run Self Test (PS2 only)
Mouse (PS2 or USB)					
0x98h	A	Off	Off	R	Resetting the mouse
0x99h	A	Off	Off	A	Detecting the mouse
0x9Ah	A	Off	G	R	Detecting the presence of mouse
0x9Bh	A	Off	G	A	Enabling the mouse
Fixed Media					
0xB0h	R	Off	R	R	Resetting fixed media device
0xB1h	R	Off	R	A	Disabling fixed media device
0xB2h	R	Off	A	R	Detecting presence of a fixed media device (IDE hard drive detection, etc.)
0xB3h	R	Off	A	A	Enabling / configuring a fixed media device
Removable Media					
0xB8h	A	Off	R	R	Resetting removable media device
0xB9h	A	Off	R	A	Disabling removable media device
0xBAh	A	Off	A	R	Detecting presence of a removable media device (IDE CDROM detection, etc.)
0xBCh	A	G	R	R	Enabling / configuring a removable media device
Boot Device Selection					
0xD0	R	R	Off	R	Trying boot device selection
0xD1	R	R	Off	A	Trying boot device selection
0xD2	R	R	G	R	Trying boot device selection
0xD3	R	R	G	A	Trying boot device selection
0xD4	R	A	Off	R	Trying boot device selection
0xD5	R	A	Off	A	Trying boot device selection
0xD6	R	A	G	R	Trying boot device selection
0xD7	R	A	G	A	Trying boot device selection
0xD8	A	R	Off	R	Trying boot device selection
0xD9	A	R	Off	A	Trying boot device selection
0XDA	A	R	G	R	Trying boot device selection
0xDB	A	R	G	A	Trying boot device selection
0xDC	A	A	Off	R	Trying boot device selection
0xDE	A	A	G	R	Trying boot device selection
0xDF	A	A	G	A	Trying boot device selection

Checkpoint	Diagnostic LED Decoder				Description
	G=Green, R=Red, A=Amber				
	MSB	Bit 2	Bit 1	LSB	
Pre-EFI Initialization (PEI) Core					
0xE0h	R	R	R	Off	Started dispatching early initialization modules (PEIM)
0xE2h	R	R	A	Off	Initial memory found, configured, and installed correctly
0xE1h	R	R	R	G	Reserved for initialization module use (PEIM)
0xE3h	R	R	A	G	Reserved for initialization module use (PEIM)
Driver Execution Environment (DXE) Core					
0xE4h	R	A	R	Off	Entered EFI driver execution phase (DXE)
0xE5h	R	A	R	G	Started dispatching drivers
0xE6h	R	A	A	Off	Started connecting drivers
DXE Drivers					
0xE7h	R	A	A	G	Waiting for user input
0xE8h	A	R	R	Off	Checking password
0xE9h	A	R	R	G	Entering BIOS setup
0xEAh	A	R	A	Off	Flash Update
0xEEh	A	A	A	Off	Calling Int 19. One beep unless silent boot is enabled.
0xEFh	A	A	A	G	Unrecoverable boot failure / S3 resume failure
Runtime Phase / EFI Operating System Boot					
0xF4h	R	A	R	R	Entering Sleep state
0xF5h	R	A	R	A	Exiting Sleep state
0xF8h	A	R	R	R	Operating system has requested EFI to close boot services (ExitBootServices ( ) has been called)
0xF9h	A	R	R	A	Operating system has switched to virtual address mode (SetVirtualAddressMap ( ) has been called)
0xFAh	A	R	A	R	Operating system has requested the system to reset (ResetSystem () has been called)
Pre-EFI Initialization Module (PEIM) / Recovery					
0x30h	Off	Off	R	R	Crisis recovery has been initiated because of a user request
0x31h	Off	Off	R	A	Crisis recovery has been initiated by software (corrupt flash)
0x34h	Off	G	R	R	Loading crisis recovery capsule
0x35h	Off	G	R	A	Handing off control to the crisis recovery capsule
0x3Fh	G	G	A	A	Unable to complete crisis recovery.

Appendix D: POST Code Errors

Whenever possible, the BIOS outputs the boot progress codes on the video screen. Progress codes are 32-bit quantities plus optional data. The 32-bit numbers include class, subclass, and operation information. The class and subclass fields point to the type of hardware that is being initialized. The operation field represents the specific initialization activity. Based on the data bit availability to display progress codes, a progress code can be customized to fit the data width. The higher the data bit, the higher the granularity of information that can be sent on the progress port. The progress codes may be reported by the system BIOS or option ROMs.

The response column in the following table is divided into two types:

- **Pause:** The message is displayed in the Error Manager screen, an error is logged to the SEL, and user input is required to continue. The user can take immediate corrective action or choose to continue booting.

- **Halt:** The message is displayed in the Error Manager screen, an error is logged to the SEL, and the system cannot boot unless the error is resolved. The user needs to replace the faulty part and restart the system.

Table 51. POST Error Messages and Handling

Error Code	Error Message	Response
004C	Keyboard / interface error	Pause
0012	CMOS date / time not set	Pause
5220	Configuration cleared by jumper	Pause
5221	Passwords cleared by jumper	Pause
5223	Configuration default loaded	Pause
0048	Password check failed	Halt
0141	PCI resource conflict	Pause
0146	Insufficient memory to shadow PCI ROM	Pause
8110	Processor 01 internal error (IERR) on last boot	Pause
8111	Processor 02 internal error (IERR) on last boot	Pause
8120	Processor 01 thermal trip error on last boot	Pause
8121	Processor 02 thermal trip error on last boot	Pause
8130	Processor 01 disabled	Pause
8131	Processor 02 disabled	Pause
8160	Processor 01 unable to apply BIOS update	Pause
8161	Processor 02 unable to apply BIOS update	Pause
8190	Watchdog timer failed on last boot	Pause
8198	Operating system boot watchdog timer expired on last boot	Pause
0192	L3 cache size mismatch	Halt
0194	CPUID, processor family are different	Halt
0195	Front side bus mismatch	Pause
0197	Processor speeds mismatched	Pause
8300	Baseboard management controller failed self-test	Pause
8306	Front panel controller locked	Pause
8305	Hotswap controller failed	Pause

Error Code	Error Message	Response
84F2	Baseboard management controller failed to respond	Pause
84F3	Baseboard management controller in update mode	Pause
84F4	Sensor data record empty	Pause
84FF	System event log full	Pause
8500	Memory Component could not be configured in the selected RAS mode.	Pause
8520	DIMM_A1 failed Self Test (BIST).	Pause
8521	DIMM_A2 failed Self Test (BIST).	Pause
8522	DIMM_A3 failed Self Test (BIST).	Pause
8523	DIMM_A4 failed Self Test (BIST).	Pause
8524	DIMM_B1 failed Self Test (BIST).	Pause
8525	DIMM_B2 failed Self Test (BIST).	Pause
8526	DIMM_B3 failed Self Test (BIST).	Pause
8527	DIMM_B4 failed Self Test (BIST).	Pause
8528	DIMM_C1 failed Self Test (BIST).	Pause
8529	DIMM_C2 failed Self Test (BIST).	Pause
852A	DIMM_C3 failed Self Test (BIST).	Pause
852B	DIMM_C4 failed Self Test (BIST).	Pause
852C	DIMM_D1 failed Self Test (BIST).	Pause
852D	DIMM_D2 failed Self Test (BIST).	Pause
852E	DIMM_D3 failed Self Test (BIST).	Pause
852F	DIMM_D4 failed Self Test (BIST).	Pause
8540	Memory component lost redundancy during the last boot.	Pause
8580	DIMM_A1 correctable ECC error encountered.	Pause
8581	DIMM_A2 correctable ECC error encountered.	Pause
8582	DIMM_A3 correctable ECC error encountered.	Pause
8583	DIMM_A4 correctable ECC error encountered.	Pause
8584	DIMM_B1 correctable ECC error encountered.	Pause
8585	DIMM_B2 correctable ECC error encountered.	Pause
8586	DIMM_B3 correctable ECC error encountered.	Pause
8587	DIMM_B4 correctable ECC error encountered.	Pause
8588	DIMM_C1 correctable ECC error encountered.	Pause
8589	DIMM_C2 correctable ECC error encountered.	Pause
858A	DIMM_C3 correctable ECC error encountered.	Pause
858B	DIMM_C4 correctable ECC error encountered.	Pause
858C	DIMM_D1 correctable ECC error encountered.	Pause
858D	DIMM_D2 correctable ECC error encountered.	Pause
858E	DIMM_D3 correctable ECC error encountered.	Pause
858F	DIMM_D4 correctable ECC error encountered.	Pause
8600	Primary and secondary BIOS IDs do not match.	Pause
8601	Override jumper is set to force boot from lower alternate BIOS bank of flash ROM	Pause
8602	Watchdog timer expired (secondary BIOS may be bad!)	Pause
8603	Secondary BIOS checksum fail	Pause

POST Error Beep Codes

The following table lists POST error beep codes. Before video initialization, the BIOS uses beep codes to indicate error conditions. The beep code is followed by a code on POST progress LEDs.

Table 52. POST Error Beep Codes

Beeps	Error Message	POST Progress Code	Description
3	Memory error		System halted because a fatal error related to the memory was detected.
6	BIOS rolling back error		The system has detected a corrupted BIOS in the flash part, and is rolling back to the last good BIOS.

The BMC may generate beep codes upon detection of failure conditions. Beep codes are sounded each time the problem is discovered, such as on each power-up attempt, but are not sounded continuously. Each digit in the code is represented by a sequence of beeps whose count is equal to the digit.

Table 53. BMC Beep Codes

Code	Reason for Beep	Associated Sensors	Supported?
1-5-2-1	CPU: Empty slot / population error – Processor slot 1 is not populated.	CPU Population Error	Yes
1-5-2-2	CPU: No processors (terminators only)	N/A	No
1-5-2-3	CPU: Configuration error (e.g., VID mismatch)	N/A	No
1-5-2-4	CPU: Configuration error (e.g, BSEL mismatch)	N/A	No
1-5-4-2	Power fault: DC power unexpectedly lost (power good dropout)	Power Unit – power unit failure offset	Yes
1-5-4-3	Chipset control failure	N/A	No
1-5-4-4	Power control fault	Power Unit – soft power control failure offset	Yes

Appendix E: System Upgrade Accessories

Upgrades for the Intel® Server System SC5400RA include the tool-less six-drive SAS/SATA hot swap drive bays, a rack mount conversion kit, and a slimline CD-ROM / USB floppy drive kit.

Selected upgrades and optional accessories for the Intel® Server System SC5400RA are shown in the following product matrix table.

Table 54. Product Matrix

Product Code	Standard Fixed Hard Drive Bays	Optional Hot Swap SAS/SATA Drives	Power Supply and Required Power Cord Configuration	Hot Swap Fans	Pedestal/ Rack
Intel® Server System SC5400RA chassis Hot Swap Redundant 830 Watt	6-drive bay	6-SAS/SATA 6-SAS/SATA Expander	One 830-watt PFC module installed. Second power module is optional. Requires one power cord per module.	Not supported.	Pedestal configuration is standard. Rack conversion kit is an accessory.

These available upgrades are described below.

SAS/SATA Hot Swap Drive Bay - AXX6DRV3G

The optional hot-swap SAS/SATA hard disk drive bay, AXX6DRV3G is compatible with either SAS or SATA 3.5-inch hard drives. The kit includes:

- Drive rails
- Data cables
- Drive mounting bay
- IPMB cable
- SES cable
- SGPIO cable
- Installation guide
- SATA/SAS configuration label

SAS/SATA Hot Swap Drive Bay - AXX6DRV3GEXP

The optional hot-swap expander SAS/SATA hard disk drive bay, AXX6DRV3GEXP is compatible with either SAS or SATA 3.5-inch hard drives. The kit includes the following:

- Drive rails
- Data cables
- Drive mounting bay
- IPMB cable
- Installation guide
- SATA/SAS configuration label

Rack Conversion Kit - ARIGRACK

The rack conversion kit includes all components needed to convert a pedestal chassis into a rack-mount chassis. The conversion kit includes rack bezel plastic parts, rack handles, and rack mounting rails.

Slimline CD-ROM and USB Floppy Drive Kit - AXXCDUSBFDBRK

This accessory provides a way to mount a slimline optical drive and USB floppy drive into a single, standard 5.25-inch external peripheral bay.

Regulatory and Certification Information

The Intel® Server System SC5400RA meets the standards and regulations listed below.

Product Safety Compliance

The Intel® Server System SC5400RA complies with the following safety requirements:

- UL 1950 – CSA 950 (US/Canada)
- EN 60 950 (European Union)
- IEC 60 950 (International)
- CE – Low Voltage Directive (73/23/EEC) (European Limits)
- EMKO-TSE (74-SEC) 207/94 (Nordics)

Product EMC Compliance

The system has been tested and verified to comply with the following EMC regulations when configured with the Intel® server boards specified. For information on compatible server boards, refer to Intel's Server Builder website (http://www.intel.com/go/serverbuilder) or contact your local Intel representative.

- FCC (Class A Verification) – Radiated and Conducted Emissions (USA)
- ICES-003 (Class A) – Radiated and Conducted Emissions (Canada)
- CISPR 22, 3rd Edition (Class A) – Radiated and Conducted Emissions (International)
- EN45022 (Class A) – Radiated and Conducted Emissions (European Union)
- EN45024 (Immunity) (European Union)
- EN6100-3-2 and -3 (Power Harmonics and Fluctuation and Flicker)
- CE – EMC Directive (89/33/EEC) (European Union)
- VCCI (Class A) – Radiated and Conducted Emissions (Japan)
- RRL (Class A) – Radiated and Conducted Emissions (Korea)

Product Ecology Requirements

All materials, parts and subassemblies must not contain restricted materials as defined in Intel's Environmental Product Content Specification of Suppliers and Outsourced Manufacturers. Substances banned under Restriction of Hazardous Substances (RoHS) European Directive are included in the Intel's Environmental Product Content Specification.

Restriction of Hazardous Substances (RoHS) Compliance: Intel has a system in place to restrict use of banned substances per in accordance to the European Directive 2002/95/EC. Compliance is based on materials banned in the RoHS Directive are either (1) below all applicable substance threshold limits or (2) an approved/pending RoHS exemption applies.

Note: *RoHS implementation details are not fully defined and may change.*

Threshold limits and banned substances are noted as follows:

- Quantity limit of 0.1% by mass (1000 PPM) for: Lead; Mercury; Hexavalent Chromium; Polybrominated Biphenyls Diphenyl Ethers (PBDE); and Quantity limit of 0.01% by mass (100 PPM) for Cadmium
- All plastic parts shall not use brominated flame retardant or any other halogenated retardants that are not accepted by environmental programs such as Blue Angels, Nordic White Swan, and Swedish TCO.
- All plastic parts that weigh >25gm shall be marked with the ISO11469 requirements for recycling. Example >PC/ABS<
- Packaging materials may not contain more than 100 ppm (total) of lead, cadmium, chromium or mercury.
- If sold as a retail product, packaging materials must be marked with applicable recycling logos for Europe (green dot) and Japan (Eco-marks).
- Product documentation shall incorporate all safety-required information to conform to certifiers and regulators and the certifications issued for the product.
- All cords and cables shall contain < 100 ppm of cadmium.

Product Regulatory Compliance Markings

This product is provided with the following Product Certification Markings:

- UL / cUL Listing Mark
- CE Mark
- German GS Mark
- Russian GOST Mark
- FCC, Class A Verification Marking
- ICES-003 (Canada EMC Compliance Marking)
- VCCI, Class A Mark
- Australian C-Tick Mark
- Taiwan BSMI Certification Number and Class A Warning

Electromagnetic Compatibility Notices

USA

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference.
- This device must accept any interference received, including interference that may cause undesired operation.

For questions related to the EMC performance of this product, contact:

Intel Corporation
5200 N.E. Elam Young Parkway
Hillsboro, OR 97124
1-800-628-8686

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment to an outlet on a circuit other than the one to which the receiver is connected.

Any changes or modifications not expressly approved by the grantee of this device could void the user's authority to operate the equipment. The customer is responsible for ensuring compliance of the modified product.

Only peripherals (computer input/output devices, terminals, printers, etcetera) that comply with FCC Class B limits may be attached to this computer product. Operation with noncompliant peripherals is likely to result in interference to radio and TV reception.

All cables used to connect to peripherals must be shielded and grounded. Operation with cables, connected to peripherals that are not shielded and grounded, may result in interference to radio and TV reception.

FCC Verification Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference
- This device must accept any interference received, including interference that may cause undesired operation.

For questions related to the EMC performance of this product, contact:

Intel Corporation
5200 N.E. Elam Young Parkway
Hillsboro, OR 97124-6497

Phone: 1 (800)-INTEL4U or 1 (800) 628-8686

ICES-003 (Canada)

> Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe A prescrites dans la norme sur le matériel brouilleur: "Appareils Numériques", NMB-003 édictée par le Ministre Canadian des Communications.

English translation:

"This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled "Digital Apparatus," ICES-003 of the Canadian Department of Communications."

Europe (CE Declaration of Conformity)

This product has been tested in accordance to, and complies with the Low Voltage Directive (73/23/EEC) and EMC Directive (89/336/EEC). The product has been marked with the CE Mark to illustrate its compliance.

Japan EMC Compatibility

Electromagnetic Compatibility Notices (International):

> この装置は、情報処理装置等電波障害白主規制協議会（ＶＣＣＩ）の基準に基づくクラスＡ情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。

English translation:

This is a Class A product based on the standard of the Voluntary Control Council for Interference (VCCI) from Information Technology Equipment. If this is used near a radio or television receiver in a domestic environment, it may cause radio interference. Install and use the equipment according to the instruction manual."

BSMI (Taiwan)

The BSMI Certification number and the following warning are located on the product safety label, which is located on the bottom side (pedestal orientation) or side (rack mount configuration).

警告使用者：

這是甲類的資訊產品，在居住的環境中使用時，
可能會造成射頻干擾，在這種情況下，使用者會
被要求採取某些適當的對策。

Glossary

Term	Definition
ACPI	Advanced Configuration and Power Interface
AP	Application Processor
APIC	Advanced Programmable Interrupt Control
ASMI	Advanced Server Management Interface
BIOS	Basic Input / Output System
BIST	Built-In Self Test
BMC	Baseboard Management Controller
Bridge	Circuitry connecting one computer bus to another, allowing an agent on one to access the other
CEK	Common Enabling Kit
CMOS	In terms of this specification, this describes the PC-AT compatible region of battery-backed 128 bytes of memory, which normally resides on the server board.
ESB2	Enterprise South Bridge 2
FBD	Fully Buffered DIMM
FMB	Flexible Mother Board
FRB	Fault Resilient Booting
FRU	Field Replaceable Unit
FSB	Front Side Bus
GPIO	General Purpose I/O
I2C	Inter-Integrated Circuit Bus
ICH	I/O Controller Hub
IERR	Internal Error
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LPC	Low Pin Count
LUN	Logical Unit Number
MAC	Media Access Control
MCH	Memory Controller Hub
ms	milliseconds
NMI	Nonmaskable Interrupt
OEM	Original Equipment Manufacturer
PEF	Platform Event Filtering
PWM	Pulse-Width Modulation
RASUM	Reliability, Availability, Serviceability, Usability, and Manageability
RTC	Real-Time Clock (Component of ICH peripheral chip)
SDR	Sensor Data Record
SEEPROM	Serial Electrically Erasable Programmable Read-Only Memory
SEL	System Event Log
SIO	Server Input / Output
SMI	Server Management Interrupt (SMI is the highest priority nonmaskable interrupt)
SMM	Server Management Mode

Term	Definition
SMS	Server Management Software
SNMP	Simple Network Management Protocol
TBD	To Be Determined
TIM	Thermal Interface Material
VID	Voltage Identification
VRD	Voltage Regulator Down
Word	16-bit quantity

Reference Documents

See the following documents for additional information:

- Intel® S5000 Server Board Family Datasheet