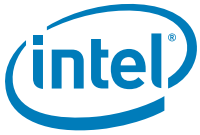

Intel® RAID Portable Cache Module AXXRPCM2

Technical Product Specification

Intel order number D86727-001

Revision 1.0

December 2006

Enterprise Platforms and Services Marketing

Revision History

Date	Revision Number	Modifications
December 2006	1.0	Initial Release

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1. Introduction

This document describes the key hardware components, firmware, and software utility requirements for the Intel® RAID Portable Cache Module (AXXRPCM2).

The RAID Portable Cache Module is available as an accessory for the Intel® Integrated RAID Controller SRCSAS18E. The module is a 32 M x 72-bit, 8 chip, 240-pin DIMM module with five 32 M x 16 (FBGA) DDR2 SDRAM, one registers, one PLL, and one 256x8 EEPROM for serial presence detect. The memory part of the module conforms to JEDEC specifications. It has smart battery backup circuitry.

Note: In this document, "RAID controller" refers only to the Intel® Integrated RAID Controller SRCSAS18E unless otherwise indicated.

Figure 1. Intel® RAID Portable Cache Module (AXXRPCM2)

Writing data to the adapter's cache memory is much faster than writing it to a storage device. Write operations complete quickly at the software application level. The RAID controller writes the cached data to the storage device when system activity is low or when the cache is full. The risk of using write-back cache is that the cached data can be lost if the AC power fails before it is written to the storage device. In addition to the battery-backed cache that improves system performance, the AXXRPCM2 mitigates risk of data loss by providing a battery backup.

The AXXRPCM2 monitors the voltage level of the DRAM modules on the RAID controller. If the voltage drops below a defined level, the battery backup module switches the memory power source from the RAID controller to the battery pack. The battery backup provides power for the memory until the voltage returns to an acceptable level, at which time the battery backup circuitry switches the power source back to the RAID controller. Pending data is then written to storage devices with no loss of data.

The AXXRPCM2 charges the battery pack automatically and communicates battery status information, such as voltage, temperature, and current, to the host computer. It can move the RAID controller's cached data to a replacement controller if the data has not been written to a disk. This could be necessary if the RAID controller fails. After moving the AXXRPCM2 and the associated hard disk drives to a new RAID controller, the AXXRPCM2 flushes the cached data through the new adapter to the disks.

2. Product Details

The AXXRPCM2 ensures data integrity for the RAID solution by ensuring that the data passing through the cache is written to the hard drives.

The battery backup preserves the contents of the RAID DIMM if the power drops below specifications. It ensures that after a power failure or fatal event, all data on the RAID cache DIMM is flushed to the hard drives. The RAID controller's I/O processor senses system power or standby power if the system is shut down or in standby mode. If the I/O processor senses that power has dropped below 2.96 V, it initiates a power-fail sequence that safely puts the RAID DIMM into a self-refresh state. After power is restored, the data from the DIMM is written to the disk array. The AXXRPCM2 provides additional fault tolerance when used with a UPS.

2.1 Components

- Battery pack: Includes a circuit logic board and attached NiMH batteries. The logic board provides sensing and management logic to support the battery charge, discharge, and monitoring. A small cable connects the battery to the battery logic board (smart battery circuit).
- Smart battery circuit: Ensures that the battery is maintained at optimal performance and charge levels. This circuit is based on the Texas Instruments* bq2060A SBS v1.1-compliant gas gauge IC.
- Monitoring / notification software: Monitoring is accomplished through RAID BIOS Console 2, RAID Web Console 2, or command line utilities. The user is notified of failures or corrective actions.

2.2 Features

- RoHS compliant
- Fully DDR2 400 compliant
- JEDEC-Standard 240-pin dual inline memory module (DIMM)
- Registered
- Based on 32 M x 16 DDR2 (BGA) SDRAM components
- Programmable CAS latency
- Programmable additive latency: 0,1,2,3 and 4
- Write latency equals read latency minus 1
- OCD (off-chip driver impedance adjustment)
- ODT (on-die termination)
- 2 K page size for x 16
- VDD = VDDQ = 1.8V +/-0.1V
- 7.8 µs maximum average periodic refresh iInterval
- Serial presence detect (SPD)
- SSTL18 compatible inputs and outputs
- One external bank

- Four internal memory banks (512 Mb)
- Pure power and ground planes
- Gold PCB connector

The battery pack is rated at a nominal voltage of 4.8 V with a typical capacity of 880 mAH.

2.3 Electrical and Mechanical Details

Table 1. Electrical and Mechanical Details

Feature	Description
Supported RAID controller	Intel® Integrated RAID Controller SRCSAS18E
Data retention	Up to 72 hrs
Chemistry	Nickel metal hydride
Dimensions	Maximum 5.395 inches by 1.44 inches
Weight	3.5 oz
Operating temperature	10 to 40 degrees Celsius
Operating humidity	20% - 80 %, non-condensing
Storage temperature	Greater than 90 days at 0 to 30 degrees Celsius 30 to 90 days at 0 to 40 degrees Celsius Less than 30 days at 0 to 50 degrees Celsius
Storage humidity	20% - 80 %, non-condensing
Battery Capacity	880 mAH
Voltages	Nominal OCV: 4.8 V, four cells in series, 1.45 v max per cell typical Charging maximum: 7.0 V
Fast charge current	350 mAH
Trickle charge rate	N/A
Battery voltage conditioning	Less than 3.6 V
Battery charge time	Typical: ~6 hours to charge from 3.6V OCV to 5.5V OCV Worst case: 8 hours if pack is completely depleted of charge
Date Retention Times	72 hours for 256MB standard cache, using 256 Mbit x 16 DDR2
MTBF (Electrical Components)	283,999 hours at 40 degrees Celsius
Battery shelf life	1 year
Battery operational life	1000 recharges cycles. Intel recommends replacing the battery yearly.
Memory Technology	DDR2 ECC SDRAM
Socket Tpe	DIMM for ECC SDRAM
Cache Memory Size Supported	256 MB
Memory Bus Speed	400 MHz
Memory Bus Width	72-bit

2.4 Functional Block Diagram

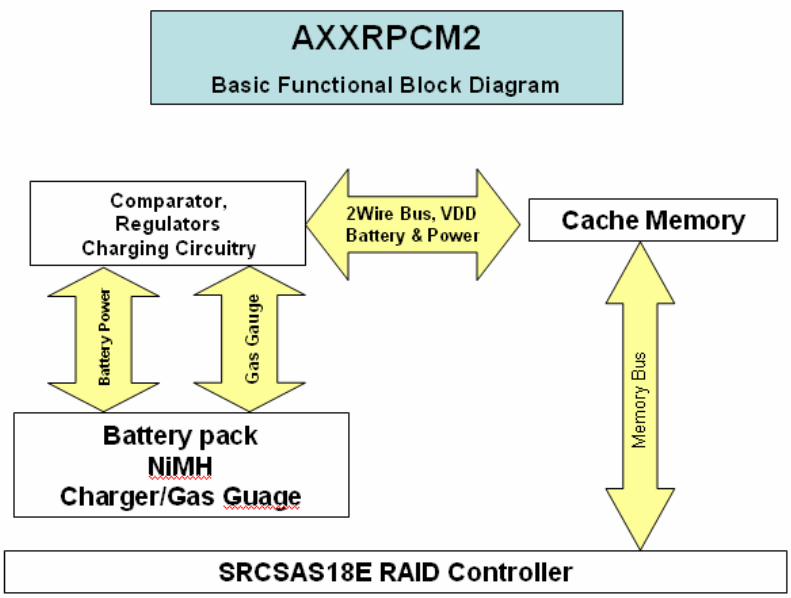

Figure 2. Block Diagram

2.5 Gold PCB Connector Pin Assignment

Table 2. PCB Connector Pin Assignment

Pin#	Symbol	Pin#	Symbol	Pin#	Symbol	Pin#	Symbol
1	VREF	61	A4	121	VSS	181	VDDQ
2	VSS	62	VDDQ	122	DQ4	182	A3
3	DQ0	63	A2	123	DQ5	183	A1
4	DQ1	64	VDD	124	VSS	184	VDD
5	VSS	65	VSS	125	DM0/DQS9	185	CK0
6	DQS0*	66	VSS	126	DQS9*	186	CK0*
7	DQS0	67	VDD	127	VSS	187	VDD
8	VSS	68	Par_In	128	DQ6	188	A0
9	DQ2	69	VDD	129	DQ7	189	VDD
10	DQ3	70	A10/AP	130	VSS	190	BA1
11	VSS	71	BA0	131	DQ12	191	VDDQ
12	DQ8	72	VDDQ	132	DQ13	192	RAS*
13	DQ9	73	WE*	133	VSS	193	S0*
14	VSS	74	CAS*	134	DM1/DQS10	194	VDDQ
15	DQS1*	75	VDDQ	135	DQS10*	195	ODT0
16	DQS1	76	S1*	136	VSS	196	A13
17	VSS	77	ODT1	137	CK1	197	VDD
18	RESET*	78	VDDQ	138	CK1*	198	VSS

Pin#	Symbol	Pin#	Symbol	Pin#	Symbol	Pin#	Symbol
19	NC	79	VSS	139	VSS	199	DQ36
20	VSS	80	DQ32	140	DQ14	200	DQ37
21	DQ10	81	DQ33	141	DQ15	201	VSS
22	DQ11	82	VSS	142	VSS	202	DM4/DQS13
23	VSS	83	DQS4*	143	DQ20	203	DQS13*
24	DQ16	84	DQS4	144	DQ21	204	VSS
25	DQ17	85	VSS	145	VSS	205	DQ38
26	VSS	86	DQ34	146	DM2/DQS11	206	DQ39
27	DQS2*	87	DQ35	147	DQS11*	207	VSS
28	DQS2	88	VSS	148	VSS	208	DQ44
29	VSS	89	DQ40	149	DQ22	209	DQ45
30	DQ18	90	DQ41	150	DQ23	210	VSS
31	DQ19	91	VSS	151	VSS	211	DM5/DQS14
32	VSS	92	DQS5*	152	DQ28	212	DQS14*
33	DQ24	93	DQS5	153	DQ29	213	VSS
34	DQ25	94	VSS	154	VSS	214	DQ46
35	VSS	95	DQ42	155	DM3/DQS12	215	DQ47
36	DQS3*	96	DQ43	156	DQS12*	216	VSS
37	DQS3	97	VSS	157	VSS	217	DQ52
38	VSS	98	DQ48	158	DQ30	218	DQ53
39	DQ26	99	DQ49	159	DQ31	219	VSS
40	DQ27	100	VSS	160	VSS	220	CK2
41	VSS	101	SA2	161	CB4	221	CK2*
42	CB0	102	NC	162	CB5	222	VSS
43	CB1	103	VSS	163	VSS	223	DM6DQS15
44	VSS	104	DQS6*	164	DM8/DQS17	224	DQS15*
45	DQS8*	105	DQS6	165	DQS17*	225	VSS
46	DQS8	106	VSS	166	VSS	226	DQ54
47	VSS	107	DQ50	167	CB6	227	DQ55
48	CB2	108	DQ51	168	CB7	228	VSS
49	CB3	109	VSS	169	VSS	229	DQ60
50	VSS	110	DQ56	170	VDDQ	230	DQ61
51	VDDQ	111	DQ57	171	CKE1	231	VSS
52	CKE0	112	VSS	172	VDD	232	DM7/DQS16
53	VDD	113	DQS7*	173	NC	233	DQS16*
54	BA2	114	DQS7	174	NC	234	VSS
55	Err_Out	115	VSS	175	VDDQ	235	DQ62
56	VDDQ	116	DQ58	176	A12	236	DQ63
57	A11	117	DQ59	177	A9	237	VSS
58	A7	118	VSS	178	VDD	238	VDDSPD
59	VDD	119	SDA	179	A8	239	SA0
60	A5	120	SCL	180	A6	240	SA1

Note: * = Active Low

Table 3. Pin Descriptions

Pin	Type	Function
CK, CK*	Input	Differential system clock inputs. All address and control inputs are sampled on the crossing of the positive edge of CK and negative edge of CK*. Output (read) data is referenced to the crossing of CK and CK* (both crossing directions)
ODT	Input	On die termination: ODT (registered high) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is applied to each DQ, DQS, DQS*and DM signal for x4 and DQ, DQS, DQS* RDQS, RDQS*and DM for x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS, UDQS LDQS, LDQS, UDM and LDM signal. The ODT pin will be ignored if the EMRS (1) is programmed to disable ODT.
CS*	Input	Chip select: All commands are masked when CS* is registered high. CS* provides for external rank selection on systems with multiple memory ranks. CS* is considered part of the command code.
CKE#	Input	Clock enable: CKE high activates and CKE low deactivate internal clock signals and device input buffers and output drivers. Taking CKE low provides precharge power-down and self-refresh operation (all banks idle), or active power-down (row active in any bank). CKE is synchronous for power down entry and exit and or self-refresh entry. CKE is asynchronous for self-refresh exit. CKE must be maintained for high throughout read and write accesses. Input buffers, excluding CK, CK*, ODT, and CKE are disabled during dower-down. Input buffers, excluding CKE, are disabled during self-refresh.
A0 - A13	Input	Address inputs: Provides the row address for activate commands and the column address and auto-precharge bit A10 (=AP) for read / write commands to select one location out of the memory array in the respective bank. A10 (=AP) is sampled during a precharge command to determine whether the precharge applies to one bank (A10=low) or all banks (A10=high). If only one bank is to be precharged, then the bank is selected by BA0 and BA1. The address inputs provide the op-code during mode register set commands. Row address A13 is used on x4 and x8 components only.
BA0, BA1	Input	Bank address inputs: BA0 and BA1 define to which bank an activate, read, write or precharge command is being applied. BA0 and BA1 also determine if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
RAS*	Input	Row address strobe: When sampled at the positive rising edge of the clock RAS* defines the operation to be executed by the SDRAM.
CAS*	Input	Column address strobe: When sampled at the positive rising edge of the clock, CAS* defines the operation to be executed by the SDRAM.
WE*	Input	Write enable :When sampled at the positive rising edge of the clock, WE* defines the operation to be executed by the SDRAM.
DM, LDM, UDM	Input	Data mask: An input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. LDM and UDM are the input mask signals for x16 components and control the lower or upper bytes. For x8 components the data mask function is disabled, when RDQS / RQDS* are enabled by EMRS (1) command.
DQS0,DQS*, LDQS, LDQS*,UDQS,UDQS*	Input/Output	Data strobe: Output with read data, input with write data. Edge aligned with read data, centered with write data. For the x16, LDQS corresponds to the data on LDQ0 - LDQ7; UDQS corresponds to the data on UDQ0-UDQ7. The data strobes DQS, LDQS, UDQS may be used in single ended mode or paired with the optional complementary signals DQS*, LDQS*, UDQS*, to provide differential pair signaling to the system during both reads and writes. An EMRS (1) control bit enables or disables the complementary data strobe signals.

RDQS0, RDQS*	Input/Output	Read data strobe: For x8 components a RDQS, RDQS* pair can be enabled via the EMRS (1) for read timing. RDQS, RDQS* is not supported on x4 and x16 components. RDQS, RDQS* are edge-aligned with read data. If RDQS, RDQS* is enabled, the DM function is disabled on x8 components.
DQ0-DQ63, LDQx,UDQx	Input/Output	Data lines :Data input / output pins DQ0~DQ3 for x4 components, DQ0~DQ7 for x8 components, LDQ0~LDQ7 and UDQ0~UDQ7 for x16 components CB0-CB7, check bit: input/output lines, used for ECC.
VDDQ	SUPPLY	DQ power supply: 1.8V +/- 0.1V
VSSQ	SUPPLY	DQ ground:
VDDL	SUPPLY	DLL power supply: 1.8V +/- 0.1V
VSSDL	SUPPLY	DLL ground
VDD	SUPPLY	Power supply: 1.8V +/- 0.1V
VSS	SUPPLY	Ground
VREF	SUPPLY	Reference voltage: For SSTL18 inputs
SCL	-	SPD clock lines: Clocks data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to VDDSPD on the system planar to act as a pull up.
SDA	-	SPD data: Bidirectional pin to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to VDDSPD on the system planar to act as a pull-up.
SA0 – SA2	SUPPLY	SPD address lines: These signals are tied at the system planar to either VSS or VDD SPD to configure the serial SPD EEPROM address range.
RESET	Input	Pin is connected to the RST pin on the register and to the OE pin on the PLL. When low, all register outputs are driven low and the PLL clocks to the DRAMs and register(s) are set to low level (the PLL remains synchronized with the input clock)
Par_In	Input	Parity bit for the address and control bus. (1 = Odd, 0 = Even)
Err_Out	Output	Parity error found in the address and control bus
NC	SUPPLY	No connection: Line is not connected in DIMM.

Note: * = Active Low

2.6 Connecting Cable

A 5-pin connector cable is installed in the battery pack.

Table 4. Interface Connector Pinout

Pin	Signal Name	Descritptions	Color
1	SMBD	SMBus data	Green
2	SMBC	SMBus clock	Blue
3	GND	Battery negative terminal	Black
4	PACK-	Battery pack negative terminal	White
5	PACK+	Battery pack positive terminal	Red

3. Battery Pack

The cache-memory hold time depends on the size and configuration of the RAID controller memory. Retention time depends on memory capacity and the number of memory components on the DIMM to support the capacity. An estimated battery backup retention time is 72 hours.

3.1 Smart Battery Circuit

The AXXRPCM2 is based on the Texas Instruments* bq2060A SBS v1.1-compliant Gas Gauge IC. The key features of the SBS v1.1 IC are:

- Provides accurate measurement of available charge
- Supports SBS Smart Battery Data Specification v1.1
- Reports voltages
- Provides voltage, temperature, and current measurements
- Measures charge flow using a V-to-F converter with offset of less than 16µV after calibration

The bq2060A SBS-compliant Gas Gauge IC for battery pack maintains an accurate record of the available charge. It determines battery capacity by monitoring the amount of charge input or removed from the smart battery.

The bq2060A measures battery voltage, temperature, and current, estimates battery self-discharge, and monitors the battery for low-voltage thresholds. It measures charge and discharge activity by monitoring the voltage across a small-value series sense resistor between the battery's negative terminal and the negative terminal of the battery pack. The battery charge is determined by monitoring this voltage and correcting the measurement for environmental and operating conditions.

For more information see the manufacturer web site.

The Intel® RAID Smart Battery features.

- Integrated into battery back
- Reduced host CPU intervention
- Shares I^2C bus with the onboard EEPROM for memory
- Real-time battery status information
- Low charge warning
- Instantaneous voltage, current, and temperature
- Battery charge percentage remaining and at-rate information

- Broadcasts event alarms to the host:
  - Out-of-temperature
  - Terminate charge
  - Terminate discharge
  - Low capacity
- Manufacturing information
- Smart Charger Protocol for improved battery maintenance, calibration, and charging performance

3.2 Battery States

Sensing logic senses battery voltage levels and recognizes the battery state.

3.2.1 Initialized State

This is the battery state during the normal power up sequence. In RAID firmware, there are two levels of initialization:

- During boot loader execution
- During RAID firmware boot

3.2.2 Discharging State

Battery voltage is being drained as part of a relearn cycle.

3.2.3 Fully Charged State

A battery that is not fully charged has a low-voltage level that indicates the level of charge. Charging begins when the battery logic detects low voltage and power is supplied.

Once fully charged, a relearn cycle is initiated for a new battery. Relearn takes a fully charged battery through a discharge-charge cycle to update the gas gauge capacity parameters. The relearn cycle takes up to 24 hours. After the relearn cycle, battery information is accurate regarding the state of charge, capacity, and other parameters that determine the health of the battery.

- The user can define a relearn cycle interval. The default is a one-month (30-day) interval.
- A relearn cycle initiates on a newly-inserted battery, even if the battery was previously fully charged.
- Some applications can start a relearn, or a relearn can be manually started.

3.2.4 Fully-discharged State

Detected as a low voltage parameter. The charger detects a fully-discharged battery state and starts charging the cells when sufficient power is available, and the firmware has completed the initialization.

3.3 RAID Firmware Interaction

RAID firmware detects the battery status and logs events:

- Battery present
- Battery not present
- New battery detected
- Battery has been replaced
- Battery temperature is high
- Battery voltage low
- Battery is charging
- Battery is discharging
- Battery voltage is normal
- Battery needs replacement: SOH bad
- Battery needs replacement: 3 years old
- Battery needs replacement: Charger is not working
- Relearn started
- Relearn in progress
- Relearn completed
- Relearn timed out
- Relearn pending: Battery is under charge.
- Relearn post phoned
- Relearn will start in 4 days
- Relearn will start in 2 day
- Relearn will start in 1 day
- Relearn will start in 5 hours

3.4 Intel® RAID Smart Battery Software

3.4.1 Intel® RAID BIOS Console 2

The system BIOS loads the RAID option ROM that is resident on the RAID controller flash. To run the utility, press <Ctrl>+<G> when prompted during POST. The option ROM checks for the presence of the battery and informs the user if the battery is missing or not fully charged. The RAID BIOS Console Utility can be used to monitor charge cycle count and voltage levels. It displays the number of fast battery charges and discharges.

3.4.2 Intel RAID® Web Console 2

An operating system based utility for supported Microsoft Windows* and Linux* operating systems. This utility can monitor battery status, charge level, and the number of recharge cycles.

3.4.3 Intel® RAID Command Line Utility 2

Text-based command-line utility for Windows* and Linux* operating systems. It shows battery status and can be used to initiate a relearn.