SRSH4 Server System

Technical Product Specification

Intel reference number 10579

Revision 1.1

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Enterprise Platforms and Services Marketing

Revision History

Date	Revision Number	Modifications
6/26/01	0.5	Preliminary Draft for Review
8/20/01	1.0	Revisions to page 13 Roll to 1.0
12/18/02	1.1	Revised to include Intel® Xeon MP® processors, Adaptec 7902 U320 support, 100MHz PCI

Disclaimers

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1. Introduction

This product specification details the features of the SRSH4 server system. Low cost, time to market, modularity, and utilization for multiple configurations are primary considerations in the design. The chassis has user friendly features and is accessible and serviceable.

The SPSH4 server system also incorporates features for high availablity servers. This includes power and cooling systems with optional redundancy, hot swap or easy to replace fans hot-plug PCI slots, and a mass storage system with hot-swappable hard drives. These are the key components for increasing availability of the server. Since the fans and power supplies typically have the lowest Mean Time Between Failure (MTBF) specifications, the optional redundancy of these components will permit the system to continue to operate with a failed fan or power supply. With the use of RAID technology the system can continue to operate with hard drive failures The hot-plug hard drives allow a failed hard drive to be replaced while the system continues to operate.

This product specification details the following:

- SRSH4 chassis features.
- SSH4 Bosrdset
- Power supply subsystem.
- Chassis cooling.
- Front panel.
- System boards.
- I/O and interconnects.
- System Certifications.
- System Configuration.
- Environmental limits.
- Reliability, serviceability, and availability.

2. SRSH4 Server System Feature Overview

This chapter describes the main features of the SRSH4 server system. Table 1 below provides a list and brief description of the SRSH4 server system features utilizing the SSH4 baseboard.

Table 1: SRSH4 Server System Feature List

Feature	Description	
Compact, high-density system	Rack-mount server with a height of 4U (7 in) and a depth of 28 in.	
Configuration flexibility	Stand-alone system in a low profile, highly reliable, and cost/value effective chassis. • Up to four Intel® Xeon™ processor MP (2.0GHz) • Eight full length PCI slots (4 PCI Hot Plug, 6 PCI-X). • Two or three power supplies. • Two Ultra 160SCSI ports on a single Adaptec* 7899 controller (on 64-bit / 66 MHz PCI) on the –603 baseboard, Two Ultra320 ports on a single Adaptec*7902 controller(64-bit /66 MHz on the -704 baseboard. • Up to five 1” hot-swap Ultra-160 SCSI/Utltra-320 SCSI hard drives. • 3½” floppy drive / CD-ROM drive combo plus one 5¼ peripheral bay. • Customizable bezel. • 24 GB DDR DRAM memory support. • External I/O / disk expansion. • Built in 10/100 and G-Bit LAN controllers.	
Serviceability	System designed to maximize service access. • Tool-less design features. • Front access to hot-swap power supplies and hard disk bays. • Top access to hot-plug PCI-X and hot-swap fans. • Color coded throughout for service items. • Detailed configuration labels on the system. • Fault indicators and system UID (Unit ID) light.	
Availability	System designed to maximize availability. • Four 64bit (100MHz) PCI-X hot plug slots. • Five 1.0” hot-swap Ultra-160/ Utltra-320 disk drive bays. • Three hot-swap power supplies in a 2+1 redundant configuration. • Two AC power input cords in a 1+1 redundant configuration. • Six hot-swap system fan banks in a 5+1 redundant configuration.	
Manageability	System designed to maximize manageability. • IPMI 1.5 compliant. • WfM 2.0 compliant. • Extensive system sensors and monitoring. • Remote management and diagnostics via Serial or LAN port. • External chassis management via ICMB.	
Front panel interface	Switches: Power, Reset, NMI, Sleep, Unit ID. Ports: USB port 3, RJ45 Serial port B.	LEDs: Main power, Standby power, HDD activity/fault, LAN1 activity, LAN2 activity, General system status/fault, Unit ID.

The SRSH4 server system is a compact, high-density, rack mount server system with support for one to four Intel® Xeon™ processors MP and up to 24 GB DDR DRAM memory. The system supports several high-availability features such as hot-plug PCI-X, hot-swap AC/DC redundant power supply modules, hot-swap redundant system fans for cooling, and hot-swap hard disk drives. The scalable architecture of the SRSH4 supports symmetrical multiprocessing (SMP) and a variety of operating systems.

Figure 1 shows an isometric view of the system.

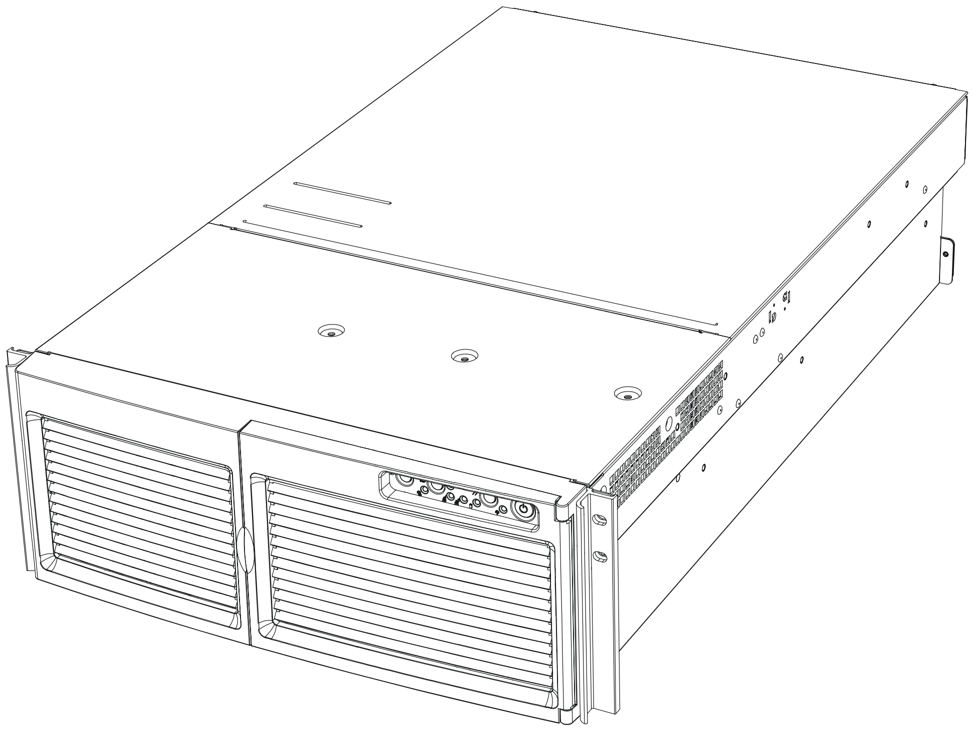

Figure 1: SRSH4 Server System

The SRSH4 server system is based on the SSH4 baseboard, processor board and memory expansion board. and the SR4000 chassis . The processor board contains sockets for installing up to four Intel® Xeon™ processors MP. The memory expansion board has 12 DIMM slots and supports up to 24 GB DDR DRAM memory. The baseboard also contains four hot plug PCI-X slots and four non-hot plug slots, I/O ports, and various controllers.

The system baseboard is mounted horizontally in a chassis subassembly called the E-bay, shown in Figure 3. The processor board mounts horizontally to the baseboard and the memory board mounts vertically to the processor board. The E-bay is mounted towards the rear of the chassis.

The hard drive bay is mounted at the right side, front of the chassis and supports five 1.0" hot-swap, Ultra-160/ Utltra-320 SCSI hard drives. SCSI drives in the hard drive bay can be hot-swapped without shutting down the server.

The peripheral bay, also located at the front of the system, contains one half-height 5¼" device bay (for a device such as a DAT) and a media bay. The media bay accommodates a slim-line (½") floppy drive and a slim-line (½") CD-ROM drive.

The front panel is located above the hard drive bay and provides user interface for system management.

The power supply bay is mounted at the left side, front of the chassis and supports up to three hswap 430 W power supply modules in a 2 + 1 DC output redundant configuration and a 1+1 AC input redundant configuration. A cover plate for an empty power module location is supplied for systems without redundancy.

Figure 2 shows the chassis with the top covers and the front bezel removed.

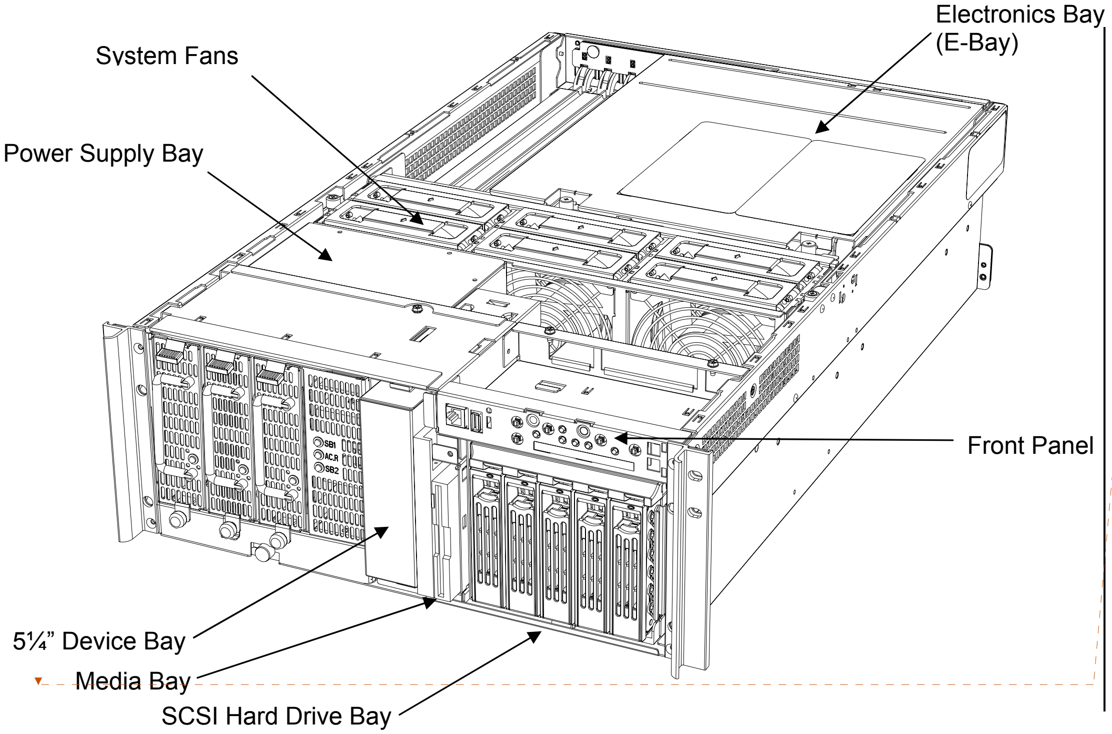

Figure 2: SRSH4 Chassis with Top Covers and Bezel Removed

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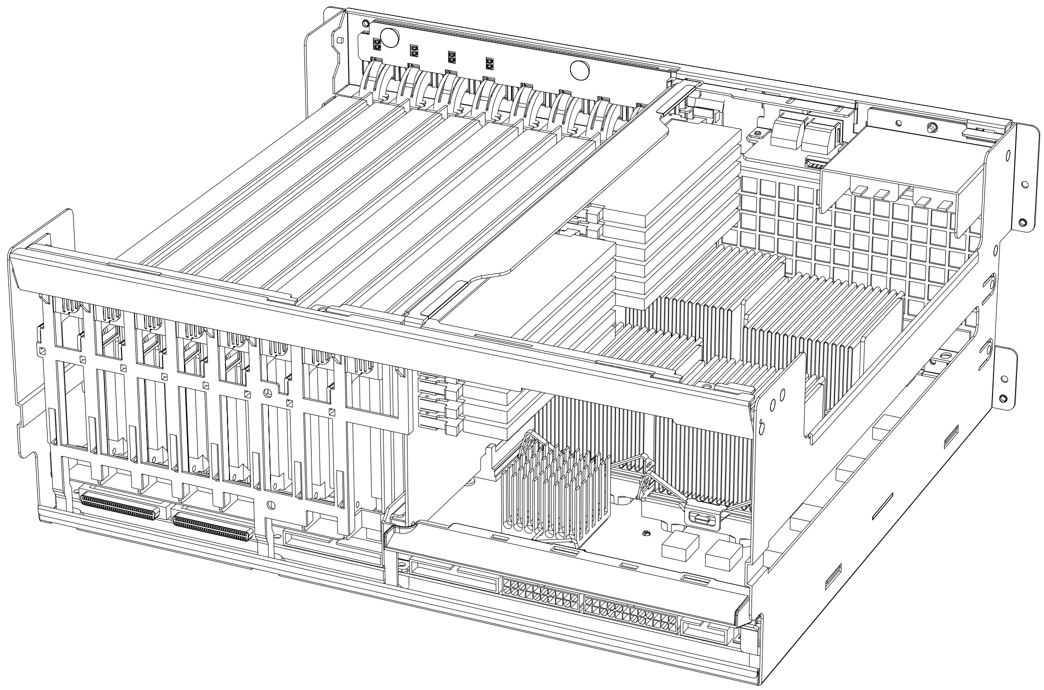

Figure 3: E-Bay Containing the SSH4 Boardset (Fully Populated)

The chassis contains six hot-swap, redundant (5 + 1) system fans to cool the baseboard and other components. The fans are installed in a bay located in front of the E-bay. Fan failure LED status indicators are located adjacent the affected fan bank and can be viewed by removing the rear top cover. A fan failure is also indicated by the general fault LED located on the front panel.

The front bezel can be customized to meet OEM industrial design requirements. The bezel design allows adequate airflow to cool the system components. It also contains a door to provide access to the peripheral devices and the hot-swap hard drives.

2.1 Front Features

2.1.1 Front View of Chassis

Figure 4 shows the chassis front view with bezel attached. The bezel has the standard color specific GE Cycoloy C6600-701 black. Figure 5 shows the same view with the front bezel removed. Opening the front bezel door provides access to the following:

- One USB and one serial port
- SCSI hard drive bay
- One 5¼" device bay
- Slim-line (½") floppy drive and a slim-line (½") CD-ROM drive

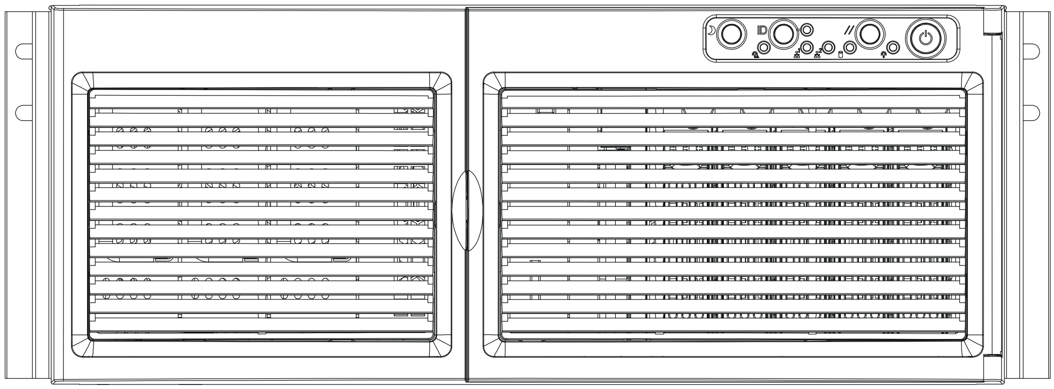

Figure 4: Front View of chassis with bezel attached

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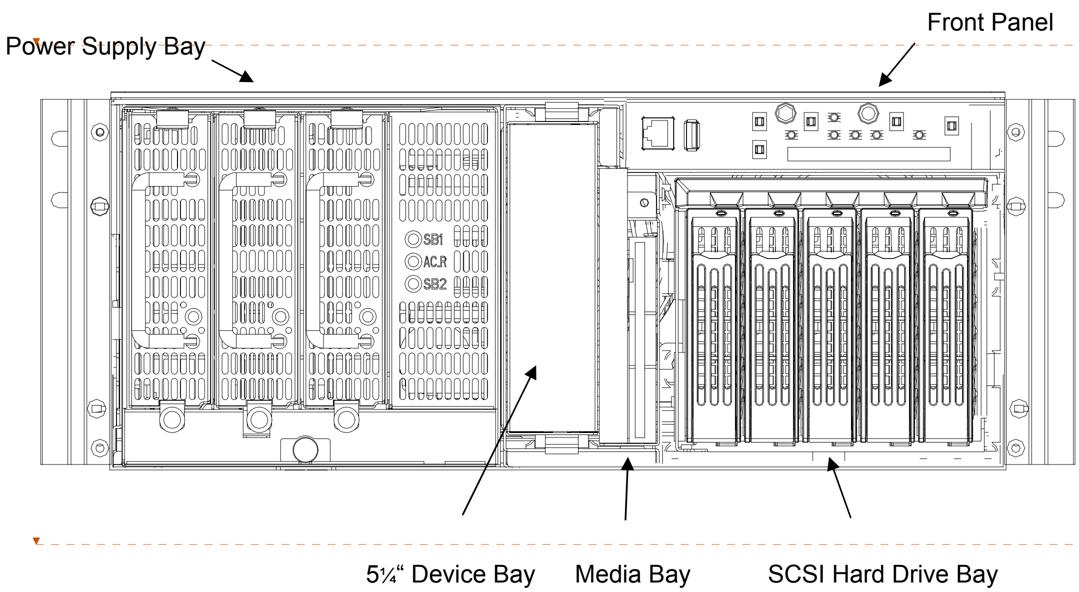

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Figure 5: Front View of Chassis (Shown with Bezel Removed)

2.2 Physical Specifications

Table 2 describes the physical specifications of the SRSH4 system.

Table 2: Physical Specifications

Specification	Value
Height	7 in (178 mm)
Width	17.5 in (445 mm)
Depth	28.0 in (711 mm)
Front clearance	3 inches (76 mm)
Side clearance	1 inches (25 mm)
Rear clearance	4.5 inches (114 mm)
Weight	57lbs (25.9 kg) minimum configuration 88lbs (39.9 kg) maximum configuration
Heat Output	3276 BTU/hr (typical)

2.2.1 Front Panel

The front panel contains system control switches and status indicators. Front panel features are shown in Figure 6 and Figure 7 and are described in Table 3.

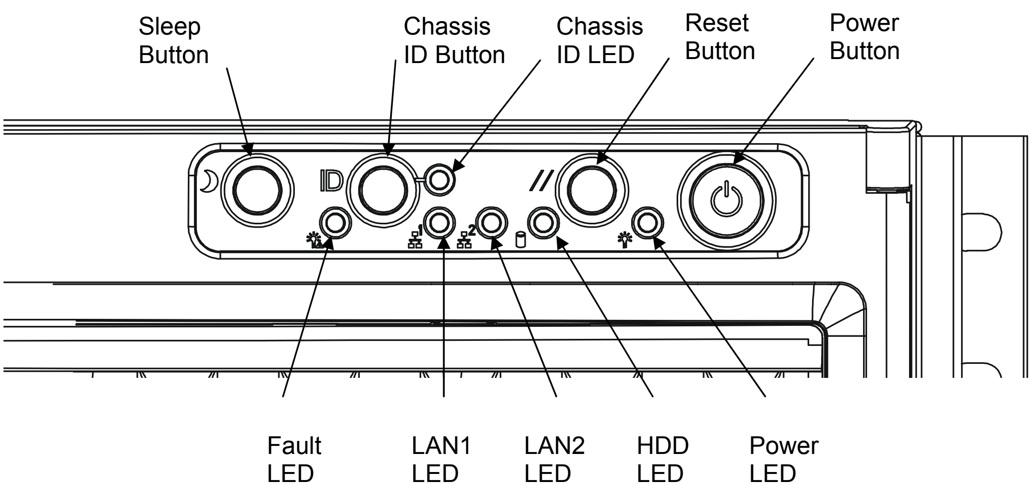

Figure 6: Front Panel Details (Bezel Door Closed)

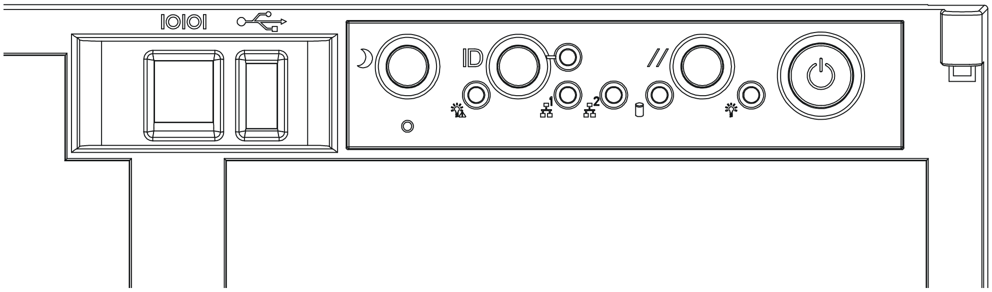

Figure 7: Front Panel Details (Bezel Door Open)

Table 3: Front Panel Features

Feature	Description
Front Panel Button	
Reset	Resets system power.
Sleep	Activates the sleep mode.
NMI *(Hidden Behind Bezel)*	Causes a non-maskable interrupt. This switch is located behind the front bezel door to prevent inadvertent activation. The front bezel door must be opened to access this switch. A narrow tool is required to activate the switch.
Power	Toggles system power.
Chassis ID	Activates the chassis LED on both the front panel board and on the baseboard at the rear panel of the chassis.
Front Panel LEDs	
Chassis ID (blue)	Indicates that matching chassis ID LED will be present at rear panel of chassis to ease identification when servicing rear of system in a rack.
Power (green)	When continuously lit, indicates the presence of DC power in the server. The LED goes out when the power is turned off or the power source is disrupted. When flashing it indicates the system is in ACPI sleep mode.
HDD Activity/Fault (green/amber)	Indicates any system hard drive activity or fault condition.
LAN1 (green)	Indicates 100/10Mb Ethernet port activity.
LAN2 (green)	Indicates 1000/100/10Mb Ethernet port activity.
System Status/Fault (green/amber)	Indicates system status or fault condition.
Front Panel IO Connectors	
USB Connector *(Hidden Behind Bezel Door)*	USB port 3.
RJ45 Connector *(Hidden Behind Bezel Door)*	Serial port B.

2.2.2 Peripheral Bay

The peripheral bay consists of the following:

- Half-height device bay for a 5¼” device such as a DAT drive
- Slim line media bay for a ½” floppy drive and ½” CD-ROM drive

2.2.3 SCSI Hard Drive Bay

The SRSH4 server system freatures one SCSI hard drive bay. This bay, shown in Figure 8, supports five 3½” wide, 1” high hot-swap Ultra-160 /Ultra-320 SCSI SCA hard disk drives. The bay is accessible by opening the front bezel door. The Ultra-160/Ultra-320 SCSI hot-swap backplane provides industry-standard 80-pin SCA-2 connectors. Ultra-160/Ultra-320 SCSI SCA type or slower hard disk drives can be installed in this bay.

The hot-swap backplane is designed to accept up to five 15k RPM hard drives that consume up to 20 W of power.

Note: This wattage number is a guideline. Thermal performance of specific hard drives must be verified to ensure compliance to the drive manufacturer specifications.

A hard drive carrier is used to mount the hard drive in the SCSI bay. The hard drive is attached to the carrier, shown in Figure 9, with four fasteners, and it is retained in the chassis by a locking handle.

An LED on each hard drive carrier displays the individual drive status. A continuously lit green LED indicates the presence of the hard drive and that drive is powered on. A flashing green LED indicates hard drive activity. A continuously lit yellow LED indicates an asserted fault status on the hard drive. A flashing yellow LED indicates that a hard drive rebuild is in progress.

When no hard drive is mounted in the carrier, an air baffle must be installed to maintain proper system airflow. See Figure 9.

This boardset consists of two boards. The SCSI backplane board provides power distribution, hard drive failure indicators, and SCSI interfacing of the hard drives. The SAF-TE board provides the SAF-TE features. Refer to Chapter 4 for detailed description of the SCSI boardset.

The hot-swap SCSI boardset performs two major functions:

- Supports hot-swapping SCSI hard drives
- Provides enclosure (chassis) monitoring and management, as specified in the *SCSI Accessed Fault-Tolerant Enclosures (SAF-TE) Specification,* Revision 1.00

The SAF-TE specified features supported by the hot-swap SCSI boardset include, but are not limited to, the following:

- Monitoring the SCSI bus for enclosure services messages, and acting on them appropriately. Examples of such messages include: Activate a drive fault indicator, Power down a drive that has failed, and Report backplane temperature
- SAF-TE intelligent agent, which acts as proxy for “dumb” I^2C devices (devices that have no bus-mastering capability) during intra-chassis communications

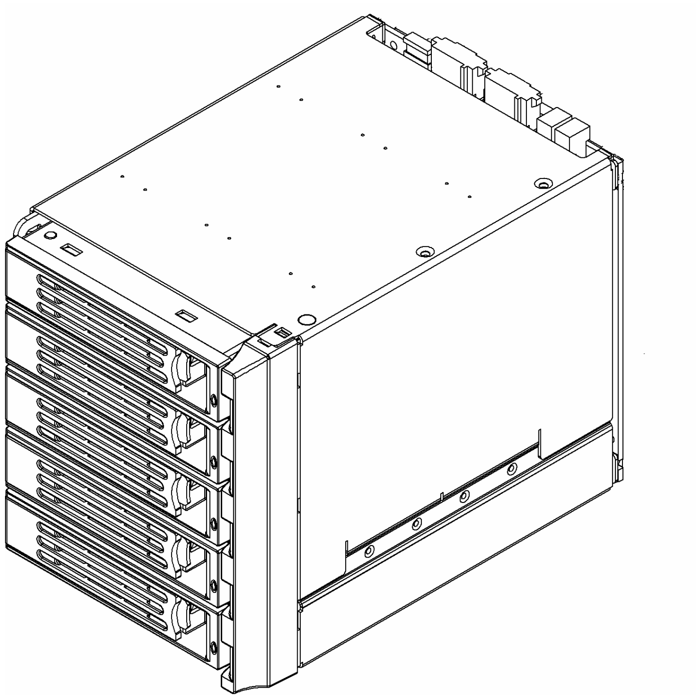

Figure 8: Hard Drive Bay

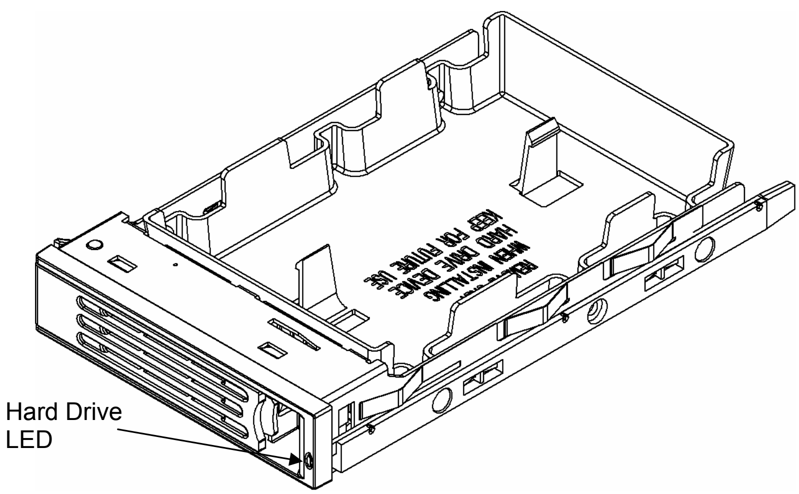

Figure 9: Hard Drive Carrier

2.3 Rear Features

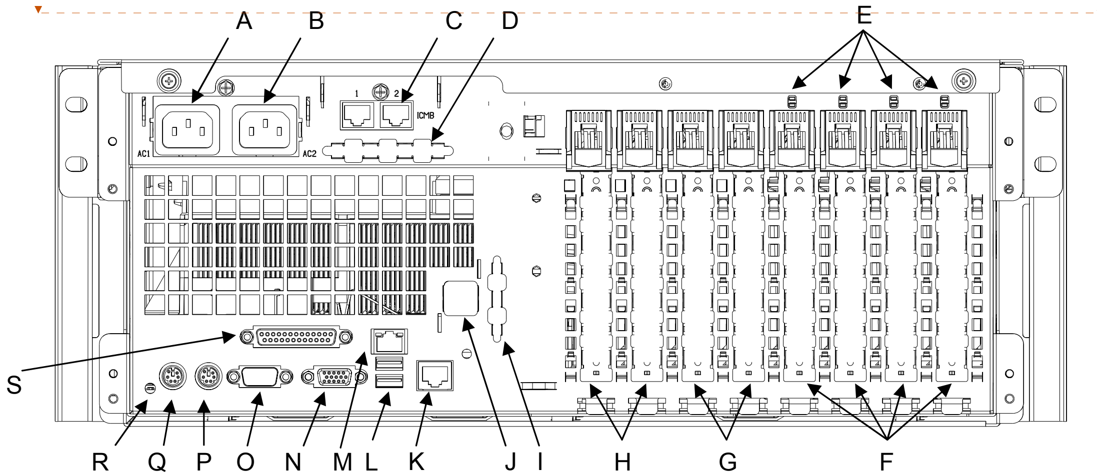

Figure 10: Rear View Of Chassis

Table 4: Rear System Features

Item	Description
A	Power supply IEC320-C14 AC Inlet 1
B	Power supply IEC320-C14 AC Inlet 2
C	Optional ICMB connector ports, keyed RJ45 8-pin connector
D	Optional External SCSI3 port
E	Hot Plug PCI-X Power/Fault LED’s
F	Four hot plug 64-bit, 100 MHz PCI-X add-in card slots
G	Two non hot plug 64-bit, 100 MHz PCI-X add-in card slots
H	Two non hot plug 32-bit, 33 MHz PCI add-in card slots
I	Optional External VHDCI SCSI port
J	Optional serial RJ45 port B
K	LAN2 1000/100/10 port
L	USB ports 0 (upper) and 1 (lower), 4-pin connectors
M	LAN1 100/10 RJ45 connector
N	Video connector
O	Serial port A, 9-pin RS-232 connector
P	PS/2-compatible mouse port, 6-pin connector
Q	PS/2-compatible keyboard port, 6-pin connector
R	Chassis ID LED
S	PS/2-compatible parallel port (LPT), 25-pin bi-directional subminiature D connector

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2.4 SSH4 Boardset

This section highlights the main features of the SSH4 baseboard. Refer to the *SSH4 Baseboard, Processor Board and Memory Module Technical Product Specification* for a detailed description of the system baseboard.

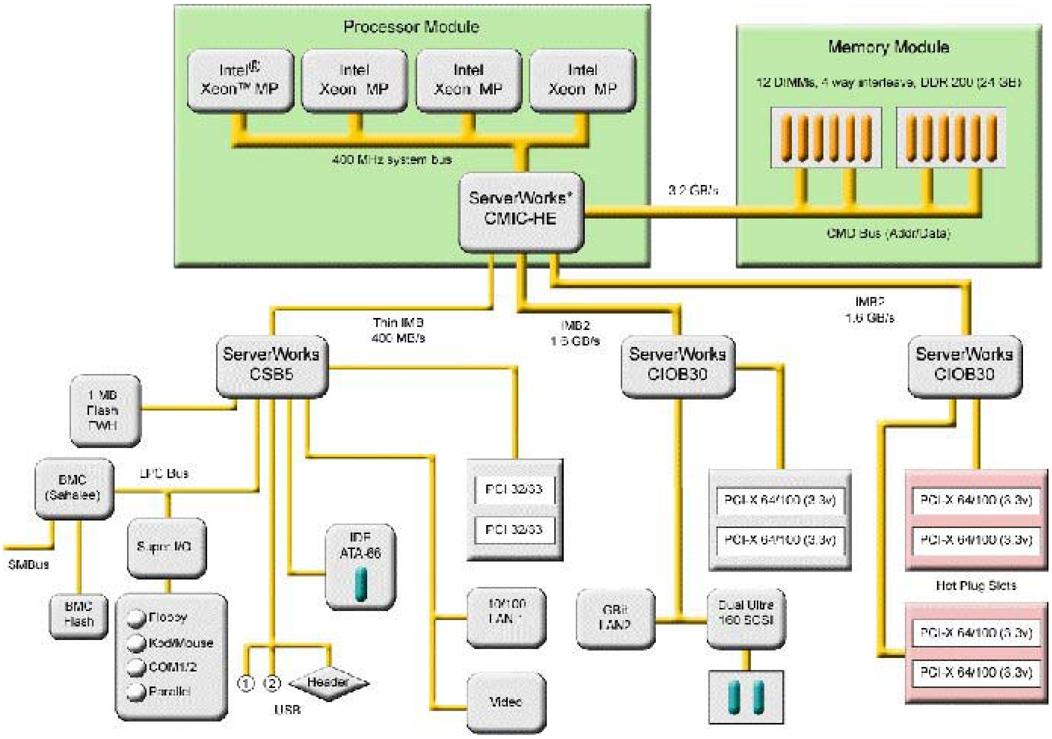

Figure 11: Functional Block Diagram of SSH4 Boardset

The SSH4 boardset is designed around the Intel®Xeon™ processor MP and the ServerWorks* ServerSet* IV Grand Champion High End (GCHE) chipset. This combination provides the basis for a high performance system with leading edge processor, memory, and I/O performance.

The SSH4 baseboard architecture supports quad processing operation using Intel Intel®Xeon™ processor MP. It also provides eight industry standard PCI expansion slots supporting a mixture of 32-bit, 33MHz (two), and 64-bit, 100/66 MHz (six) slots. The baseboard includes an array of embedded I/O devices, including:

- One SCSI controller providing two independent channels bus speeds up to 320 Mb/second

- An embedded 100/10 Ethernet Network Interface Controller
- An embedded 1000/100/10 Ethernet Network Interface Controller
- A 4 MB 2D/3D graphics accelerator
- PCI hot-plug support
- Server management and monitoring hardware

The SSH4 memory subsystem consists of a single memory expansion board. This board supports up to 24 DDR DRAM memory modules. The SSH4 baseboard implementation in SPSH4 server supports both stacked and unstacked memory modules for up to 24 GB of system memory.

The SSH4 boardset provides the following features:

- Quad Intel Intel®Xeon™ processor MP cartridge support
- Four Intel MP Xeon sockets for installation of one to four identical Intel®Xeon™ processor MP
- ServerWorks ServerSet IV Grand Champion High End (GCHE) chipset
- One CMIC-HE
- Two CIOB30
- Five REMC
- One CSB5
- Support for 12 PC200 DDR DRAM memory modules, single or stacked
- ECC single-bit correction, and multiple-bit error detection, supports the Chip Kill feature and memory scrubbing
- 32-bit, 33 MHz, 5V or 3.3V PCI segment (P32) with two expansion connectors and two embedded devices
- PCI network interface controller: 10/100 Intel® 82550 Fast Ethernet Controller
- PCI network interface controller: Gigabit Intel® 82554 Fast Ethernet Controller
- 2D/3D Graphics Accelerator: ATI* RAGE* XL Video Controller with 4 MB of video memory
- Three 64-bit, 100-MHz, 3.3V Hot-Plug PCI-X segments with six expansion connectors and three embedded devices
- IBM PCI-X Hot-Plug Controller
- Dual Channel Wide Ultra-160/Ultra-320 Adaptec* SCSI controller
- National Semiconductor* Super I/O* (PC87417) controller chip providing all PC-compatible I/O (floppy, parallel, two serial, keyboard, mouse, RTC)
- Baseboard Management Controller (BMC) providing monitoring, alerting, and logging of critical system information obtained from embedded sensors on baseboard
- 8 megabit Flash device for system BIOS
- Three externally accessible USB ports; two at rear bulkhead and one at front panel
- One IDE connector, supporting up to two ATA 66 compatible devices

2.5 Power Subsystem

This section defines the features and functionality of the switching power subsystem. The power supply modules are located in the power supply bay, which is mounted towards the front, left of the chassis. The power subsystem may be configured either with two 430 W power supply modules in a non-redundant configuration, or three 430 W power supply modules for a DC redundant power (2 + 1) configuration. Separate dual AC power cords provide AC line redundancy. Each AC input has two fuses rated at 250V/15A, one for line and one neutral. The AC inputs are not required to be on the same AC power phase. When the system is configured with three power supply modules, the following features are supported:

- The user can replace a failed power supply module without interrupting system functionality under any loading condition.
- AC power to one of the power cords can be interrupted without loss of functionality.

Power from the power subsystem is carried to internal system boards and peripheral devices via discrete cables. Two 430 W power supply modules are capable of handling the worst-case power requirements for a fully configured SRSH4 system. This includes four 75-W Intel® Xeon™ processors MP, 24 GB of memory and five hard drives at 20 W per drive.

!WARNING!
The total power requirement for the SRSH4 server system exceeds the 240VA energy hazard limit that defines an operator accessible area. Therefore, only qualified service personnel should access the processor, memory, and non-hot plug I/O areas on the system baseboard while the system is connected to a power supply.

The following are the main features of the power subsystem:

- 800 W output capability in full AC input voltage range
- Three 430 Watt PFC power supply modules
- Power good indication LEDs
- Predictive failure warning
- External cooling fans with multi-speed capability
- Remote sense of 3.3 V, 5 V, and 12 V outputs
- AC_OK circuitry for brown out protection
- Built-in load sharing capability
- Built-in overloading protection capability
- On board field replaceable unit (FRU) information
- I^2C interface for server management functions
- Integral handle for insertion/extraction
- Dual power cords for AC redundancy

The power modules are populated in a specific order as viewed from the front of the system.

- The first module is installed into the left-most bay (labeled PS1/AC1)
- The second module is installed into the right most bay (labeled PS2/AC2)
- The third module is installed into the center shared bay (labeled PS_SHARE)

Power modules are easily installed with use of blind mating connectors.

The power supply sub-system has four externally enabled outputs (+12V,+5V,+3.3V,-12V), and one +5VSB (standby) output. The +5VSB standby output is present whenever AC power is applied and either PS1 or PS2 are installed.

When the green LED on each of the power supply modules is lit, it indicates AC power is applied and the power module is functioning properly. Three green LEDs are on the power supply cage. Two +5VSB power green LEDs, labeled SB1 and SB2, are lit when +5VSB power is present. The third green LED, labeled AC_R, is lit when the center power module is installed and the AC transfer switch is functioning properly.

A Power LED is also located on the front panel. It is labeled PWR and is green when power is applied to the system.

When the power module configuration changes, the SDR utility must be rerun so that server management will properly monitor this new configuration.

2.5.1 Mechanical Dimensions

Mechanical drawings and dimensions, in millimeters, for the power cage are shown in Figure 12 and for the power module in Figure 13.

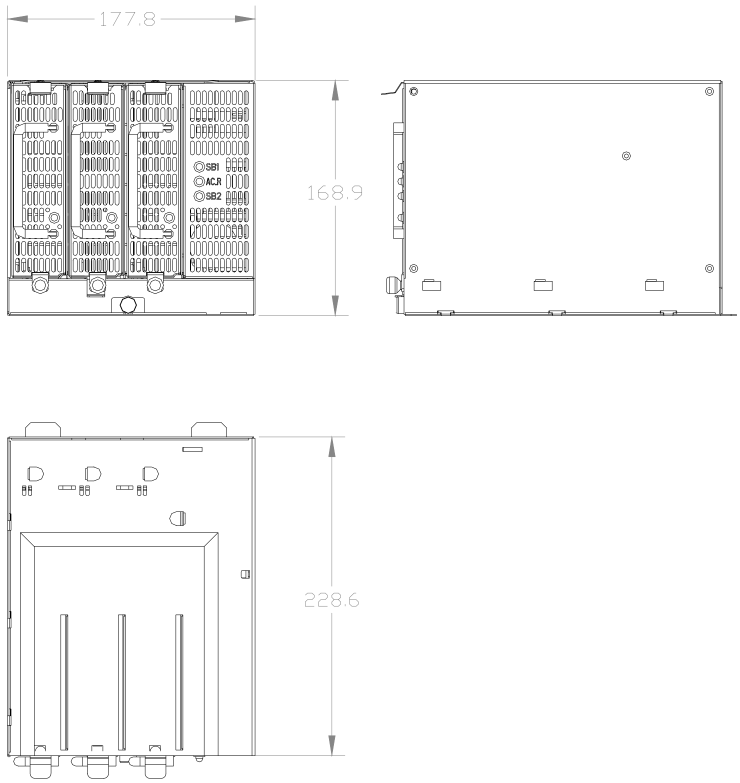

Figure 12: Power Subsystem Enclosure Outline Drawing

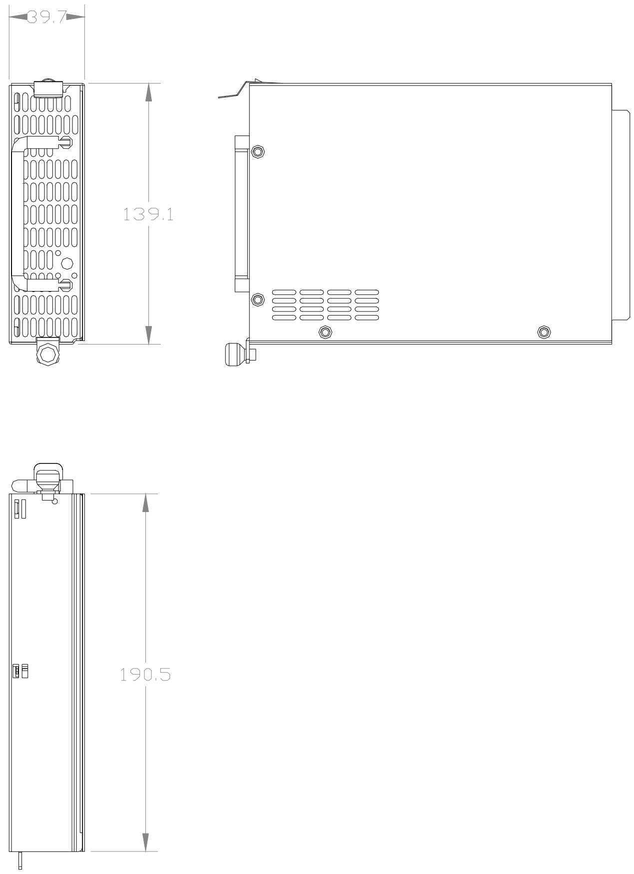

Figure 13: Power Supply Module Enclosure Outline Drawing

2.5.2 Airflow Requirements

The system fans provide airflow to the power supplies. Air enters the power subassembly from the front of the chassis, flows through the power subassembly, and exits at the rear. Air entering the power subassembly should be between 5°C and 35°C, and can have a temperature rise of 25°C when exiting the power subassembly. Air exiting the power subassembly will generally flow through the PCI adaptor area of the E-bay.

The amount of airflow provided to the power subsystem will vary depending upon the number of power supplies installed and the number of fans installed. The airflow volumes supplied to the power subassembly are shown in Table 5.

Table 5: Power Subsystem Airflow Requirements

	Power Supplies Installed	
Fans Installed	3	2
6	> 58	
5 (6 installed, with one failed)		> 46
3		> 43

2.5.3 Over-Temperature Protection

The power subsystem is protected by Over Temperature Protection (OTP) circuits. The power subsystem sends an alert for an OTP condition to the system via the I^2C bus and turns off the corresponding power subsystem LED for either the power module or standby power.

If a specific power module exceeds the thermal limits, that module will not supply DC power to the system with the exception of the +5VSB power (for PS1 and PS2). If an over-temperature condition is detected in the +5VSB section of the power subassembly, all DC power to the system will be removed, including the +5VSB power. When temperatures read by the sensors return to normal operating range, DC power supplied by either the power module or power subsystem is restored. To prevent power from cycling through on/off/on conditions a 5°C hysteresis (margin) is implemented.

2.5.4 Connectors and Pinouts

2.5.4.1 AC Inlet

The AC power pins and wiring prior to the protective fuse(s) have a peak current rating higher than the peak inrush current or maximum fault current drawn by the power subsystem. The safety ground pin of the power supply module is the first pin to connect and the last to disconnect when the module is inserted or removed from the power subsystem housing. The area near the AC inlet is service-only access and protected with one level of protection – shrink insulation wrap on the bare parts.

2.5.4.2 DC Output Connectors

The power subsystem has a wire harness that provides the interface for all signals from the power subsystem to the server system. The voltage supply rails provided are +5VSB, -12V, +12V, +5V, and +3.3V. In addition, connector pins are provided for the following signals:

- +3.3V remote sense
- +5V remote sense
- +12V remote sense
- Remote sense return
- Power Subsystem On (DC power enable)
- Power Good
- I^2C (Monitoring of PS Failure, PS Presence, PS Predictive Fail, +12V, +5V, 5VSB, and PS redundancy)

2.5.4.2.1 P1 Main Power Connector

Housing: 24 Pin Molex* 39-01-2240
Contact: Molex 39-00-0038
Harness length: 340mm(13.4") from rear of housing

Table 6: P1 Connector Pin Assignments

Pin	Signal	18 AWG COLOR	Pin	Signal	18 AWG COLOR
1	+3.3V	Orange	13	+3.3V	Orange
2	+3.3V	Orange	14	+3.3V	Orange
3	+3.3V	Orange	15	+3.3V	Orange
4	GND	Black	16	GND	Black
5	GND	Black	17	GND	Black
6	GND	Black	18	GND	Black
7	GND	Black	19	GND	Black
8	GND	Black	20	GND	Black
9	+12V	Yellow	21	+12V	Yellow
10	+12V	Yellow	22	+12V	Yellow
11	+12V	Yellow	23	+12V	Yellow
12	+12V	Yellow	24	+12V	Yellow

2.5.4.2.2 P2 AUX Power Connector

Housing: Amp 102387-2
Contact: Amp 87809-1
Harness length: 360mm(14.2") from rear of Housing

Table 7: P2 Connector Pin Assignments

Pin	Signal	24 AWG COLOR	Pin	Signal	24 AWG COLOR
1	GND	Black	2	+5VRS	Red
3	+3.3VRS	Orange	4	Fan Speed Input*	Brown
5	I2C-SCL	Brown/White stripe	6	I2C-SDA	Green/White stripe
7	GND	Black	8	PS-GOOD	Gray
9	PS-ON	Green	10	GND	Black
11	-12V	Blue	12	No connection	No connection
13	+12VRS	Yellow	14	Remote Sense Return	Black

2.5.4.2.3 P3 Main Power Connector

Housing: 20 Pin Molex 39-01-2200
Contact: Molex 39-00-0038
Harness length: 260mm(10.3”) from rear of housing

Table 8: P3 Connector Pin Assignments

Pin	Signal	18 AWG COLOR	Pin	Signal	18 AWG COLOR
1	+12 V	Yellow	11	+5 VSB	Purple
2	GND	Black	12	GND	Black
3	GND	Black	13	GND	Black
4	GND	Black	14	GND	Black
5	GND	Black	15	GND	Black
6	+5 V	Red	16	+5 V	Red
7	+5 V	Red	17	+5 V	Red
8	+5 V	Red	18	+5 V	Red
9	+5 V	Red	19	+5 V	Red
10	+5 V	Red	20	+5 V	Red

2.5.4.2.4 P4 Floppy Power Connector

Housing: Amp 171822-4
Contact: Amp 170262-1
Harness length: 200mm(7.9”) from P5

Table 9: P4 Connector Pin Assignments

PIN	SIGNAL	22 AWG COLOR
1	+5 V	Red
2	GND	Black
3	GND	Black
4	+12V	Yellow

2.5.4.2.5 P9 CD-ROM Power Connector

Housing: Honda-Tushin* HKP-8F02
Key: Honda-Tushin HKP-44F201
Harness length: 185mm(7.3") from P5

Table 10: P9 Connector Pin Assignments

PIN	SIGNAL	22 AWG COLOR	PIN	SIGNAL	22 AWG COLOR
1	No connection	-	2	+5V	Red
3	No connection	-	4	GND	Black
5	No connection	-	6	No connection	-
7	No connection	-	8	No connection	Keying Plug

2.5.4.2.6 P5-P7 Peripheral Power Connector

Housing: Amp 1-480424-0
Contact: Amp 61117-1
Harness length P5: 275mm(10.8") from rear of housing
Harness length P6 and P7: 265mm(10.4") from rear of housing

Table 11: P5-P7 Connectors Pin Assignments

Pin	Signal	18 AWG COLOR
1	+12V	Yellow
2	GND	Black
3	GND	Black
4	+5 V	Red

2.5.4.2.7 P8 FAN Power Connector

Housing: 6 Pin Molex 39-01-2060
Contact: Molex 39-00-0038
Harness length: 290mm(11.4") from rear of housing
Note: All wires are UL1007 rated: 90°C, 300V or Intel approved equivalent.

Table 12: P8 Connector Pin Assignments

Pin	Signal	18 AWG COLOR	Pin	Signal	18 AWG COLOR
1	+12V	Yellow	4	+12V	Yellow
2	No connection	-	5	No connection	-
3	GND	Black	6	GND	Black

2.5.4.2.8 AC Power Cords

Cord Inlet: 15A Delta Snap-In IEC Connector (P/N 15GENG3E)

Harness length: 1000mm(39.4”) from rear of Housing

Note: All AC wires are 600V, 105 Celsius, VW-1 or better flammability rating

Table 13: AC Distribution Cord Wiring

PIN	Signal	16 AWG COLOR
G	Earth	Green/yellow stripe
N	Neutral	Light Blue
L	Line	Brown

2.5.5 AC Electrical Specifications

2.5.5.1 AC / DC Supply Redundancy

The power supply subsystem has two AC inlets, AC1 and AC2. AC1 is connected to the inputs of power module PS1/AC1 (left-most module). AC2 is connected to the inputs of power module PS2/AC2 (right-most module). The third shared power module PS_SHARE (center module) is usually connected to AC2 through a normally closed transfer switch. Each AC input is fully isolated. Therefore, the power supply subsystem is not subject to AC phase differential issues.

The +5VSB power is supplied by two of the power modules, PS1 and PS2. Most of the circuitry for +5VSB is contained in the power subsystem cage. PS_SHARE does not provide +5VSB power. As long as a functional power module is installed in PS1 or PS 2, and the +5VSB circuitry of the power subsystem is functional, the system will have +5VSB available. The SB1 and SB2 LEDs on the power subsystem indicate the presence of +5VSB from the respective power modules.

2.5.5.2 AC Transfer Switch

The power supply subsystem provides AC/DC redundancy when three power modules are installed in a system. The center PS_SHARE power module can receive AC input from either AC1 or AC2. Normally, AC1 supplies PS1 and AC2 supplies PS2 and PS Share. If AC1 fails, AC supply is uninterrupted to PS2 and PS_SHARE. If AC2 fails the AC transfer switch changes the supply for PS_SHARE to AC1. In this condition, AC1 supplies PS1 and PS_SHARE. When AC2 is restored, the transfer switch changes the supply for PS_SHARE back to AC2.

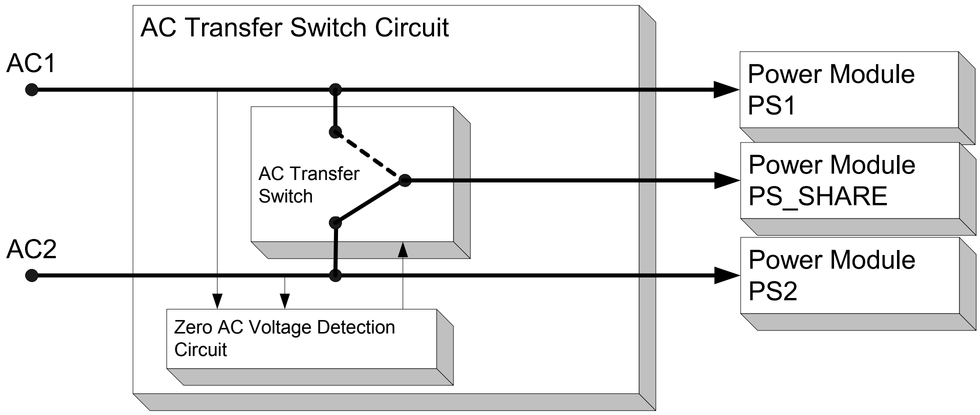

Figure 14: AC Transfer Switch Circuit

Table 14: Power Module Operation Modes

Power Module	AC1 / AC2 Input Voltage		
	OK / OK	OK / FAIL	FAIL / OK
PS1	Operational	Operational	Non-Operational
PS2	Operational	Non-Operational	Operational
PS_SHARE	Operational	Operational	Operational

2.5.5.3 AC Input Voltage Ranges

The nominal input voltage ranges specified in AC Volts RMS are 100, 120, 208, 220 and 240Vac. The power subsystem incorporates a universal power input with active power factor correction, which reduces line harmonics in accordance with EN61000-3-2 and JEIDA MITI standards. The ratings are marked on the power supply labels as referenced in Table 15.

Table 15: Input Voltage Requirements

Parameter	Min	Nom	Max	Max Input Current
Vin (115)	90 V_{rms}	100-120 V_{rms}	132 V_{rms}	15 A_{rms}
Vin (230)	180 V_{rms}	200-240 V_{rms}	264 V_{rms}	7.5 A_{rms}
Vin Frequency	47Hz	50/60 Hz	63 Hz	-

2.5.5.4 AC Line Dropout and Hold-up Time

AC line dropout occurs when the AC line input to the power subsystem drops to 0 Volts.

When all three power modules are installed and functional, an AC line dropout less than or equal to one complete cycle at AC input frequency (i.e. 20 milliseconds at 50Hz) will not cause any adverse affect on system operation and will not cause any out of regulation conditions such as overshoot or undershoot. In addition, there is no notification to the system (i.e. Power Good does not go low) that an AC line dropout occurred.

When a power supply module fails and the power subsystem is not in the redundant mode (three power modules installed), it will not meet this requirement. This requirement does not apply during mean time to repair (MTTR), when the failed power supply module will be replaced.

Any AC dropout transients in excess of one complete cycle at AC input frequency (i.e. 20 milliseconds) may cause shutdown of the power subsystem or out of regulation conditions, but will not cause a latch off condition or damage to the power subsystem.

2.5.5.5 AC Line Transient Specification

AC line transient conditions are defined as “Sag” and “Surge” conditions. Sag (also referred to as a “brownout”) condition is defined as the AC line voltage dropping below the nominal voltage. Surge is defined as a condition when the AC line voltage rises above the nominal voltage. The power subsystem meets the performance requirements of the AC line sag and surge conditions described below.

AC Line Sag Transient Performance

Duration	Sag	Operating AC Voltage	Line Frequency	Performance Criteria
0 to 15 minutes	15% 97.75V	Mid-point of Rated AC Voltages 115 / 220 Vac	50/60Hz	No loss of function or performance
0 to ½ AC cycle	30% 80.5V	Mid-point of Rated AC Voltages 115 / 220 Vac	50/60Hz	No loss of function or performance
0 to 5 AC cycles	50% 57.5V	Mid-point of Rated AC Voltages 115 / 220 Vac	50/60Hz	Loss of system functionality acceptable, self recoverable

AC Line Surge Transient Performance

Duration	Surge	Operating AC Voltage	Line	Performance Criteria

			Frequency	
0 to 15 minutes	15% 253 V	Mid-point of Rated AC Voltages 115 / 220 Vac	50/60Hz	No loss of function or performance
0 to ½ AC cycle	30% 286 V	Mid-point of Rated AC Voltages 115 / 220 Vac	50/60Hz	No loss of function or performance

2.5.5.6 Susceptibility

The power subsystem complies with the limits defined in *EN50082-2* while maintaining normal performance within the specification limits.

Electrostatic Discharge, IEC 801-2/IEC 1000-4-2

Level	Test Voltage, Contact Discharge	Test Voltage, Air Discharge
3	8Kv	15Kv

Electrical Fast Transient/Burst, IEC 801-4/IEC 1000-4-4

Level	AC Inlet
3	1Kv

Radiated Immunity [1], IEC 801-3/IEC1000-4-3

Field Strength	Frequency Range	Step Size	Modulation
5V/meter	26MHz to 500MHz	1% of previous frequency	None

Note:

1. *CISPR 24/IEC 61000-4-3* requires 80MHz to 1000MHz, 3V/m, 80% AN (1kHz)

Conducted Immunity, IEC 61000-4-6

Field Strength	Frequency Range	Step Size	Modulation
3V/meter	0.15MHZ to 80MHz	1kHz	80% AM

2.5.5.7 Surge Immunity

In addition to complying with *EN50082-2 for Surge Immunity*, the power subsystem also complies with *ANSI C62.45-1992*. The *Intel Environmental Standards Handbook* describes the test methods and levels used during Intel system qualification testing for surge withstand capability.

Surge Immunity IEC 1000-4-5

Level	Open Circuit Voltage	Minimum time between Surges
3	2.0Kv ± 10%	20 sec

Ring Wave

Open Circuit Voltage	Minimum time between Surges
3.0Kv ± 10%	20 sec

2.5.5.8 AC Line Inrush

The AC line inrush current of one power supply module does not exceed I^2t fuse rating when the power subsystem is turned on at the 90 degree phase point of a 264Vac line input.

2.5.5.9 Dielectric Strength Requirements

The power supply module and the power subsystem meet all safety agency requirements for dielectric strength.

2.5.5.10 AC Line Fuse

The LINE and NEUTRAL AC inputs are fused. AC line fusing is acceptable for all safety agency requirements.

2.5.5.11 Power Factor Correction

The power supply modules incorporate Power Factor Correction circuits.

The power subsystem was tested in accordance with *EN 61000-3-2: Electromagnetic Compatibility (EMC) Part 3: Limits- Section 2: Limits for harmonic current emissions*, and meets the harmonic current emissions limits specified for ITE equipment.

The power subsystem was tested in accordance with *JEIDA MITI Guideline for Suppression of High Harmonics in Appliances and General-Use Equipment* and meets the harmonic current emissions limits specified for ITE equipment.

2.5.6 DC Output Specifications

The system is operationally supported with either two or three power modules installed in the power subsystem. The power modules operate with their outputs directly paralleled inside the power subsystem. The power supply modules equally share the total load currents within the limits specified. Equal power sharing of paralleled power supply modules is required to prevent life shortening stress concentration in individual power supply modules. Power sharing is accomplished by actively matching the output currents on the high power outputs. The Current Sharing load deviation is defined as:

```
Load_Deviation = [(Actual_Load – Mean_ Load)/(Mean Load)] * 100%
```

The +3.3V, +5V, and +12V output currents of paralleled modules maintain a maximum Load Deviation of ± 10% at max rated current. At one-half of the rated current, the maximum Load Deviation is ± 20%. At less than one-half of the rated current, the maximum Load deviation can be greater than ± 20%.

With a redundant power module configuration (2+1), failure of a power module or removal (hot swap) of a power module does not cause DC output transients in excess of the limits specified. Adding an operational power supply module to the power subsystem or extracting a power supply module from the power subsystem does not cause DC output transients in excess of the limits specified. Power module hot swap is not supported with two or less power module configurations.

The power subsystem has a minimum efficiency of 64% to its DC output pins at maximum load currents and at rated nominal input voltages and frequencies per Table 15. The four externally enabled outputs have the ratings shown in Table 16.

Table 16: DC Output Ratings

Power Supply Module	Power Subsystem
+3.3V at 16 A [1]	+3.3V at 31A [2]
+5V at 18 A [1]	+5V at 34 A [2]
+12V at 26 A with 30A/10ms peak [3]	+12V at 49 A with 60A/10ms peak [4]
-12V at 0.5A	-12V at 0.5A

Notes:

1. The total combined output power of the +3.3 and +5V channels shall not exceed 120W
2. The total combined output power of the +3.3 and +5V channels shall not exceed 230W
3. The total combined output power of the +3.3, +5V and +12V channels shall not exceed 430W
4. The total combined output power of the +3.3, +5V and +12V channels shall not exceed 800W

Maximum current drawn on the +12V output from power subsystem shall not exceed 60 A for greater than 10 seconds. The steady state voltage limits and DC output currents of the power subsystem are specified in Table 17 and Table 18.

Table 17: Steady State DC Output Voltage Limits

Parameter	Min	Max	Units	Tolerance
+3.3V	+3.201	+3.43	V	-3%, + 4%
+5V	+4.80	+5.20	V	-4% + 4%
+12V	+11.52	+12.60	V	-4% + 5%
-12V	-11.40	-12.60	V	± 5%
+5VSB	+4.75	+5.25	V	-4% + 5%

Table 18: DC Load Range

Voltage	Total Power Subsystem load condition (2 and 3 modules configuration)		
	Minimum Continuous	Maximum Continuous	Peak
+3.3V	1.0 A	31 A	
+5V	1.0 A	34 A	
+12V	0A	49 A	60 A peak
-12V	0 A	0.5 A	
+5VSB	0.1A	2.0 A	

Table 19: Sleep Mode DC Load Range

Voltage	Total Power Subsystem load condition, A					
	S1		S4 (SdBy)		S5 (SdBy)	
	min	max	min	max	Min	max
+3.3V	6.6	6.6	0	0	0	0
+5V	2.1	4.98	0	0	0	0
+12V	2.35	3.55	0	0	0	0
-12V	0.2	0.2	0	0	0	0
+5VSB	0.05	2.0	0	2.0	0	2.0

Table 20: Absolute Worst Case System Power Budget

Subsystem	Qty	+5V	+3.3V	+12V	-12V	+5VSB	Total(W)
Board Set	1	4.36	10.76	1.15	0.01	0.38	73.13
CPU	4			30.85			370.20
DDR DRAM	12		1.97	6.10			79.70
FAN	6			5.00			60.00
HDD	5	5.50		4.50			81.50
CD-ROM	1	0.40					2.00
FDD	1	0.24					1.20
5" Device	1	0.77		0.40			8.65

Subsystem	Qty	+5V	+3.3V	+12V	-12V	+5VSB	Total(W)
PCI-X (64bit/100MHz)	6	9.00	13.64			0.31	91.56
PCI (32bit/33MHz)	2	6.00				0.03	30.15
System Total		26.27	26.37	48.00	0.01	0.72	798.09
Power Subsystem Spec		34.00	31.00	49.00	0.50	2.00	800.00
Margin		7.73	4.63	1.00	0.49	1.28	1.91

2.5.6.1 Remote Sense

The power subsystem has remote sense on the +3.3V, +5V, and +12V outputs and their common DC return to provide regulation at those remote points. In the event of an open remote sense line, the power subsystem maintains local sense regulation. In the event of an open DC power line or shorted remote sense line, the power subsystem will not be damaged. The remote sense is capable of regulating out the drops shown in Table 21 while still meeting the regulation requirements.

Table 21: Remote Sense Drops

Output	Max Drops	Units
+3.3V	200	mV
+5V	250	mV
+12V	300	mV
Remote Sense return	200	mV

2.5.6.2 DC and Transient Load Output Voltage Limit

The power subsystem maintains regulation under all specified conditions including parallel operation of 2 and 3 power supply modules, line variations, load variations, transient load conditions, peak ripple/noise, maximum remote sense drops, and temperature change. The +3.3V, +5V, and +12V output voltages are measured at their respective remote sense points. The output voltages stay within the regulation requirements with the remote sense regulating out the maximum drops shown in Table 21.

2.5.6.3 Ripple and Noise

Ripple and noise are defined as periodic or random signals over the frequency band of 10 Hz to 20 MHz. The power subsystem DC output ripple and noise will not exceed the values shown in Table 22. Ripple and noise are measured at minimum and maximum load with 10μF electrolytic and 0.1μF low ESR ceramic capacitors connected to the power subsystem output. The test set-up is shown in Figure 15

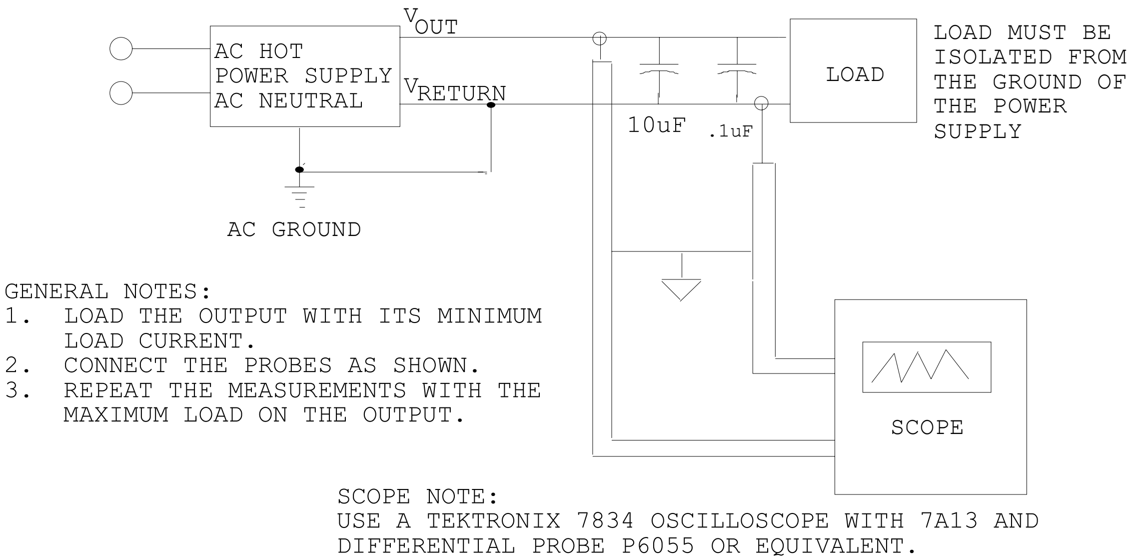

Figure 15: Differential Noise Test Setup

Note: When performing this test, the probe clips and capacitors should be located close to the load.

Table 22: Ripple and Noise

Voltage	Ripple/Noise pk-pk	Ripple/Noise pk-pk
+3.3V	1.5%	50 mV
+5V	1%	50 mV
+12V	1%	120 mV
-12V	1%	120 mV
++5VSB	1%	50 mV

Note: The combination of setpoint limits, line/load regulation and ripple/noise cannot exceed the DC output voltage limits specified in Table 17.

2.5.6.4 Power Timing

The DC output voltages rise from 10% to within regulation limits (T_{vout_rise}) within 5 to 200ms. The +3.3V, +5V and +12V output voltages start to rise approximately at the same time. All outputs rise monotonically. Each output voltage reaches regulation within 100ms (T_{vout_on}) of each other and begin to turn off within 100ms (T_{vout_on}) of each other (refer to Figure 16). Figure 17 shows the timing requirements for a single power supply being turned on and off via the AC input, with PSON held low and the PSON signal, with the AC input applied. The AC_OK# signal is not being used to enable the turn on timing of the power supply.

Table 23: Output Voltage Timing

Item	Description	Min	Max	Units
T_{vout_rise}	Output voltage rise time from each main output.	5	200	msec
T_{vout_on}	All main outputs must be within regulation of each other within this time.		100	msec

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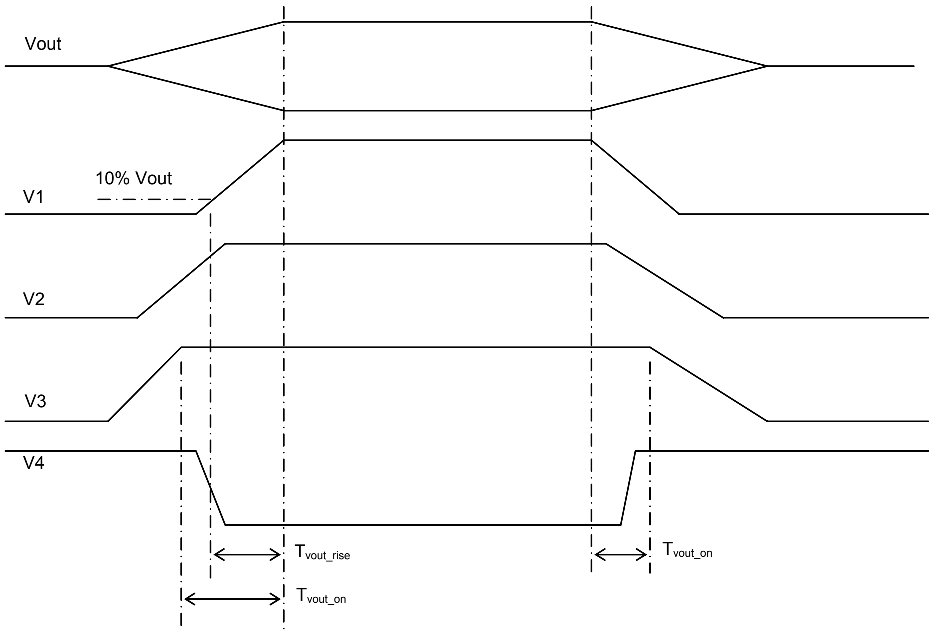

Figure 16: Output Voltage Timing

Table 24: Turn On/Off Timing

Item	Description	Min	Max	Units
$T_{sb\_on\_delay}$	Delay from AC being applied to 5VSB being within regulation.		1500	msec
$T_{ac\_on\_delay}$	Delay from AC being applied to all output voltages being within regulation.		2500	msec
T_{vout_holdup}	Time all output voltages, including 5VSB, stay within regulation after loss of AC.	21		msec
T_{pwok_holdup}	Delay from loss of AC to deassertion of PWOK	20		msec
$T_{pson\_on\_delay}$	Delay from PSON# active to output voltages within regulation limits.	5	400	msec
T_{pson_pwok}	Delay from PSON# deactive to PWOK being deasserted.		50	msec
T_{acok_delay}	Delay from loss of AC input to deassertion of ACOK#.	20		msec
T_{pwok_on}	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	1000	msec
T_{pwok_off}	Delay from PWOK deasserted to output voltages (3.3V, 5V, 12V, -12V, 5VSB) dropping out of regulation limits.	1	200	msec
T_{pwok_low}	Duration of PWOK being in the deasserted state during an off/on cycle using AC or the PSON signal.	100		msec

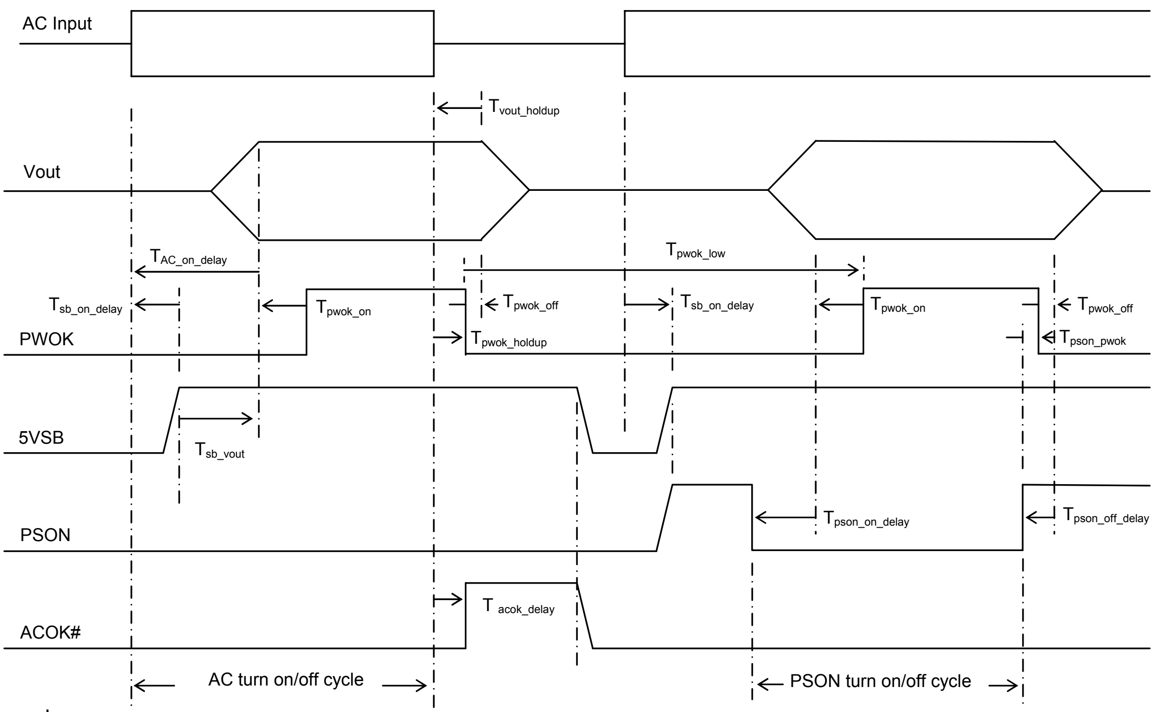

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Figure 17: Turn On/Off Timing

2.5.6.5 Turn-on Delay and Rise Time

Output voltages reach their nominal ranges within 1.5 seconds after the Power Subsystem On signal is asserted. The three main output voltages and –12V rise from 10% to within regulation limits within a minimum of 5 ms and a maximum of 350 ms measured at full load range on each output. The +3.3V, +5V, +12V and -12V output voltages are within their respective regulation band within 100 ms of each other. The 3.3V output is not be delayed from the +5V output.

2.5.6.6 Turn-off Delay

The DC outputs drop below 80% of nominal voltage within 2 seconds and below 20% of nominal voltage within 10 seconds after receipt of the turn-off Power Supply On signal level. A minimum of 100 ms power down time is required. The power down time is defined as the time the power subsystem must be powered down before being powered back up again.

2.5.6.7 Over Voltage Protection

The power supply module over voltage protection is locally sensed. The power subsystem shuts down and latches in off mode after an over voltage condition. This latch can be cleared by toggling Power Subsystem On signal or by an AC power interruption of greater than 1 second. The following Table 25 contains the over voltage limits as measured at the output of the power subsystem connector.

Table 25: Over Voltage Protection

Output Voltage	Protection Point [V]
+3.3 V	3.8 -- 4.5
+5 V	6.0 -- 6.5
+12 V	13.5 – 15

Overshoot at turn-on is less than 10%. All outputs have an increasing monotonic turn on until reaching regulation limits, after which there may be an overshoot of less than 10% above the output nominal voltage.

2.5.6.8 Over Current Protection

The power subsystem has current limit protection to prevent the +3.3V, +5V, and +12V outputs from exceeding the values shown in Table 26. Other outputs are short circuit protected. The PS may latch off without any time delay if the 5VsdBy or –12V outputs are overloaded or shorted to ground. The latch can be cleared by toggling Power Supply On signal or by an AC power interruption of greater than 1 second.

Table 26: Over Current Protection

Voltage	Over-current Limit [1]
+3.3V	34 A minimum; 38A maximum
+5V	38 A minimum; 42 A maximum
+12V	55 A minimum; 58 A maximum

Note:

1. The limits above do not depend on the number of the power supply modules in the power subsystem.

2.5.7 Control Signals

2.5.7.1 Power Subsystem On (DC Power Enable) Signal (Input)

The Power Subsystem On circuit is Safety Extra Low Voltage (SELV). Upon receiving a logic LOW at this signal, the power subsystem is turned on and power outputs and other signals are provided at the corresponding DC connector output pins.

A logic HIGH on this pin at the DC connector will turn the power subsystem off. The normal turn off delay and shut down sequence described in Section 2.5.6.4 are followed when the Power Subsystem On signal is used to turn the power subsystem off.

The characteristics of the Power Subsystem On signal are shown in Table 27. The Power Subsystem On is an input signal to the power subsystem from the system.

Table 27: Power Subsystem On Signal Specification

DC Power Enable Signal	Voltage Level [1]	Current
HIGH, PWR SUPPLY DISABLED	2 V min	0.5mA max source current
LOW, PWR SUPPLY ENABLED	1 V max or open circuit	

Note:

1. Measured relative to the power subsystem DC common output ground pins.

2.5.7.2 Power Good (Output)

The power subsystem provides a Power Good signal. This signal indicates that all outputs have reached acceptable operating voltage. The Power Good signal levels and souring/sinking requirements are described in Table 28. The Power Good is an output signal from the power subsystem to the system.

Table 28: Power Good Signal

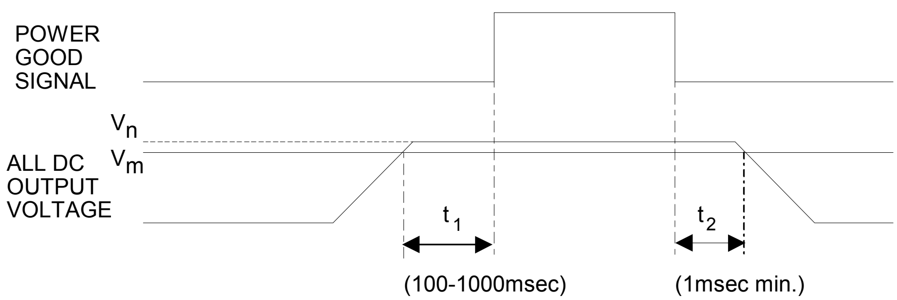
Power Good Signal	Voltage Level [1]	Current
LOW STATE DE-ASSERTED (Power Not Good)	0.4V max	4 mA min sink current
HIGH STATE ASSERTED (Power Good)	2.4 V min	0.5mA max source current

Note:

1. Measured relative to the power subsystem DC common ground output connector pins.

The Power Good signal is held low until all outputs have reached at least 95% of their respective operating voltages. The turn on delay for the Power Good signal is between 100 and 1000 msec.

The Power Good signal will be low for a minimum of 1 msec before any of the output voltages falls below the regulation limits as shown in Figure 18.



Vn Nominal Output Voltage +5 VDC
Vm Minimum Output Voltage + 4.8 VDC
t_1 Delay Turn-on (100-1000msec)
t_2 Delay Turn-off (1msec min)

Figure 18: Power Good Signal Characteristics

2.5.7.3 I^{2}C Interface Signals

The following signals are communicated to the system from the power subsystem via the I^{2}C bus.

Table 29: I^{2}C Interface Signals

Signal	Description
PS1_PRESENT PS2_PRESENT PS3_PRESENT	The Power Supply Module Present Indicator (PSx_PRESENT) signal is used to sense the number of power supply modules in the system (operational or not).
PS1_PREDICT_FAIL PS2_PREDICT_FAIL PS3_PREDICT_FAIL	The Predictive Failure Signal indicates that the power subsystem or the power supply module is likely to fail in the near future due to high temperature, lack of the airflow, poorly performing fan, etc. The Predictive Fan Failure Signal does not cause the Power Supply to shut down. This signal is utilized by the system to generate signal to alert an operator that the loading condition, ambient temperature, or airflow are not adequate, and one or several power modules will be shut down if no actions are taken to correct the condition. The Predictive Failure signal is an output from the Power Subsystem to the System.
PS1_ FAIL PS2_ FAIL PS3_ FAIL	The Power Supply Module Failure Signal is available on the power supply module connector. Upon receiving this signal, the system informs the operator that one of the power supply modules has failed and a replacement of that module is necessary. The Power Supply Module Failure is defined as OVP at any output, UV at any output, and/or Latch off condition inside the power supply module. The Power Supply Module Failure is an output signal from the power subsystem to the system.
+5VSB_FAIL	The +5VSB circuitry generates standy failure signal to indicate if one of the redundant standby converters (SB1 or SB2) has failed.
+12V_MON	The +12V output monitoring signal is utilized by the system to monitor the 12V rail tolerances.
+5V_MON	The +5V output monitoring signal is utilized by the system to monitor the 5V rail tolerances.
AC_R	The Transfer switch/AC redundancy monitoring signal is utilized by the system to monitor the AC redundancy feature. By monitoring relay operation functionality during initial AC turn on and presence of all 3 modules, this signal indicates that system is AC redundant, i.e. capable to operate when one of 2 AC lines fails.

2.5.7.4 AC_OK Signal (1)

Each power supply module provides an "AC_OK" signal. This signal is utilized by the Power Subsystem to synchronize the Power On timing of the three power supply modules (if all the modules are present) within nominal line input AC voltage range and under PFC CKT operational condition. The AC_OK allows the system to turn on at 90 VAC with 10% THD. The AC_OK signal has hysteresis such that the power system will not oscillate on/off due to normal AC source impedance (0.5 ohms). The power supply has thermal and current margin at 35 °C with maximum DC load at minimum AC voltage when AC_OK is asserted.

Table 30: AC_OK Signal

AC_OK Signal	Voltage Level 1	Current
LOW STATE DE-ASSERTED (AC not OK)	0.4V max	4 mA min sink current
HIGH STATE ASSERTED (AC is OK)	2.4 V min	Pull up resistor 1.3k on system side

Note:

1. Measured relative to the power subsystem DC common ground output connector pins.

2.5.7.5 Power Supply Field Replacement Unit (FRU) Signal (1)

The FRU data format is compliant with the Intelligent Platform Management Interface (IPMI) Specification, revision 1.5.

The I^2C slave address of the Power Subsystem EEPROM is 0xA6/A7h. The FRU circuits inside the power supply are powered by 5VSB on the system side of the or'ing device and grounded to ReturnS (remote sense return). The Write Control (or Write Protect) pin is tied to ReturnS inside the power supply module so that information can be written to the EEPROM.

2.6 Cooling Subsystem

All system components are cooled by a set of six individually hot swappable fans mounted in a fan bay near the middle of the chassis and in front of the E-bay. The fan bay is shown Figure 19.

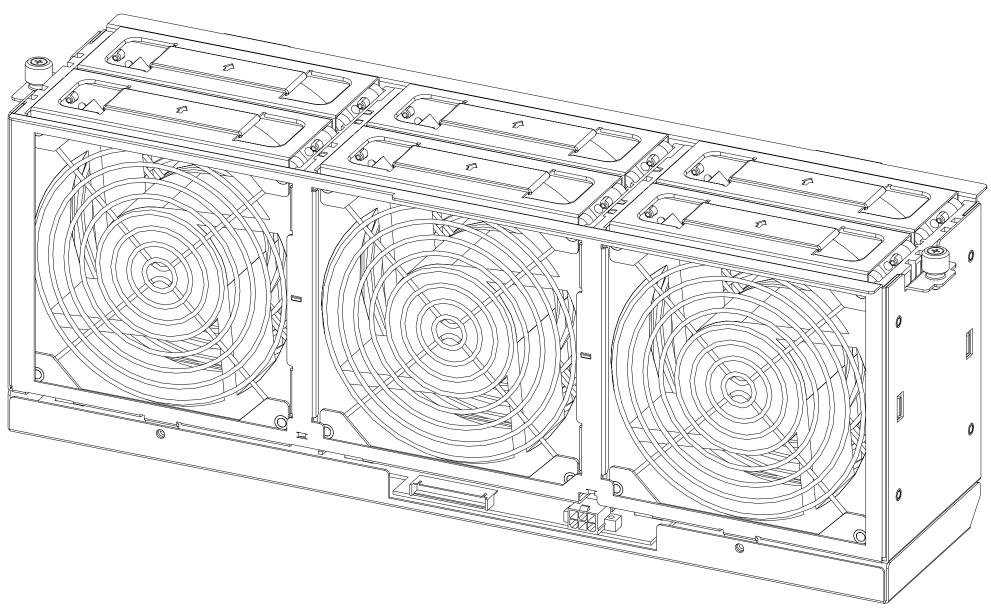


Figure 19: Fan Bay with Six System Fans Installed

The SRSH4 system comes in a 5+1 redundant fan configuration. This configuration supports any system configuration. Air flows in through the front bezel over the power supply bay, the peripheral bay and the hard drive bay, passes through the fan bay and the E-bay, and exits through the rear and left side of the chassis. Each fan provides tachometer signal output to the fan PCB to indicate a fan failure. Each fan also provides a fan-presence signal to the fan PCB.

2.6.1 Redundancy and Ambient Temperature Control

The fan PCB contains a pulse-width-modulation (PWM) circuit, which cycles the +12 V fan voltage to provide quiet operation when system ambient temperature is low, and there are no fan failures. Under normal room ambient conditions (less than 30°C) the fan power circuit operates the fans at low speed. When ambient temperature is between 30°C and 35°C or a fan fails, the fan power control circuit operates the fans at maximum speed.

2.6.2 Cooling Summary

The redundant, six fan cooling subsystem is sized to provide cooling for:

- Up to four Intel® Xeon™ processors MP dissipating 75W each
- 24 GB of DDR memory
- Five 15k RPM hard drives
- Eight full length PCI cards
- DC output redundant, fully-loaded power subsystem

The cooling subsystem is designed using a worst case analysis with no margin under a single fan failure condition. The lower fan speed setting was chosen to meet acoustic and thermal requirements. To ensure that all components remain within specification under all system environmental conditions, there will be a recommended time limit for fan and power supply module hot-swap operations.

3. Cables and Connectors

This chapter describes interconnections between the various components of the SRSH4 system. This chapter includes an overview diagram of the SRSH4 server system interconnections. Refer to the appropriate board *External Product Specification* for other connector signal descriptions and pin-outs.

3.1 Interconnect Block Diagram

Figure 20 shows interconnections for all of the boards used in the SRSH4 server system.

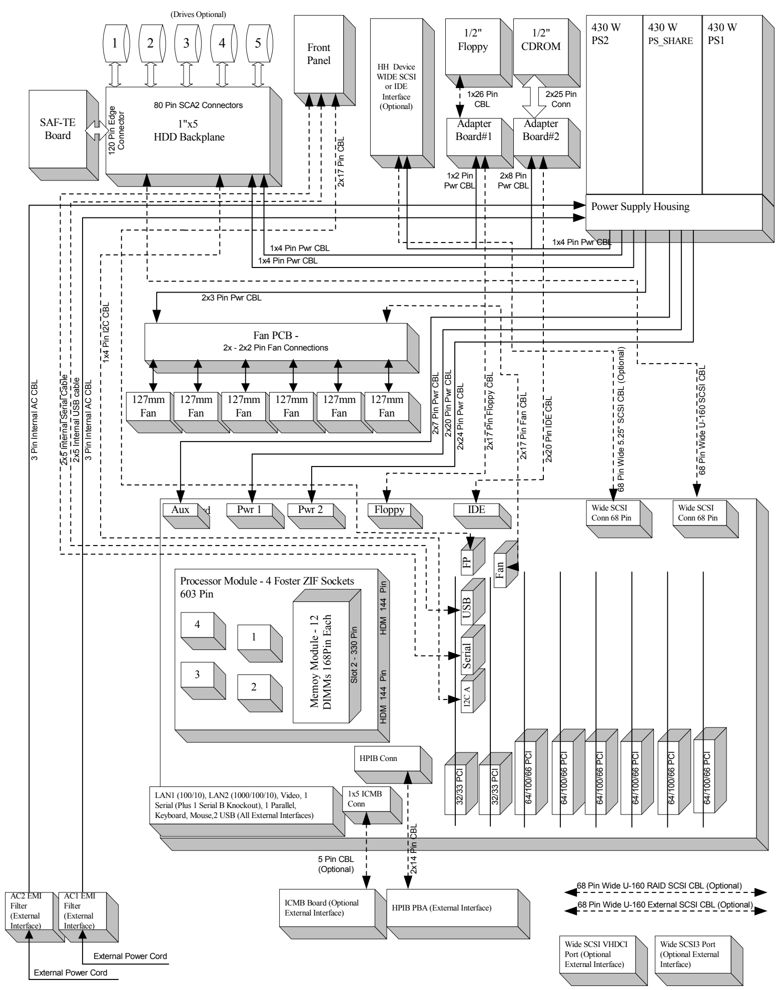


Figure 20: SRSH4 System Interconnect Block Diagram

3.2 Cable and Interconnect Descriptions

Table 31 describes all cables and connectors of SRSH4 server system.

Table 31: System Interconnect Descriptions

Type	Qty	From	To	Interconnect Description
32-bit PCI	2	SSH4 baseboard	PCI adapter card	120-pin card edge connect
64-bit PCI-X, 3.3V	6	SSH4 baseboard	PCI-X adapter card	184-pin card edge connect
Keyboard	1	SSH4 baseboard	External interface	PS2 keyboard device
Mouse	1	SSH4 baseboard	External interface	PS2 mouse device
System Control	1	SSH4 baseboard	Front panel board	2x17 flat ribbon cable
Floppy	1	SSH4 baseboard	Floppy device	2x17 flat ribbon cable
IDE	1	SSH4 baseboard	CD-ROM device	2x20 flat ribbon cable
HPIB	1	SSH4 baseboard	HPIB board	2x14 flat ribbon cable
Parallel Port	1	SSH4 baseboard	External interface	25-pin parallel port connector
Serial Port A	1	SSH4 baseboard	External interface	9-pin serial port connector
100/10 Ethernet	1	SSH4 baseboard	External interface	RJ45 connector port
1000/100/10 Ethernet	1	SSH4 baseboard	External interface	10-pin connector port
Internal Wide Ultra-320 SCSI, Channel A	1	SSH4 baseboard	SCSI bay HDD backplane	68-pin solid core twisted pair ribbon cable
External Wide Ultra-160 SCSI, Channel B	1	SSH4 baseboard	5¼" Device	68-pin solid core twisted pair ribbon cable
Aux IMB	1	SSH4 baseboard	SCSI bay HDD backplane	1x4-pin connector on baseboard discrete cabled to a 1x4 -pin connector on SCSI bay HDD backplane
ICMB internal	1	SSH4 baseboard	ICMB board	1x5-pin cable
ICMB external	2	ICMB board	External interface	1x6 -pin ICMB cable
USB 1 and 2	2	SSH4 baseboard	External interface	1x4-pin USB cables
Video	1	SSH4 baseboard	External interface	15-pin, monitor device
Main power 1	1	Power supply cage	SSH4 baseboard	2x10-pin discrete cable
Main power 2	1	Power supply cage	SSH4 baseboard	2x12-pin discrete cable
Aux power	1	Power supply cage	SSH4 baseboard	2x7-pin discrete cable
FP Serial Port B internal	1	SSH4 baseboard	Front panel board	2x5 round cable
FP USB 3 internal	1	SSH4 baseboard	Front panel board	2x5 sheilded round cable
Processor Board	2	SSH4 baseboard	SSH4 processor board	6x24-pin HDM connect
Processor	4	SSH4 processor board	Intel® MP Xeon™ processor	603-pin ZIF BGA socket
Memory	1	SSH4 baseboard	SSH4 memory module	330-pin card edge connect
DIMM	12	SSH4 memory module	DIMM	168-pin card edge connect

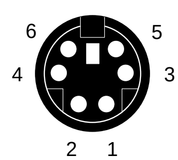
Type	Qty	From	To	Interconnect Description
SCA-2 HDD	5	SCSI bay HDD Backplane	External Interface	80-pin SCA-2 compatible device
Aux HDD fans	2	SCSI bay HDD Backplane	No connection	1x3-pin connector, NOT USE FOR SRSH4
SAFE-TE	1	SCSI bay HDD Backplane	SAF-TE board	120-pin card edge connect
HDD power	2	Power supply cage	SCSI bay HDD Backplane	1x4-pin discrete cable
USB 3	1	Front panel	External Interface	1x4-pin USB cables
Serial port B	1	Front panel	External Interface	8-pin RJ45 cable
Fan power	1	Power supply cage	Fan board	2x3-pin discrete cable
System fan bank	6	Fan board	Fan modules	2x2-pin blind mate connector
Peripheral power	2	Power supply cage	Floppy device (adapter board) and half height device	1x4-pin connectors (daisy chained)
½” floppy signal	1	½” floppy adapter board	½” floppy device	26-pin flex cable
½” CD-ROM power	1	Power supply cage	½” CD-ROM adapter board	2x8-pin discrete cable
½” CD-ROM signal	1	½” CD-ROM adapter board	½” CD-ROM device	2x25-pin connector
AC Distribution	2	Power cord	Power supply cage	3-pin PVC double insulated power cordage
AC Power	2	AC distribution	External interface	Recommend 3-pin SJT power cord

3.3 Operator-Accessible Interconnects

3.3.1 Keyboard and Mouse Ports

The identical keyboard and mouse PS/2-compatible ports share a common housing.

Table 32: Keyboard and Mouse Ports

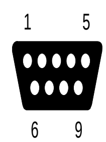
Mouse		Keyboard or Mouse Connector	Keyboard	
Pin	Signal		Pin	Signal
1	MSEDAT (mouse data)		1	KEYDAT (keyboard data)
2	No connection		2	No connection
3	GND		3	GND
4	Fused VCC (+5 V)		4	Fused VCC (+5 V)
5	MSECLK (mouse clock)		5	KEYCLK (keyboard clock)
6	No connection		6	No connection

3.3.2 Serial Ports

The baseboard provides two RS-232C serial ports. Serial A is at the rear panel of the system, Serial B is either at a knockout at the rear panel of the system or defaults to the front panel of the system. Serial A is a D-subminiature 9-pin connector. Serial B is an RJ45 8-pin connector on the front panel or it is a D-subminiature 9-pin connector at the rear panel of the system. Each serial port can be enabled separately with the configuration control provided on the baseboard.

The serial B port can be used either as an Emergency Management Port or as a normal serial port. As an Emergency Management Port, serial B port is used as a communication path by the Server Management RS-232 connection to the Front Panel Controller. This provides a level of emergency management through an external modem. The RS-232 connection can be monitored by the FPC when the system is in a powered down (standby) state. Additional information can be found in the *Emergency Management Port Interface External Product Specification*.

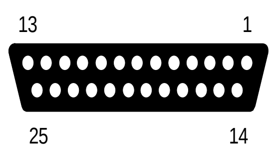
Table 33: Serial Port A Connector

Pin	Signal	Serial Port A Connector
1	DCD (carrier detect)	
2	RXD (receive data)	
3	TXD (transmit data)	
4	DTR (data terminal ready)	
5	GND	
6	DSR (data set ready)	
7	RTS (request to send)	
8	CTS (clear to send)	
9	RIA (ring indicator)	

3.3.3 Parallel Port

The IEEE 1284-compatible parallel port is primarily used for a printer. It sends data in parallel format. The parallel port is accessed through a D-subminiature 25-pin connector.

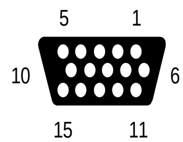
Table 34: Parallel Port Connector

Pin	Signal	Parallel Port Connector	Pin	Signal
1	STROBE_L		14	AUFDXT_L (auto feed)
2	Data bit 0		15	ERROR_L
3	Data bit 1		16	INIT_L (initialize printer)
4	Data bit 2		17	SLCTIN_L (select input)
5	Data bit 3		18	GND
6	Data bit 4		19	GND
7	Data bit 5		20	GND
8	Data bit 6		21	GND
9	Data bit 7		22	GND
10	ACK_L (acknowledge)		23	GND
11	BUSY		24	GND
12	PE (paper end)		25	GND
13	SLCT (select)			

3.3.4 Video Port

The video port interface is a standard VGA compatible 15-pin connector. On-board video is supplied by an ATI RAGE-XL video controller with 4 MB of video SGRAM.

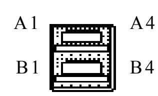
Table 35: Video Connector

Pin	Signal	Video Connector
1	Red (analog color signal R)	
2	Green (analog color signal G)	
3	Blue (analog color signal B)	
4	No connection	
5	GND	
6	GND	
7	GND	
8	GND	
9	Fused VCC (+5V)	
10	GND	
11	No connection	
12	DDCDAT	
13	HSYNC (horizontal sync)	
14	VSYNC (vertical sync)	
15	DDCCLK	

3.3.5 Universal Serial Bus (USB) Interface

The baseboard provides two stacked USB ports (Port 1 on top, Port 2 on bottom). The built-in USB ports permit the direct connection of two USB peripherals without an external hub. If more devices are required, an external hub can be connected to either of the built-in ports.

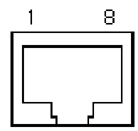
Table 36: Dual USB Connector

Pin	Signal	Dual USB Connector
A1	Fused VCC (+5V /w overcurrent monitor of both port 1 and 2)	
A2	DATAL1 (Differential data line paired with DATAH1)	
A3	DATAH1 (Differential data line paired with DATAL1)	
A4	GND	
B1	Fused VCC (+5V /w overcurrent monitor of both port 1 and 2)	
B2	DATAL2 (Differential data line paired with DATAH2)	
B3	DATAH2 (Differential data line paired with DATAL2)	
B4	GND	

3.3.6 ICMB Connectors

The external Intelligent Management Bus (ICMB) provides external access to IMB devices that are within the chassis. This makes it possible to externally access chassis management functions, alert logs, post-mortem data, etc. It also provides a mechanism for chassis power control. As an option, the server can be configured with an ICMB adapter board to provide two SEMCONN 6-pin connectors to allow daisy chained cabling. Additional information about ICMB can be found in the *External Intelligent Management Bus Bridge External Program Specification* and in the *SSH4 Intelligent Chassis Management Board (ICMB) External Product Specification*.

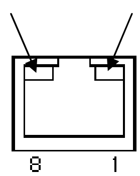
Table 37: ICMB Connector

Pin	Signal	ICMB Connector
1	Tx/Rx+	
2	Tx/Rx-	
3	GND	
4	No connection	
5	GND	
6	No connection	
7	No connection	
8	No connection	

3.3.7 100/10 Ethernet Connector (LAN 1)

The system supports one on-board 100/10 Ethernet connection.

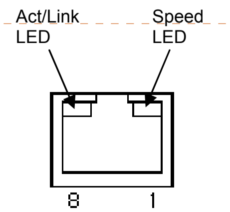
Table 38: Ethernet Connector

Pin	Signal	100/10 Ethernet Connector
1	Tx+	
2	Tx-	
3	Rx+	
4	Termination	
5	Termination	
6	Rx-	
7	Termination	
8	Termination	

3.3.8 1000/100/10 Ethernet Connector (LAN 2)

The system supports one on-board 1000/100/10 Ethernet connection.

Table 39: Ethernet Connector

Pin	Signal	100/100/10 Ethernet Connector
1	TR1+	
2	TR1-	
3	TR2+	
4	TR3+	
5	TR3-	
6	TR2-	
7	TR4+	
8	TR4-	

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3.3.9 Internal SCA-2 HDD Connector

An SCA-2 connector is used on the primary side of the HDD backplane. The pin-out is the same as SCA-1. The connector pin assignment is for the current draft *Small Form Factor-8046 Rev. 1.1* document.

Table 40: SCA-2 Connector

80-pin connector contact and signal name			Cable conductor numbers are not applicable	80-pin connector contact and signal name		
1	12 V Charge	(L)		(L)	12 V Ground	41
2	12 V	(S)		(L)	12 V Ground	42
3	12 V	(S)		(L)	12 V Ground	43
4	12 V	(S)		(S)	Mated 1	44
5	Reserved/ESI-1	(S)		(L)	-EFW	45
6	Reserved/ESI-2	(S)		(L)	DIFFSNS	46
7	-DB(11)	(S)		(S)	+DB(11)	47
8	-DB(10)	(S)		(S)	+DB(10)	48
9	-DB(9)	(S)		(S)	+DB(9)	49
10	-DB(8)	(S)		(S)	+DB(8)	50
11	-I/O	(S)		(S)	+I/O	51
12	-REQ	(S)		(S)	+REQ	52
13	-C/D	(S)		(S)	+C/D	53
14	-SEL	(S)		(S)	+SEL	54
15	-MSG	(S)		(S)	+MSG	55
16	-RST	(S)		(S)	+RST	56
17	-ACK	(S)		(S)	+ACK	57

80-pin connector contact and signal name			Cable conductor numbers are not applicable	80-pin connector contact and signal name		
18	-BSY	(S)		(S)	+BSY	58
19	-ATN	(S)		(S)	+ATN	59
20	-DB(P)	(S)		(S)	+DB(P)	60
21	-DB(7)	(S)		(S)	+DB(7)	61
22	-DB(6)	(S)		(S)	+DB(6)	62
23	-DB(5)	(S)		(S)	+DB(5)	63
24	-DB(4)	(S)		(S)	+DB(4)	64
25	-DB(3)	(S)		(S)	+DB(3)	65
26	-DB(2)	(S)		(S)	+DB(2)	66
27	-DB(1)	(S)		(S)	+DB(1)	67
28	-DB(0)	(S)		(S)	+DB(0)	68
29	-DB(P1)	(S)		(S)	+DB(P1)	69
30	-DB(15)	(S)		(S)	+DB(15)	70
31	-DB(14)	(S)		(S)	+DB(14)	71
32	-DB(13)	(S)		(S)	+DB(13)	72
33	-DB(12)	(S)		(S)	+DB(12)	73
34	5V	(S)		(S)	Mated 2	74
35	5V	(S)		(L)	5 V Ground	75
36	5V Charge	(L)		(L)	5 V Ground	76
37	Spindle Sync	(L)		(L)	Active LED Out	77
38	MTRON	(L)		(L)	DLYD_START	78
39	SCSI ID (0)	(L)		(L)	SCSI ID (1)	79
40	SCSI ID (2)	(L)		(L)	SCSI ID (3)	80

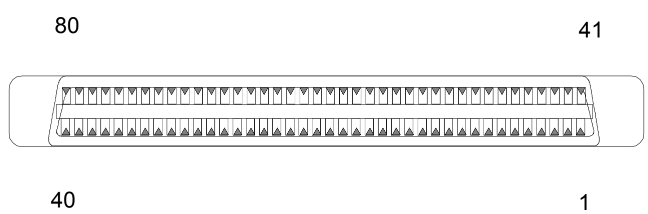
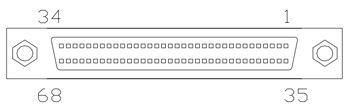
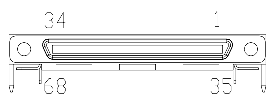


Figure 21: SCA-2 Connector

3.3.10 External SCSI

As an option, the server system can support a shielded 68pin external VHDCI or SCSI3 connection. This connection is normally to Channel B of the onboard SCSI controller.

Table 41: SCSI Connector

Signal Name	Pin	SCSI Connector	Pin	Signal Name
Signal Return	1		35	-DB(12)
Signal Return	2	SCSI3	36	-DB(13)
Signal Return	3		37	-DB(14)
Signal Return	4		38	-DM(15)
Signal Return	5		39	-DB(P1)
Signal Return	6		40	-DB(0)
Signal Return	7		41	-DB(1)
Signal Return	8		42	-DB(2)
Signal Return	9	VHDCI	43	-DB(3)
Signal Return	10		44	-DB(4)
Signal Return	11		45	-DB(5)
Signal Return	12		46	-DB(6)
Signal Return	13		47	-DB(7)
Signal Return	14		48	-DB(P)
GND	15		49	GND
GND	16		50	GND
TERMPWR	17		51	TERMPWR
TERMPWR	18		52	TERMPWR
No connection	19		53	No connection
GND	20		54	GND
Signal Return	21		55	-ATN
GND	22		56	GND
Signal Return	23		57	-BSY
Signal Return	24		58	-ACK
Signal Return	25		59	-RST
Signal Return	26		60	-MSG
Signal Return	27		61	-SEL
Signal Return	28		62	-C/D
Signal Return	29		63	-REQ
Signal Return	30		64	-I/O
Signal Return	31		65	-DB(8)
Signal Return	32		66	-DB(9)
Signal Return	33		67	-DB(10)
Signal Return	34		68	-DB(11)

3.3.11 AC Power Input

Dual IEC320-C14 receptacles is provided at the rear of the server. The use of an appropriately sized power cord and AC main is recommended. Refer to Section 2.5 for system voltage, frequency and current draw specifications.

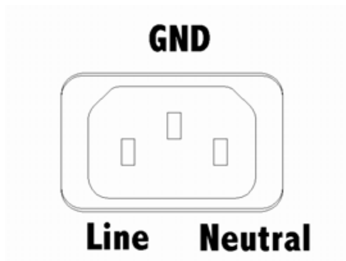


Figure 22: AC Power Input Connector

3.3.11.1 AC Power Cord Specification

The AC power cord supplied with the SRSH4 server system is the North American type. AC power cords must be rated for 100-240VAC voltage range, and have a low line current rating of at least 10A.

The wall outlet end of the AC power cord must be terminated in a grounding-type male plug designed for use in your region. The plug must have certification marks showing certification by an agency acceptable in your region.

The server end of the AC power cord must be an IEC 320, sheet C13, type female connector.

The AC power cord must be less than 4.5 meters (14.76 feet) long, and must be flexible (harmonized) cord or VDE-certified cordage to comply with server's safety certifications.

4. SCSI Bay Boardset

This chapter provides an overview of the LVD/SE SCSI boardset, describing the architecture of backplane boardset, and physical board layout diagrams.

The SCSI boardset consists of hot swap backplane and a SAF-TE board. The hot swap backplane supports the following features:

- SE SCSI and LVD SCSI modes
- Five 1 inch LVD/SE SCSI drives per board
- Single connector attachment (SCA-2) connectors to simplify insertion and removal of hard disk drives
- Insertion and removal of hard drives in any power or SCSI bus state (Hot Swap)
- FET power control for each hard drive
- FET short protection
- SCSI-2 SPI-2 (Ultra SCSI and Ultra2 SCSI) and SCSI-2 (Fast-10)
- SCSI-3 SPI-3 (Ultra-160 SCSI)
- SCSI-4 SPI-4 (Ultra-320 SCSI)
- Support for two backplanes on SCSI bus via “Y” cable
- Drive fault and drive activity LEDs for each disk drive

In addition, a SAF-TE addin card contributes the following features:

- Microcontroller to monitor enclosure services
- I^2C bus for management information
- Flash memory for upgrading firmware
- Thermal friendly mechanical form factor
- SAF-TE compliant
- Two-fan tachometer monitoring

4.1 Hot Swap Hard Drive Backplane

The backplane is a LVD/SE SCSI design that provides support for SCSI devices using Low Voltage Differential Signaling (Ultra-160/Ultra-320) as well as older SE SCSI devices (Ultra-320 and older). The backplane has a connector to accommodate a SAF-TE controller on an add-in card. The backplane supports five 1” hot swapping SCA-2 style drives when mounted in the docking drive carrier. By using a “Y” cable, two of these backplane assemblies may be connected for a total of ten SCSI drives off one SCSI channel.

4.1.1 Architectural Overview

The drive backplane is an integral part of the system chassis. It is designed to provide a cost effective ease of power-on (Hot Swap) drive replacement. It also provides easy RAID integration over a wide range of RAID controller products. It is designed to be vendor independent.

The feature that simplifies RAID integration is the addition of an on-board SCSI target whose command set allows vendor independent controller management and monitoring for associated drive functions such as: Drive insertion and removal, light indicators, and drive power control. Its use simplifies cable management and eliminates errors caused by the possibility of incorrect correlation of several cables.

The LVD/SE SCSI Backplane performs the tasks associated with hot-swappable SCSI drives, and enclosure (chassis) monitoring and management supported by the LVD/SE SCSI Backplane. They include, but are not limited to, the following:

- Monitoring the SCSI bus for enclosure services messages, and acting on them appropriately. Examples of such messages include:
  - Activate a drive fault indicator
  - Power down a drive, which has failed
  - Report fan tachometer status
- SAF-TE intelligent agent, which acts as proxy for “dumb” I^2C devices (that have no bus mastering capability) during intra-chassis communications.

4.2 Design Constraints and Assumptions

This section specifies certain assumptions and limitations taken into consideration during the design of the LVD/SE SCSI backplane.

4.2.1 SCSI Bus Considerations

The SCSI bus is based on the SPI-4 specification. It is designed to allow any SCSI device to communicate with any other SCSI device. To that end, SPI-4 requires that all SCSI devices be at certain distances apart, depending on the media capacitance measured in pF/m. The lower the media capacitance the greater the spacing needs to be because the loading from the device becomes more significant.

Historically, backplane designs have successfully violated this guideline because of careful simulation backed up with signal integrity validation. Those past designs were able to have straight-to-straight connections between three devices with some meandering between another three devices. The layout and board stackup was driven from LVD SCSI bus simulation, which yielded the following:

- SCA-2 to SCA-2 electrical distance of four inches
- Six-layer board with two internal SCSI layers with 90 Ohm impedance targeted
- Total backplane SCSI length max 30 inches

The electrical spacing of the SCA-2 connectors was a combination of the faster edge rate and faster transfer speed.

The following are key points to know:

- The LVD (Ultra2) length specification is 15 devices at 12 meters and 1-2 devices at 25 meters
- The SE (Ultra) length specification is 5-8 devices at 1.5 meters (59 inches) and 1-4 devices at 3 meter
- If used in SE Ultra mode, the backplane uses 30 of the 59 inches of the SCSI Bus length
- The backplane's SCSI interface counts as one device on the SCSI Bus regardless the presence of any SAF-TE compliant host controller.

4.3 Functional Description

This chapter defines the architecture of the LVD/SE SCSI Backplane, including descriptions of functional blocks and how they operate.

Figure 23 shows the functional blocks of the LVD/SE SCSI Backplane. The two boards are split such that the backplane has the SCSI connectors, drive fault/activity LEDs, and termination, and the SAF-TE addin card has the rest of the blocks. An overview of each block follows.

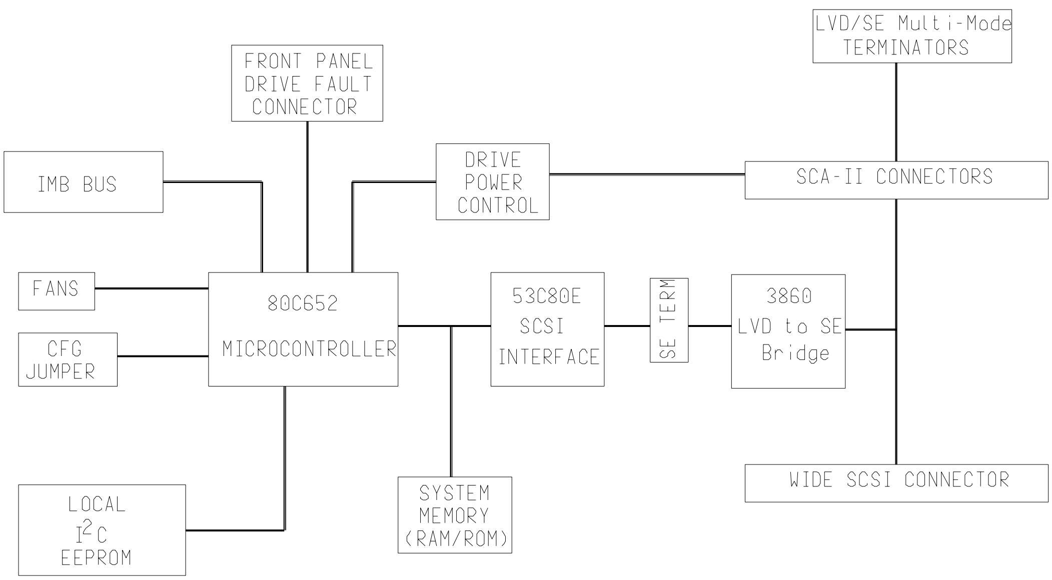


Figure 23: Functional Block Diagram

4.3.1 Wide SCSI Connector

SCSI input from Host SCSI Controller (baseboard or RAID card) in a press-fit connector.

4.3.2 SCA-2 Connectors

The LVD/SE SCSI backplane provides five SCA-2 connectors. These provide power and SCSI signals using a single connector. Each connector has control signals that enable the backplane to provide SCSI ID assignments as well as drive motor spin-up configuration. Each SCSI drive attaches to the backplane using one of these connectors.

4.3.3 SCSI Multi-ModeTermination

The multi-mode terminators provide SCSI-4 compliant termination for the backplane. These terminators provide termination in both SE modes and LVD mode.

4.3.4 SCSI Interface

The SCSI interface on the LVD/SE SCSI backplane provides the link between the SCSI bus and the microcontroller (containing the intelligence for the LVD/SE SCSI backplane). This interface allows the microcontroller to respond as a SCSI target to implement the SAF-TE protocol. This is implemented using a Symbios Logic* 53C80S SCSI interface chip (or equivalent).

4.3.5 Power Control

Power control on the LVD/SE SCSI backplane supports the following features. Without the population of the SAF-TE card, power to the drives is always on.

- Spin-down of a drive when failure is detected and reported (using enclosure services messages) via the SCSI bus. An application or RAID controller detects a drive-related problem that indicates a data risk. In response, it removes the drive from service and sends a spin-down SCSI command to the drive. This decreases the likelihood that the drive will be damaged during removal from the hot-swap drive bay. When a new drive is inserted, the power control waits a short amount of time for the drive to be fully seated before it applies power with a controlled power ramp.
- If the system power is on, the LVD/SE SCSI backplane immediately powers off a drive slot when it detects that a drive has been removed. This prevents possible damage to the drive when it is partially removed and re-inserted while full power is available, and disruption of the entire SCSI array from possible sags in supply voltage and resultant current spikes.

4.3.6 FET Short Protection

The FET short protection circuit is useful to protect both 12 volt and 5 volt power control FETs located on LVD/SE SCSI backplane.

4.3.7 Microcontroller

The microcontroller is an 80C652 microcontroller with a built-in I^2C interface. This provides the intelligence for the LVD/SE SCSI Backplane. The 80C652 microcontroller uses Flash for program code storage, and static RAM for program variables and buffers.

4.3.8 Device SCSI ID

Each device on a SCSI bus must have a unique SCSI ID. The 5 x 1.0" LVD/SE SCSI backplane device SCSI ID is dependant on whether it is configured as a primary or a secondary backplane. This configuration is defined by the logic of pin 1 on the I^2C connector (J2A1).

Table 42: SCSI ID Assignments

Device	SCSI ID as Primary Backplane I^2C connector (J2A1) pin1=1	SCSI ID as Primary Backplane I^2C connector (J2A1) pin1=0
Drive 1	0x0H	0x8H
Drive 2	0x1H	0x9H
Drive 3	0x2H	0xAH
Drive 4	0x3H	0xBH
Drive 5	0x4H	0xCH
SAF-TE Controller	0x6H	0x5H

4.3.9 Hard Drive Activity LED

Each SCSI drive turns on a green LED when it is accessed. The LEDs are 4-terminal dual-color (yellow and green) lights that are physically located on the backplane.

Table 43: Hard Drive Activity LED

Drive	HSBP LED Activated	LED Designator	LED Color
1	1	DS5A1	Green
2	2	DS5B1	Green
3	3	DS5C1	Green
4	4	DS5D1	Green
5	5	DS5E1	Green

4.3.10 Hard Drive Fault LED

The Hot-Swap Controller is responsible for turning the drive fault LEDs on or off according to the states specified via commands received via SAF-TE and the IMB. The drive fault LEDs are yellow and indicate the failure status for each drive. The LEDs are physically located on the LVD/SE SCSI Backplane. For further information on Slot Status to Fault Light State mapping refer to *SC5000 Hot-swap Controller Interface EPS.*

The LEDs are 4-terminal dual-color (yellow and green) physically located on the backplane.

Table 44: Hard Drive Fault LED

Drive	HSBP LED Activated	LED Designator	LED Color
1	1	DS5A1	Yellow
2	2	DS5B1	Yellow
3	3	DS5C1	Yellow
4	4	DS5D1	Yellow
5	5	DS5E1	Yellow

4.3.11 IMB (I^2C bus)

The I^2C bus is a system-wide server management bus. It provides a way for various system components to communicate independently of the standard system interfaces (e.g., PCI bus or processor/memory bus). The I^2C bus controller is integrated into the microcontroller.

4.3.12 Fan Support

The LVD/SE SCSI backplane supports up to two tach fans with a digital-output that can be used by the microcontroller to assess the fans' operating condition before total failure, which could result in hardware damage.

Microcontroller program code is responsible for monitoring the fan speed, which is directly controlled from backplane, and reporting the fan condition via the I^2C bus. The Hot-swap Controller is responsible for reporting fan speed. The speed of the fans is sensed by the Hot-swap Controller and compared against a 'low speed' threshold. The Hot-swap Controller issues a message on the IMB when the fan speed falls below this threshold. When a fan fails, it should be replaced; the backplane does not detect second fan failure.

4.3.13 Temperature

The DS1624 on the SAF-TE addin card provides a temperature sensor in the center of the SAF-TE addin card. This is accessed by a private I^2C bus.

4.3.14 Serial EEPROM

The DS1624 provides 256 bytes of non-volatile storage. This hold the serial number, part number, FRU inventory information, and miscellaneous application code used by firmware about the LVD/SE SCSI backplane. This is accessed by a private I^2C bus.

4.4 Board Functions

This section describes functioning parts as required by the *Management Bus Architecture Specification* and the *Enclosure Services SCSI Command Set*. In addition to these requirements, the board is capable of downloading code via IMB to update the FLASH executable code. The backplane functions begin at power-up. The microprocessor boots itself via code residing in the FLASH boot block.

4.4.1 Reset

A cold reset occurs when power is cycled or the SCSI bus can be reset by a SAF-TE command.

4.4.2 Microcontroller

The microcontroller is a Philips* P80C652FBB operating at 12 MHz. The 80C652 is a derivative of the 80C51 8-bit CMOS microcontroller. The 80C652 contains all of the features of the 80C51 (that is, the standard counter/timers T0 and T1, the standard serial I/O (UART), and four 8-bit I/O ports).

The organization of the data memory is similar to the 80C51 except that the 80C652 has an additional 128 bytes of RAM overlapped with the special function register space. This additional RAM is addressed using indirect addressing only and is available as stack space.

The 80C652 is pin-for-pin compatible and code compatible with the 80C51, except for additional Vss pins at the QFP package.

The features can be outlined as follows:

- Operating frequency from 1.2 MHz to 16 MHz
- 80C51-based architecture
- Four 8-bit I/O ports
- Two 16-bit timer/counters
- Full-duplex UART facilities
- I^2C Serial Interface
- Two power control modes; idle mode, power-down mode
- Operating temperature range: 0°C to +70°C

4.4.2.1 Special Function Registers

The 80C652 special function register space is the same as that on the 80C51 except that it contains four additional SFRs. The added registers are S1CON, S1STA, S1DAT, and S1ADR. In addition to these, the standard UART special function registers SCON and SBUF have been renamed S0CON and S0BUF for clarity.

Since the standard 80C51 on-chip functions are the same on the 80C652, the SFR locations, bit locations, and operation are unchanged. The only exception is in the interrupt enable and interrupt priority SFRs. These have been changed to include the interrupt from the I^2C serial port.

4.4.2.2 I^2C Serial Communication

The I^2C pins are alternate functions to port pins P1.6 and P1.7. Because of this, P1.6 and P1.7 on these parts do not have a pull-up structure as found of the 80C51. Therefore, P1.6 and P1.7 have open drain outputs on the 80C652.

4.4.2.3 I^{2}C Electrical Input/Output Specification

The I^{2}C bus allows communication between devices using different technologies that might also use different supply voltages.

For devices with fixed input levels, operating on a supply voltage of +5V ±10%, the following levels have been defined:

- V_{Ilmax} = 1.5V (maximum input low voltage)
- V_{Ihmin} = 3V (minimum input High voltage)

Devices operating on a fixed supply voltage different from +5V (e.g. I^{2}L), must also have these input levels of 1.5V and 3V for V_{IL} and V_{IH} respectively.

For devices operating over a wide rage of supply voltages (e.g. CMOS), the following levels have been defined:

- V_{Ilmax} = 0.3V_{DD} (maximum input Low voltage)
- V_{Ihmin} = 0.7V_{DD} (minimum input High voltage)

For both groups of devices, the maximum output Low value has been defined:

- V_{Olmax} = 0.4V (max. output voltage Low) at 3ma sink current

The maximum low-level input current at V_{Olmax} of both the SDA pin and the SCL pin of an I^{2}C device is –10uA, including the leakage current of a possible output stage.

The maximum high-level input current at 0.9V_{DD} of both the SDA pin and SCL pin of an I^{2}C device is 10uA, including the leakage current of a possible output stage.

The maximum capacitance of both the SDA pin and the SCL pin of an I^{2}C device is 10pf.

4.4.2.3.1 Noise Margin

- Noise margin minimum on the Low level is 0.1 V_{DD}.
- Noise margin minimum on the High level is 0.2 V_{DD}.

4.4.3 SCSI Controller

The SYM53C80S controller is an 8-bit controller. It is reset on power-up and when reset is asserted to the backplane.

SYM53C80S access slows down the bus, it is recommended to pulse SAF-TE infrequently. SAF_TE command processing is 2-10ms.

The features of the SCSI controller are as follows:

- Supports the ANSI X3.131-1994 standard
- Parity generation with optional checking
- No external clock required
- On-chip 48ma single-ended drivers and receivers
- Functions in both the target and initiator roles
- Direct control of all SCSI signals
- Asynchronous data transfers of up to 5.0 MB/second
- Variety of packaging options
- SCSI protocol efficiency is directly proportional to the speed of the microprocessor
- CMOS parts provide additional grounding and controlled fall times that reduce noise generated by SCSI bus switching
- SCAM Level 1 and 2 compatibility

4.4.4 Multi-Mode SCSI Termination

The SCSI-3 and SCSI-4 standards recommend the use of active termination at both ends of every cable segment in a SCSI system with single-ended drivers and receivers.

Two Unitrode* UCC5638 devices are used for active termination that detect SE or LVD mode and terminate appropriately.

4.5 Memory Map

This chapter describes the microcontroller memory map and individual regions of memory. 80C51 architecture allows up to 64KB of byte-addressable memory. No I/O map is provided, since 80C51 architecture makes no distinction between memory and I/O addresses (all I/O accesses are memory-mapped). However, four “I/O ports” available to the microcontroller are also defined in this chapter.

4.5.1 Memory Map

The Figure 24 below shows the memory map viewed from the perspective of the microcontroller. Descriptions of each memory block are provided, showing their purpose and function as determined by microcontroller programming. These functions may also be controlled by system software using SCSI commands defined in the SAF-TE specification. Status and control regions act like an I/O port with many aliases.

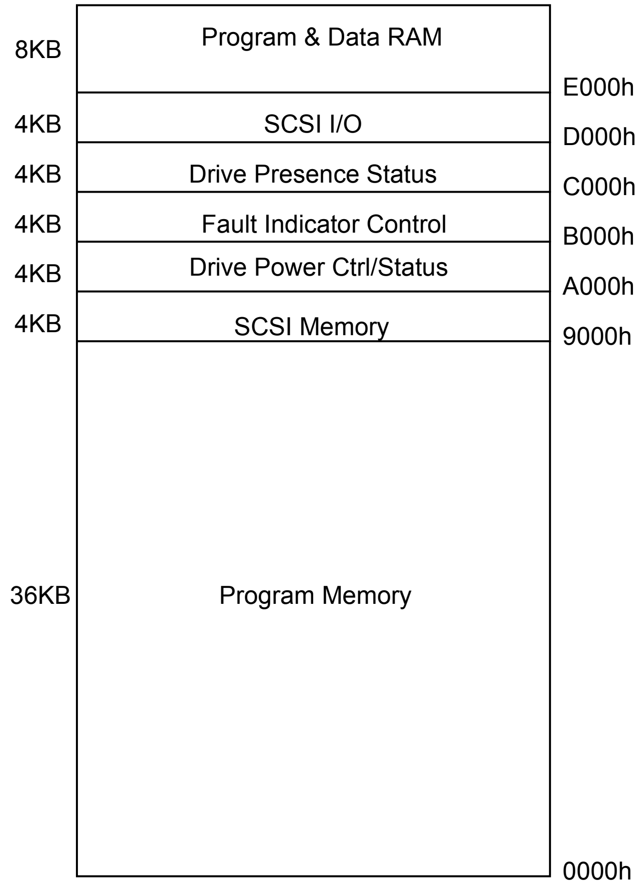


Figure 24: Microcontroller Memory Map

4.5.1.1 Program Memory Region (0000h – 8FFFh)

Program memory is usually considered read-only. However, the Hot-swap SCSI Backplane is designed to allow writes to the program memory area, thereby supporting field-upgradeable code. The bottom 8 KB is the boot block, which can only be written to if the Flash Boot Block Write jumper is in the *write* position.

4.5.1.2 SCSI Memory Region (9000h – 9FFFh)

Buffer memory area for DMA transfers on the SCSI interface. Accesses to this region activate the appropriate DACK_L and Read/Write strobes to the 53C80S SCSI chip (which has been properly configured for DMA operations).

4.5.1.3 Drive Power Control/Status Region (A000h – AFFFh)

A read operation of any byte address within this region produces the current value of the Power Control byte. This value does not report the actual state of drive power (e.g., whether or not drive power is within specifications). Instead, this indicates whether the power for a particular drive has been switched on or off.

A write operation to any byte address within this region updates the current value of the Power Control byte, which causes selected drive slots to power on or off. The initial (default) value is 11011111b (all drives on). This allows normal server operation even if the firmware is corrupted or the microcontroller is not operational. The lower five bits function as power switches for each drive slot. The remaining three bits are read-only, and are defined below.

!WARNING!
If a drive is powered up immediately upon detection, it is likely to be damaged, as the drive will not be fully seated. It is recommended that firmware "debounce" the drive presence detect bits, and power up the drive no less than 250ms after the drive is detected as being present.

Table 45: Drive Power Status Byte Format

Bit(s)	Name	Description
7	Internal/External	Read only. Logic 1 indicates the backplane is installed in an "internal" chassis. Logic 0 indicates the backplane is installed in an "external" chassis (e.g. peripheral box).
6	Reserved	Reserved for future use.
5	SCSI ID	Read only. This bit determines the SCSI ID for the drive array.
4::0	DRVPWR[4::0]	Drive power control bits (read/write). Bit 0 corresponds to drive 0, bit 1 to drive 1, and so on. An active bit (1=active) indicates power is turned on for that drive; an inactive bit indicates power is turned off for that drive. Writing a 1 to a bit position turns on, or maintains power on, for the associated drive.

4.5.1.4 Fault Indicator Control Region (B000h – BFFFh)

A write operation to any byte address controls drive fault indicator LEDs. The value is initially 00h, which means all drive-fault LEDs are off. The lower five bits of the data byte function as on/off switches for each LED.

Table 46: Fault Indicator Control Byte Format

Bit(s)	Name	Description
7::5	Reserved	Reserved for future use.
4::0	FLTON[4::0]	Fault Indicator On. If 1, the fault LED is turned on, and if 0, turned off, on the drive associated with selected SCA connector. Bit 0 corresponds to backplane slot 0, etc. To avoid false indication of Drive fault on other drives, software should maintain a local copy of the last value written, modify the bit in this value that corresponds to the selected drive slot, before writing the new result.

4.5.1.5 Drive Presence Status Region (C000h – CFFFh)

A read operation of any byte address within this region produces a value that indicates the presence of the hard disks in the SCSI backplane.

Table 47: Drive Presence Status Byte Format

Bit(s)	Name	Description
7	Reserved	Reserved for future use.
6	Primary/Secondary or Low/High	Read only. Logic 1 indicates the backplane is the primary backplane in a chassis/system. Logic 0 indicates the backplane is the secondary backplane in a chassis/system. This corresponds to the SCSI ID jumper. • Low = Primary • High = Secondary
5	Force Update	Read only, active low. When active (low), the “Force firmware update” jumper has been moved to its active position. When inactive (high), the firmware on the backplane should operate as normal.
4::0	DRVPRSN[4::0]	Drive Present bits. A set bit indicates that a drive is physically present in the corresponding slot. Bit 0 corresponds to backplane slot 0, etc.

4.5.1.6 SCSI I/O Region (D000h – DFFFh)

Provides Read/Write access to the SCSI device as memory-mapped I/O. The 53C80S SCSI chip on the Hot-swap SCSI Backplane decodes three of the 12 address lines for this memory region. SCSI controller registers are addressed with an offset of D000h (i.e., I/O address 3Ah for the SCSI controller is physical address D03Ah).

4.5.1.7 Program and Data RAM Region (E000h – FFFFh)

This Read/Write memory region accesses 8 KB of RAM available for general usage. The hardware supports this memory region as both data memory and program memory. During normal operation, the microcontroller executes code from the program memory region (Flash). During the firmware upgrade process, the microcontroller executes code from the program and data RAM memory region.

4.5.2 I/O Ports

80C51 architecture provides four memory-mapped I/O ports:

- Port #0 (P0)
- Port #1 (P1)
- Port #2 (P2)
- Port #3 (P3)

4.5.2.1 P0

Since the firmware for the microcontroller is located in a Flash memory device (for ease of debugging and field upgradeability), and all memory and memory-mapped I/O are located outside the microcontroller, P0 is used as a time-multiplexed low-order address and data bus. It is not used for general I/O purposes.

4.5.2.2 P1

P1 has two dedicated-function signals, and six implementation specific control signals, as shown in Table 48.

Table 48: P1 Functions

Bit	Name	I/O	Fixed 1	Function
7	SDA	I/O	Y	I^2C Serial Data signal for the intra-chassis I^2C bus.
6	SCL	I/O	Y	I^2C Serial Clock signal for the intra-chassis I^2C bus.
5	I2C_ADDR_CNTRL	I	N	I^2C address control: • 1=primary HSBP controller • 0=secondary HSBP controller Following the I^2C Address Allocation Specification the primary HSBP controller has an I^2C address of 0xC0 and the secondary controller has an I^2C address of 0xC2.
4	SCSI ctrlr reset	O	N	Reset SCSI controller. • If 0, places the 53C80S SCSI chip into reset • If 1, the SCSI interface chip comes out of reset and operates normally.
3	SCSI_DRQ	I	N	SCSI DMA Request. Connected to the DRQ signal of the 53C80S SCSI chip. Allows the microcontroller to use the DMA transfer capabilities of the SCSI interface chip, which results in higher performance.
2	Fan Power	O	N	Switches fan power on or off. • 0=on • 1=off
1	SDA_Local	I/O	N	Serial Data for private I^2C connection to temperature sensor
0	SCL_Local	O	N	Serial Clock for private I^2C connection to temperature sensor

1. "Fixed" indicates whether the function/pin is defined by the microcontroller pinout (fixed) or implementation-specific (not fixed)

4.5.2.3 P2

P2 is the high-order address and data bus for external device access. It is not used for general I/O purposes.

4.5.2.4 P3

P3 provides four dedicated function signals, and four implementation specific control signals, as shown in Table 49.

Table 49: P3 Functions

Bit	Name	I/O	Fixed 1	Function
7	RD_L	O	Y	Read strobe. Indication from the microcontroller that the current bus cycle is a read operation.
6	WR_L	O	Y	Write strobe. Indication from the microcontroller that the current bus cycle is a write operation.
5	Fan 2	I	N	Fan 2 tachometer input.
4	Fan 1	I	N	Fan 1 tachometer input.
3	INT1_L	I	Y	Interrupt 1. Connected to the SCSI bus reset signal RST_L.
2	INT0_L	I	Y	Interrupt 0. Connected to the 53C80S SCSI IRQ signal.
1	Reserved	-	N	Reserved for future use.
0	HSBP_SEL	I	N	SCSI backplane select: 0=5 x 1” LVD/SE SCSI Backplane; 1=3 x 1.6” LVD/SE SCSI Backplane.

1. “Fixed” indicates whether the function/pin is defined by the microcontroller pinout (fixed) or implementation-specific (not fixed).

4.6 Programming Information

This chapter describes briefly the programming and firmware information for the Hot-swap SCSI Backplane. The information in this section is an overview only. For detailed information, refer to *Hudson/Cabrillo-2 Hot-swap Controller Interface EPS*.

The firmware for the Hot-swap SCSI Backplane is stored in the Flash ROM. It is divided into two sections; the 8KB boot block area and the 24KB operational code area. The boot block area contains the basic IMB communication routines and the firmware transfer commands. The code in this area is permanently stored and can only be updated if the Flash Boot Block Update jumper is in the proper position. The operational code area contains the run-time code, including the SCSI and SAF-TE routines, monitoring routines, and IMB routines. All code in this area can be updated using the firmware transfer commands.

4.6.1 Firmware Support Requirements

See the *Hudson/Cabrillo-2 Hot-swap Controller Interface EPS*.

4.6.1.1 Software Upgrade Process

Firmware update is accomplished by entering Firmware Transfer Mode, either through an IMB command or by placing the Firmware Update Jumper in the Force Update position. The jumper position can be changed only when the system is powered off. Firmware transfers are done only through the IMB.

If an IMB command was used to enter Firmware Transfer Mode, the corresponding exit command is used to return to normal operation. If the jumper was used, the system must be powered down and the jumper restored to the Normal Operation position to return to Operational Mode.

4.7 External Interface Specifications

This chapter specifies electrical characteristics of the connector pins.

4.7.1 Connector Specifications

Table 50 shows the quantity, manufacturers, and Intel part numbers for connectors on the LVD/SE SCSI Backplane. Refer to the manufacturers' documentation for more information on connector mechanical specifications.

Table 50: Connector Specifications

Item	Qty.	Manufacturer(s) and Part #	Description
1	2	TYCO* (794697-1) Intel P/N (107774-005)	4-pin (1x4) power connector
2	2	Molex* (22-05-3031) Intel P/N (109786-004)	1x3 RA fan header
3	1	Molex (22057045) Intel P/N (739197-001)	4-pin (1x4) I^2C connector
4	5	FCI-BERG* (72436-003) Intel P/N (626530-382)	80-pin SCA-2 connector
5	1	Foxconn* (EH06099) Intel P/N (201082-565	PCI connector
6	1	TYCO (788644-7) Intel p/n (A03228-001)	68-pin SCSI pressfit input connector

4.7.2 SCSI Input Connector 68P

The SCSI input connector is a non-shielded device connector.

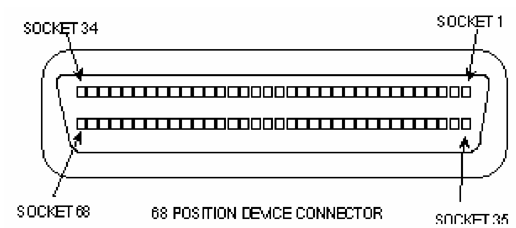


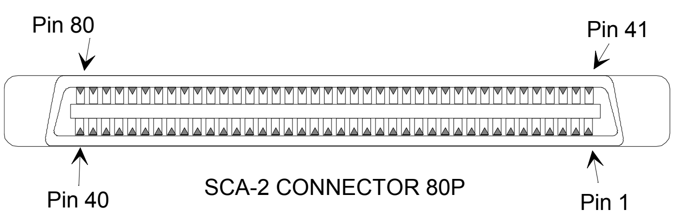
Figure 25: SCSI Input connector 68P Non-Shielded

Table 51: SCSI Input connector (J1D1)

Signal Name	Connector Contact Number	SCSI Bus Conductor Number	SCSI Bus Conductor Number	Connector Contact Number	Signal Name
+DB(12)	1	1	2	35	-DB(12)
+DB(13)	2	3	4	36	-DB(13)
+DB(14)	3	5	6	37	-DB(14)
+DB(15)	4	7	8	38	-DB(15)
+DB(P1)	5	9	10	39	-DB(P1)
+DB(0)	6	11	12	40	-DB(0)

Signal Name	Connector Contact Number	SCSI Bus Conductor Number	SCSI Bus Conductor Number	Connector Contact Number	Signal Name
+DB(1)	7	13	14	41	-DB(1)
+DB(2)	8	15	16	42	-DB(2)
+DB(3)	9	17	18	43	-DB(3)
+DB(4)	10	19	20	44	-DB(4)
+DB(5)	11	21	22	45	-DB(5)
+DB(6)	12	23	24	46	-DB(6)
+DB(7)	13	25	26	47	-DB(7)
+DB(P)	14	27	28	48	-DB(P)
GND	15	29	30	49	GND
GND	16	31	32	50	GND
RESERVED	17	33	34	51	RESERVED
RESERVED	18	35	36	52	RESERVED
RESERVED	19	37	38	53	RESERVED
GND	20	39	40	54	GND
+ATN	21	41	42	55	-ATN
GND	22	43	44	56	GND
+BSY	23	45	46	57	-BSY
+ACK	24	47	48	58	-ACK
+RST	25	49	50	59	-RST
+MSG	26	51	52	60	-MSG
+SEL	27	53	54	61	-SEL
+C/D	28	55	56	62	-C/D
+REQ	29	57	58	63	-REQ
+I/O	30	59	60	64	-I/O
+DB(8)	31	61	62	65	-DB(8)
+DB(9)	32	63	64	66	-DB(9)
+DB(10)	33	65	66	67	-DB(10)
+DB(11)	34	67	68	68	-DB(11)

4.7.3 SCSI SCA-2 Drive Connector



Note: In this board SCA-2 PressFit connector is used on the secondary side of the board.

Figure 26: SCA-2 Connector 80P

Table 52: SCA-2 Connectors (J3E1, J3D1, J3C1, J3B1, J3A1)

Pin	80pin connector contact and signal name		Pin	80pin connector contact and signal name	
1	12V PreCharge	(L)	41	12V Ground	(L)
2	12V	(S)	42	12V Ground	(L)
3	12V	(S)	43	12V Ground	(L)
4	12V	(S)	44	Mated 1	(S)
5	3.3V	(S)	45	3.3V PreCharge	(L)
6	3.3V	(S)	46	DIFFSNS	(L)
7	-DB(11)	(S)	47	+DB(11)	(S)
8	-DB(10)	(S)	48	+DB(10)	(S)
9	-DB(9)	(S)	49	+DB(9)	(S)
10	-DB(8)	(S)	50	+DB(8)	(S)
11	-I/O	(S)	51	+I/O	(S)
12	-REQ	(S)	52	+REQ	(S)
13	-C/D	(S)	53	+C/D	(S)
14	-SEL	(S)	54	+SEL	(S)
15	-MSG	(S)	55	+MSG	(S)
16	-RST	(S)	56	+RST	(S)
17	-ACK	(S)	57	+ACK	(S)
18	-BSY	(S)	58	+BSY	(S)
19	-ATN	(S)	59	+ATN	(S)
20	-DB(P)	(S)	60	+DB(P)	(S)
21	-DB(7)	(S)	61	+DB(7)	(S)
22	-DB(6)	(S)	62	+DB(6)	(S)
23	-DB(5)	(S)	63	+DB(5)	(S)
24	-DB(4)	(S)	64	+DB(4)	(S)
25	-DB(3)	(S)	65	+DB(3)	(S)
26	-DB(2)	(S)	66	+DB(2)	(S)
27	-DB(1)	(S)	67	+DB(1)	(S)
28	-DB(0)	(S)	68	+DB(0)	(S)
29	-DB(P1)	(S)	69	+DB(P1)	(S)
30	-DB(15)	(S)	70	+DB(15)	(S)
31	-DB(14)	(S)	71	+DB(14)	(S)
32	-DB(13)	(S)	72	+DB(13)	(S)
33	-DB(12)	(S)	73	+DB(12)	(S)
34	5V	(S)	74	Mated 2	(S)
35	5V	(S)	75	5V Ground	(L)
36	5V PreCharge	(L)	76	5V Ground	(L)
37	Spindle Sync	(L)	77	Active LED Out	(L)
38	RMT_START	(L)	78	DLYD_START	(L)
39	SCSI ID (0)	(L)	79	SCSI ID (1)	(L)
40	SCSI ID (2)	(L)	80	SCSI ID (3)	(L)

4.7.4 I^{2}C Connector

Table 53: I^{2}C Connector (J2A1)

Pin	Signal
1	I2C_ADDR_CNTRL
2	IMB_CLK
3	GND
4	IMB_SDA

4.7.5 Power Connector

Table 54: Power Connector (J4A1, J3A2)

Pin	Signal
1	12V
2	GND
3	GND
4	+5V

4.7.6 Fan 3-pin Connector

There are two 3-pin fan connectors on the backplane. Table 55 shows the pin-out of each connector. Fan power is defaulted to a voltage close to +12V and can be controlled by the SAF-TE card to be turned off.

Table 55: Fan Connector

Pin	Signal (J2A2)	Signal (J2A3)
1	GND	GND
2	FAN1 (tach)	FAN2 (tach)
3	Fan power	Fan power

4.7.7 SAF-TE PCI Connector Interface

The PCI connector interfaces the LVD bus to the AIC3860 on the SAF-TE card.

Table 56: PCI connector (J5C1)

Pin	Signal	Pin	Signal
A1	FAULT_L:4	B1	GND
A2	LVD_SCSI:1	B2	LVD_SCSI:0
A3	LVD_SCSI:28	B3	LVD_SCSI:27

Pin	Signal	Pin	Signal
A4	LVD_SCSI:3	B4	LVD_SCSI:2
A5	LVD_SCSI:30	B5	LVD_SCSI:29
A6	LVD_SCSI:5	B6	LVD_SCSI:4
A7	LVD_SCSI:32	B7	LVD_SCSI:31
A8	LVD_SCSI:7	B8	LVD_SCSI:6
A9	LVD_SCSI:34	B9	LVD_SCSI:33
A10	LVD_SCSI:9	B10	LVD_SCSI:8
A11	LVD_SCSI:36	B11	LVD_SCSI:35
A12	LVD_SCSI:11	B12	LVD_SCSI:10
A13	LVD_SCSI:38	B13	LVD_SCSI:37
A14	LVD_SCSI:13	B14	LVD_SCSI:12
A15	LVD_SCSI:40	B15	LVD_SCSI:39
A16	LVD_SCSI:15	B16	LVD_SCSI:14
A17	LVD_SCSI:42	B17	LVD_SCSI:41
A18	LVD_SCSI:17	B18	LVD_SCSI:16
A19	LVD_SCSI:44	B19	LVD_SCSI:43
A20	LVD_SCSI:19	B20	LVD_SCSI:18
A21	LVD_SCSI:46	B21	LVD_SCSI:45
A22	LVD_SCSI:21	B22	LVD_SCSI:20
A23	LVD_SCSI:48	B23	LVD_SCSI:47
A24	LVD_SCSI:23	B24	LVD_SCSI:22
A25	LVD_SCSI:50	B25	LVD_SCSI:49
A26	LVD_SCSI:25	B26	LVD_SCSI:24
A27	LVD_SCSI:52	B27	LVD_SCSI:51
A28	LVD_SCSI:53	B28	LVD_SCSI:26
A29	GND	B29	GND
A30	DRVPRSN:0	B30	TP_DRVACT:0
A31	DRVPRSN:1	B31	TP_DRVACT:1
A32	DRVPRSN:2	B32	TP_DRVACT:2
A33	DRVPRSN:3	B33	TP_DRVACT:3
A34	DRVPRSN:4	B34	TP_DRVACT:4
A35	GND	B35	GND
A36	DIFFSENSE	B36	PWRON:0
A37	FAN_CNTRL	B37	PWRON:1
A38	FAN1_TACH	B38	PWRON:2
A39	FAN2_TACH	B39	PWRON:3
A40	GND	B40	PWRON:4
A41	IMB_SDA	B41	GND
A42	IMB_CLK	B42	VCC
A43	I2C_ADDR_CNTRL	B43	VCC
A44	GND	B44	GND
A45	GND	B45	GND
A46	GND	B46	GND
A47	GND	B47	+12V

Pin	Signal	Pin	Signal
A48	GND	B48	+12V
A49	GND	B49	GND
A50	N/C	B50	N/C
A51	N/C	B51	N/C
A52	GND	B52	GND
A53	GND	B53	GND
A54	GND	B54	GND
A55	GND	B55	GND
A56	GND	B56	GND
A57	GND	B57	GND
A58	GND	B58	GND
A59	FAULT_L:3	B59	GND
A60	FAULT_L:2	B60	GND
A61	FAULT_L:1	B61	GND
A62	FAULT_L:0	B62	GND

4.8 Cables

4.8.1 Signal Cables

One Wide SCSI cable connects the embedded PCI SCSI controller card on the baseboard and one cable connects I^2C from either the front panel or the baseboard.

4.8.2 Power Cables

Two power cables, from peripheral devices to the disk backplane and one fan cable connects the fans to the disk backplane.

4.9 Mechanical Specifications

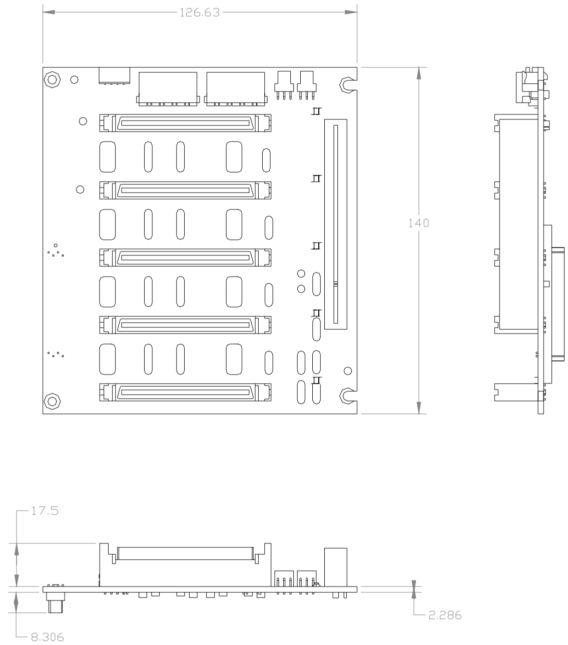


Figure 27: Hotswap Backplane Mechanical Drawing

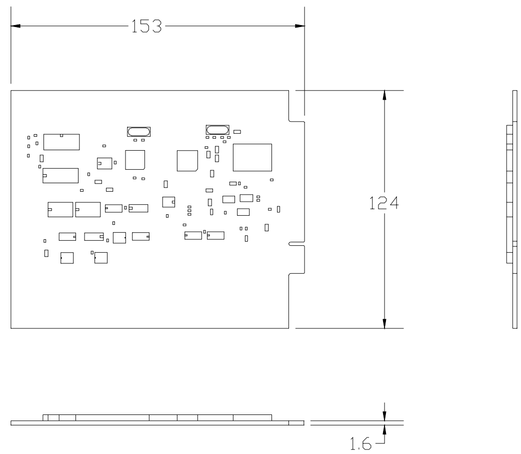


Figure 28: SAF-TE Addin Card Mechanical Drawing

5. System Boards

This chapter describes the design and features of the SRSH4 system boards.

5.1 Front Panel Board

The front panel board has five momentary switches and six LEDs visible through the chassis front bezel. The five switches control power on/off, sleep mode, system reset, chassis ID, and NMI. The NMI switch is accessible via a small hole in the front of the chassis once the front bezel door is open and requires a small instrument to push it.

The six front panel LEDs are:

- Power-on LED: Sold green indicates system power in a steady-on state and blinking green indicates Advanced Configuration and Power Interface (ACPI) sleep mode
- LAN 1 activity LED: Green during network activity
- LAN 2 activity LED: Green during network activity
- HDD activity LED: Green indicates system hard drive activity and amber indicates hard drive fault
- Chassis ID LED: Blue LED provides system identification to aid in servicing
- System status: Green indicates normal system status and amber indicates fault for power supply, hard drive, or cooling subsystem.

The front panel also contains five connectors:

- A 34-pin connector provides control and status information to/from the baseboard.
- Two internal 10-pin connectors provide data and power for the USB and serial port B RJ45 ports
- Two external connectors provide data and power for the external USB and RJ-45 Serial B ports

The front panel board mounts to sheet metal at the front of the system and this is secured to the chassis with one 6-32 screw.

In addition, the front panel board has a 24C02LM8 serial EEPROM for Field Replaceable Unit information access. The 24C02LM8 has an I^2C slave address of 0xA0/A1h.The front panel board has a DS1621S digital thermostat for measuring ambient air temperature into the server system. The DS1621S has an I^2C slave address of 0x9A/9Bh.

5.1.1 Board Layout

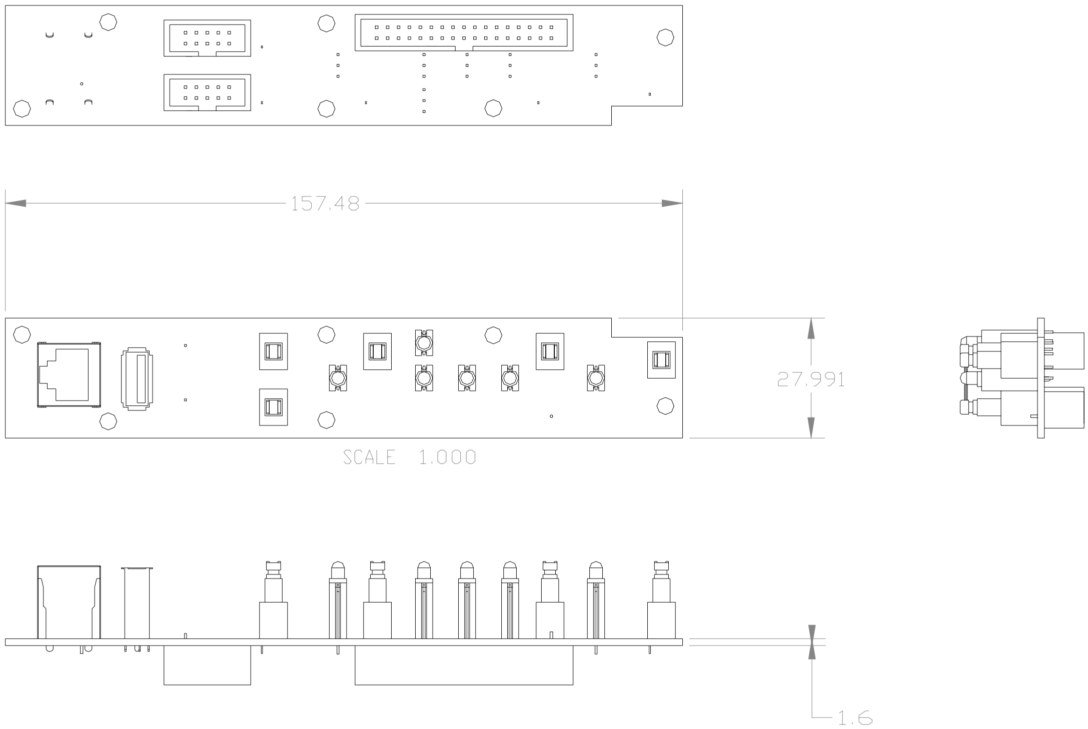


Figure 29: Fan Board Layout

5.1.2 Connector Pinouts

Table 57: Front Panel Signal Connector (P5)

Pin	Signal	Pin	Signal
1	PWR_LED_PWR	2	+5VSB
3	No pin	4	FAN_FAIL_PWR
5	PWR_LED-0	6	PWR_FAULT-0
7	HDD_ACT_PWR	8	No connection
9	HDD_ACT-0	10	PWR_FAULT-0
11	PWR_SW-0	12	NIC1_ACT_PWR
13	GND	14	NIC1_ACT-0
15	RESET_SW-0	16	I2C_SDA
17	GND	18	I2C_SCL
19	SLEEP_SW-0	20	CI
21	GND	22	NIC2_ACT_PWR
23	NMI_SW-0	24	NIC2_ACT-0
25	No pin	26	No pin
27	ID_LED_PWR	28	No connection
29	ID_LED-0	30	STATUS_LED-0
31	ID_SW-0	32	No connection
33	GND	34	HDD_FAULT-0

Table 58: USB Port 3 Input Connector (P3)

Pin	Signal	Pin	Signal
1	No connection	2	USBP3_VCC
3	No connection	4	USB_P3_N
5	No connection	6	USB_P3_P
7	No connection	8	USBP3_GND
9	No Pin	10	GND

Table 59: USB Port 3 (P2)

Pin	Signal
1	USBP3_VCC
2	USB_P3_N
3	USB_P3_P
4	USBP3_GND

Table 60: Serial Port B Input Connector (P4)

Pin	Signal	Pin	Signal
1	No connection	2	SIODSR+00
3	SIORXD+00	4	SIORTS+00
5	SIOTXD+00	6	SIOCTS+00
7	SIODTR+00	8	SIORI+00
9	GND	10	No Pin

Table 61: RJ45 Serial Port B (P1)

Pin	Signal
1	SIORTS+00
2	SIODTR+00
3	SIOTXD+00
4	GND
5	SIORI+00
6	SIORXD+00
7	SIODSR+00
8	SIOCTS+00

5.2 Fan Distribution Board

The SRSH4 fan distribution board (FDB) provides power, speed control, tachometer monitoring, and presence detect for the six system fans. The fan distribution board mounts to fan bay sheet metal at the center of the system and this is secured with four 6-32 screws.

The fan distribution board is populated with six 127mm fans.

Amber LEDs on the fan board indicate a fan fault condition. These LEDs can be viewed when the chassis rear top cover is removed. Fan bank fault condition is generated by server management from either a missing fan presence signal or from too slow of a fan tachometer reading.

The speed of the system fans is controlled by pulse width modulation (PWM) of power. PWM control of fan speed is implemented by toggling fan power between +12V and +5V power rails. This is done via a server management control signal input to a power FET. In the event of a fault or over temperature condition, only +12V power is applied to all fans thus providing maximum fan speed and cooling capability. In addition, fan power is fused to improved system availability in the event of a fan fault.

5.2.1 Board Layout

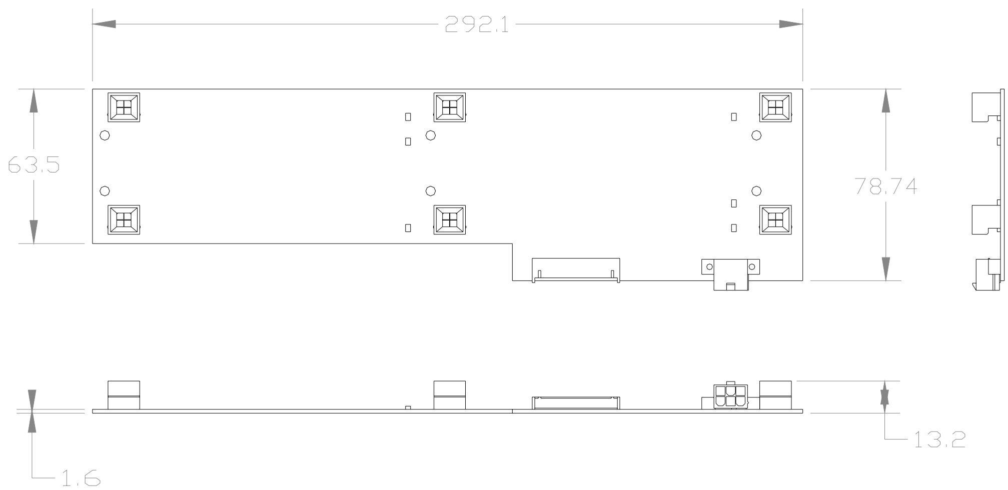


Figure 30: Fan Board Layout

5.2.2 Connector Pinouts

Table 62: Power Connector (P2)

Pin	Signal	Pin	Signal
1	+12V	4	+12V
2	No connection	5	No connection
3	GND	6	GND

Table 63: Front Left Fan Bank Connector (P3)

Pin	Signal	Pin	Signal
1	LFSENSE+0	3	FANLFPOW+0
2	GND	4	FPRESLF-0

Table 64: Front Middle Fan Bank Connector (P4)

Pin	Signal	Pin	Signal
1	MFSENSE+0	3	FANMFPOW+0
2	GND	4	FPRESMF-0

Table 65: Front Right Fan Bank Connector (P5)

Pin	Signal	Pin	Signal
1	RFSENSE+0	3	FANRFPOW+0
2	GND	4	FPRESRF-0

Table 66: Rear Left Fan Bank Connector (P6)

Pin	Signal	Pin	Signal
1	LRSENSE+0	3	FANLRPOW+0
2	GND	4	RPRESLR-0

Table 67: Rear Middle Fan Bank Connector (P7)

Pin	Signal	Pin	Signal
1	MRSENSE+0	3	FANMRPOW+0
2	GND	4	RPRESMR-0

Table 68: Rear Right Fan Bank Connector (P8)

Pin	Signal	Pin	Signal
1	RRSENSE+0	3	FANRRPOW+0
2	GND	4	RPRESRR-0

Table 69: Fan Signal Connector (P1)

Pin	Signal	Pin	Signal
1	RPRESLR-1	2	RPRESMR-1
3	REARPCILED+0	4	RPRESRR-1
5	LRSPEED+0	6	FPRESLF-1
7	LRSENSE+0	8	FPRESMF-1
9	GND	10	FPRESRF-1
11	RFLED+0	12	+5V
13	RFSPEED+0	14	No connection
15	RFSENSE+0	16	No connection
17	GND	18	RRLED+0
19	MFLED+0	20	+5V
21	MFSPEED+0	22	RRSPEED+0
23	MFSENSE+0	24	RRSENSE+0
25	GND	26	MRLED+0
27	FRNTPCILED+0	28	+5V
29	LFSPEED+0	30	MRSPEED+0
31	LFSENSE+0	32	MRSENSE+0
33	GND	34	+5V

5.3 HPIB Board

The SRSH4 hot plug indicator board (HPIB) provides power on and status LEDs for hot plug PCI-X adapters. Power can be cycled to four hot plug PCI-X adapters via software or via individual magnetic switches actuated by mechanical latches retaining the PCI-X adapters.

The mechanical latch releases the PCI-X adapter filler panel and can be accessed from inside the system. Two pop rivets secure this board.

LEDs can be viewed from both inside and outside the system and indicate the functional state of the hot plug PCI-X adapter slots.

- A green LED indicates power to the hot plug slot is on.
- An yellow LED indicates there is a fault on the hot plug slot.
- A blinking green LED indicates power is transitioning on the hot plug slot.

Slots 5 through 8 are hot-plug PCI-X and slots 1 through 4 are non-hot plug PCI. See Figure 31 for slot numbering sequence.

5.3.1 Board Layout

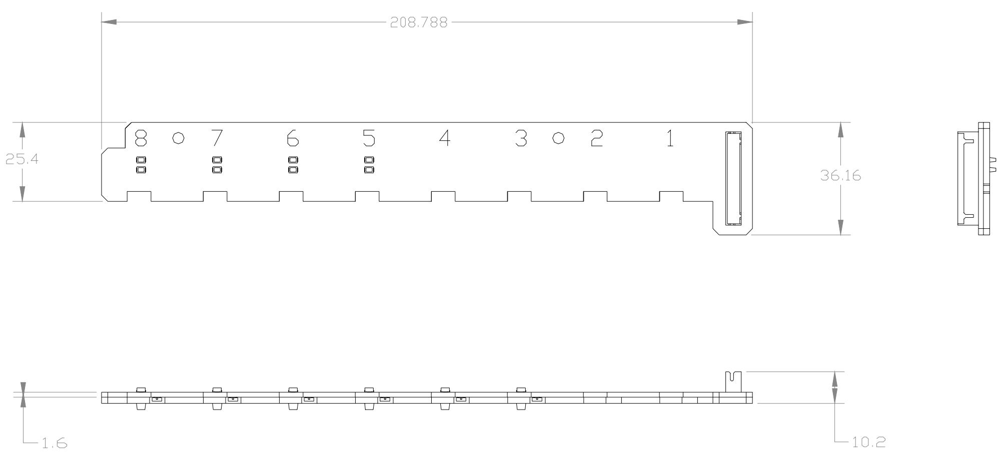


Figure 31: HPIB Board Layout

5.3.2 Connector Pinouts

Table 70: HPIB Signal Connector (P1)

Pin	Signal	Description	Pin	Signal	Description
1	+3.3Vstandby	Switch power	2	+5V	LED power
3	GND	GND	4	GND	GND
5	No connection	–	6	No connection	–
7	No connection	–	8	No connection	–
9	SLT31SW-00	Switch – slot 5 : C1	10	SLT32SW-00	Switch – slot 6 : C2
11	SLT41SW-00	Switch – slot 7 : D1	12	SLT42SW-00	Switch – slot 8 : D2
13	No connection	–	14	No connection	–
15	No connection	–	16	No connection	–
17	No connection	–	18	No connection	–
19	No connection	–	20	No connection	–
21	ATTEN310-10	Yellow LED – slot 5 : C1	22	ATTEN311-10	Green LED – slot 5 : C1
23	ATTEN320-10	Yellow LED – slot 6 : C2	24	ATTEN321-10	Green LED – slot 6 : C2
25	ATTEN410-10	Yellow LED – slot 7 : D1	26	ATTEN411-10	Green LED – slot 7 : D1
27	ATTEN420-10	Yellow LED – slot 8 : D2	28	ATTEN421-10	Green LED – slot 8 : D2

5.4 Floppy Adapter Board

The ½” slim line floppy peripheral connection is a short length of Flexible Circuit, the power connector is a right angle four-position header and the cable interface is a standard vertical floppy header (with pin #3 pulled). One 6-32 screw are used to secure this board.

5.4.1 Board Layout

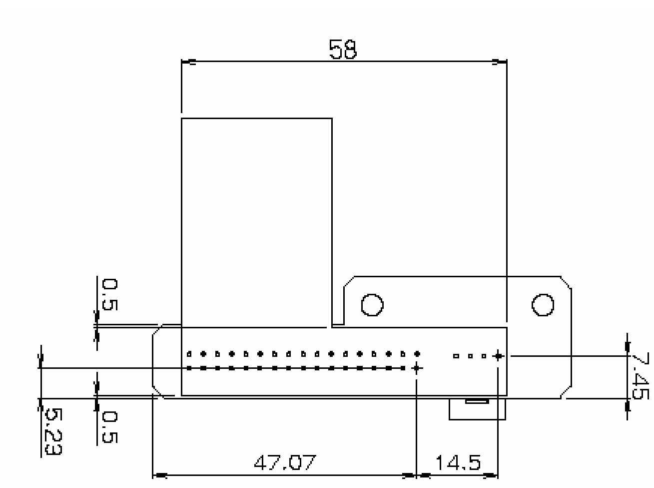


Figure 32: Floppy Adapter Board Layout

5.4.2 Connector Pinouts

Table 71: 34-Position Floppy Connector Pin-Out

Pin	Signal	Signal	Pin
1	No connection	HD IN/ HD Out/ Open	2
3	No pin	No connection	4
5	No connection	No connection	6
7	GND	FD_INDEX_L	8
9	GND	Drive Select 0	10
11	GND	Drive Select 1	12
13	GND	No connection	14
15	GND	Motor On	16
17	GND	Direction Select	18
19	GND	STEP	20
21	GND	Write Data	22
23	GND	Write Gate	24
25	GND	Track 00	26
27	GND	Write Protect	28
29	GND	Read Data	30
31	GND	Side One Select	32
33	GND	Disk Change/ Ready	34

Table 72: Floppy Adapter Board Power Connector

Pin	Signal
1	+5V
2	GND
3	GND
4	No Connection

Table 73: FFC Cable Pin-Out

Pin	Signal	Signal	Pin
1	+5V	INDEX	2
3	+5V	DRIVE SELECT	4
5	+5V	DISK CHANGE	6
7	No connection	READY	8
9	HD OUT (HD AT HIGHT LEVEL)	MOTOR ON	10
11	No connection	DIRECT SELECT	12
13	No connection	STEP	14
15	GND	WRITE DATA	16
17	GND	WRITE GATE	18
19	GND	TRACK 00	20
21	No connection	WRITE PROTECT	22
23	GND	READ DATA	24
25	GND	SIDE ONE SELECT	26

5.5 CD-ROM Adapter Board

The CD-ROM adapter board converts the 50 pin JAE signal interface connector of the ½" slim line CD-ROM device to a standard 40 pin IDE interface connector. The CD-ROM peripheral connector is a .8mm 50 pin JAE receptacle, the power and signal cable interface are standard .100" center-line headers (40 pin IDE header has pin #20 pulled). The CD-ROM adapter board supports cable select feature. Three M2 screws are used to secure this board to the CD-ROM device.

5.5.1 Board Layout

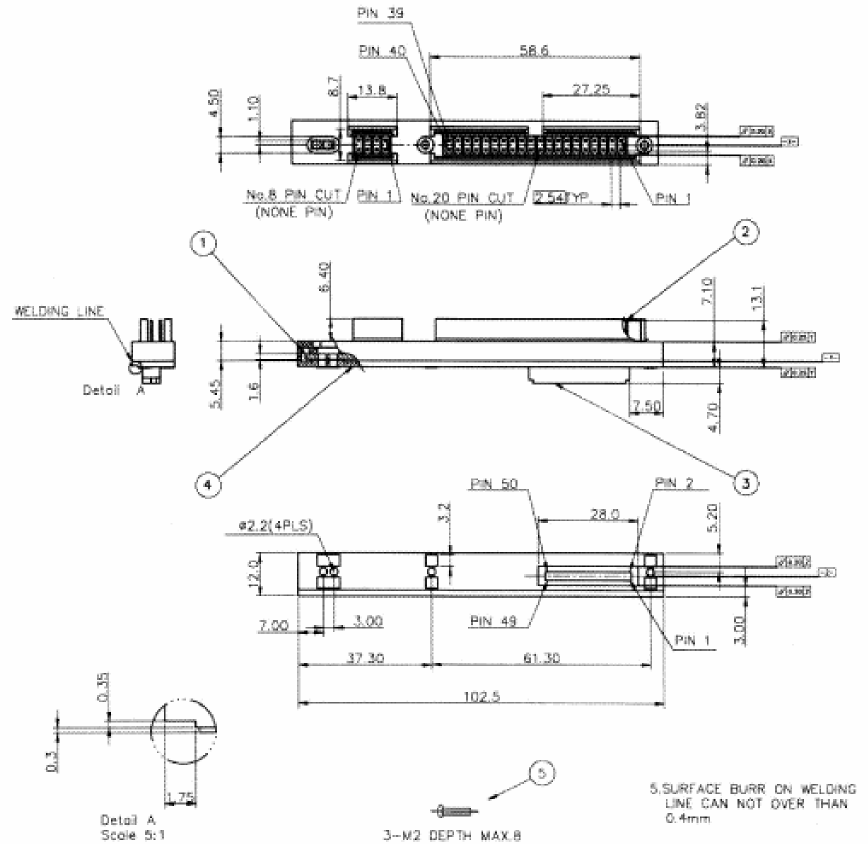


Figure 33: CD-ROM Adapter Board Layout

5.5.2 Connector Pinouts

Table 74: CD-ROM Adapter Board 40 Position IDE Connector

Pin	Signal	Pin	Signal
1	RESET-	2	GND
3	DD7	4	DD8
5	DD6	6	DD9
7	DD5	8	DD10
9	DD4	10	DD11
11	DD3	12	DD12
13	DD2	14	DD13
15	DD1	16	DD14
17	DD0	18	DD15
19	GND	20	No pin
21	DMARQ	22	GND
23	DIOW-	24	GND
25	DIOR-	26	GND
27	IORDY	28	CSEL
29	DMACK-	30	GND
31	INTRQ	32	No connection
33	DA1	34	No connection
35	DA0	36	DA2
37	CS0-	38	CS1-
39	DASP-	40	GND

Table 75: CD-ROM JAE Connector Pin-Out

Pin	Signal	Signal	Pin
1	Audio LOUT	Audio ROUT	2
3	Audio GND	GND	4
5	RESET-	DD8	6
7	DD7	DD9	8
9	DD6	DD10	10
11	DD5	DD11	12
13	DD4	DD12	14
15	DD3	DD13	16
17	DD2	DD14	18
19	DD1	DD15	20
21	DD0	DMARQ	22
23	GND	DIOR-	24
25	DIOW-	GND	26
27	IORDY	DMACK-	28
29	INTRQ	No connection	30
31	DA1	PDIAG-	32
33	DA0	DA2	34
35	CS0-	CS1-	36
37	DASP-	+5V	38
39	+5V	+5V	40
41	+5V	+5V	42
43	GND	GND	44
45	GND	GND	46
47	CSEL	GND	48
49	RESERV	RESERV	50

Table 76: Power Connector

PIN	SIGNAL	PIN	SIGNAL
1	Audio LOUT	2	+5V
3	GND	4	GND
5	GND	6	GND
7	Audio ROUT	8	No pin

5.6 ICMB Board

The SRSH4 ICMB board complies with requirements for an SSI midrange server. This board passes ICMB data signals from the SSH4 baseboard to two keyed RJ45 ports. The ICMB board mounts to a sheetmetal bracket located at the rear panel of the system with two 4-40 screws and this bracket is then secured to the chassis with one 6-32 screw.

5.6.1 Board Layout

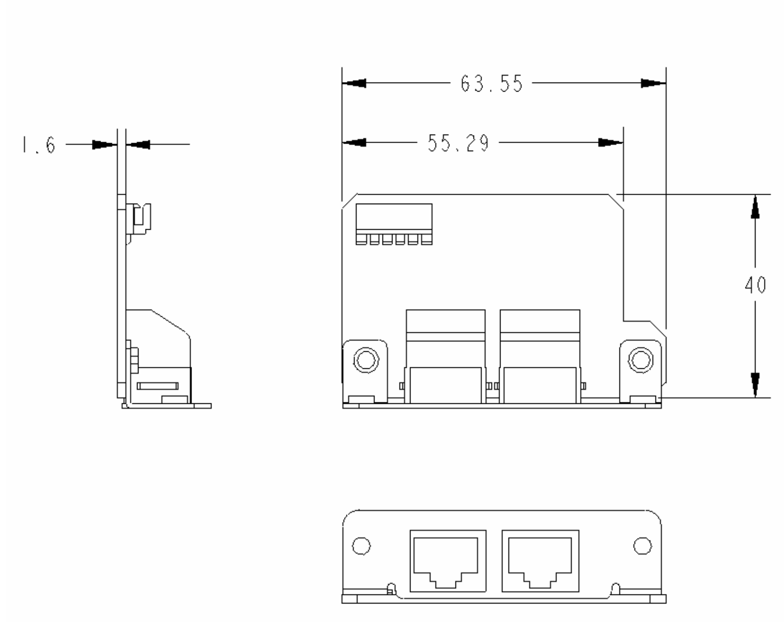


Figure 34: ICMB Board Layout

5.6.2 Connector Pinouts

Table 77: Keyed RJ45 ICMB Port Connector (P1 & P2)

Pin	Signal
1	Tx/Rx+
2	Tx/Rx-
3	GND
4	No connection
5	GND
6	No connection
7	No connection
8	No connection

Table 78: ICMB Signal Connector to Baseboard (P3)

Pin	Signal
1	XP05S
2	ICMB_TX
3	ICMB_TX_ENB
4	ICMB_RX
5	GND

6. Hardware Configuration

6.1 System Configuration

SRSH4 server system is available in one standard configuration described in Table 79.

Table 79: System Configuration

Feature	High Integration System
Chassis	1
Front bezel with handles (black)	1
SSH4 baseboard	1
SSH4 processor board	1
SSH4 memory board	1
Front panel board	1
Hot plug indicator board	1
Fan distribution board	1
Power supply cage	1
430W Power supply modules	2
½” Floppy drive (black)	1
½” CD-ROM drive (black)	1
5 x 1” HDD bay (black)	1
System fans	6
Resource kit (2 AC power cords, resource CD, ISM CD, 5¼” rails & screws)	1
Welcome mat	1
System packaging	1
Rack slide rail kit	0
Processors	0
DDR DRAM modules	0
SCSI hard disk drives	0

6.2 Spares / Accessories

SRSH4 server system comes with several spares and accessories described in Table 80.

Table 80: Spare / Accessory List

Spare/Accessory	Description	Min Order
Baseboard	SSH4 baseboard using Serverworks Serverset IV Grand Champion HE Chipset.	1
Processor board	SSH4 processor board	1
Memory board	SSH4 DDR DRAM memory module	1
Power module	430 W SRSH4 power module	1
Rack kit	Rack slide rails, nut clips, mounting hardware, and assembly instructions	1
1” x 5 hard drive bay	SCSI hard drive bay supporting up to five 1” hard drives	1
1” hard drive carrier	1” black hard drive carrier with mounting screws	10
ICMB kit	ICMB board, cable, mounting hardware and assembly instructions	1
Cable kit	All SRSH4 cables (except for PCI and external SCSI cables)	1
PCI SCSI cable	Cable from internal PCI adapter card to internal SCSI hard drive bay	5
External SCSI cable	Cable from internal SCSI connection to external SCSI knockouts on back panel	5
5.25” bay SCSI cable	Cable from baseboard to 5.25” peripheral device (includes LVD/SE terminator)	5
Retention module kit	Set of four processor retention modules, screws, and assembly instructions	1
System board kit	Fan board, front panel board, HPIB, slim floppy adapter, and slim CD-ROM adapter	1
Fan kit	One 127mm system fan	1
Integrator parts kit	Includes replacement screws, rivets, gaskets, processor installation parts, and other plastic parts	1

7. Product Regulatory Compliance Specifications

The SRSH4 server system meets the following Safety and EMC specifications.

7.1 Product Safety Compliance

Table 81: Product Safety Compliance

Country	Standard
USA/Canada	UL60 950 – 3rd Edition
European Union	EN60 950 Low Voltage Directive, 73/23/EEC (CE Mark)
Nordic Countries	EMKO-TSE (74-SEC) 207/94
Russia	GOST R 50377-92
Argentina	IRAM – Resolution No. 92/98
International	IEC60 950 3rd Edition

7.2 Product EMC Compliance

Table 82: Product EMC Compliance

Country	Standard
USA	FCC 47 CFR Parts 2 and 15, Class A Limit, Radiated and Conducted Emissions
Canada	ICES-003, Class A Limit, Radiated and Conducted Emissions
Europe	EMC Directive, 89/336/EEC (CE Mark) EN55022, Class A Limit, Radiated and Conducted Emissions EN55024 (Immunity) EN61000-3-2 / EN610003-3, Harmonic Currents / Voltage Flicker
Russia	GOST R 29216-91, Class A Limit, Radiated and Conducted Emissions GOST R 50628-95 (Immunity)
Australia/New Zealand	AS/NZS 3548, Class A Limit, Radiated and Conducted Emissions
Taiwan	BSMI, CNS13438, Class A Limit, Radiated and Conducted Emissions
Korea	RRL, MIC Notices No 1997-41 and 1997-42, Class A Limit, Radiated and Conducted Emissions
Japan	VCCI, (via CISPR 22, Class A Limit).
International	CISPR 22, Class A Limit, Radiated and Conducted Emissions CISPR 24 (Immunity)

7.3 Regulatory Markings

The SRSH4 server system will be marked with the following regulatory markings.

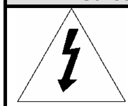
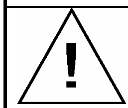
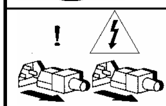
Table 83: Regulatory Markings

Regulatory Mark	Symbol
cULus Listing Marks	LISTED ITE E139761 C US
German GS Mark	Nemko GS geprüfte Sicherheit
CE Mark	CE
FCC Marking (Class A)	This device complies with Part 15 of the FCC Rules. Operation of this device is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation. Manufactured by Intel Corporation
Canada EMC Marking (Class A)	CANADA ICES-003 CLASS A CANADA NMB-003 CLASSE A
Japan VCCI Marking (Class A)	この装置は、クラス A 情報技術 装置です。この装置を家庭環境で 使用すると電波妨害を引き起こす ことがあります。この場合には使 用者が適切な対策を講ずるよう要 求されることがあります。VCCI-A
Australia C-Tick Mark	N232
Taiwan BSMI Marking (Class A)	警告使用者：檢磁 39121903 這是甲類的資訊產品，在居住的環境中使用時， 可能會造成射頻干擾，在這種情況下，使用者會 被要求採取某些適當的對策
Russia GOST R Marking	ME06

7.4 Product Safety Markings

The product has been provided with the following safety markings.

Table 84: Product Safety Markings

Safety Mark	Description
	This symbol indicates hazardous voltages. WARNING: Improper use may cause shock hazard. No operator serviceable parts.
	This symbol indicates a general warning, and to refer to manual for warning information
	This symbol indicates fan hazard. WARNING: To reduce risk of injury, do not put fingers into rotating fan blades
	This symbol indicates the system is provided with multiple AC power cords. WARNING: To reduce risk of electric shock, remove all AC power cords to disconnect all power.
WARNING - Apparaten skall anslutas till jordat uttag när den ansluts till ett nätverk. Must connect to an earthed mains socket-outlet	WARNING: To reduce risk of electric shock, system must be connected to an earthed mains socket-outlet

7.5 Power Supply Regulatory Agency Certifications

The power supply module will have the following:

Safety Compliance

- UL, cuL (USA / Canada) – UL60 950
- German Bauart (Germany) – EN60 950
- CE Declaration of Conformity (Europe)– EU Low Voltage Directive 73/23/EEC
- CB Certificate and Report (International) – IEC60 950 and EMKO-TSE (74-SEC) 207/94
- CCIB Safety (China)

Emission Compliance

- FCC, Class A Verification (USA/Canada)
- CE Declaration of Conformity (Europe)– EU EMC Directive 89/336/EEC
- EN55022

- EN55024
- EN61000-3-2 and -3-3
- CCIB EMC (China)
- C-Tick (Australia) – AS/NZS 3548

7.6 Regulatory Compliance Notices, Statements and Information

This equipment has been tested and found to comply with the limits for a Class A digital device. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at their own expense.

7.6.1 USA FCC Verification Notice

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

For questions related to the EMC performance of this product, contact:

Intel Corporation
5200 N.E. Elam Young Parkway
Hillsboro, OR 97124
1-800-628-8686

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and the receiver
- Connect the equipment to an outlet on a circuit other than the one to which the receiver is connected

7.6.2 Canada

Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe A prescrites dans la norme sur le matériel brouilleur: “Appareils Numériques”, NMB-003 édictée par le Ministre Canadian des Communications.

English translation of the notice above:

This digital apparatus does not exceed the Class A limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled “Digital Apparatus,” ICES-003 of the Canadian Department of Communications.

7.6.3 European Union

This product complies with the European Directives, 73/23/EEC – Low Voltage Directive and 89/336/EEC – EMC Directive. The CE Mark is marked on the product to indicate compliance.

7.6.4 Australia / New Zealand

This product complies with AS/NZS 3548, and complies with the Australian Communication Authority and Ministry of Economic Development Regulations. The C-Tick Mark with Intel’s supplier code N232 is marked on the product to indicate compliance.

7.6.5 Japan

この装置は、情報処理装置等電波障害自主規制協議会（ＶＣＣＩ）の基準に基づくクラスＡ情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。

English translation of the notice above:

This is a Class A product based on the standard of the Voluntary Control Council for Interference by Information Technology Equipment (VCCI). If this equipment is used in a domestic environment, radio disturbance may arise. When such trouble occurs, the user may be required to take corrective actions.

7.6.6 Taiwan

This server complies with CNS13438 and complies with Taiwan BSMI Regulations. The product is marked with the following BSMI Certification number and EMC Warning.

警告使用者：檢磁 3912I903
這是甲類的資訊產品，在居住的環境中使用時，
可能會造成射頻干擾，在這種情況下，使用者會
被要求採取某些適當的對策

The English translation for the above warning is:

This is a class A product. In a domestic environment this device may cause radio interference in which case the user may be required to take adequate measures.

7.7 Replacing the Back-up Battery

The lithium battery on the server board powers the real time clock (RTC) for up to ten years in the absence of power. When the battery starts to weaken, it loses voltage, and the server settings stored in CMOS RAM in the RTC (for example, the date and time) may be wrong. Contact your customer service representative or dealer for a list of approved devices.

WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the equipment manufacturer. Discard used batteries according to manufacturer's instructions.

ADVARSEL

Lithiumbatteri – Eksplosionsfare ved fejlagtig håndtering. Udskiftning må kun ske med batteri af samme fabrikat og type. Levér det brugte batteri tilbage til leverandøren.

ADVARSEL

Lithiumbatteri – Eksplosjonsfare. Ved utskifting benyttes kun batteri som anbefalt av apparatfabrikanten. Brukt batteri returneres apparatleverandøren.

VARNING

Explosionsfara vid felaktigt batteribyte. Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren. Kassera använt batteri enligt fabrikantens instruktion.

VAROITUS

Paristo voi räjähtää, jos se on virheellisesti asennettu. Vaihda paristo ainoastaan laitevalmistajan suosittelemaan tyyppiin. Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.

WARNUNG

Explosionsgefahr bei nicht ordnungsgemãssem Einbau der Batterie. Nur mit gleichen oder vom Hersteller empohlenen Teilen zu ersetzen. Gebrauchte Batterien bitte nach Herstellerangaben entsorgen.

8. Environmental Specifications

The SRSH4 system is tested to the environmental specifications as indicated in Table 85. All testing will be performed per procedures defined in *Intel Environmental Standards Handbook*.

Table 85: Environmental Specifications Summary

Environment	Specification
Temperature operating	10^{o} C to 35^{o} C
Temperature non-operating	-40^{o} C to 70^{o} C
Humidity non-operating	90%, non-condensing at temperatures of 25^{o} C to 35^{o} C
Vibration non-operating	2.2 Grms, 10 minutes per axis on all 3 axes as per *Intel Environmental and Reliability Board and System Validation Test Handbook*
Shock operating	Half-sine 2 G, 11 msec pulse, 100 pulses in each direction, on each of the three axes as per *Intel Environmental and Reliability Board and System Validation Test Handbook*
Shock non-operating	Trapezoidal, 25 G, 175 inches/sec delta V, 2 drops in each direction, on each of the six side as per *Intel Environmental and Reliability Board and System Validation Test Handbook*
Electrostatic discharge (ESD)	Tested to ESD levels up to 15 kilovolts (kV) air discharge and up to 8 kV contact discharge without physical damage as per *Intel Environmental and Reliability Board and System Validation Test Handbook*
Acoustic	Sound pressure: < 55 dBA at ambient temperatures < 28°C +/- 2°C measured at bystander positions in operating mode Sound power: < 7.0 BA at ambient temperatures < 28°C +/- 2°C in operating mode
Altitude	0 to 1,520 m (0 to 5,000 ft)

9. Serviceability and Usability

9.1 Mean Time to Repair

The system is designed to be serviced by qualified technical personnel only.

The desired mean time to repair (MTTR) of the system is 30 minutes including diagnosis of the system problem. To meet this goal, the system enclosure and hardware have been designed to minimize the MTTR.

Following are the maximum times that a trained field service technician should take to perform the listed system maintenance procedures, after diagnosis of the system.

System Component	Total Time	Remove	Replace/Add
Front Cover	1	0.5	0.5
Rear Cover	1	0.5	0.5
Power Supply	1	0.5	0.5
Hot Swap Fan [1]	2	1	1
Hot Swap PCI-X Card	2	1	1
Non-Hot Swap PCI Card	2	1	1
Disk Drive [2]	4	1	3
HPIB Board	4	1	3
Front Panel Board	4	2	2
Memory DIMM [3]	5	2	3
ICMB	5	2	3
Memory Board	9	4	5
Slimline CD-ROM	10	4	6
Fan PDB	11	5	6
Processor [4]	11	6	5
Slimline Floppy	14	6	8
SCSI Drive Bay	17	8	9
SCSI Backplane	17	8	9
SCSI SAF-TE Board	17	8	9
BaseBoard	21	8	13
Processor Board [5]	22	10	12
Power Cage	28	10	18

Notes:

1. Assumes single fan is removed and replaced in system.
2. Assumes removal is time required to remove SCSI HDD from System. Replacement time includes time to remove the HDD from the drive carrier and replace with new HDD before reinserting HDD in SCSI Bay.
3. Memory DIMM replacement assumes a single DIMM is replaced. Memory DIMM addition assumes four new DIMMs were added to the Memory Board and no DIMMs were removed. This would add an additional minute to the total time.
4. Assumes CPU board is populated with a single processor and heatsink. If populated with additional processors total time is increased by 4.75 minutes per processor.
5. Assumes single processor is removed.

9.2 Special Usability Features

- All hot swap user "touch" surfaces color coded green (GE GN3058), these include the power supply, system fans, SCSI hard drive carriers, and hot plug PCI quick release latches
- All non-hot swap user "touch" surfaces color coded blue (Pantone 285C), these include the memory board and processor board latches, processor air duct, AC bracket, and non hot plug PCI quick release latches
- Non user interface internal parts color coded black (GE 701), these include the PCI card guides, rack rails, SCSI backplane insulator, and peripherial rails
- Corresponding color coding of all appropriate system labels to speed up and ease usability
- LED status indicators provided for the following: power supply, hot plug PCI slots, hard drives, system fans
- AC cord retention feature to prevent accidental AC power disconnect
- Customizable FRU part number identification label

Glossary

This appendix contains terms used in this document.

Term	Definition
μF	micro-farad.
μs	micro-second.
Ω	Ohm.
A, Amp	Ampere.
AC	Alternating Current.
ACPI	Advanced Configuration and Power Interface.
ANSI	American National Standards Institute.
APIC	Advanced Programmable Interrupt Controller.
AWG	American Wire Gauge.
BIOS	Basic Input-Output System.
BMC	Bus Management Controller.
Bridge	The circuitry that connects one computer bus to another.
Byte	An 8-bit quantity.
dB	Decibel.
dBA	Decibel (measured using “A” scale).
CD-ROM	Compact Disk – Read Only Memory.
CE	Community European.
CFM	Cubic Feet per Minute.
CISPR	International Special Committee on Radio Interference.
CSA	Canadian Standards Organization.
DAT	Digital Audio Tape (a type of digital media storage tape).
DC	Direct Current.
DIMM	Dual Inline Memory Module.
DMI	Desktop Management Interface.
DOS	Disk Operating System.
DRAM	Dynamic Random Access Memory.
DWORD	Double Word. A 32-bit quantity.
ECC	Error Checking and Correcting.
E-Bay	Electronics Bay
EEPROM	Electrically Erasable Programmable Read-Only Memory.
EMC	Electromagnetic Compatibility.
EMI	Electromagnetic Interference.
EN	European Standard (Norme Européenne or Europäische Norm).
ESCD	Extended System Configuration Data.
ESD	Electrostatic Discharge.
ESR	Equivalent Series Resistance.
FCC	Federal Communications Commission.
Flash ROM	EEPROM.
FRB	Fault Resilient Booting.

Term	Definition
FRU	Field Replaceable Unit.
G	Acceleration in gravity units, 1G = 9.80665 m/s2.
Grms	Root mean square of acceleration in gravity units.
GB	Gigabyte. 1024 MB.
GPIO	General Purpose Input-Output.
HDD	Hard Disk Drive.
HPIB	Hot Plug Indicator Board.
HSC	Hot-Swap Controller.
I/O	Input/Output.
I^2C *	Inter Integrated Circuit bus.
ICMB	Intelligent Chassis Management Bus.
IDE	Integrated Drive Electronics, an interface to drives and storage devices.
IEC	International Electrotechnical Commission.
IEEE	Institute of Electrical and Electronics Engineers.
IFLASH	A utility to update Flash EEPROM.
IMB	Intelligent Management Bus.
IPMB	Intelligent Platform Management Bus.
IPMI	Intelligent Platform Management Initiative.
IRQ	Interrupt Request line.
ITE	Information Technology Equipment.
ITP	In Target Probe.
KB	Kilobyte. 1024 bytes.
L2	Second-level cache.
LAN	Local Area Network.
LED	Light-Emitting Diode.
LVDS	Low Voltage Differential SCSI.
mΩ	milli-Ohm.
mA	milli-Amp.
MB	Megabyte. 1024 KB.
MPS	MultiProcessor Specification.
NEMKO	Norges Elektriske Materiellkontroll (Norwegian Board of Testing and Approval of Electrical Equipment).
NIC	Network Interface Card.
NMI	Non-Maskable Interrupt.
OCP	Over-Current Protection.
OEM	Original Equipment Manufacturer.
OPROM	Option ROM. An expansion BIOS for a peripheral.
OS	Operating System.
OTP	Over-Temperature Protection.
OVP	Over-Voltage Protection.
PC-200	The collection of specifications for 200MHz memory modules.
PCB	Printed Circuit Board.
PCI	Peripheral Component Interconnect, the I/O expansion bus.
PHP	PCI Hot-Plug.

Term	Definition
PID	Programmable Interrupt Device.
PIRQ	PCI Interrupt Request line.
PMM	POST Memory Manager.
PnP	Plug and play
POST	Power-On Self Test, the BIOS boot code.
PWM	Pulse Width Modulation.
RAS	Reliability, Availability, and Serviceability.
RPM	Revolutions Per Minute.
SAF-TE	SCSI Accessed Fault-Tolerant Enclosures.
SCA	Single Connector Attachment.
SCL	Serial Clock.
SCSI	Small Computer Systems Interface, typically used for storage devices.
SDR	Sensor Data Records.
SDRAM	Synchronous Dynamic RAM.
DDR	Double Data Rate
SEC	Single Edge Contact.
SEL	System Event Log.
SELV	Safety Extra Low Voltage.
SEMKO	Sverge Elektriske Materiellkontroll (Swedish Board of Testing and Approval of Electrical Equipment).
SGRAM	Synchronous Graphics RAM.
SMBIOS	System Management BIOS.
SMBus	A subset of the I^2C bus/protocol, developed by Intel.
SMI	System Management Interrupt.
SMM	System Management Mode.
SMP	Symmetric Multiprocessing.
SMRAM	System Management RAM.
SMS	System Management Software.
SPD	Serial Presence Detect. A feature of PC-100 DIMMs that provides configuration information through serial EEPROMs.
SSI	Server System Infrastructure.
TUV	Technischer Uberwachungs-Verein (A safety testing laboratory with headquarters in Germany).
UL	Underwriters Laboratories, Inc.
USB	Universal Serial Bus.
VA	Volt-Amps, Volts multiplied by Amps.
Vac	Alternating Current (AC) Voltage.
Vdc	Direct Current (DC) Voltage.
VCCI	Voluntary Control Council for Interference.
VDE	Verband Deutscher Electrotechniker (German Institute of Electrical Engineers).
VGA	Video Graphics Array.
VRM	Voltage Regulator Module.
VSB	Voltage StandBy.
W	Watt.
WfM	Wired for Management.
Word	A 16-bit quantity.

Reference Documents

Refer to the following documents for additional information:

- *SSH4 Baseboard, Processor, and Memory Module External Product Specification*, Revision 1.0
- *SSH4 Basic Input Output System (BIOS) External Product Specification*, Revision 1.0
- *Intelligent Chassis Management Bus Bridge Specification*, Revision 1.0
- *Intelligent Platform Management Interface (IPMI) Specification*, Revision 1.5
- *SCSI Accessed Fault-Tolerant Enclosures (SAF-TE) Specification*, Revision 1.0
- *Emergency Management Port Interface External Product Specification*, Revison 1.0
- *SCA-2 Connector Small Form Factor Document 8046*, Rev. 1.1
- *Intel Environmental & Reliability Board and System Validation Test Handbook*, Revision 05