intel® Technical Advisory

TA-407-3

5200 NE Elam Young Parkway
Hillsboro, OR 97124

August 10, 2001

STL2 Server Board DPLLRST Signal Timing Issue

Products Affected

Product Code	Material Master (MM) number	Printed Board Assembly (PBA) number
STL2	830522	A28808-301, A28808-302, A28808-303, A28808-304, A28808-305
BTLBB	830519, 834388, 836619, 836661, 837756	A28808-301, A28808-302, A28808-303, A28808-304, A28808-305

Description

During AC power cycle testing, some combinations of STL2 server boards and SR2050 server chassis have exhibited Microsoft* Windows* 2000 operating system blue screens during operating system boot. This issue has occurred infrequently during AC power cycle testing when the testing continued for extended time periods. The blue screen operating system panics do not occur at every boot and are recoverable by pressing the system power button. There is no data loss or data corruption when this issue occurs. It is not expected that the customer will see this issue under normal system operating conditions.

This issue occurs only with certain STL2 server board and SR2050 server chassis combinations. Not all STL2 / SR2050 systems exhibit this issue. This issue has not occurred in testing when the STL2 server board is used in the SC5000 or SR2100 server chassis. This issue may be observed using a third-party chassis.

All STL2 server boards with printed board assembly (PBA) numbers A28808-301, A28808-302, or A28808-303 have the potential of being affected by this issue.

Root Cause

Under certain power supply voltage rail ramp conditions that may occur at system power on, the DPLLRST signal, supplied to the ServerWorks* ServerSet* III LE chipset CNB30LE component, may be asserted before the PCLK signal. When this DPLLRST signal and PCLK signal timing relationship occurs, blue screen operating system panics have been observed under Microsoft* Windows* 2000 Advanced Server during operating system boot with continuous AC power cycle testing.

This signal timing relationship differs on all STL2 server boards. This signal timing relationship is related to the power supply voltage rail ramp conditions that may occur at system power on. Power supplies that do not have simultaneous voltage rail ramps are the most likely to cause this signal timing relationship. The SR2050 power supply has the potential to cause this timing relationship.

Corrective Action / Resolution

As a resolution for this issue, Intel will incorporate a factory rework change into new STL2 server boards. The factory rework change ensures that the DPLLRST signal will always be asserted after the PCLK signal with any power supply voltage rail ramp conditions. This ensures proper initialization of the chipset and allows the operating system to properly load. The details of this factory rework change are described in STL2 Product Change Notification (PCN) 101656-xx.

This Technical Advisory describes an issue which may or may not affect the customer's product

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STL2 server boards with PBA number A28808-304 and A28808-305 contain the rework change. This rework change meets the specifications in the widely accepted IPC-610C Industry Standards. Intel Corporation stands behind the rework quality with the standard Intel warranty.

Please contact your Intel Sales Representative if you require more specific information about this issue.

Enterprise Platforms & Services Division
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