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DrMOS Specifications

November 2004

Revision 1.0

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Revision History

Revision Number	Description	Revision Date
1.0	Initial Release.	November 2004

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1 *Introduction*

This document summarizes the different requirements needed to enable a standard integrated Driver-MOSFET (DrMOS) specification for implementation in a typical PC platform. The aim of this specification is to enable features that are necessary to develop an integrated device such that inter-operability between various devices and controllers is feasible.

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2   *Background*

The power requirements of microprocessors are increasing with every process generation. This is reflected in the increased static (steady state) and dynamic (transient) power that the processor Voltage Regulator (VR) needs to generate at very low voltages (~1V) and very high currents (100+A). This trend is foreseen to continue in the near future. The consequence of the increased power manifests itself in the form of two technology needs:

A need for increased power density in the VR to satisfy higher power transfer in a limited real estate environment (such as a desktop)

A need for increased efficiency at higher switching frequencies (a result of a need for faster dynamic response) to maintain losses at low levels

The above two requirements have driven technology advances in the building blocks of the VR, i.e., MOSFETs. These advanced semiconductor switches have been used in synchronous buck converter, which has remained the main workhorse for the voltage regulators feeding microprocessors. Due to the lopsided nature of the voltage conversion ratio needed in the VR's, the two switches used in the VR's have been optimized for different characteristics to reduce losses. Lately the concept has been moved a step further by integrating the switches and their drivers into a DrMOS combination that have shown increased performance.

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3 Technical Specifications

The feature set for the DrMOS can be divided into two major areas. They address the electrical characteristics and the thermal/mechanical characteristics of the device. These major areas of focus can be subdivided further to address many aspects of the devices

3.1 Electrical Characteristics & Features

The DrMOS device has been treated as a black box with some input output characteristics from an electrical characteristics perspective. The technical specifications for the device are listed in Table 1.

Table 1. Desired Electrical Characteristics / Features of a DrMOS device

Parameters	Typical Range	Feature	Remarks
Switching Frequency	> 500KHz	Required	1MHz preferred. > 1MHz Fs capability acceptable
Input Voltage Range	5V ~ 16V	Required	12V typical input voltage assumed for desktop application. Future applications may use < 12V.
Output Voltage Range	0.5V ~ 1.5V	Required	Expected output is ~1V. Future applications may have < 1V output. In such cases input voltage may be less than 12V.
Continuous Output Current	>25A	Required	25A @ 1MHz Fs is required. This may translate to > 25A @ a switching frequency < 1MHz. Example 25A @ 1MHz may mean the module is capable of 35A @ 500KHz.
Power Enable/Disable		Required	Logic Level input to module. Tri-state logic
PWM Control Input		Required	Complementary Logic Level
Drive Logic Select		Required	Logic level select for gate drive voltage
Current Sense accuracy	< ± 10%	Optional	Specified over a given temperature range
Area/Size of the module	~ 8 mm x 8 mm	Required	**A common footprint or motherboard interface definition is essential (critical) for adoption.**
Testability		Optional	Could define test conditions to guarantee power loss at a later time

Thermal Characteristics/Features			
Maximum Power Dissipation	~3W @ 1MHz & 25A continuous output current		Actual dissipation varies based on boundary conditions. See boundary conditions listed below for the desktop application. Idea is to reduce power loss to meet desktop environment. See boundary conditions
Thermal Shutdown		Optional	
Dual Sided Cooling		As needed / Optional	Interface to provide heat sink on the top of the device is preferable.

The above table lists many of the features that are required and desired from a VR implementation perspective but is not meant to restrict the development of other design features that could possibly improve the performance of the module. The parameters in the table should be taken as a guideline given the requirements of voltage regulators in a desktop environment.

It is also to be noted that the detailed electrical characteristics pertaining to switching times, logic level requirements have not been spelled out. This is to maintain the feature set at a general level so that each module developer has the freedom to innovate within a given set of features.

In addition the device needs to meet Intel environmental requirements per Intel Blue Book.

3.2   Boundary Conditions

The following boundary conditions are envisioned on the desktop motherboard. The VR using the specified modules would be designed as a "down" solution to supply ~150A at 1V.

- Input voltage: 12V
- Output voltage: ~1V
- Output current: 150A

Total VR power loss target: 30W max
- Total silicon (module) power loss target: 20W max
- Switching frequency: 1 MHz min
- Airflow: 100 ~ 150 radial airflow (LFM)
- Heat-sink for module: not preferred but negotiable
- PCB: 4 layers, 1 oz copper
- Max PCB temp: 120 degree C

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- Common motherboard module interface (for multiple sourcing)

- Price target: suitable for desk top market

- Ambient Temperature: 50 C

<u>Notes:</u>

1. Desktop environment typically calls for 4-layer motherboards with 1-Oz Cu per layer. Maximum PCB temperature is limited to 120°C typically. Need for additional PCB layers, increase of CU thickness etc are not an option for desktop motherboard applications. In other words, the desktop motherboard should not be required to be modified to have 6-layers and/or 3 to 4 –oz Cu per layer to "maintain" the temperature at a lower value than 120°C. The module needs to be efficient such that the power loss is reduced to keep the PCB temperature below 120°C.

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4   Nomenclature

A common motherboard interface would form the basis for the adoption of the DrMOS into the desktop arena along with suitable price points and performance. The following table provides the input output signals with appropriate nomenclature to define the common interface so that different devices from various vendors can be compared. The common signal definition will bring clarity to the muddled area of various input-output designations that exist today.

 The essential signals for the DrMOS device from an input-output perspective are shown in Figure 1. Some signals have been included from the perspective of future expansion of the device to accommodate additional features. Some of these features may not be available on all devices based on application and cost. In such cases the corresponding signals may be left open (unconnected or grounded as the case maybe) to accommodate a simpler design (which in turn means that such signals may be designated as optional in the specifications).
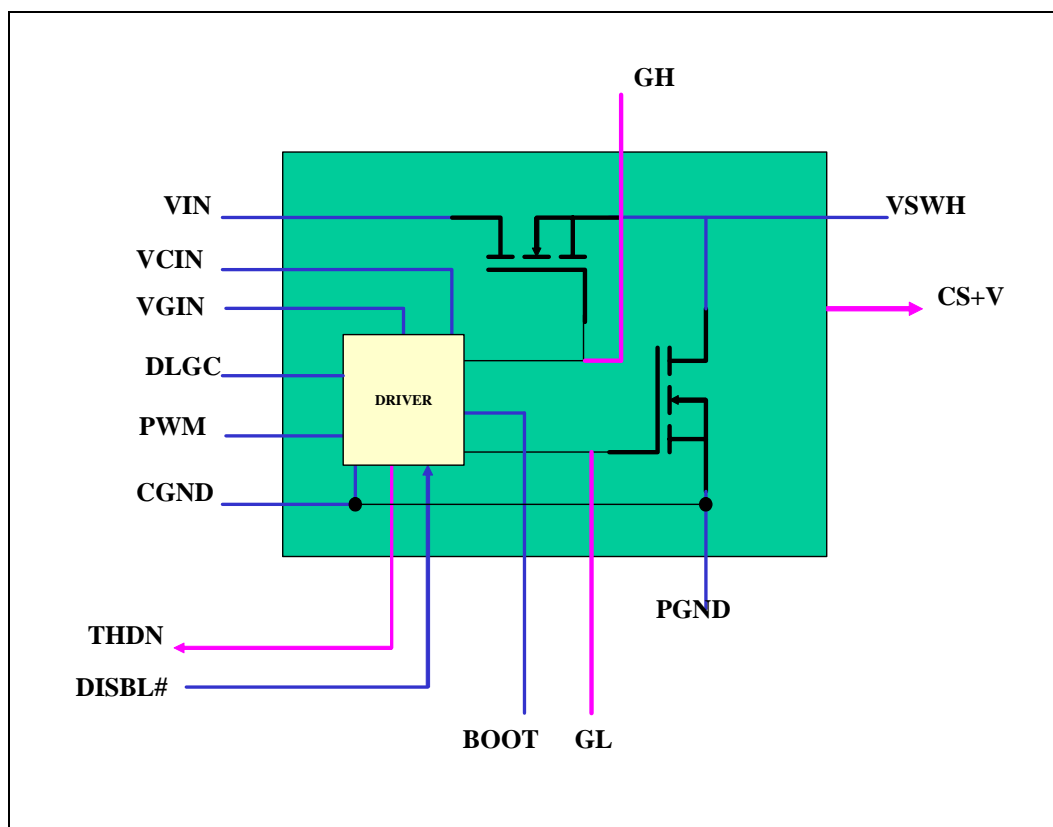
Figure 1. Basic Input-Output Signal Definition for a typical DrMOS

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The definition and functionality of each pin is explained in Table 2. The pin-out or pad interface to the motherboard required for the DrMOS device is as shown in Figure 2. The 56-pin Multi-Lead Frame (MLF) package footprint with a 8mm X 8mm size is recommended as the footprint. The footprint has been chosen to accommodate future expansion for pins to carry higher current and also for inclusion of future signal interfaces that may be defined. The package size has also been chosen keeping in mind the cost of implementing.
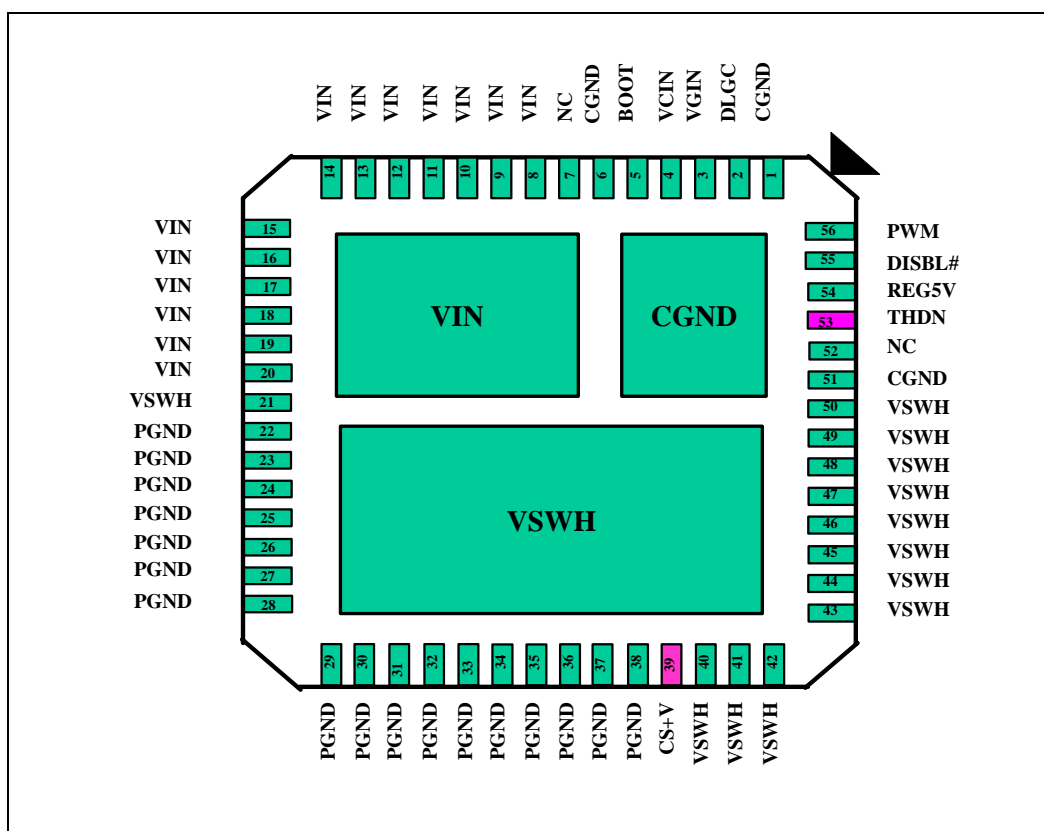
Figure 2. Recommended Input-Output Signal Interface for the DrMOS (Top View: Pin-Out as seen through the package)

Table 2. Pin-Out Functional Description

Pin Name	Pin #	Description	Remarks
CGND	1, 6, 51	Control Signal Ground	Internally connected to PGND
DLGC	2	Gate Drive Voltage Select	12 / 5V Gate Drive logic select
VGIN	3	Lower Gate Supply Voltage	For either 12 / 5G gate drive
Pin Name	Pin #	Description	Remarks
VCIN	4	Control Input Voltage	Driver Vcc Input
BOOT	5	Bootstrap Voltage Pin	

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Pin Name	Pin #	Description	Remarks
NC	7, 52	No connect	Optional / For future Expansion No external connection on PCB
VIN	8 - 20	Input Voltage	
PGND	22 - 38	Power Ground	
CS+V	39	Current Sense +VE signal pin	Optional / Future feature
VSWH	21, 42 - 50	Phase Output / Switch Output	
THDN	53	Thermal Shutdown / Switching Indicator Output	Optional / Future feature
REG5V	54	5V Output	5V output @ 10mA
DISBL#	55	Disable Signal (Active low)	
PWM	56	PWM Drive Logic	

4.1   Signal Description

This section provides a detail on the functionality of the signal/power pins on the DrMOS device.
- CGND: Control Signal Ground (Type: Analog)

Separate ground signal / pins / pad provided to isolate the drive (PWM, control logic etc) signals. May be used to either internally and/or externally connected to the power ground (PGND).
- DLGC: Drive Logic Select (Type: Digital Input)

Table 3. Lower Gate Voltage Select Operation

Input	Logic Level	Action
Pin left open or not connected		No external Gate voltage connections, Lower FET Gate voltage is determined by internal voltage generated by DrMOS device
Pin Grounded to CGND / PGND	0	Connect external Gate voltage (5V – 12V) to Pin#3 VGIN

- VGIN: Lower Gate Drive Voltage (Type: Analog Input)

Lower Gate Drive Supply Voltage. See DLGC pin description for proper operation with internal & external gate voltages.

- VCIN: Control (Driver) Supply Voltage (Type: Analog Input)

Control / Driver Supply Voltage. Typical +12V (Future features may need operation from +5V.

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- BOOT: Bootstrap Pin (Type: Analog)

Pin to connect an external capacitor to switch node (VSWH) to provide bootstrap drive signal to the high side FET.

- VIN: Input Voltage (Type: Analog Input)

Typical +12V Input Voltage pins / pad. Electrically same as the drain of the High Side FET

- PGND: Power Ground (Type: Analog)

Self-explanatory.

- CS+V: Current Sense (Type: Analog Output)

Current sense output signal (Optional at present). Future feature definition in conjunction with controller feature standardization.

- VSWH: Phase/ Switch Voltage Node (Type: Analog)

Switch Node to be connected to the output inductor. Self-explanatory.

- THDN: Thermal Shutdown/Switching Indicator (Type: Digital Output)

A logic signal output that indicates a shutdown of the device either due to a thermal problem or due to an internal fault (Optional at present). Future feature definition in conjunction with controller feature upgrades.

- REG5V: Provides a 5V output with 10mA drive capability for purposes of sequencing etc.
- DISBL#: Device Disable (Type: Digital Input; Active Low)

Should be capable of taking both +12V & +5V levels for logic high (1)

Typically the pin has a pull up resistor to VCIN. Need an external transistor that pulls it low for disabling the device.

Logic input Low (0): Device is disabled. Output is in tri-state mode. No voltage available at the switch node even in the presence of input voltage (VIN), PWM signals (PWM), control (VCIN) & gate voltages (VGIN).

Logic input High (1): Device is enabled.

- PWM: Drive Signal (Type: Digital Input)

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Should be capable of taking both +12V & +5V levels for logic high (1)

Following conditions need to be met:

Table 4. PWM Operation Description

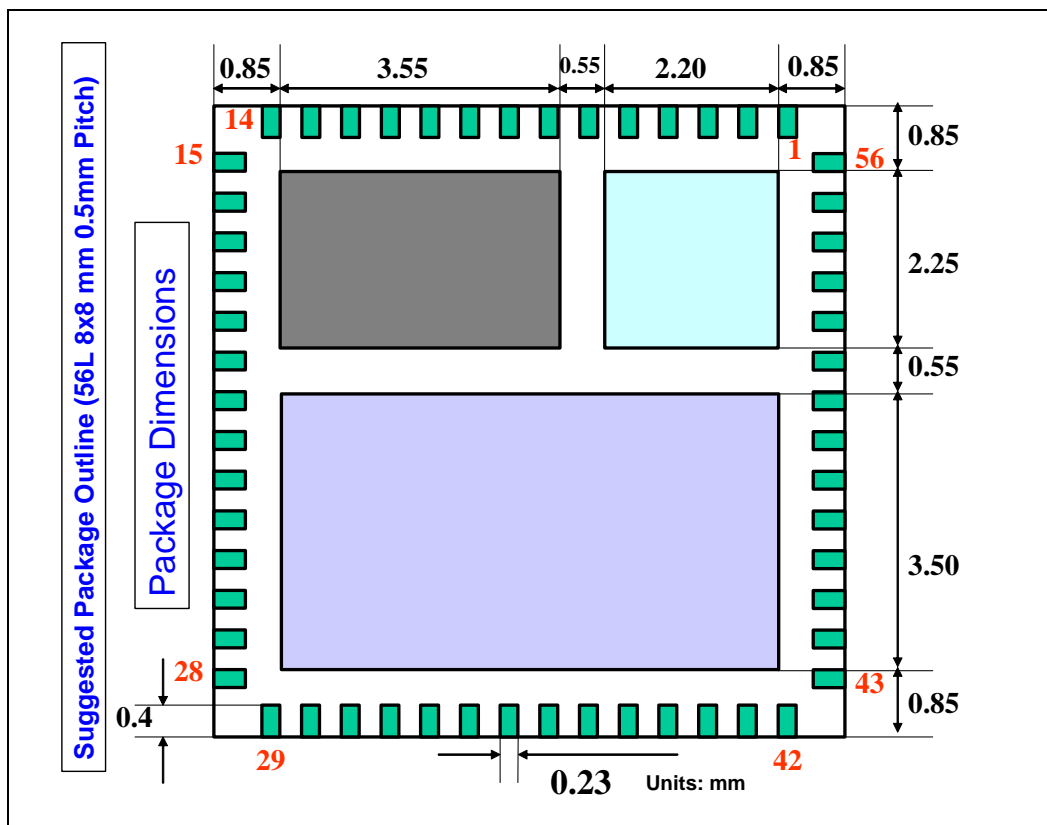| Input	Logic Level	Action
Pin left open or not connected		Lower FET is OFF; Hi side FET is OFF (Tristate)
Logic Input low	0	Lower FET is ON; Hi side FET is OFF
Logic Input High	1	Lower FET is OFF; Hi side FET is ON

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5 Mechanical Dimensions

Figure 3. Recommended mechanical dimensions for DrMOS package

Notes:

1. All dimensions are in millimeters

2. Dimensions specified here are the key dimensions for package outline

3. Other package dimensions and tolerances not specified here should comply with manufacturer's standard drawing and JEDEC specification

4. Refer to individual manufacturer's data sheets for exact package dimensions

Figure 3 shows the mechanical dimensions of the footprint as seen on the motherboard. The package dimensions of the device should be compatible with the footprint as shown in Figure 3

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Appendix A Electrical & Mechanical Compatibility

The DrMOS specifications provide a basis for the development of a device that meets the requirements of a typical board designer. However it is recognized that the industry can develop various versions of the device with slightly different characteristics and features that still meet the basic requirements but are not exactly compatible with one another. This section provides the electrical and mechanical modifications that can be performed on a typical layout such that multiple devices can be used interchangeably on the same layout.
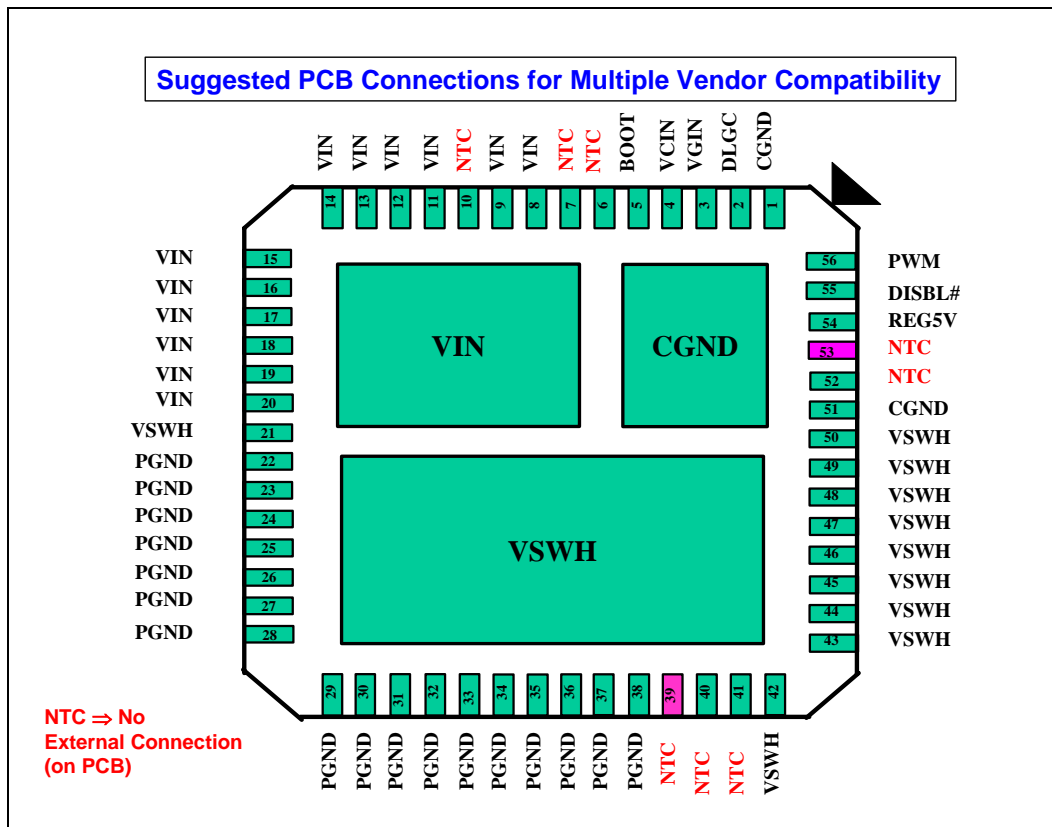

Figure 4. Suggested Electrical Pin-Out on PCB for multiple vendor compatibility

Figure 4 shows a suggested electrical connections on a typical PCB such that different DrMOS devices (from different industry developers) that can be used on the same PCB footprint. In this case the "NTC" connections are some minor signals that can be left "open" (no connected) on the PCB layout such that two or more DrMOS devices can be used interchangeably. It is to be noted that the designer needs to ensure that all interface signals that are needed for proper operation are

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available. Similarly Figure 4 shows the mechanical footprint that can accommodate two (or more) vendor parts such that multi-sourcing issues can be addressed.
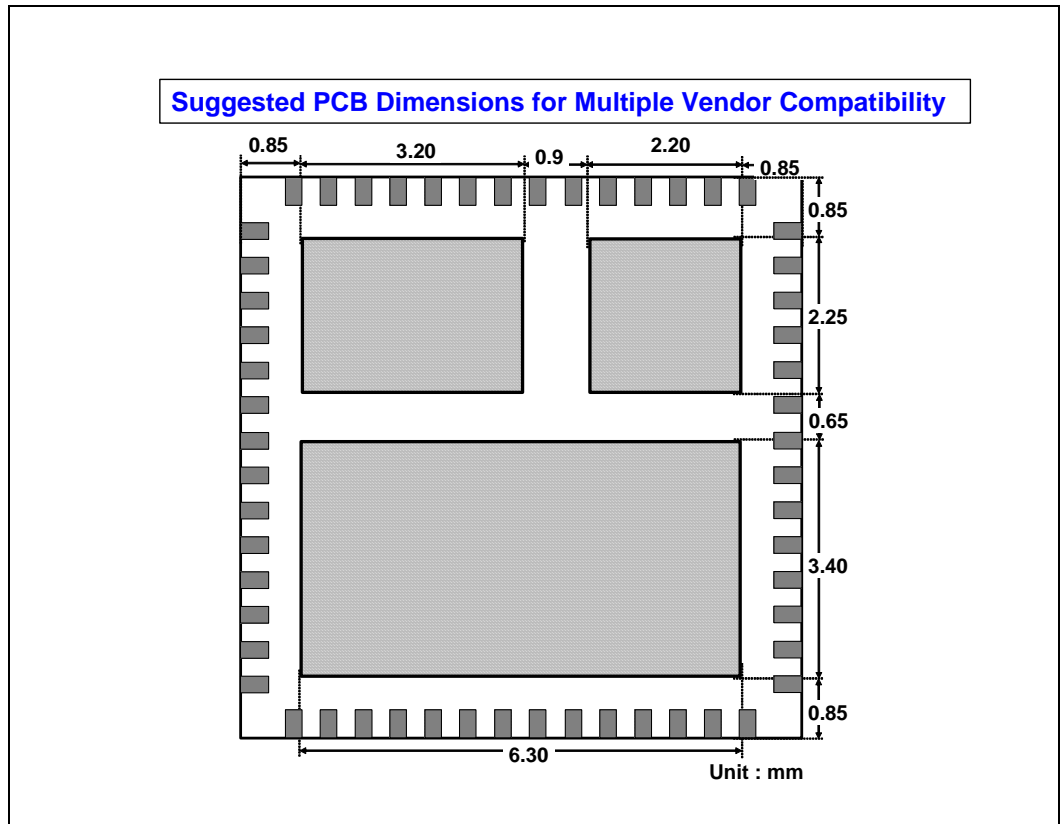
Figure 5. Suggested Mechanical PCB Layout for Multiple Vendor Compatibility

The designer needs to refer to the manufacturer's data sheet to ensure proper electrical and mechanical layout to achieve compatibility between devices from different manufacturers. For example the above electrical and mechanical layouts shown in Figure 4 & Figure 5 will provide a common interface for DrMOS devices R2J20601NP (from Renesas) & PIP212-12M (from Philips). Similar layout modifications can be arrived at to accommodate different DrMOS devices.

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