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INTRODUCING THE i960® Hx PROCESSOR TO CURRENT i960® Cx PROCESSOR USERS

ABSTRACT

Intel's i960® HA/HD/HT processors (abbreviated "Hx") provide a performance upgrade path from the i960 CA/CF (or "Cx") processors. Several new features appear on the Hx while some of the Cx features have been dropped. Designers need to understand the differences between these two processor families so they can decide whether to upgrade to the Hx family immediately or stay with the Cx family for a while.

This Technical Note summarizes the differences and similarities between the two processor families and briefly describes the new features of the Hx family. This comparison is not exhaustive. Instead, it highlights only the main differences and advantages of the Hx processor. It assumes you already understand the CA/CF product features. See the references listed at the end of this paper for more details on both product families.

The most apparent difference for some applications is the lack of an on-chip DMA controller on the Hx. This paper explores several DMA alternatives.

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FEATURE SUMMARY

The Hx provides “more” and “less” for the current Cx system designer.

- ⇑ More internal cache for instructions, data, registers, and stacks
- ⇑ More internal general purpose RAM
- ⇑ More processing speed with core clock doubling and tripling
- ⇑ More processor efficiency without a DMA stealing clock cycles
- ⇑ More memory integrity through data parity
- ⇑ More debug control with the Guarded Memory Unit and additional debug pins
- ⇑ More board diagnostics support through JTAG testing features
- ⇑ More efficient bus accesses with unaligned memory accesses handled by on-chip circuits rather than microcode

- ⇓ Less power consumption at 3.3 V, and even less with HALT mode
- ⇓ Less interrupt latency
- ⇓ Less external timing hardware with on-chip programmable timers

Table 1 summarizes the major differences between the Hx and Cx processor families.

TABLE 1 CONDENSED Hx vs. Cx FEATURE COMPARISON.

FEATURE	Hx	Cx
Compatibility	Backwards compatible for software and hardware with the Cx processors. Though not drop-in replacements, system hardware can be designed to accept either a Cx or an Hx processor.	The CF is the pin- and code-compatible upgrade from the CA.
Processor Core Clock	HA: 1x bus clock. HD: 2x bus clock. HT: 3x bus clock.	1x bus clock mode, only.
Instruction Cache	16KByte Four-Way Set Associative.	CF: 4KByte Two-Way Set Associative CA: 1KByte Two-Way Set Associative
Data Cache	8KByte Four-Way Set Associative. Rapid invalidate instruction quickly removes specific data from the cache without affecting the rest of cache.	CF: 1KByte Two-Way Set Associative CA: None
Internal Data RAM	2KByte	1KByte

TABLE 1 CONDENSED Hx vs. Cx FEATURE COMPARISON (continued).

FEATURE	Hx	Cx
Unaligned Memory Accesses	Handled by on-chip circuitry. Faster than the Cx and does not steal CPU cycles to perform the translation.	Handled by microcode.
DMA	Not supported directly. Several options are available.	4 channels supported on-chip.
V_{CC}	3.3 V ±0.3 V; 5 V tolerant inputs. TTL compatible outputs.	5 V ±5%
Power Consumption	≈ 4W at 66 MHz internal clock	≈ 6W at 40 MHz
Power Conservation (HALT) Mode	Significant power savings during idle periods. Invoked by user software.	None
External Address / Data Bus	Same as Cx, plus... • Some additional byte enable bit (BE3:0#) codes • N_{XDA} wait states expanded from 3 up to 15 • Improved unaligned memory access performance	• 32-bit demultiplexed • 160 Mbyte/s transfer rate (at 40 MHz external bus speed) • On-chip wait state generator • Bursting • Read pipelining • READY# and BTERM# handshaking • Programmable data bus width (8-, 16-, or 32-bits)
AC Timings	9.5 ns available for external logic between output valid and input setup at 40 MHz bus rate and 3.3 V data bus signals. 5 V data bus systems allow 6 ns under the same conditions. Faster output valid time on 3.3 V systems. T_{OV} max. = 10 ns for 3.3 V, 13 ns for 5 V. T_{OH} min. = 1.5 ns T_{IS} min. = 6 ns T_{IH} min. = 1.5 ns	CF: Only 2-8 ns between output valid and input setup at 40 MHz bus rate. CA: Maximum speed of 33 MHz. CF 40 MHz: T_{OV} max. = 14-16 ns, 5 V only. T_{OH} min. = 3-6 ns T_{IS} min. = 3-7 ns T_{IH} min. = 2-5 ns
Data Parity	Optional even or odd	None

TABLE 1 CONDENSED Hx vs. Cx FEATURE COMPARISON (continued).

FEATURE	Hx	Cx
Peripheral Clocking	Peripherals synchronized to the CPU clock input.	Peripherals synchronized to 2 PCLK outputs.
Interrupts	Same as Cx except • Improved latency (dedicated mode, typical latencies): HA: 27 bus clocks HD: 13 bus clocks HT: 9.3 bus clocks • Inputs sampled every bus clock cycle.	• 8 interrupt channels plus NMI. • Direct, expanded (up to 240 interrupts), and mixed interrupt modes. • Inputs sampled every 2 bus clock cycles. • 31 programmable priorities. • Typical latency 30 bus cycles.
On-Chip Timers	Two 32-Bit timers. Auto reload capability and one-shot. CLKIN prescaling (÷1, 2, 4, or 8).	None
Guarded Memory Unit	Software establishes reserved memory regions and controls whether unauthorized memory accesses are prevented or only detected and reported.	None
External Debugging Features	Same as Cx, plus... • Cycle Type pins • Bus Stall pin	FAIL# pin
JTAG Support	IEEE 1149.1 compliant.	None
Initialization Boot Record	Begins at FEFF FF30H. A single EPROM can contain separate boot records for Cx and Hx. Some other minor changes.	Begins at FFFF FF00H.

Cx COMPATIBILITY

The Hx processors maintain backward compatibility with the i960 CX processors. Software written for the Cx processors runs on the Hx processors, with the exception of DMA-specific code. The PGA pinouts are compatible and a socket can be designed to accept either a Cx or an Hx processor without modification.

Customers can design a single board to accept the Cx and then upgrade to the Hx.

Upgrading to the Hx requires an upgraded compiler tool set, too. Old compilers do not support the Hx hardware improvements and incremental instructions.

See AP-506 *Designing for 80960Cx and 80960Hx Compatibility*for details of designing hardware to accept either processor.

CORE CLOCK MULTIPLIERS

The Hx family includes three core clock variations:

HA: core clock	*equals*	bus clock speed
HD: core clock	is *double*	bus clock speed
HT: core clock	is *triple*	bus clock speed

The doubled and tripled core clock versions increase the processor performance without increasing memory system costs. Maximum performance occurs when the instructions and data fit in internal caches and RAM. Otherwise, the relatively slow external bus response bottlenecks the processor's performance.

The Cx does not offer clock multiplier options.

See SECTION 1.0 THE INTEL 80960Hx PROCESSOR in the *80960HA/HD/HT Embedded 32-bit Microprocessor Data Sheet* for a list of the speed grades offered for each Hx model.

CACHES

The Hx can hold time-critical code and data in four internal memory regions:

- a 16KByte instruction cache
- an 8KByte data cache
- a 2KByte internal scratchpad RAM
- a register set cache that can handle 5 - 15 levels of procedure and interrupt calls before spilling to external memory

These internal memories help you reach high-speed performance with slow, inexpensive external memory systems. Also, the interrupt vectors and interrupt service routines (ISRs) can be locked in these memories to improve interrupt response.

The Hx beefs up the on-chip cache sizes and also provides more efficient organization. The four-way set associative architecture provides better performance than direct-mapped caches twice the size.

Best performance happens by using the internal memories as follows:

- Interrupt vectors are locked into the lower addresses of internal RAM
- The interrupt stack is cached in the data cache
- ISRs are loaded and locked into one way of the instruction cache
- Time critical code is locked into the instruction cache

- The register set cache is large enough to hold the deepest procedure and interrupt call without spilling to external memory
- Register cache sets have been reserved for time-critical, high priority interrupts
- Frequently manipulated data (e.g., matrix arrays, network data buffer regions, graphic images, etc.) resides in the data cache. Also, the data cache can be used like a zero wait state extension of internal scratchpad RAM
- Frequently changing data (from an external source like an I/O port or DMA target region) is tagged non-cacheable, and therefore does not interfere with genuinely cacheable data
- Calculation constants, loop counters, intermediate results reside in internal RAM

Four-Way Set-Associative Design

The Instruction and Data Caches are both four-way set-associative. Each cache is organized into four segments (or “ways”). Four ways reduce the likelihood that the contents will be overwritten and have to be re-fetched from external memory. A value from any given address in external memory can potentially be stored in any of four available ways of the cache. Therefore, if you lock any instruction cache way, remaining ways still provide caching for the entire address space.

Instruction Cache

The 16KByte instruction cache is the largest of any i960 product to date. Normal instruction sequences can reside there. Also, time critical software, such as interrupt service routines (ISRs), can be locked into any of the ways.

Data Cache

The 8KByte data cache is also the largest of any i960 product to date.

Internal RAM

The 2KByte internal RAM serves multiple purposes. It provides “zero wait state” scratchpad space for variables and constants. Interrupt vectors can be locked into the lower portion of RAM. Also, the register set cache can optionally grow into the upper addresses of RAM if necessary.

The updated Hx-aware compiler recognizes the internal RAM and uses it to optimize execution speed.

Register Set Cache

User software configures the register cache to provide up to 15 on-chip register sets. The cache expands into the internal RAM memory space if more than five register sets are needed. Also, you can reserve any number of register cache locations exclusively for high priority interrupts.

See CHAPTER 4 CACHE AND ON-CHIP DATA RAM, in the *i960® Hx Microprocessor User’s Manual*.

UNALIGNED MEMORY ACCESSES

On-chip circuitry handles unaligned big- and little-endian memory accesses rather than using the processor microcode. The result is faster accesses with no reduction of processing speed.

See CHAPTER 16, EXTERNAL BUS DESCRIPTION, in the *i960® Hx Microprocessor User's Manual*.

DMA

Unlike the i960 Cx family, the Hx processor does not include on-chip DMA support. Users who need DMA have several options. An external DMA controller improves system performance since it does not steal computing cycles from the processor. However, external DMA solutions add system complexity and increase parts count. The Hx can still provide customized DMA-like functions at the cost of processing MIPS.

Here is a summary of some available DMA options for the Hx.

Full-Featured vs. Application-Specific Design

Users should decide which transfer modes are necessary (and cost effective), and which are just useful if available. The Cx DMA controller supports a variety of transfer modes including:

- Simple fly-by
- Block moves among aligned memory regions
- Unaligned data chaining on demand

Most applications do not use all of the features, but instead use one transfer mode exclusively. Know which modes you need before settling on an option.

Software Controlled Transfers

User software can transfer data between memory and I/O ports using the load- and store-quad instructions in a simple loop. Software can poll a flag to determine when to initiate a transfer. The disadvantage is that the processor squanders cycles on polling. The advantage is that small transfer tasks can be performed cost effectively without additional hardware.

Interrupts

Rather than spending processor cycles polling, use interrupts for demand mode transfers. The internal timers can schedule periodic transfers into staccato bursts rather than hog the processor for long intervals. Use both methods together to get both benefits.

Customized DMA Controller Logic

Create your own field programmable gate array (FPGA) or ASIC design. Use the bus arbitration, BREQ# and BSTALL# features of the Hx so processor MIPS are not lost during transfers, thus improving system performance.

Customized DMA logic lets you design (and pay for) only the functions necessary for the application. For example, if the application only requires data transfers between an I/O port or FIFO and main memory, a simple fly-by single-cycle transfer state machine can do the job in the least bandwidth.

On the other hand, if you require variable length, unaligned, multi-cycle, memory-to-memory chained transfers, the design becomes considerably more complex and expensive. Very complex DMA requirements suggest sophisticated ASIC designs.

Off-the-Shelf DMA Controller

The market offers some chips that support 32-bit DMA, but gone are the days of suitable, low-cost, dedicated DMA chips. Today's DMA chips usually include other features as well and are expensive just for DMA use. However, if your application requires some of these other features, you get DMA virtually free. Table 2 lists some of those chips. Not all of the chips listed below interface well with the Hx. Check each chip's specifications carefully before making a design decision.

TABLE 2 EXTERNAL 32-BIT DMA CONTROLLER CHIPS

Part Number	Manufacturer	Description
82380	Intel	Monolithic DMA, Interrupt Controller, Timers, Wait State Generator, and DRAM Controller for the 80386 which closely resembles the Hx bus. 32-, 16-, and 8-bit transfers. 25 MHz operation maximum.
MB92411	Fujitsu	Dedicated DMA controller. Dual control buses for multiple bus masters. 32-, 16-, and 8-bit transfers. 33 MHz operation maximum. Expensive, e.g., prices start around $110 US.
V96ESC	V3 Corporation	Monolithic DMA, Timers, DRAM Controller, and Serial Ports. Designed specifically for the Hx and Cx buses.
PCI 9060	PLX Technology	PCI bus bridge with DMA.
DSP3210	AT&T	DSP chip with DMA, Timer, and Parallel and Serial I/O's.
TMS320C1x	TI	DSP chip. Some versions also include DMA.

Cx as a Dedicated DMA Controller

If you are familiar with the Cx DMA implementation, consider using a Cx as a dedicated DMA controller. Certainly, the extra processing power of the Cx could handle intelligent I/O, data formatting, or other tasks, too. If the specialized application software is small enough, it can be locked into the Cx instruction cache to maximize speed and minimize multiprocessor bus arbitration.

POWER SUPPLY ISSUES

The squeeze is on for more MIPS per watt. The Hx responds with 33 MIPS/Watt by reducing V_{CC} to 3.3 V while remaining compatible with 5 V logic and memories, and offering a power reduction Halt mode. The Cx proves up to 13 MIPS/Watt.

V_{CC}

The Hx uses a 3.3 V nominal power supply voltage. As such, the Hx promotes the migration path to the lower voltage standard. Power dissipation is about 4W (at 66 MHz internal clock rate), or 30% less than the 40 MHz CF.

See the *80960HA/HD/HT Embedded 32-bit Microprocessor Data Sheet* for more details on the V_{CC} requirements.

5 V TTL Compatibility

The Hx accepts either standard 5 V or 3 V logic input signals. A dedicated input pin, VCC5, lets you set the reference voltage for logic "1" input signals.

The 0 to 3.3 V processor outputs comply with standard 5 V and 3 V TTL logic thresholds for external logic and memory chips.

See the *80960HA/HD/HT Embedded 32-bit Microprocessor Data Sheet* for more details on the 5 V tolerance feature.

Halt Mode

User software can suspend processing and significantly reduce power dissipation with Halt mode. The on-chip clock and timers continue to operate and the processor still responds to the HOLD and BOFF# bus arbitration inputs. Any enabled interrupt of sufficient priority terminates Halt mode. You can restart the processor by scheduling an on-chip timer interrupt, waiting for an external interrupt, or using both methods together. A hardware reset also terminates Halt mode.

See CHAPTER 12 HALT MODE, in the *i960® Hx Microprocessor User's Manual*.

EXTERNAL BUSES

Other changes to the Hx include modified AC timings, elimination of PCLK output pins, addition of parity checking, and some new BE3:0# bit codes.

AC Timings

The Hx input timings require 6 ns T_{IS} setup and 1.5 ns T_{IH} hold. The hold time is compatible with common fast, synchronous logic and memories.

The output timings depend on the data bus signal voltages. A 3.3 V system provides 9 ns of propagation time for external logic to respond in one clock cycle at 40 MHz, which is 1.5 to 7.5 ns more time than the Cx. 5 V data buses require extra time to discharge, leaving 6 ns of propagation time for external logic.

Also see the *80960HA/HD/HT Embedded 32-bit Microprocessor Data Sheet* for a list of the AC timing specifications.

Byte Enable Codes

Three new codes have been added to the BE3:0# pins to accommodate unaligned bus accesses. Now the processor can directly access the middle two, the lower three, or the upper three bytes in a word with a single bus access. System memory decode logic now needs to accommodate these three additional codes.

See CHAPTER 16 EXTERNAL BUS DESCRIPTION, in the *i960® Hx Microprocessor User's Manual*.

No PCLK Outputs

All peripheral logic synchronizes to the CLKIN input of the processor. This change improves Hx AC timing specifications; jitter on the internally generated PCLK no longer degrades the timing specs. Also, you can select the clock driver according to the system loads rather than limiting the loads based on the drive strength of PCLK outputs.

See CHAPTER 16 EXTERNAL BUS DESCRIPTION, in the *i960® Hx Microprocessor User's Manual*. Also see the *80960HA/HD/HT Embedded 32-bit Microprocessor Data Sheet* for a list of the AC timing specifications.

Data Parity Checking

The Hx provides optional data parity checking to improve integrity of the external memory system. The processor generates four parity bits, one for each byte of the data bus. User software selects even or odd parity, or none. If the processor detects a parity failure, it asserts an output pin (PCHK#) and issues an internal fault message.

See CHAPTER 16 EXTERNAL BUS DESCRIPTION, in the *i960® Hx Microprocessor User's Manual*.

INTERRUPTS

Interrupt latency is a function of the core clock speed. Hence, the HD and HT processors respond in roughly 60% and 36% the time, respectively, as the HA. Latency is further reduced as the Hx can recognize interrupt inputs every bus clock cycle whereas the Cx can recognize them only every two cycles.

User techniques to further improve latency include:

- Using all the capabilities of the internal caches (see the section on CACHES in this Technical Note for more details).
- Eliminating multi-cycle instructions that cannot be interrupted, like **mul** or **div**, from the instruction stream.
- Polling the interrupt flag before returning from the interrupt service routine (ISR). If another interrupt is queued, service it again without incurring the overhead of exiting and re-entering the ISR.

See CHAPTER 11 INTERRUPTS, in the *i960® Hx Microprocessor User's Manual*.

TIMERS

Two 32-bit timers are included in the Hx. They decrement at the bus clock frequency and can be programmed as one-shot or automatic reload timers. Timing ranges can be extended by ÷1, ÷2, ÷4, and ÷8 clock prescaling. The timers continue to decrement in Halt mode. Table 3 shows the maximum resolutions and ranges possible using these timers.

TABLE 3 TIMER RESOLUTIONS AND RANGES POSSIBLE ON THE Hx

Bus Speed	Max. Resolution	Max. Range
40 MHz	25.0 ns	14.3 mins
33 MHz	30.3 ns	17.4 mins
25 MHz	40.0 ns	22.9 mins
20 MHz	50.0 ns	28.6 mins
16 MHz	62.5 ns	35.8 mins

The internal timers conserve processor interrupt input pins for other tasks, reduce external timing hardware, and obsolete most internal software time delay loops.

The Cx has no timers.

See CHAPTER 10 TIMERS, in the *i960® Hx Microprocessor User's Manual*.

DEBUG FEATURES

The Hx adds several new debug features:

- Guarded Memory Unit (GMU)
- Cycle Type Pins
- Bus Stall Pin (BSTALL)
- Data Parity Check Pin (PCHK#)

Guarded Memory Unit (GMU)

The GMU guards regions of memory and either reports or prevents unauthorized memory accesses. The GMU issues a fault message in either case. You can use it to protect kernel code from User mode accesses, stack areas from Supervisor and User mode execution, read-only I/O ports from writes, and so on. Typical applications use the GMU during software development to prevent corruption by pieces of software not yet debugged and then to protect kernel code in the production release.

The Cx does not have a GMU.

See CHAPTER 13 GUARDED MEMORY UNIT (GMU), in the *i960® Hx Microprocessor User's Manual*.

Cycle Type Pins

Four Cycle Type pins are added to the Hx to indicate the origin and the bus width of the current access and whether the processor is in HALT mode or not. A logic analyzer trace of these pins during system debug can distinguish between a program-initiated bus access and an event-initiated access. For example, you can trigger only when an interrupt ISR accesses an address and ignore non-interrupt accesses.

The Cx does not have Cycle Type pins.

See the *80960HA/HD/HT Embedded 32-bit Microprocessor Data Sheet* for more details on the Cycle Type pins.

Bus Stall Pin (BSTALL)

The Bus Stall pin indicates that execution is stalled until pending bus accesses from the processor are serviced. During normal operation, BSTALL warns external bus masters (such as a DMA controller) to relinquish the bus so processing can resume. During system development and debugging, BSTALL indicates cache misses and bottlenecks in the external bus that should be minimized to optimize your system performance.

The Cx does not have a BSTALL pin.

See the *80960HA/HD/HT Embedded 32-bit Microprocessor Data Sheet* for more details on the Bus Stall pin.

Data Parity Check Pin (PCHK#)

Unreliable memory systems can often be diagnosed through data parity checking. The PCHK# pin asserts one clock cycle after a parity fault occurs during an external read access. If the application system implements data parity, set a logic analyzer trigger condition to watch for PCHK# while debugging. PCHK# is the closest thing to “trigger on branch to weeds” for a memory system failure. Many times PCHK# offers the only chance to capture evidence of the problem.

The Cx does not support parity checking.

See CHAPTER 16 EXTERNAL BUS DESCRIPTION, in the *i960® Hx Microprocessor User’s Manual*.

BOUNDARY SCAN (JTAG)

The Hx fully complies with the IEEE 1149.1 Boundary Scan (JTAG) test methodology. Users who employ Boundary Scan testing on their system can verify continuity between the processor and the interconnecting logic. Boundary Scan is typically performed during board-level production testing.

INITIALIZATION

Basically, the Hx initialization sequence imitates the Cx. Some of the PRCB entries are slightly different. See the User’s Manual for those details.

Boot up can proceed faster on the Hx. By reading the first four words of the boot ROM, the Hx learns the memory configuration and wait state profile for the rest of the boot ROM. Thereafter, initialization proceeds as fast as the boot ROM can support, so initialization completes in less time than for a Cx.

Also, the initialization for the two processors can coexist in a single boot ROM. The Hx Initialization Boot Record (IBR) resides at a different ROM address than the Cx IBR. This feature helps you design a single socket that can accept a Cx or upgrade to an Hx.

See CHAPTER 14 INITIALIZATION AND SYSTEM REQUIREMENTS, in the *i960® Hx Microprocessor User’s Manual*. Also, see *Designing for 80960Cx and 80960Hx Compatibility*, Application Note AP-506, order number 272556 for details on designing a single socket for the Cx and Hx processors.

REFERENCES

The following documents provide more information on the i960 Hx and Cx microprocessor families.

1. *i960® Hx Microprocessor User's Manual*, Intel order number 272484. Pre-production draft copies are available from your Intel representative, listed in the back of any Intel data book or user's manual.

2. *80960HA/HD/HT Embedded 32-bit Microprocessor Product Preview Data Sheet*, order number 272495. Also available in the i960® *Processors and Related Products* handbook, Intel order number 272084.

3. *Designing for 80960Cx and 80960Hx Compatibility*, Application Note AP-506, Intel order number 272556. Also available in the i960® *Processors and Related Products* handbook, order number 272084.

4. *Cache Tutorial*, Intel order number 296543.

5. i960® Cx Microprocessor User's Manual, Intel order number 270710.