White Paper

BIOS Compatibility for i960® Rx I/O Processor

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CONTENTS

INTRODUCTION 1
BIOS SUPPORT REQUIREMENTS 1
KNOWN BIOS COMPATIBILITY ISSUES WITH THE 80960RP 33/3.3 & 80960RP 66/3.3 2
Memory Resource Allocation 2
Byte or Word Configuration Cycle to BAR 3
Secondary Bus Reset 3
KNOWN BIOS COMPATIBILITY ISSUES WITH THE 80960RP 33/5.0 4
Memory Resource Allocation 4
Byte or Word Configuration Cycle to BAR 4
Read of BAR Multiple Times 4
First Configuration Cycle is a Configuration Write 5
Secondary Bus Reset 5
BIOS COMPATIBILITY ISSUE SUMMARY 5
COMPATIBILITY PLANS 6
BIOS RELEASES SUPPORTING I960 RX I/O PROCESSORS 6
SYSTEM COMPATIBILITY LIST 6
PCI CONFIGURATION UTILITY 9

Revision: 003

INTRODUCTION

The i960® Rx I/O Processor is an integrated PCI multifunction device. When designed into a system motherboard or an Intelligent I/O adapter card, portions of the i960 Rx I/O Processor are configured by system BIOS. For proper configuration of the I/O Processor functions, system BIOS must support the capabilities of the i960 Rx I/O Processor.

The 80960RD 66/3.3 and the 80960RP 33/3.3 are the newest products in the i960 Rx I/O Processor family. These are 3.3 volt components as compared to the 80960RP 33/5.0 which is a
5 volt device. Based on extensive testing of various desktop and server platforms which use these devices, a number of compatibility issues have been discovered with some BIOS. The purpose of this paper is to document the possible compatibility issues.

This paper identifies the support requirements of system BIOS which are compatible with the i960 Rx I/O Processors. Known versions of BIOS which provide this level of support are also provided as an aid in determining a particular platform's BIOS compatibility with the i960 Rx I/O Processors.

This document identifies BIOS support requirements, known BIOS compatibility issues with the 3.3 Volt and 5.0 Volt versions of the i960 Rx I/O processor, a list of compatible BIOS products, a list of known compatible systems and vendors, and a PCI configuration utility (PCI.EXE).

BIOS SUPPORT REQUIREMENTS

The "PCI multifunction" definitions of the i960 Rx I/O Processor are:

- Function 0 is the PCI-to-PCI bridge, which meets the *PCI Local Bus Specification* Revision 2.1, and the *PCI-to-PCI Bridge Architecture Specification* Revision 1.0.
- Function 1 is the Address Translation Unit (ATU), which is classified as a Memory Controller per the *PCI Local Bus Specification.*

System BIOS must support the configuration of these PCI functions for the product based on the i960 Rx I/O Processor to operate in the system. System BIOS support includes:

- PCI-to-PCI Bridge support
- Multi-function device support
- Support for Function 0 being a PCI-to-PCI bridge

Revision: 003

Many early PCI systems, especially desktop systems, did not include support for PCI-to-PCI bridging or multi-function PCI devices in the system BIOS. Depending on the system manufacturer, it may be possible to get a BIOS upgrade which includes support for these features. Intel strongly urges you to contact the system or motherboard manufacturer or BIOS vendor to verify whether or not the system can support these features.

KNOWN BIOS COMPATIBILITY ISSUES WITH THE 3.3 VOLT VERSIONS (80960RP 33/3.3 & 80960RP 66/3.3)

This section identifies BIOS compatibility issues and workarounds (when appropriate) discovered during system tests with adapter cards based on the 80960RD 66/3.3 and the 80960RP 33/3.3 in various systems. Refer to the *i960® Rx I/O Processor Specification Update* (document number 272918) for stepping information.

Memory Resource Allocation

The Address Translation Unit (ATU) of the 80960RD 66/3.3 and 80960RP 33/3.3 requires the BIOS to allocate PCI address space as a resource. The BIOS allocates PCI address space, then assigns an address for the PCI resource through the Base Address Register (BAR) in the ATU's PCI Configuration Space. The ATU requires one block of memory on the Primary PCI bus and allows for an Expansion ROM, therefore implementing two BARs.

The mechanism defined for determining memory block size requirements of a PCI resource is defined in the *PCI Local Bus Specification*. The process described is: *"Power-up software can determine how much address space the device required by writing a value of all 1's to the* (BAR) *register and then reading the value back. The device will return all 0's in don't care bits, effectively specifying the address required"*

The ATU provides a programmable mechanism for defining the memory block size requested. This mechanism involves a companion Limit Register for each BAR. The value programmed in the Limit register by application software is the value to be returned on the read back after a write of all 1's (per PCI specification above). It has been determined that some BIOS does not write bit 0 as suggested in the *PCI Local Bus Specification.* Therefore the 80960RD 66/3.3 and 80960RP 33/3.3 will return the contents of the Limit register after a 32-bit configuration write of FFFF FFFFH or FFFF FFFEH to the BAR.

The 80960Rx (80960RD 66/3.3 and 80960RP 33/3.3) is the first PCI device to employ a programmable mechanism for defining memory block size requirements, and a number of BIOS compatibility issues have been discovered during testing. The following issue has been verified.

Byte or Word Configuration Cycle to BAR

When determining the address space required by the 80960RD 66/3.3 or 80960RP 33/3.3, the BIOS must perform a 32-bit configuration write. Writing 1's to the BAR through multiple configuration write cycles which are only a Byte or Word long will not result in correct configuration. In systems where this occurs, the 80960RP 33/5.0 ATU will appear as if requesting only 4 Kbytes of address space. This is the minimum address space the 80960RP 33/5.0 ATU can request. This issue is planned to be fixed in a future stepping of these components.

Secondary Bus Reset

The 80960RD 66/3.3 and 80960RP 33/3.3 PCI-to-PCI Bridge unit provides for generation of a software reset to the secondary PCI bus. Setting the Bridge Control Register's Secondary Bus Reset bit (80960 local bus address 103EH, bit 06 = 1) causes the S_RST# output (ball J25) to be asserted. This resets devices on the secondary PCI bus as well as specified 80960RD 66/3.3 and 80960RP 33/3.3 registers, queues and units. Clearing the bit results in the S_RST# output to be deasserted.

The 80960RD 66/3.3 and 80960RP 33/3.3 has no internal mechanism to automatically detect when a secondary bus reset has occurred. When application software requires the re-initialization of public PCI devices on the secondary PCI bus, or re-programming of the affected 80960RD 66/3.3 and 80960RP 33/3.3 registers, two possible workarounds are:

1. Connect the S_RST# output to the XINT4# input (ball P2). Set bit 4 in the Interrupt Mask Register (80960 local bus address FF00 8504H) and program bits 03:00 in the Interrupt Map Register 1 (80960 local bus address FF00 8524H) to the desired vector. The interrupt service routing for XINT4# should check the state of Secondary Bus Reset bit. When this bit is cleared, the reset is complete. The Interrupt Service Routine (ISR) can then initialize the secondary PCI devices and 80960RD 66/3.3 and 80960RP 33/3.3 registers.

2. After the secondary bus is reset, the host BIOS runs PCI configuration cycles to reinitialize any PCI devices on the secondary PCI bus. Configuration cycles to non-existent devices generate master aborts on the secondary PCI bus, which causes an NMI# to the 80960 core. A software workaround is to add a check to the Secondary Bus Master Abort NMI interrupt service routine to confirm when the secondary ATU registers are reset

   The NMI Interrupt Service routine — when finding the NMI Interrupt Status Register's Secondary Bridge Error bit set (80960 local bus address 1700H, bit 04) — reads the Secondary Bridge Interrupt Status Register (SBISR) (80960 local bus address 1048H). In the SBISR, the PCI Master Abort bit (bit 03) is set in the event of a Master Abort occurring on the 80960RD 66/3.3 or 80960RP 33/3.3's Secondary PCI interface. When this bit is set, the ISR checks the contents of the secondary ATU registers that were originally programmed by the initialization code.

Revision: 003

— When the register(s) is reset, the ISR re-initializes the secondary ATU registers and any public PCI devices on the secondary PCI bus.

— When the register(s) is not reset, the ISR can perform the existing servicing of the master abort.

One bit that may be used as a check is the Secondary ATU Command Registers Memory Enable bit (80960 local bus address 1298H, bit 1)

KNOWN BIOS COMPATIBILITY ISSUES WITH THE 5 VOLT VERSION (80960RP 33/5.0)

Through testing with adapter cards based on the 80960RP 33/5.0 in various systems, some BIOS compatibility issues have been identified. This section provides details of these issues and identifies workarounds where appropriate. Refer to the *i960® Rx I/O Processor Specification Update* (document number 272918) to identify the stepping a particular issue affects.

Memory Resource Allocation

As described in the previous section, the Address Translation Unit (ATU) of the 80960RP 33/5.0 requires the BIOS to allocate PCI address space as a resource. During testing of the 80960RP 33/5.0's programmable mechanism for defining the memory block size requirements a number of BIOS compatibility issues have been discovered. The following issues have been verified.

Byte or Word Configuration Cycle to BAR

When determining the address space required by the 80960RP 33/5.0, the BIOS must perform a 32-bit configuration write. Writing 1's to the BAR through multiple configuration write cycles which are only a Byte or Word long will not result in correct configuration. In systems where this occurs, the 80960RP 33/5.0 ATU will appear as if requesting only 4 Kbytes of address space. This is the minimum address space the 80960RP 33/5.0 ATU can request.

Read of BAR Multiple Times

The current stepping of the 80960RP 33/5.0 (A-1 step) requires the BIOS to perform the write (described in the previous paragraph) before every read of the register when reading the BAR to determine the address space required. The A-1 step returns the contents of the corresponding Limit register on the next read after the write. Subsequent reads of the BAR will return the contents of the BAR, and not the contents of the Limit register.

BIOS which relies on reading the value more than once to determine the address space required will not properly configure the 80960RP 33/5.0. Systems with this behavior have been found to leave the default value in the BAR (0000 0008H) or program the BAR to a value of 8000 8008H.

First Configuration Cycle is a Configuration Write

Some system BIOS has been found to perform a configuration write to PCI devices as the first step of system configuration. This initial configuration cycle is a write of 00H to the Command Register to disable the PCI device. The system BIOS then reads PCI space for devices present. An erratum in the current stepping of the 80960RP 33/5.0 (A-1 step) requires the first configuration cycle be a Configuration Read cycle.

Systems with BIOS which perform a configuration write cycle to the 80960RP 33/5.0 as the first access will not boot properly. The system will appear to hang during the boot sequence if this condition exists.

Secondary Bus Reset

The 80960RP 33/5.0 PCI-to-PCI Bridge Unit provides for generation of a software reset to the secondary PCI bus. As previously described for the 80960RD 66/3.3 and 80960RP 33/3.3, the 80960RP 33/5.0 also has no internal mechanism to automatically detect when a secondary bus reset has occurred. Refer to the section Known BIOS Compatibility Issues for the 80960RD 66/3.3 & 80960RP 33/3.3 for details on this issue and suggested workarounds.

BIOS COMPATIBILITY ISSUE SUMMARY

Table 1. BIOS Compatibility Issue Summary

Issue Description	Affected Stepping			
	80960RP 33/5.0 A-0 Step	80960RP 33/5.0 A-1 Step	80960RD 66/33 80960RP 33/3.3 A-0 Step	80960RD 66/33 80960RP 33/3.3 Future Step
Memory Resource Allocation Configuration Write must be FFFF FFFFH or FFFF FFFEH	X	X	X	
Byte or Word Configuration Cycle to BAR	X	X	X	
Read of BAR Multiple Times	X	X		
First Configuration Cycle is a Configuration Write	X	X		

Revision: 003

Secondary Bus Reset	X	X	X	X

COMPATIBILITY PLANS

Intel is actively working with BIOS vendors and server OEMs to ensure compatibility the i960 Rx I/O Processor in systems. This document will be updated as additional systems and BIOS are confirmed to properly configure the i960 Rx I/O Processor.

BIOS RELEASES SUPPORTING i960 Rx I/O PROCESSORS

Desktop and server platform from system OEMs incorporate BIOS from various sources. Some systems have BIOS which is developed internally. More often a core BIOS is purchased from another vendor, then modified for the platform by the OEM. The platform will then display the BIOS vendor and revision number or revision date of the core BIOS.

Note: This list is the latest information available to Intel through first-hand testing in vendor labs. However, vendors may change features of their products without notifying Intel; Intel cannot guarantee the accuracy of this list. Intel strongly urges you to call system or motherboard vendors to verify the availability of required PCI device support in the system BIOS.

Table 2. Compatible BIOS

BIOS Vendor	Release
American Megatrends Inc.	AMIBIOS with core date of 10/10/94 or 07/15/95 or later
Award	AWARD BIOS with a core date of 3/1/97 or later
Phoenix Technologies Ltd.	PhoenixBIOS 4.0, Release 5.10 PhoenixBIOS 4.0, Release 5.12 PhoenixBIOS 4.0, Release 6.00

SYSTEM COMPATIBILITY LIST

The 80960RD 66/3.3, 80960RP 33/3.3 and 80960RP 33/5.0 have been tested in the following systems and verified to be properly configured by the system BIOS. The systems in this list do not exhibit any of the mechanisms described in this paper, except for systems which may perform a Secondary Bus Reset during configuration. Designs should implement one of the workarounds for the Secondary Bus Reset for compatibility with all systems.

While the following systems have been found to properly configure the i960 Rx I/O Processor as a PCI device, a design based on the 80960RD 66/33, 80960RP 33/3.3 or 80960RP 33/5.0 may exhibit other issues in these systems. Improper initialization of the i960 Rx I/O Processor by application software can prevent proper configuration by system BIOS.

Revision: 003

Table 3. Compatible Systems (Sheet 1 of 2)

OEM	System Model	BIOS Version(s)	Component(s)
ALR	Revolution Q SMP	4.04.4	all
ALR	Evolution 6	1.00.06CG0 4/5/96	80960RD 66/3.3 & 80960RP 33/3.3
AST	Bravo MST-166	1.00.05BU0Q	all
AST	Bravo MST-6150	1.00.01CG0Q	80960RD 66/3.3 & 80960RP 33/3.3
Austin	Affinity	730081396,Orion-H	all
Compaq	ProLinea 5133	10/31/95	all
Compaq	ProLinea 6180e	1.00.01CG0P	80960RD 66/3.3 & 80960RP 33/3.3
Compaq	ProSignia 500	E15 05/08/96	all
Compaq	ProLiant 1500	E12 12/30/96	all
Compaq	ProLiant 5000	E16 Nov, 96	all
Dell	Dimension XPS-P133C	1.00.05FX0J	all
Dell	Dimension XPS PRO150	A01	80960RD 66/3.3 & 80960RP 33/3.3
Dell	Dimension XPS PRO200S	A03	80960RD 66/3.3 & 80960RP 33/3.3
Dell	PowerEdge SP5166-2	1.00 A05	all
Dell	Optiplex GXPRO200	1.10 A02	80960RD 66/3.3 & 80960RP 33/3.3
Dell	Optiplex GXMT-5150	1.10.A15	80960RD 66/3.3 & 80960RP 33/3.3
Dell	Optiplex GXMT-5166	1.10.A15 2/8/96	80960RD 66/3.3 & 80960RP 33/3.3
Fujitsu	FMV 6150	4.05	all
Fujitsu	FMV 5200T4	V2.0 6/27/96	80960RD 66/3.3 & 80960RP 33/3.3
Gateway	P5-100	1.00.03BR0T	all
Gateway	P5-133XL	1.00.03BR0T	all

Gateway	P5-166	1.00.01CN0T	all

Table 4. Compatible Systems (Sheet 2 of 2)

OEM	System Model	BIOS Version(s)	Component(s)
Gateway	P5-200XL	1.00.06CY1T	80960RD 66/3.3 & 80960RP 33/3.3
Gateway	G6-200	1.00.01CG0T	80960RD 66/3.3 & 80960RP 33/3.3
Hewlett Packard	LH+	4.05.11	all
Hewlett Packard	XU-5/133	GS.05.02	all
IBM	PC-350/133	10/13/95 10/26/95	all
Intel	Xtended Xpress	1.00.09DG0	all
Intel	RC440FX UP	Beta 2.02	all
Intel	BB440FX DP	1.00.03DA0	all
Intel	AP450GX MP	1.00.06CD0	all
Micron	Pentium 133	4.04 M54Pe-15P	all
Micron	SMP Pentium 133	4.04 M54Pe-14m	all
Micron	Millennia Pro	1.00.03CS15	80960RD 66/3.3 & 80960RP 33/3.3
Micron	Millennia Venus P200MT	1.00.03CS15	80960RD 66/3.3 & 80960RP 33/3.3
NEC	5800	4.05.U.0252	all
NEC	Promate P133	1.00.02CQ0K	all
NEC	Promate P166	4.05.4	all
Olivetti	NetStrada 3000	1.00.01DMO	80960RD 66/3.3 & 80960RP 33/3.3
Siemens	Primergy 560	4.05, Rev 1.03.887	all

Revision: 003

PCI CONFIGURATION UTILITY

The included PCI utility (PCI.EXE) was used to verify proper configuration of the i960 Rx I/O Processor. This utility has been included for your use. The program is a DOS utility which allows examination of PCI Configuration Space. You can use this utility to read the configuration settings programmed in the i960 Rx I/O Processor by the system BIOS. The PCI.EXE utility cannot be run from a DOS window. It is suggested that the utility is copied to a bootable floppy disk which can be used in the test system.

REVISION HISTORY

Rev. Date	Version	Description
November 1996	001	This is the original release of this white paper.
January 1997	002	Additional systems added to Table 3. Secondary Bus Reset section added.
February 1997	003	80960RD 66/3.3 and 80960RP 33/3.3 added Additional systems added to Table 3.