



VRM 9.0 DC-DC Converter Design Guidelines

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VRM 9.0 DC-DC Converter Design Guidelines

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Guideline Categories

This document defines one or more DC-to-DC converters to meet the power requirements of computer systems using Intel microprocessors. It does not attempt to define a specific voltage regulator module (VRM) implementation. VRM requirements will vary according to the needs of different computer systems, including the range of processors a specific VRM is expected to support in a system. The “VRM” designation may refer to a voltage regulator on a system board, as well as to the module defined in Section 2.

The VRM 9.0 definition is specifically intended to meet the needs of systems based on the Intel[®] Xeon[™] and Pentium[®] 4 processors.

Each guideline is placed into one of three categories. The category immediately follows the section heading and is one of the following:

- | | |
|------------------|--|
| REQUIRED: | An essential part of the design—necessary to meet processor voltage and current specifications and follow processor layout guidelines. |
| EXPECTED: | Part of Intel’s processor power definitions; necessary for consistency among the designs of many systems and power devices. May be specified or expanded by system OEMs. |
| PROPOSED: | Normally met by this type of DC-to-DC converter and, therefore, included as a design target. May be specified or expanded by system OEMs. |

1 Electrical Specifications

1.1 Output Requirements

1.1.1 Voltage and Current

REQUIRED

The VRM 9.0 Voltage Regulator Module is a DC-DC converter that supplies the required voltage and current to a single processor as shown in Table 1. The maximum voltage is determined by the five-bit VID code provided to the VRM, as described in Section 1.3.2. The specifications in Table 1 are for the VRM only. The computer system board must supply additional decoupling capacitance and sufficient plane area to carry the high DC currents. It is desirable that a single model of the VRM be able to support all processor types, if this does not significantly affect VRM cost and availability, so that field upgrades of processors will not require a new VRM.

1.1.2 Output Voltage Tolerance

REQUIRED

The voltage measured at the VRM connector pins on the system board must be within the range shown in Table 1, except during input voltage turn-on and turn-off. See Section 1.1.5 for turn-on and turn-off tolerance.

Voltage tolerance includes:

- Initial DC output voltage set-point error
- Component aging effects
- Output ripple and noise
- Full ambient temperature range and warm up specified in Section 3.1.
- Both static operation and dynamic output load changes from minimum-to-maximum or maximum-to-minimum loads specified in the tables above.

Output voltage tolerances increase with output current levels to compensate for the increasing voltage drops in the power distribution path. Table 1 shows the relationship of V_{CC_CORE} (measured at the processor pins) and I_{CC} for different processors.

1.1.3 No Load Operation

EXPECTED

The VRM should operate in a no-load condition: i.e., with no processor installed. The VRM does not need to meet the output regulation specifications described in Table 1, but its output must not exceed 110% of the value of the maximum DC output voltage, and it must not trigger over-voltage fault detection circuitry. When the VRM is subsequently loaded with the minimum values listed in Table 1, it must begin to regulate and source current without triggering failures or causing control signal malfunction.

1.1.4 Turn-on Response Time

PROPOSED

The output voltage should reach its specified range within 50 msec of the input power reaching its minimum voltage.

1.1.5 Overshoot at Turn-On or Turn-Off

REQUIRED

Overshoot upon the application or removal of the input voltage must be less than 2% above the nominal output voltage set by the Voltage Identification (VID) code. No negative voltage may be present on any output during turn-on or turn-off.

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Table 1, VRM Output Ratings

Note: This table shows processor specifications for reference only. Please refer to the processor specifications in the latest Intel® Xeon™ or Pentium® 4 processor data sheet.

Symbol	Parameter	VID	Minimum	Maximum	Unit
V _{out-VRM}	Output voltage measured at the solder side of the VRM mating connector ^{1,2,3}	1.70	1.609	1.70	V
		1.50	1.408	1.50	
V _{CC_CORE}	Output voltage measured at the processor sense pins on the solder side of the processor socket ^{1,2,3}	1.70	1.560	1.70	V
		1.50	1.330	1.50	
V _{MAX}	Maximum, non-operating (failure) voltage	1.70		2.1	V
		1.50		1.75	
I _{out_MAX}	Maximum static VRM current for V _{out} ^{4,5}	1.70		60	A
		1.50		65	
dI _{out} /dt _{MAX}	Output slew rate ⁶			50	A/μs

1. V_{CC_CORE} –minimum at I_{out_MAX} below. For V_{CC_CORE} –minimum at other loads, please refer to specifications in the latest processor data sheet.
2. V_{CC_CORE} -maximum is set by the processor’s Voltage Identification (VID) code inputs to the VRM.
3. Maximum (VID setting) and minimum output voltages are for both static and transient conditions. Intel’s power distribution model assumes a VRM set-point accuracy of 0.8%. The processor should not be subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds (V_{CC-MAX} + V_{CC-MIN})/2 + 0.055•(1 – I_{CC}/I_{CC-MAX}) (volts). Moreover, V_{CC} should never exceed V_{CC-MAX} (VID). Failure to adhere to this specification can shorten the processor lifetime.
4. I_{out_MAX} is measured at (V_{CC-MAX} + V_{CC-MIN})/2.
5. I_{out_MAX} allows for a 10% current-sharing imbalance in FMB applications (Section 1.1.7).
6. dI_{out}/dt_{MAX} is the output slew rate capability of the VRM for a minimum-to-maximum or maximum-to-minimum load step with no external load capacitance at the VRM output, for testing purposes. In actual use, it is expected that the system board has sufficient capacitive decoupling to slow the processor slew rate to 50A/μS at the VRM output pins. When the module is specified to require output capacitance on the system board (e.g., in the option proposed in Section 2.4), the test load must include the capacitance.

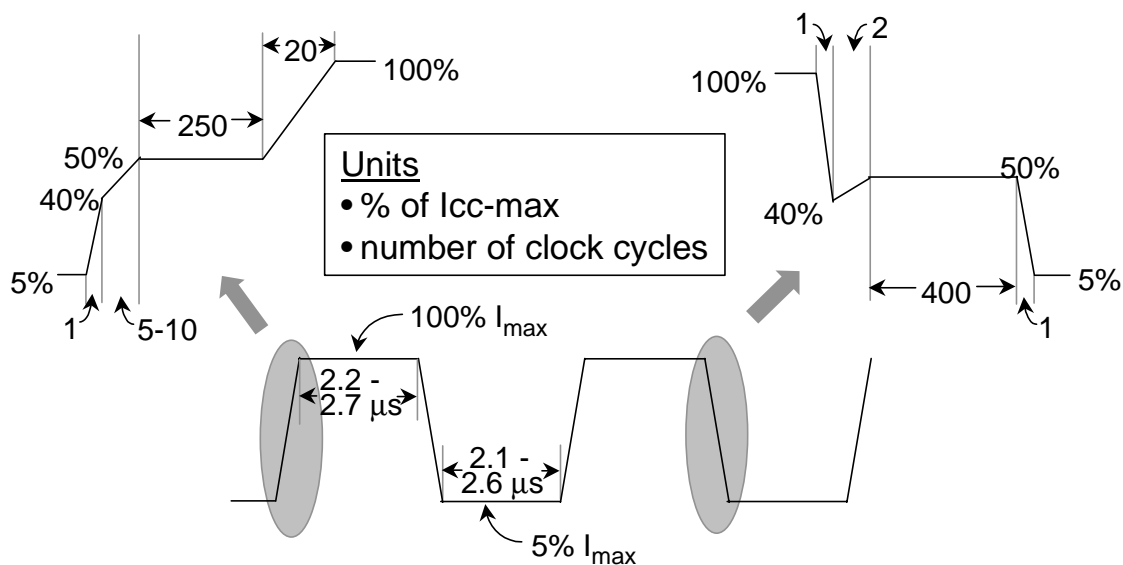
1.1.6 Converter Stability

REQUIRED

The VRM needs to be unconditionally stable under all output voltage ranges and current transients with system board capacitance ranging from 0 μF to 20,000 μF and with less than 2.0 mΩ ESR. A voltage regulator imbedded on a system board needs to meet stability requirements with the output filter capacitance design on that board.

Stability requirements include a Thermal Monitor operating condition in which the processor may periodically stop to reduce its average power dissipation in response to a high-temperature alert. Figure 1 shows worst-case Thermal Monitor operation (maximum current in the ON state).

Figure 1, Processor Current during Thermal Monitor Operation



Notes:

- Duration of on-off periods depends on processor speed: faster processors have shorter durations.
- Other operating system-controlled events could have on-times as short as 700 cycles.
- A possible worst-case routine could cause processor I_{cc} to go through a 100% → 40% → 100% set of transitions within 30-50 cycles.

1.1.7 Current Sharing**REQUIRED**

Multiple-processor applications require that current-sharing capability be available to avoid power-plane splits.

Current sharing should be accurate to within 10% of the rated output current over the full output current range, except during initial power-up and transient responses. For instance, if a particular VRM model is designed to supply a 50-Ampere processor as a maximum, the difference between the output currents of two or more VRMs in parallel may be as much as 5 Amperes at any value of current actually produced, even to the point where one VRM is producing 5 Amperes and one in parallel with it is producing no current in supplying a 5-Ampere load. There is no time limit for response to power-up or transients: VRMs must meet all other electrical specifications during transitions, and output current levels must not damage the VRMs.

The VRM must supply current equal to $(\text{total load}) \times (1 + \text{tol}) / (n + \text{tol})$, where tol is the current-sharing accuracy and n is the number of VRMs sharing the load. For example, each of two parallel VRMs supplying a 130A load could have 66.6A I_{cc} capacity with 5% current sharing accuracy or 68.1A capacity with 10% accuracy.

One pin of the VRM is reserved for current sharing control for a VRM designed for starpoint or single-wire current sharing. This pin will be connected to other VRMs within the system. VRMs designed for current sharing by means of accurate output control need not use this pin. If a VRM does not use the current sharing pin, it should not be connected on the module.

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Current sharing among different VRM models, including VRMs from different manufacturers, is an expected feature, required for most multiple-processor systems. Hot-swapping capability is not a requirement.

1.2 Input Voltage and Current

1.2.1 Input Voltages

EXPECTED

The main power source for the VRM is 12V +5%, -8%. This voltage is supplied by a conventional computer power supply through a cable to the system board. The system board will supply local bulk bypassing on the 12V rail.

1.2.2 Load Transient Effects on Input Current

EXPECTED

When the VRM is providing an output current step to the load from I_{out_MIN} to I_{out_MAX} or I_{out_MAX} to I_{out_MIN} at the slew rate listed in Section 1.1.1, the slew rate of the input current to the VRM should not exceed $1.0A/\mu\text{sec}$. The system board needs sufficient bulk decoupling to ensure that the supply voltage on the system board does not go outside of regulation requirements during times of transient load on the VRM(s).

1.3 Control Inputs

Control inputs should accept an open-collector, open-drain, open-switch-to-ground, low-voltage TTL or low-voltage CMOS signal.

1.3.1 Output Enable—(OUTEN)

EXPECTED

The VRM must accept an input signal to enable the output. An open-circuit or active high enables the VRM and a ground or active low disables the VRM. The input should have an internal pull-up resistor between $1k\Omega$ and $10k\Omega$ to 3.3 or 5.0 volts. The maximum low-input voltage is 0.8V; the minimum high-input voltage is 1.7V. These inputs should be capable of withstanding up to 5.5V.

When disabled, the VRM should sink less than 100mA from the 12V Input and less than 1A from shared VRMs that remain on.

1.3.2 Voltage Identification—(VID[0:4])

REQUIRED

The VRM must accept five lines to set the nominal (maximum) voltage as defined by the table below. Five processor package pins will have a high-low pattern corresponding to the voltage required by the individual processor. When all five VID inputs are high (11111), the VRM should disable its output.

The maximum low-input voltage is 0.8V; the minimum high-input voltage is 1.7V. Each VID input should have a $1k\Omega \pm 10\%$ pull-up resistor to $3.3V \pm 5\%$.

Table 2, Voltage Identification (VID)

Processor Pins (0 = low, 1 = high)					Vcc	Processor Pins (0 = low, 1 = high)					Vcc
VID4	VID3	VID2	VID1	VID0	(VDC)	VID4	VID3	VID2	VID1	VID0	(VDC)
1	1	1	1	1	Off	0	1	1	1	1	1.475
1	1	1	1	0	1.1	0	1	1	1	0	1.5
1	1	1	0	1	1.125	0	1	1	0	1	1.525
1	1	1	0	0	1.15	0	1	1	0	0	1.55
1	1	0	1	1	1.175	0	1	0	1	1	1.575
1	1	0	1	0	1.2	0	1	0	1	0	1.6
1	1	0	0	1	1.225	0	1	0	0	1	1.625
1	1	0	0	0	1.250	0	1	0	0	0	1.65
1	0	1	1	1	1.275	0	0	1	1	1	1.675
1	0	1	1	0	1.3	0	0	1	1	0	1.7
1	0	1	0	1	1.325	0	0	1	0	1	1.725
1	0	1	0	0	1.35	0	0	1	0	0	1.75
1	0	0	1	1	1.375	0	0	0	1	1	1.775
1	0	0	1	0	1.4	0	0	0	1	0	1.8
1	0	0	0	1	1.425	0	0	0	0	1	1.825
1	0	0	0	0	1.45	0	0	0	0	0	1.85

1.4 Remote Sense (VO-sen+, VO-sen-)**EXPECTED**

A remote sense connection should be provided at the connector to allow the VRM to sense voltage elsewhere in the system and compensate for an output voltage offset of ≤ 55 mV in the power distribution path. VO-sen+ is the + sense line, and VO-sen- is the sense return. Differential sense inputs are required. In the event of an open sense line the VRM should maintain regulation through a local sense resistor on the VRM board. Systems that do not use remote sense will not connect these lines on the system board. The remote sense lines should draw no more than 1 mA, to minimize offset errors.

1.5 Power Good Output (PWRGD)**EXPECTED**

The VRM should provide an open collector Power Good signal consistent with TTL DC levels. This signal should transition to the open ($>100k\Omega$) state within 10 milliseconds of the output voltage stabilizing within the range specified in Section 1.1.1. The signal should be in the low-impedance (to ground) state whenever $V_{out_{VRM}}$ is outside of the required range below and be in the open state whenever $V_{out_{VRM}}$ is within its specified range (Table 1). On power up, the PWRGD signal must remain in the low-impedance state until the output voltage has stabilized within the required tolerance.

The minimum PWRGD voltage should be the minimum $V_{out_{VRM}}$ specified in Table 1, minus margin to prevent false de-assertion, but at least 95% of the minimum $V_{out_{VRM}}$.

The maximum PWRGD voltage should be the nominal (maximum) $V_{out_{VRM}}$ specified in Table 1, plus margin to prevent false de-assertion, but no greater than the maximum, non-operating voltage, V_{MAX} , specified in Table 1.

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This output should be capable of sinking up to 4mA, while maintaining a voltage of 0.4V or lower. When the output is in the open state it should be capable of withstanding up to 5.5V. Latch-up or damage cannot occur if the pull-up voltage on the system board is present with no +12V input present.

VRM Power Good should remain low if the VRM is disabled by the Output Enable pin. System designers need to provide appropriate logic on the system board to decode VRM Power Good, VRM Enable, and system Power Good to prevent a false not-good condition (Power Good = low) when the VRM is disabled.

The VRM should be able to detect a failure and de-assert PWRGD even if the output is within the defined PWRGD range. It is sufficient for this purpose to detect whether all phases are switching at their output inductors. The intention of this provision is to detect failures independently when VRMs are sharing current to a common power plane in a multiple-processor system.

1.6 VRM Present (VRM-pres)

EXPECTED

This line is ground when the VRM is installed. The system board can use this signal to detect when a VRM is installed in the system.

1.7 Efficiency

PROPOSED

The efficiency of the VRM should be greater than 80% at maximum output current and input voltage. It should not dissipate more power under any load condition than it does at maximum output current and maximum input voltage.

1.8 Isolation

PROPOSED

Isolation from input to output is optional. A transformer-based topology may have advantages over a non-isolated buck converter: Over-voltage due to a shorted FET is eliminated, and duty cycles can be optimized to simplify control or improve efficiency. Common ground between input and output is required with an isolated topology.

1.9 Fault Protection

These are features built into the VRM to prevent damage to itself or the circuits it powers.

1.9.1 Over Voltage Protection

EXPECTED

The VRM should provide over-voltage protection (OVP) by including a circuit, separate from the voltage sense path, capable of shutting off the output drive when the output voltage rises beyond V_{trip} . If practical, the protection circuit should also enable a low-resistance path to ground such that if the output transistor shorts to input power the output voltage will not rise above V_{trip} . A non-resettable or resettable fuse may be included in the input of the VRM for this function.

Minimum V_{trip} should be the nominal (maximum) $V_{out_{VRM}}$ specified in Table 1 plus 55mV to compensate for remote sense plus margin to prevent false trips.

Maximum V_{trip} should be the maximum, non-operating voltage, V_{MAX} , specified in Table 1.

No combination of input voltage sequences should falsely trigger an OVP event.

1.9.2 Fuse Protection for Power Input

PROPOSED

The power input (12V) should be protected with a fuse rated not greater than 30A, which sustains all operating and inrush conditions and which “blows” only on catastrophic failure of the converter.

1.9.3 Overload Protection

EXPECTED

The VRM should be capable of withstanding a continuous, abnormally low resistance on the output without damage or over-stress to the unit. Output current under this condition will be limited to no more than 150% of the maximum rated output of the VRM. Latching off or hiccup mode is acceptable during over-current conditions. The VRM should be capable of starting into a constant current load of 50% of maximum rated load current with maximum load capacitance, as defined in Section 1.1.6, without tripping the OCP circuitry. For multiple-processor systems, errors in current sharing (see Section 1.1.7) during startup should not cause OCP circuits to shut down the converter.

1.9.4 Reset After Shutdown

PROPOSED

If the VRM goes into a shutdown state due to a fault condition on its output (not an internal failure) it should return to normal operation after the fault has been removed, or after the fault has been removed and power has been cycled off and on.

2 Module Layout Guidelines

2.1 VRM Connector

EXPECTED

The VRM interface with the system board is a 0.100” pitch, 62-pin edge connector, with an overall 3.95” length: Tyco* 1364125-1 or equivalent. The connector uses a retention clip to hold the VRM in place. The connector contacts have a maximum rated temperature of 90°C, based on 4-oz. copper lands on the VRM PCB and 19 pin pairs carrying 3.6A each. (Intel does not endorse the third party products featured and/or mentioned in this document.)

Table 3 shows the VRM pin-out definitions.

Table 3, VRM Pins

Pin	Function	Pin	Function
1	VIN+	62	VIN-
2	VIN+	61	VIN-
3	VIN+	60	VIN-
4 ¹	VIN+	59 ¹	VIN-
5 ¹	Reserved ³	58 ¹	VRM-pres
6	key	57	VID4
7	VID3	56	VID2
8	VID1	55	VID0
9	Reserved ³	54	Ishare
10	PWRGD	53	OUTEN
11 ²	VO-sen-	52 ²	VO-sen+
12 ²	Reserved ³	51 ²	Reserved ³
13	VO-	50	VO+
14	VO+	49	VO+
15	VO-	48	VO-

Pin	Function	Pin	Function
16	VO+	47	VO+
17	VO-	46	VO-
18	VO+	45	VO+
19	VO-	44	VO-
20	VO+	43	VO+
21	VO-	42	VO-
22	VO+	41	VO+
23	VO-	40	VO-
24	VO+	39	VO+
25	VO-	38	VO-
26	VO+	37	VO+
27	VO-	36	VO-
28	VO+	35	VO+
29	VO-	34	VO-
30	VO+	33	VO+
31	VO-	32	VO-

¹ A single notch between pins 4&5 and between pins 58&59 is reserved for +48V input VRMs

² A single notch between pins 11&12 and between pins 51&52 identifies a +12V-input VRM

³ Reserved pins can be used for an I²C interface:

- 5 I2C_CLK
- 9 I2C_DATA
- 12 I2C_A0
- 51 I2C_A1

Figure 2 shows the connector details.

Figure 2, VRM Connector (for 12V-input VRM)
 (Intel does not endorse the third party products featured and/or mentioned in this document.)

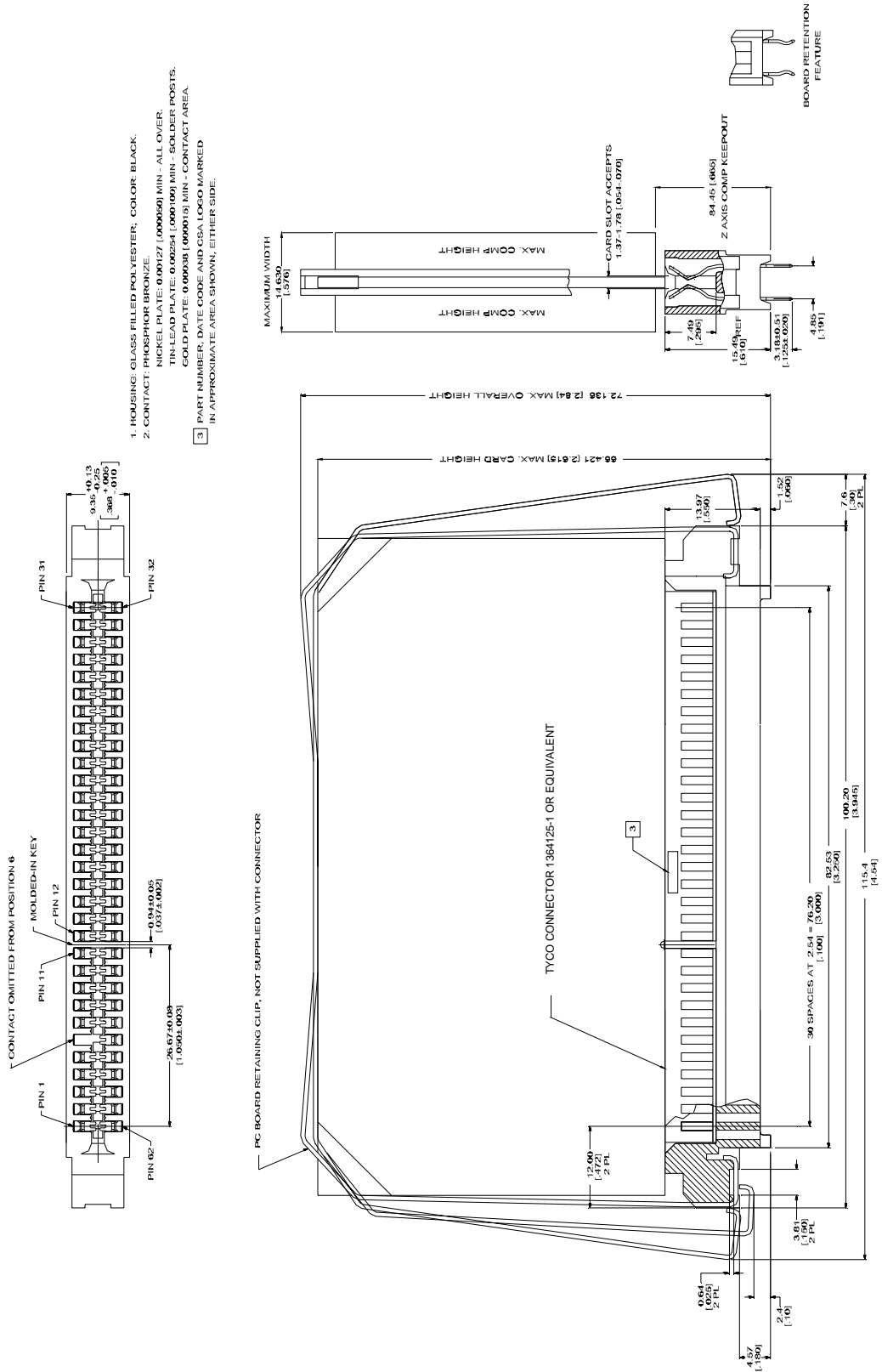
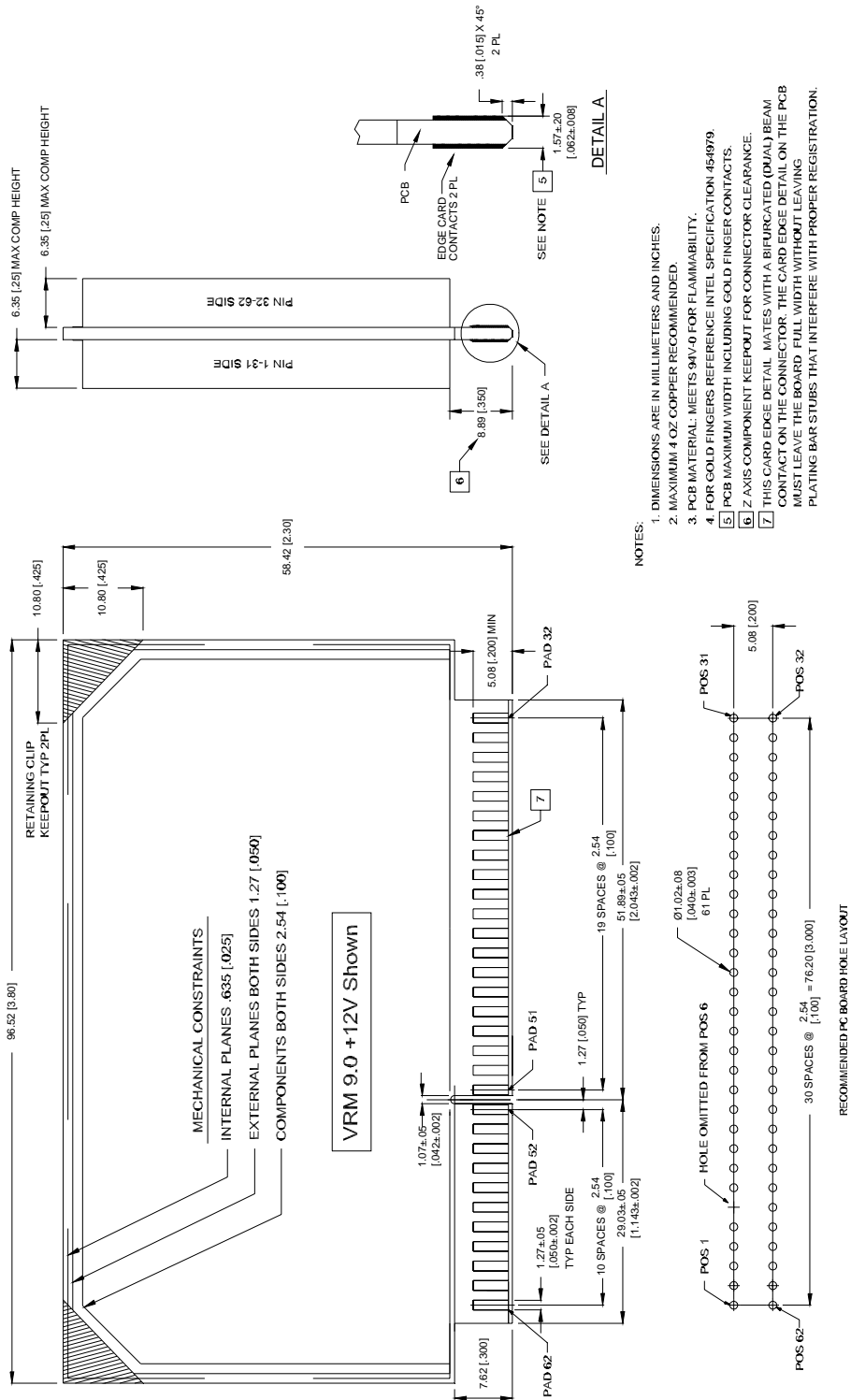


Figure 3, VRM Footprint and Space Requirements



2.2 Mechanical Dimensions

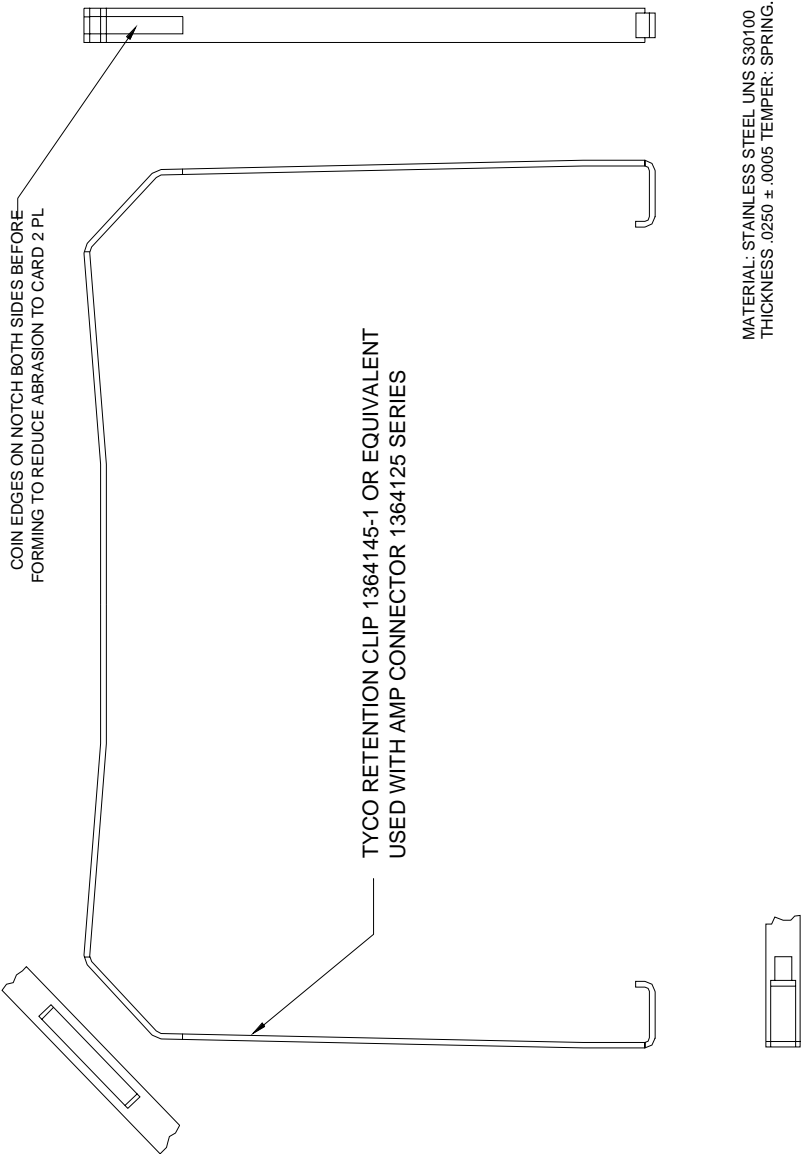
PROPOSED

The maximum outline dimensions of the VRM should be as shown in Figure 3:

2.3 Retention Clip

The module will require retention hardware to maintain mechanical and electrical contact during system use and handling. Figure 4 describes one example of such a clip, which fits within the dimensional envelope of Figure 3.

Figure 4, VRM Retention Clip
(Intel does not endorse the third party products featured and/or mentioned in this document.)



2.4 Alternate Module Dimensions

An optional module with the following features provide cost and thermal advantages in some systems.

2.4.1 Dimensions

The dimensional option increases the maximum component thickness on the pin 1-31 side of the module PCB from 0.25" to 0.50" (increases total module thickness from 0.576", shown in Figure 3, to 0.826").

2.4.2 Thermal capability

The intention of the greater thickness is to make room for heat sinking, accommodating higher temperatures or lower airflow.

2.4.3 Capacitors

A further option places input and output filter capacitors on the system board instead of the module. This puts the filtering on the load side of the VRM connector, opening up additional heat sink space and reducing total component costs.

2.5 Heat Sink Connection

Heat sinks cannot be connected to any potential other than ground.

2.6 Board Temperature

To maintain the connector within its operating temperature, the VRM board temperature at the connector interface must not exceed a temperature of 90°C within 2.54 mm (0.1") from the top of the connector. To meet the 90°C limit, a board constructed from 4-ounce cladding is recommended.

The VRM board must interface with the connector through gold lands (fingers) that are 1.27 ± 0.05 mm ($.050 \pm .002$ ") wide by a minimum of 5.08 mm (.200") long and spaced 2.54 ± 0.05 mm ($.100 \pm .002$ ") apart. Traces from the lands to the power plane should be a minimum of 0.89 mm (.035") wide and a minimal length.

3 Tests and Standards

3.1 Environmental

PROPOSED

Design, including materials, should be consistent with the manufacture of units that meet the environmental reference points in Table 4.

Table 4, Environmental Specifications

	Operating	Non-Operating
Temperature	VRM ambient 0°C to +60°C at full load with a maximum rate of change of 10°C/hour and air at a velocity of 400 LFM directed along the connector axis ¹	Ambient –40°C to 70°C with a maximum rate of change of 20°C/hour. ²
Humidity	To 85% relative humidity.	To 95% relative humidity.
Altitude	0 to 10,000 feet	0 to 50,000 feet.
Electrostatic discharge	15 KV initialization level. The direct ESD event shall cause no out-of-regulation conditions. ³	25 KV initialization level.

¹ See Section 1.1 for test conditions. Air flow at 400 LFM applies to modules for server and workstation systems; desktop motherboards typically get much less airflow.

² Thermal shock of –40°C to +70°C, 10 cycles; transfer time shall not exceed 5 minutes, duration of exposure to temperature extremes shall be 20 minutes.

³ Includes overshoot, undershoot, and nuisance trips of over-voltage protection, over-current protection or remote shutdown circuitry.

3.2 Shock and Vibration

PROPOSED

The VRM should not be damaged and the interconnect integrity not compromised during:

- A shock of 50G with an 11 millisecond half sine wave, non-operating, the shock to be applied in each of the orthogonal axes.
- Vibration of 0.01G² per Hz at 5 Hz, sloping to 0.02G² per Hz at 20 Hz and maintaining 0.02G² per Hz from 20 Hz to 500 Hz, non-operating, applied in each of the orthogonal axes.

3.3 Electromagnetic Compatibility

PROPOSED

Design, including materials, should be consistent with the manufacture of units that comply with the limits of FCC Class B and CISPR22 Class B for radiated emissions.

3.4 Reliability

PROPOSED

Design, including materials, should be consistent with the manufacture of units with an MTBF of 500,000 hours of continuous operation at 55°C, maximum-outputs load, and worst-case line, while meeting specified requirements. MTBF should be calculated in accordance with MIL-STD-217F.

3.5 Safety

PROPOSED

The voltage regulator is to be UL Recognized to standard UL1950 3rd Ed., including requirements of IEC950 and EN 60950. Plastic parts and printed wiring board are to be UL Recognized with 94V-0 flame class.