Voltage Regulator-Down (VRD) 10.0

Design Guide Addendum

Intel® Pentium® 4 processor Extreme Edition supporting Hyper-Threading Technology[1] in Socket 478

November 2003

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Revision History

Revision Number	Description	Revision Date
-001	• Initial Release.	November 2003

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1 Introduction

This document defines DC-to-DC converters to meet the power requirements of desktop computer systems using Intel® Pentium® 4 processor Extreme Edition supporting Hyper-Threading Technology[1] in socket 478. Requirements vary according to the needs of different computer systems and processors that a specific voltage regulator is expected to support. The voltage regulator-down (VRD) designation in this document refers to a voltage regulator embedded on a motherboard, for a single processor.

Each implementation on a specific board must meet the specifications of all processors supported by that board. The specifications in the respective processor Datasheets always take precedence over the data in this document.

Note: A load line selection circuit is required to switch between the two processor voltage specifications if the processor code named Prescott is to be supported in a system designed for Intel® Pentium® processor Extreme Edition supporting Hyper-Threading Technology in socket 478. In addition, the platform must support the full Dynamic Voltage Identification functionality of VRD10.0.

VRD 10 incorporates functional changes from prior VRD and VRM guidelines:

- Addition of dynamic voltage identification to change the output voltage during normal operation, in response to an input from the processor.
- Simplified definition of power-good as a power-up indication (Section 6.1)
- Extended use of the VRD enable function to turn off the output in response to an input from the processor.
- Thermal monitoring of the VRD (Section 6.2).
- Addition of V_{CC} Overshoot specification (Section 2.8)

1.1 Terminology

The following guideline categories are used throughout this document:

Term	Description
REQUIRED	An essential part of the design — necessary to meet processor voltage and current specifications and follow processor layout guidelines
EXPECTED	Part of Intel® processor power definitions; necessary for consistency among the designs of many systems and power devices. May be specified or expanded by system OEMs.
PROPOSED	Normally met by this type of DC-to-DC converter and, therefore, included as a design target. May be specified or expanded by system OEMs.

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2 Processor Voltage Requirements

2.1 Voltage and Current (REQUIRED)

A six-bit VID code supplied by the processor to the VRD determines a reference output voltage, as described in Section 3.2. The load lines in Section 2.2 show the relationship between Vcc and Icc for the processor, and the tolerances between Vcc-minimum and Vcc-maximum.

Intel performs exhaustive testing against multiple software applications and software test vectors to identify valid processor Vcc operating ranges. Failure to satisfy the load line, load line tolerance band, and overshoot specifications (section 2.2, 2.3 and 2.8) may cause data corruption, intermittent system lockup and lead to premature processor failure. In addition this could void the Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology in socket 478 processor warranty.

2.2 Load Line Definitions (REQUIRED)

The following load lines contain DC and transient-droop data as well as maximum and minimum voltage levels. The voltages are measured at the processor-socket Vcc and Vss pins between the voltage regulator and the processor cavity. For standard layouts these measurements are taken at Vcc pin AC14 and Vss pin AC15. In some instances these two pins will not be located between the voltage regulator and the processor cavity. In these cases, select pins that are centered in the pin field between the cavity and the voltage regulator. It is recommended to place test points to these pins on the bottom side of the motherboard to enable load line tuning and validation.

Table 1: Intel® Pentium® 4 processor Extreme Edition Supporting Hyper-Threading Technology Power Delivery Specifications

Iccmax	VR TDC	Dynamic Icc	Socket Load Line	VRD Tolerance Band	Max VID
91A	80A	70A	1.50mOhms	+/- 19mV	1.600[1]

NOTE:

1. Maximum projected Pentium 4 processor Edition supporting Hyper-Threading Technology VID

The following figures and tables show load-line voltage offsets and current levels based on the VID settings specified in Table 6. The following equations for the load lines are valid for the range of load current from 0 A to 91 A.

Intel® Pentium® 4 processor Extreme Edition Supporting Hyper-Threading Technology Load Line Equations

V_{MAX} load line: Vcc = VID – (1.50 mOhms * Icc)

V_{TYP} load line: Vcc = VID – 0.019 V – (1.50 mOhms * Icc)

V_{MIN} load line: Vcc = VID – 0.038 V - (1.50 mOhms * Icc)

Figure 1. Intel® Pentium® 4 processor Extreme Edition Supporting Hyper-Threading Technology Vcc Load Line at Processor Socket Represented as Deviation From VID.

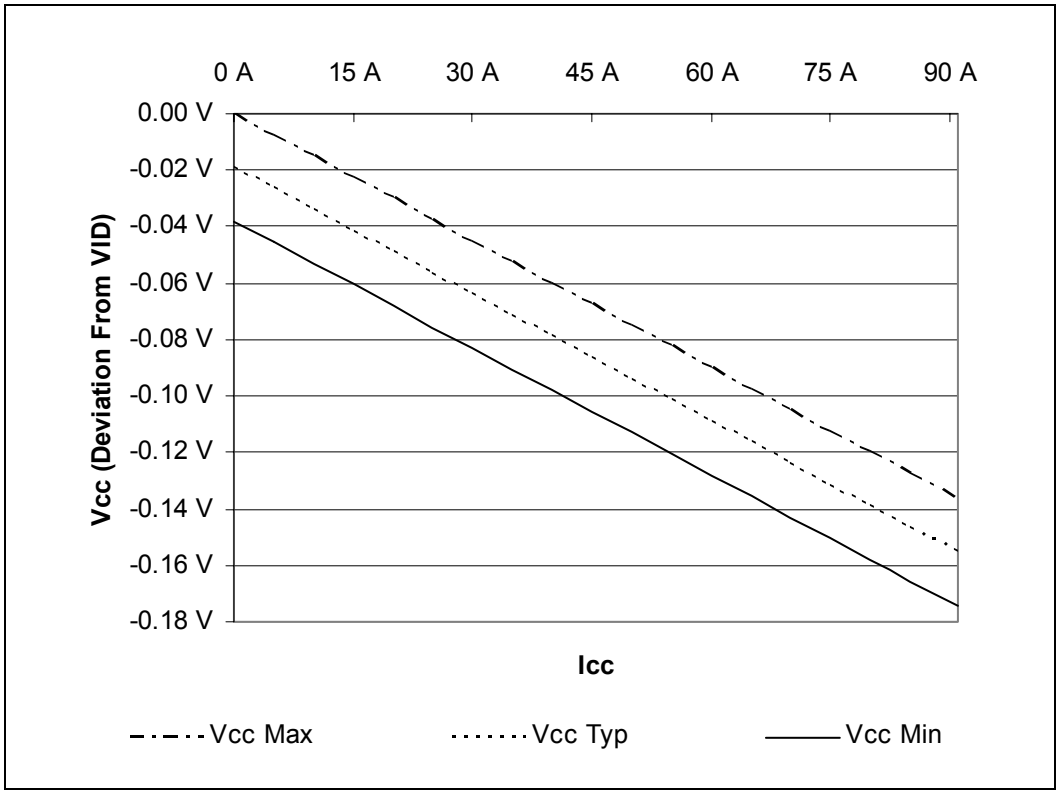


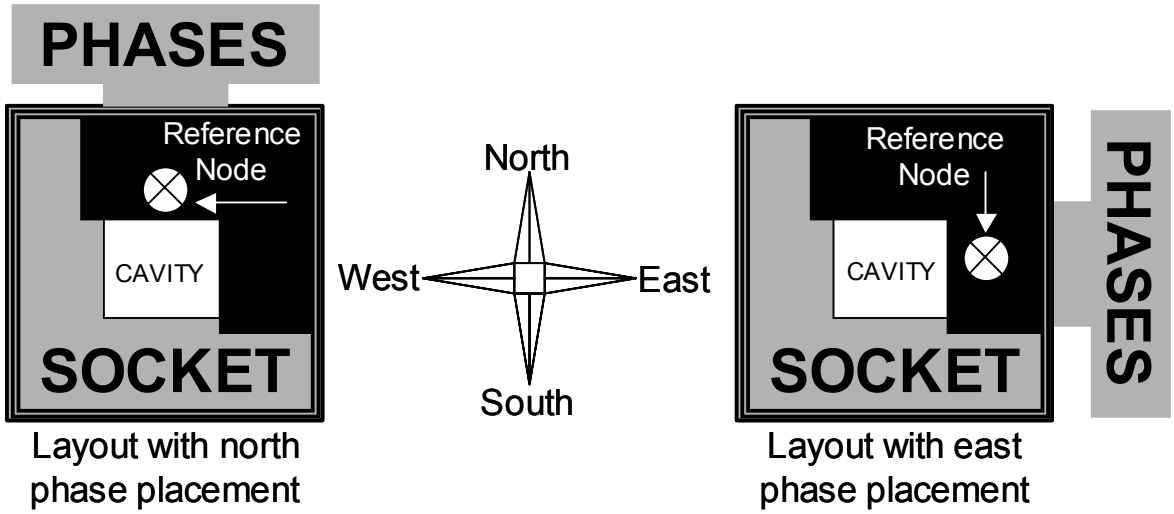
Table 2. Intel® Pentium® 4 processor Extreme Edition Supporting Hyper-Threading Technology Vcc Load Line at Processor Socket Represented as Deviation From VID.

Icc	Vcc Max	Vcc Typ	Vcc Min
0 A	0.000 V	-0.019 V	-0.038 V
10 A	-0.015 V	-0.034 V	-0.053 V
20 A	-0.030 V	-0.049 V	-0.068 V
30 A	-0.045 V	-0.064 V	-0.083 V
40 A	-0.060 V	-0.079 V	-0.098 V
50 A	-0.075 V	-0.094 V	-0.113 V
60 A	-0.090 V	-0.109 V	-0.128 V
70 A	-0.105 V	-0.124 V	-0.143 V
80 A	-0.120 V	-0.139 V	-0.158 V
91 A	-0.137 V	-0.156 V	-0.175 V

NOTES

1. The load line specifications include both static and transient limits.
2. Always use the specific processor's datasheet or design guides for actual Vcc and Icc requirements.

Figure 2: VRD Phase Orientation



2.3 TOB: Voltage Tolerance Band (REQUIRED)

Processor load line specifications must be guaranteed across component process variation, system temperature extremes, and age degradation limits. For the Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology, the VRD topology and component selection must maintain a 3-sigma tolerance of +/-19mV around the typical load line (see Table 2). The critical parameters include voltage ripple, VRD controller tolerance, and current sense tolerance. Individual tolerance components will vary among designs; the processor requires only that the total error stack-up stay within the defined +/-19mV at the FMB limits.

2.3.1 Sources of Voltage Deviation & Input Parameters

The standard VRD tolerance band (TOB) can be sliced into three main categories: controller tolerance, current sense variation, and voltage ripple.

Controller tolerance is determined by the DAC accuracy (digital to analog conversion) and DC offset of the internal controller circuitry (i.e. op amp offset). These tolerance parameters are functions of the operating voltage associated with the programmed VID (defined in Table 1). Internal controller circuitry also includes a tolerance associated with current sense signal conversion that must be included in the TOB calculation. Consult the controller data sheet or vendor for the particular component specifications.

VRD current sensing occurs by processing a sensed voltage across a component in the direct output current path. Current conversion occurs with knowledge of the device resistance. The tolerance of this sense method is directly aligned with the sense element's tolerance. For inductor, resistor, and FET sensing, the series resistance tolerance of the sense component is a critical factor for calculating the TOB. Integrating capacitors are part of the inductor current sense circuit and the manufacturing tolerance including thermal drift must be identified to ensure correct TOB calculations. For inductor and FET sensing, thermal compensation (see section 2.4) is required to maintain a linear load line across the full, operational system temperature range.

Peak ripple must not exceed +/-5mV at the VRD measurement nodes. Ripple is typically suppressed by increasing the value of the output inductance or by increasing the value/quantity of ceramic capacitors in the high frequency filter (see 2.9).

Table 3: Input parameters for VRD TOB calculation

Parameter	Definition	Units
I_{dyn}	FMB defined current step amplitude [1]	A
I_{max}	Maximum FMB load current [1]	A
k_C	Tolerance of CS capacitance [2 3]	[±% @ 3-σ]
k_{ESR}	Tolerance of inductor ESR [4 6]	[±% @ 3-σ]
k_{gm}	Controller tolerance of current signal conversion	[±% @ 3-σ]
k_L	Tolerance of output inductance [4]	[±% @ 3-σ]
k_{RDS}	Tolerance of FET RDS-ON [4]	[±% @ 3-σ]
k_{rsense}	Tolerance of sense resistor [4]	[±% @ 3-σ]
k_{VID}	Controller reference voltage (VID) tolerance	[±% @ 3-σ]
n_{ph}	Number of independent phases in VRD	-
n_{rsense}	Number of sense resistors	-
R_{AVP}	AVP (Socket Load Line) resistance	[Ω]
V_{ripple}	Peak ripple voltage: Max = 5mV peak	[±V]
V_{TC}	Thermal compensation transient error	[±V]

NOTES:
1: See Table 1
2: Statistical root-sum-square may be applied if more than one component is used
3: Tolerance is to include parameter thermal drift across operational temperature
4: Thermal variation of parameter is included in VTC if thermal compensation is applied
5: All parameter tolerances are defined at 3-sigma. Many vendors define some common parameters, such as inductor tolerance and inductor ESR, at 6-sigma. These numbers should be translated to 3-sigma to obtain an accurate TOB calculation.
6: Vendors commonly refer to this parameter as RDC and it is generally a 6-sigma tolerance value

2.3.2 TOB: Tolerance Band Calculation

Reference TOB equations for each major current sense topology are provided in the next three subsections. Equations are presented in a manner for simple entry into a spreadsheet to simplify TOB calculation and design iterations.

2.3.2.1 Inductor RDC Current Sense TOB Calculations

Inductor sensing is the best general approach to satisfying the tolerance band requirements. TOB can be directly controlled by selecting output inductors and integrating capacitors of sufficient tolerance. Inductor thermal drift will require thermal compensation to keep the load line linear (see 2.4). Capacitor thermal drift must also be considered in the tolerance and Intel recommends COG capacitors for their thermal stability. Understanding component variation is critical for calculating Inductor Sense TOB; many component tolerances are defined under 6-sigma variation, which should be translated to 3-sigma for calculation purposes.

$$TOB_{manuf} = \sqrt{(VID.k_{VID})^2 + V_{AVP}^2.(k_{gm}^2 + \frac{k_{ESR}^2}{n_{ph}}) + V_{AVPdyn}^2.(\frac{k_L^2 + k_C^2}{n_{ph}})}$$

$$V_{AVPdyn} = I_{dyn}.R_{AVP}$$

$$V_{AVP} = I_{max}.R_{AVP}$$

$$TOB = TOB_{manuf} + V_{ripple} + V_{TC}$$

2.3.2.2 Resistor Current Sense TOB Calculations

Resistor sensing topologies have the capability to provide the tightest TOB solutions due to a wide industry selection of precision resistors. However, the accuracy comes at a price. Resistors are placed in series with the output current, which results in substantial power loss and heat generation. The resulting power dissipation requires large, expensive, high wattage resistors, which demand additional cooling to keep components and motherboard layers below maximum allowable temperature limits. Power loss may be mitigated by selecting a low value of resistance, however minimum signal amplitude must be considered for adequate current conversion (i.e. signal to noise ratio).

$$TOB_{manuf} = \sqrt{(VID.k_{VID})^2 + V_{AVP}^2.(k_{gm}^2 + \frac{k_{rsense}^2}{n_{rsense}})}$$

$$V_{AVP} = I_{max}.R_{AVP}$$

$$TOB = TOB_{manuf} + V_{ripple}$$

2.3.2.3 FET RDS-ON Current Sense TOB Calculations

Current can be determined by sensing the voltage across the VRD switching FET's drain to source 'on' resistance. While this provides a direct method of voltage to current conversion, the standard FET RDS-ON tolerance of ~20% is not acceptable to satisfy the Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology tolerance band requirements. If RDS-ON sensing is to be applied, FET thermal compensation is required (see section 2.4) together with a tight FET RDS-ON distribution (approximately 5% at 3-sigma). Since boards are generally build with FETs from similar manufacturing lots, process to process variation is not random and the RDS-ON parameter may not be reduced through statistical analysis.

$$TOB_{manuf} = \sqrt{(VID.k_{VID})^2 + V_{AVP}^2.(k_{gm}^2 + k_{RDS}^2)}$$

$$V_{AVP} = I_{max}.R_{AVP}$$

$$TOB = TOB_{manuf} + V_{ripple} + V_{TC}$$

2.4 VRD Thermal Compensation (REQUIRED)

The Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology can draw significant levels of current, resulting a varying temperature gradient across electrical components. Electrical parameters of these components are functions of temperature and their values will drift with the thermal gradient. This drift will result in a load line violation. To ensure compliance to specifications, the voltage regulator requires thermal compensation.

Thermal compensation allows the processor Vcc voltage regulator to respond to temperature drift in VRD electrical parameters. It is required to ensure that regulators using inductor or FET RDS-ON current sensing maintain a stable voltage over the full range of load current and system temperatures.

If thermal compensation is not included, the output voltage of the regulator will droop as the resistance of the sense element increases with temperature. With the increased resistance, the regulator falsely detects an increase in load current and regulates to a lower voltage. Thermal compensation prevents this thermally induced voltage droop by adjusting the feedback path based on the temperature of the regulator. This is accomplished by placing a thermistor in the feedback network, tuned with a resistor network to negate the effects of the increased resistance of the sense element.

The thermal compensation circuit is to be validated by running the regulator at VR TDC for 30 to 45 minutes. This is to ensure the board is thermally saturated and system temperatures have reached a maximum steady state condition. If the thermal compensation has been properly implemented, the output voltage will only drift 1-2 mV from its coolest temperature condition. If the thermal compensation has not been properly implemented, the voltage can droop in the 10's of mV range

2.5 Electrical & Thermal Current Support (EXPECTED)

System boards supporting Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology should have voltage regulator designs compliant to the FMB parameters defined in Table 1. This includes full electrical support of 91 A Icc max specifications and robust cooling solutions to support 80 A thermal design current (VR TDC) indefinitely within the envelope of system operating conditions

Intel processor's VR TDC is the sustained (DC equivalent) current parameter that is to be used for voltage regulator thermal design with supporting Thermal Monitor circuitry (see Section 6.2). At VR TDC, switching FETs reach maximum temperature heating the motherboard layers and neighboring components to the pass/fail boundary of thermal limits. Actual component and board temperatures are established by the envelope of the system's operating conditions. This includes voltage regulator layout, processor fan selection, ambient temperature, chassis configuration, etc.

In some instances the CPU VRD will also power other motherboard components such as the chipset. Under these conditions the VRD will supply current above the FMB limits; VRD designers must budget this additional current support in final VRD designs while remaining compliant to electrical and thermal specifications.

2.6 Stability (EXPECTED)

The VRD needs to be unconditionally stable under all specified output voltage ranges and current transients. The VRD should operate in a no-load condition: i.e., with no processor installed. Normally the no-processor VID code will be x1111, disabling the VRD (Section 2.10).

2.7 Processor Power Sequencing (REQUIRED)

The VRD must support platforms with defined power-up sequences. Figure 3 is a block diagram of a power sequencing implementation, and Figure 4 is a timing diagram of the power sequencing requirements.

Figure 3. Power-on Sequence Block Diagram

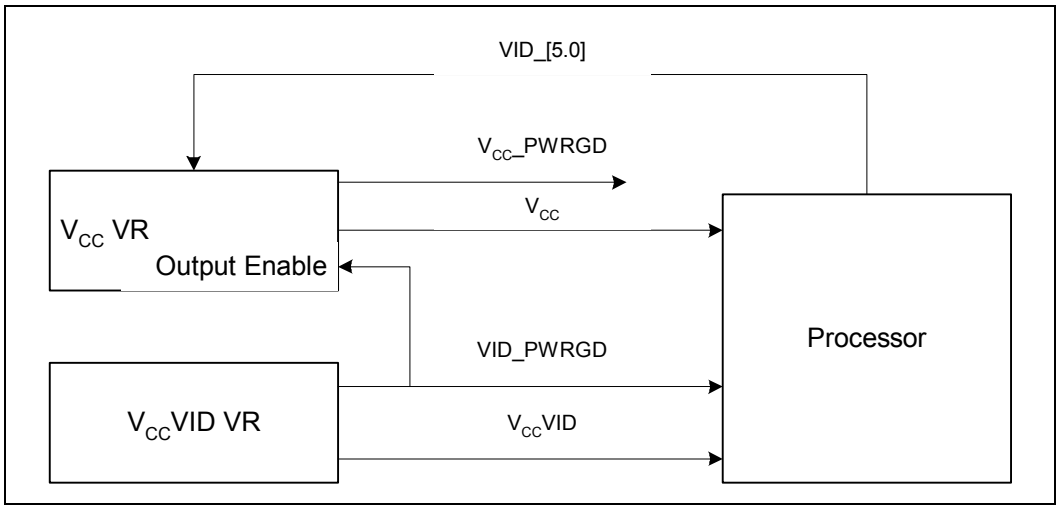
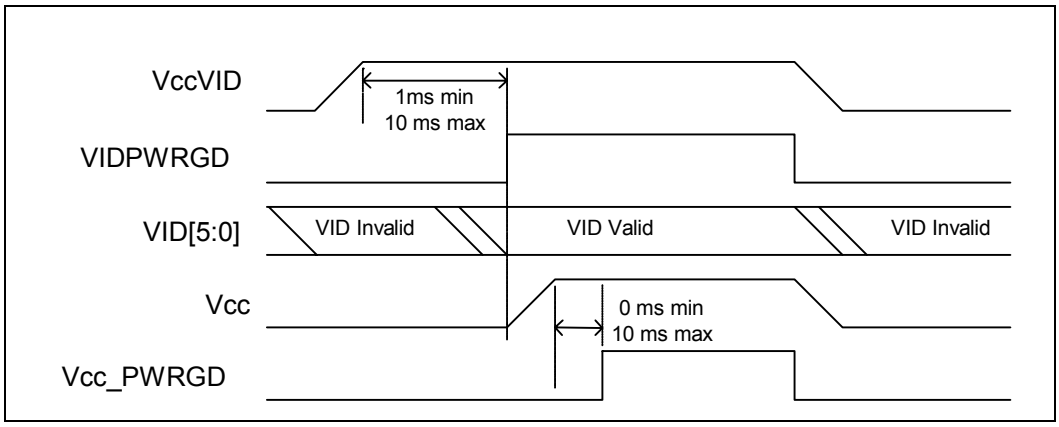


Figure 4. Power Sequence Timing Diagram



NOTES:
1. VccVID comes up at the application of system power to the VccVID VRD.
2. VccVID VRD generates VID_PWRGD, to latch the processor's VID outputs and enable Vcc VRD, after the VccVID supply is valid.
3. Vcc_PWRGD is generated by the Vcc VRD and may be used elsewhere in the system.

2.8 Processor Vcc Overshoot (REQUIRED)

The Pentium processor 4 Extreme Edition supporting Hyper-Threading Technology in socket 478 is capable of tolerating short transient overshoot events above VID on the Vcc supply that will not impact processor lifespan or reliability. Maximum processor Vcc overshoot, V_{OS}, cannot exceed VID+V_{OS_MAX}. Overshoot duration, T_{OS}, cannot stay above VID for a time more than T_{OS_MAX}.

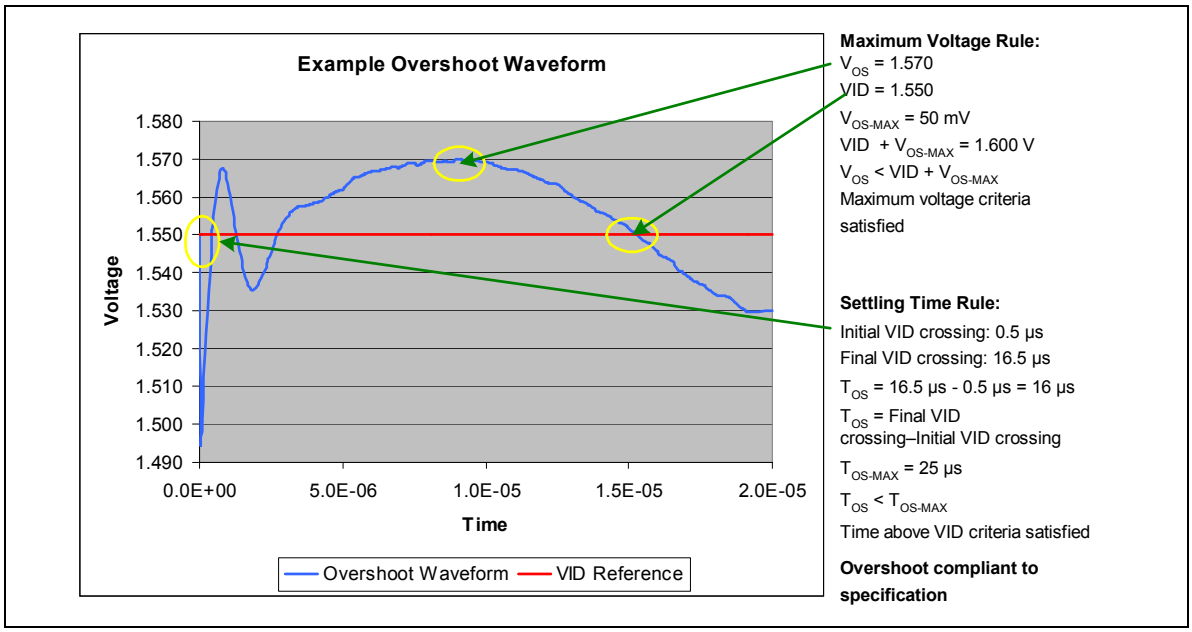
Overshoot Specifications:
V_{OS_MAX} = Maximum overshoot voltage above VID = 50 mV
T_{OS_MAX} = Maximum overshoot time duration above VID = 25 µs

See Figure 5 for an example of the socket Vcc overshoot specification.

Socket Specification: Maximum overshoot in socket 478 can to be tuned by applying a current load release across the socket Vcc and Vss pin field and measured across reference pins identified in Section 2.2. The platform voltage regulator output filter must be stuffed with a sufficient number of capacitors to ensure that overshoot says above VID for a time no longer than T_{OS_MAX} and never exceeds the maximum amplitude of VID+V_{OS_MAX}+. Boards in violation must be redesigned for compliance to avoid processor damage. For the Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology, the defined current load release is 70 A. See Figure 5.

Note: + Assumes measurement with a 20 MHz bandwidth limited oscilloscope.

Figure 5. Example Socket Vcc Overshoot Waveform



2.9 Desktop VRD Output Filter (REQUIRED)

Processor voltage regulators include an output filter to minimize transient noise on the Vcc rail. Design analysis determined that the most cost efficient filter solution, for satisfying load line requirements, incorporates 680 µF aluminum-poly capacitors with 5mOhm average ESR. High frequency noise and ripple suppression is best minimized by 22 µF multi-layer ceramic capacitors (MLCC's). It is recommended to maximize the MLCC count in the socket cavity to help suppress transients induced by processor packaging hardware. Remaining MLCC's should be first placed adjacent to the socket edge in the region between the socket cavity and the voltage regulator. If additional MLCC's are needed to satisfy the load line, they should be placed on the socket edge that is opposite the VRD adjacent edge.

Prescott Processor Dynamic VID mode of operation is directly impacted by the choice of bulk capacitors in the output filter. If the Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology motherboard design is to be compatible with the Prescott processor, it is recommended to minimize Vcc setting time during Dynamic VID operation to hasten the speed of power and core temperature reduction. The speed of recovery is directly related to the RC time constant of the output filter. To ensure adequate thermal recovery time, it is recommended to design the output filter with a minimal amount of bulk capacitance with minimum ESR, while providing a sufficient amount of decoupling to maintain load line requirements. At this time, 680uF aluminum poly capacitors with 5 mΩ average ESR have been identified as the preferred solution. =

Note: A load line selection circuit is required to switch between the two processor voltage specifications if the processor code named Prescott is to be supported in a system designed for Intel® Pentium® processor Extreme Edition supporting Hyper-Threading Technology in socket 478. In addition, the platform must support the full Dynamic Voltage Identification functionality of VRD10.0.

Consult the relevant chip-set design guidelines for further information on the output filter capacitor selection, quantity, and placement. Consult appropriate design guidelines for mobile output filter design.

2.10 Shutdown Response (REQUIRED)

Once the VRD is operating after power up, if it sees a disable signal in the form of either de-asserted Output Enable or VID [4:0] (VID5 is a don't care in this case) = 11111, it should turn off its output (the output should go to high impedance) within 500 ms.

3 Control Inputs

3.1 Output Enable (REQUIRED)

The VRD should accept an input signal to enable the output. When disabled, the VRD output should be in a high-impedance state and should not source current. Once the VRD is operating after power-up, it should respond to a de-asserted Output Enable by turning off its output within 500 ms. When Output Enable is pulled low during the shutdown process, the VRD should not exceed its previous voltage level regardless of the VID setting during the shutdown process. No negative voltage below –100 mV may be present at the VRD output.

Table 4. Output Enable Specifications

Design Parameter	Specification		
	Minimum	Maximum	Units
Pull-Up Voltage Range	0	V_{CC} VID	
Pull-Up Resistor1	1 k	2.6 k	Ohms
V_{IH}	0.8		Volts
V_{IL}		0.3	Volts

NOTES:
1. Range includes tolerances

3.2 Voltage Identification (VID [5:0]) (REQUIRED)

The VRD must accept six lines to set the nominal processor voltage as defined by the table below. Six processor pins will have a pattern corresponding to the voltage required by the individual processor.

VID [4:0] are compatible with Intel® Xeon™ and Pentium 4 processors using five-bit VID codes. VID [5:0] will be used on processors with six-bit codes.

Table 5. VID Specifications

Design Parameter	Specification		
	Minimum	Maximum	Units
Pull-Up Voltage Range	3.135	3.465	Volts
Pull-Up Resistor[1]	950	1050	Ohms
VIH[2]	0.8		Volts
VIL[2]		0.4	Volts
Processor leakage current, for pull-up to > 2.5V)	100	200	Microamperes

NOTES:

1. Range includes tolerances. Pull-up resistors should not be integrated into the PWM controller (values may be adjusted on the system board for signal integrity).
2. Other platform components may use VID inputs and require tighter limits.

Table Shown for reference.

Table 6. Voltage Identification (VID)

Processor Pins (0 = low, 1 = high)						Vout (V)		Processor Pins (0 = low, 1 = high)						Vout (V)
VID5	VID4	VID3	VID2	VID1	VID0			VID5	VID4	VID3	VID2	VID1	VID0	
0	0	1	0	1	0	0.8375		0	1	1	0	1	0	1.2125
1	0	1	0	0	1	0.8500		1	1	1	0	0	1	1.2250
0	0	1	0	0	1	0.8625		0	1	1	0	0	1	1.2375
1	0	1	0	0	0	0.8750		1	1	1	0	0	0	1.2500
0	0	1	0	0	0	0.8875		0	1	1	0	0	0	1.2625
1	0	0	1	1	1	0.9000		1	1	0	1	1	1	1.2750
0	0	0	1	1	1	0.9125		0	1	0	1	1	1	1.2875
1	0	0	1	1	0	0.9250		1	1	0	1	1	0	1.3000
0	0	0	1	1	0	0.9375		0	1	0	1	1	0	1.3125
1	0	0	1	0	1	0.9500		1	1	0	1	0	1	1.3250
0	0	0	1	0	1	0.9625		0	1	0	1	0	1	1.3375
1	0	0	1	0	0	0.9750		1	1	0	1	0	0	1.3500
0	0	0	1	0	0	0.9875		0	1	0	1	0	0	1.3625
1	0	0	0	1	1	1.0000		1	1	0	0	1	1	1.3750
0	0	0	0	1	1	1.0125		0	1	0	0	1	1	1.3875
1	0	0	0	1	0	1.0250		1	1	0	0	1	0	1.4000
0	0	0	0	1	0	1.0375		0	1	0	0	1	0	1.4125
1	0	0	0	0	1	1.0500		1	1	0	0	0	1	1.4250
0	0	0	0	0	1	1.0625		0	1	0	0	0	1	1.4375
1	0	0	0	0	0	1.0750		1	1	0	0	0	0	1.4500
0	0	0	0	0	0	1.0875		0	1	0	0	0	0	1.4625
1	1	1	1	1	1	OFF[1]		1	0	1	1	1	1	1.4750
0	1	1	1	1	1	OFF[1]		0	0	1	1	1	1	1.4875
1	1	1	1	1	0	1.1000		1	0	1	1	1	0	1.5000
0	1	1	1	1	0	1.1125		0	0	1	1	1	0	1.5125
1	1	1	1	0	1	1.1250		1	0	1	1	0	1	1.5250
0	1	1	1	0	1	1.1375		0	0	1	1	0	1	1.5375
1	1	1	1	0	0	1.1500		1	0	1	1	0	0	1.5500
0	1	1	1	0	0	1.1625		0	0	1	1	0	0	1.5625
1	1	1	0	1	1	1.1750		1	0	1	0	1	1	1.5750
0	1	1	0	1	1	1.1875		0	0	1	0	1	1	1.5875
1	1	1	0	1	0	1.2000		1	0	1	0	1	0	1.6000

NOTES:
1. Output disabled – the same as de-asserting the output enable input (Section 3.1).

3.3 Differential Remote Sense Input (REQUIRED)

The PWM controller should include differential sense inputs to compensate for an output voltage offset of ≤ 300 mV in the power distribution path. The remote sense lines should draw no more than 10 mA, to minimize offset errors. Refer to Section 2.2 for measurement location.

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4 Input Voltage and Current

4.1 Input Voltages (EXPECTED)

The main power source for the VRD is 12 volts ±15%. This voltage is supplied by an AC DC power supply through a cable to the motherboard. For input voltages outside the normal operating range, the VRD should either operate properly or shut down.

4.2 Load Transient Effects on Input Current (EXPECTED)

The design of the VRD, which includes the input power delivery filter, must ensure that the maximum slew rate of the input current does not exceed 1A/µsec, as specified for the ATX12V, SFX12V or TFX12V (Thin Form Factor with 12V connector) power supply.

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5 Output Protection

These are features built into the VRD to prevent damage to itself, the processor, or other system components.

5.1 Over-Voltage Protection (OVP) (PROPOSED)

An OVP circuit should monitor the output for an over-voltage condition. If the output is more than 200mV above the maximum VID level, the VRD should shut off the Vcc supply to the processor.

5.2 Over-Current Protection (OCP) (PROPOSED)

The VRD should be capable of withstanding a continuous, abnormally low resistance on the output without overstressing the voltage regulator. Output current under this condition should be limited to avoid component damage and violation of the VRD thermal specifications (see Section 2.5).

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6 Output Indicators

6.1 Processor Power Good Output (Vcc_PWRGD) (PROPOSED)

The VRD should provide a power-good signal, which remains in the low state until a maximum of 10 milliseconds after the output voltage reaches the range specified in Section 2.2. The signal should then remain asserted when the VRD is operating, except for fault or shutdown conditions. Vcc_PWRGD must not be de-asserted during the Dynamic VID operation.

Table 7. Power Good Specifications

Design Parameter	Specification
Signal Type	Open-collector or equivalent
Voltage Range	5.5 V (maximum) in open state
Minimum I_{OL}	4 mA
Maximum V_{OL}	0.4 V

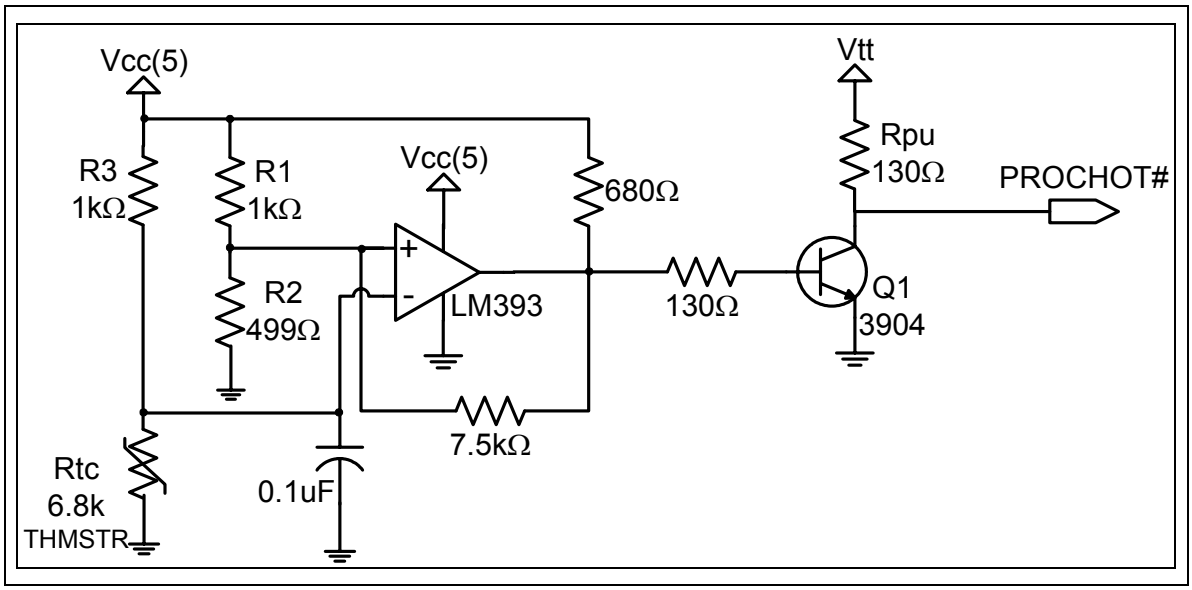
6.2 VRD Thermal Monitoring (Proposed)

This section describes how to protect the voltage regulator design from heat damage while supporting thermal design current (VR TDC) specifications. It is included for reference and is applicable to Pentium 4 processor Extreme Edition supporting Hyper-Threading Technology in socket 478 designs. It is not recommend integrating this feature into Vcc PWM controller designs.

Each customer is responsible for identifying maximum temperature specifications for all components in the voltage regulator design and ensuring that these specifications are not violated while continuously drawing specified VR TDC levels. In the event of a catastrophic thermal failure, the thermal monitoring circuit is to assert the PROCHOT# signal immediately prior to exceeding maximum motherboard and component thermal ratings to prevent heat damage. Assertion of this signal will lower processor power consumption and reduce current draw through the voltage regulator, resulting in lower component temperatures. Assertion of PROCHOT# degrades system performance and must never occur when drawing less than specified thermal design current.

VRD temperature violations can be detected using a thermal sensor and associated control circuitry (see Figure 6). For this implementation, a thermistor (THMSTR) is placed in the temperature sensitive region of the voltage regulator. The location must be chosen carefully and is to represent the position where initial thermal violations are expected to occur. When exceeded, the thermal monitor circuit is to initiate PROCHOT# to protect the voltage regulator from heat damage.

Figure 6. Example VRD Thermal Monitor Circuit Design



Note: Where $R_2 = R_1/R_3 * R_{tc}$. Thermister is NTHS0603N02N6801JR or equivalent. Where R_{tc} represents the thermister resistance at maximum allowable temperature.

Assertion of PROCHOT# is governed by the comparator (LM393) using the sensor voltage (at the negative comparator terminal) and a trigger reference voltage (at the positive comparator terminal). As the thermistor temperature increases due to system loading, the resistance will decrease. When the voltage drop across the thermistor falls below the trigger reference voltage, established by R1 and R2, the comparator will change state and bias the bipolar transistor (Q1). When biased, Q1 provides the active low signal assertion of PROCHOT# compliant to signaling specifications (see Table 8).

Table 8. Thermal Monitor Specifications

Parameter	Specification			Units
	Min	Typ	Max	
V_{TT} voltage		$(V_{TT})^1$		Volts
V_{CC}[1]	4.75	5.00	5.25	Volts
Transistor Q1 output 'on' (low) resistance			11	Ohms
PROCHOT# leakage current			200	Microamperes
Transition time20% to 80% signal rise for PROCHOT#	0.550	100		Nanoseconds
Minimum time in or out of Thermal Monitor state	1.0			Milliseconds
RPU (Pull-up Resistor)[2]		130 Ω ± 5%		Ohms

NOTES:
1. Consult Vtt specifications for min and max limits.
2. The thermal monitor circuit is to use a single motherboard pull up resistor to bias the Q1 collector. This is provided in the PROCHOT# circuit design. Additional termination must not be integrated into the thermal monitoring circuit.

PROCHOT# is an open-drain, active-low i/o buffer terminated to the system Vtt (FSB termination voltage). To maintain reliable signaling between thermal monitor circuit, processor, and chipset, the bipolar transistor must be selected to operate with a collector bias established using a single, 130 Ω pull-up resistor. Use of additional termination or pull-up resistors may lead to signal integrity or logic threshold failures. The values for R1, R2 and R3 in Figure 6 are included as an example and must be calculated using specific design parameters. The value of R2 is adjusted to calibrate the comparator's trigger reference voltage (and assertion of PROCHOT#) against the sensor voltage representing a thermal violation.

6.3 Load Indicator Output (PROPOSED)

The VRD may have an output with a voltage level that varies linearly with the VRD output current. The PWM controller supplier may specify a voltage-current relationship consistent with the controller's current sensing method. Motherboards may route this output to a test point for system validation.

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7 VccVID Voltage

7.1 VccVID Voltage (PROPOSED)

This section is included for reference: Intel does not recommend integration with the processor Vcc PWM controller.

The VccVID output powers the processor VID outputs. This rail must come up and assert an active-high VID_PWRGD output according to the timing specified in Figure 7 and Table 9. There is no enable function for the VccVID regulator controller

Figure 7. VID PWRGD Timing

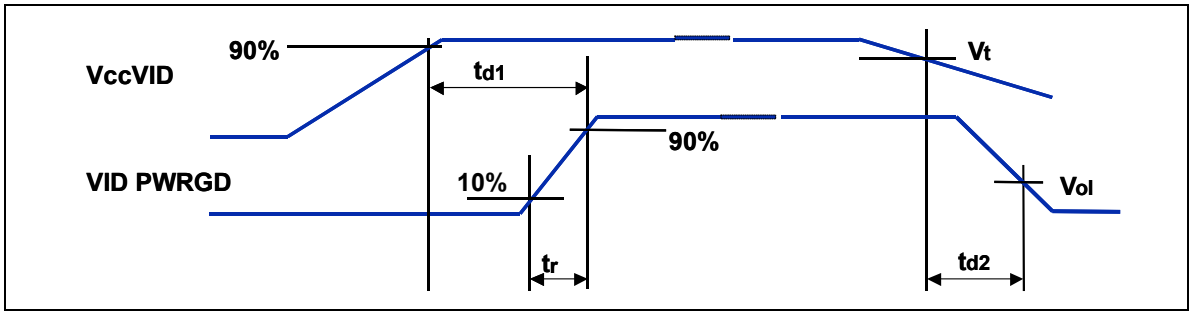

Table 9. VccVID Specifications

Parameter	Specification		Units
	Minimum	Maximum	
VccVID	1.14	1.26	Volts
VccVID current	150		Milliamperes
VID PWRGD voltage	1.14	1.32	Volts
VID PWRGD Voh	1.0	VccVID	Volts
VID PWRGD Vol	- 0.2	0.2	Volts
VID PWRGD de-assertion threshold, Vt	0.95		Volts
VID PWRGD leakage		50	Microamperes
Delay from VccVID to VID PWRGD, td1	1.0	10	Milliseconds
VID PWRGD rise time, tr		150	Nanoseconds
VID PWRGD de-assertion delay, td2		1.0	Milliseconds