Voltage Regulator-Down (VRD) 10.1

Design Guide

For Desktop LGA775 Socket

April 2005

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Revision History

Revision Number	Description	Revision Date
-001	Initial Release.	June 2004
-002	• Updated Table 3-1 • Added Note 5 Under Figure 4-2 • Added Note 1 Under Table 4-1 • Added Section 10.5 Resonance Suppression	July 2004
-003	• Updated Table 4-1T_{d4} information	July 2004
-004	• Updated Table 2-2 • Added Figure 2-3 • Added Table 2-5 • Updated Table 2-6 • Updated Table 2-11 • Changed 2.8.2 socket cavity MLCC total capacitance from 150 uF to 180 uF • Updated Table 3-1 • Updated Table 4-1 • Changed Figure 9-2 • Added Figure 9-3 • Changed Table 11-2, CMB2 from 150 uF to 180 uF and LMB2 from 54 pH to 60 pH • Added Appendix	April 2005

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1 Introduction

1.1 Applications

This document defines the power delivery feature set necessary to support Intel processors' Vcc power delivery requirements for desktop computer systems using the LGA775 socket. This includes design recommendations for DC to DC regulators, which convert the input supply voltage to a processor consumable Vcc voltage along with specific feature set implementation such as thermal monitoring and dynamic voltage identification.

Hardware solutions for the Vcc regulator are dependent upon the processors to be supported by a specific motherboard. At this time, two different VRD hardware configurations have been defined for LGA775 processors. The Vcc regulator design on a specific board must meet the specifications of all processors supported by that board. The voltage regulator configuration for a given processor is defined in that processor's datasheet.

The voltage regulator-down (VRD) designation of this document refers to a regulator with all components mounted directly on the motherboard for intent of supporting a single processor. For the corresponding documentation detailing voltage regulator modules (VRM) or a multiple-processor VRD, please refer to the VRM 10 and EVRD 10 design guidelines document.

1.2 Terminology

Table 1-1. Feature Support Terminology

Categories	Description
REQUIRED	An essential feature of the design that must be supported to ensure correct processor and VRD functionality.
EXPECTED	A feature to ensure correct VRD and processor functionality that can be supported using an alternate solution. The feature is necessary for consistency among system and power designs and is traditionally modified only for custom configurations. The feature may be modified or expanded by system OEMs if the intended functionality is fully supported.
PROPOSED	A feature that adds optional functionality to the VRD and, therefore, is included as a design target. May be specified or expanded by system OEMs.

Table 1-2. Glossary

Term	Description
D-VID	Dynamic Voltage Identification. A low power mode of operation where the processor instructs the VRD to operate at a lower voltage.
DAC	Digital to Analog Converter.
DCR	Direct Current Resistance.
ESL	Effective series inductance.
ESR	Effective series resistance.
FET	Field Effect Transistor.
FR4	A type of printed circuit board (PCB) material.
HVM	High volume manufacturing.
I_{cc}	Processor current.
Itt	Bus current associated with the Vtt supply.
LGA775 Socket	The surface mount Zero Insertion Force (ZIF) socket designed to accept the Intel® Pentium® 4 processor in the LGA 775 land grid array package.
Load Line	A mathematical model that describes voltage current relationship given system impedance (R_{LL}). The load line equations is V_{cc} = VID – I*R_{LL}. In this document, the load line is referenced at the socket unless otherwise stated.
MOSFET	Metal Oxide Semiconductor Field Effect Transistor.
OCP	Output current protection.
OVP	Output voltage protection.
Processor Datasheet	A document that defines the processor electrical, mechanical, and thermal specifications. Also known as the EMTS.
PROCHOT#	Under thermal monitoring, the VRD asserts this processor input to indicate an over-temperature condition has occurred. Assertion of this signal places the processor in a low power state, thereby cooling the voltage regulator.
RDS	FET source to drain channel resistance
RDS-ON	FET source to drain channel resistance when bias on.
R_{LL}	Load line impedance. Defined as the ratio: Voltage droop/current step. This is the load line slope. In this document, the load line is referenced at the socket unless otherwise stated.
RSS	Root Sum Square. A method of adding statistical variables.
Slope	Load line resistance. See $R_{LL.}$ In this document, the load line is referenced at the socket unless otherwise stated.

Term	Description
Socket Load Line	Defines the characteristic impedance of the motherboard power delivery circuit to the node of regulation. Not the same as the processor load line that is published in the processor datasheet, which is defined across the processor Vccsense and Vsssense lands. In conjunction with high frequency decoupling, bulk decoupling, and robust power plane routing, design compliance to this parameter ensures that the processor voltage specifications are satisfied.
Static Load Line	DC resistance at the defined regulation node. Defined as the quotient of voltage and current (V/I) under steady state conditions. This value is configured by proper tuning of the PWM controller voltage positioning circuit. In this document, the static load line is referenced at the socket unless otherwise stated.
Thermal Monitor	A feature of the voltage regulator that places the processor in a low power state when critical VRD temperatures are reached, thereby reducing power and VRD temperature.
TOB	Vcc regulation tolerance band. Defines the voltage regulator's 3-σ voltage variation across temperature, manufacturing variation, and age factors. Must be guaranteed by design through component selection. Defined at processor maximum current and maximum VID levels.
Transient Load Line	Equal to dV/di or Vdroop/Istep and is controlled by switching frequency, decoupling capacitor selection, motherboard layout parasitics. In this document, the transient load line is referenced at the socket unless otherwise stated.
Vcc	Processor core voltage defined in the processor datasheet.
VID	Voltage Identification: A code supplied by the processor that determines the reference output voltage to be delivered to the processor Vcc lands. At zero amperes and the tolerance band at + 3-σ, VID is the voltage at the processor.
VR_TDC	Voltage Regulator Thermal Design Current. The sustained DC current which the voltage regulator must support under the system defined cooling solution.
VRD	Voltage regulator down. A VR circuit resident on the motherboard.
VRM	Voltage regulator module that is socketed to a motherboard.
Vtt	Voltage provided to the processor to initiate power up and drive I/O buffer circuits.

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2 Processor Vcc Requirements

2.1 Voltage and Current (REQUIRED)

A six-bit VID code supplied by the processor to the VRD determines a reference output voltage as described in Section 6.2. The socket load lines in Section 2.2 show the relationship between Vcc and Icc for the processor at the motherboard-socket interface.

Intel performs exhaustive testing against multiple software applications and software test vectors to identify valid processor Vcc operating ranges. Failure to satisfy the socket load line, load line tolerance band, and overshoot voltage specifications (Sections 2.3 and 2.7) may invalidate Intel warranties and lead to premature processor failure, intermittent system lock-up, and/or data corruption.

2.2 Socket Loadline Definitions (REQUIRED)

To ensure processor reliability and performance, platform DC voltage regulation and transient-droop noise levels must always be contained within the Vccmin and Vccmax socket load line boundaries (known as the load line window). Socket load line compliance must be guaranteed across 3-σ component manufacturing tolerances, thermal variation, and age degradation. Socket load line boundaries are defined by the following equations in conjunction with the Vcc regulator design parameter values defined in Table 2-1. Load line voltage tolerance is defined in Section 2.3. In these equations, VID, R_{LL}, and TOB are known. Plotting Vcc while varying Icc from 0 A to Iccmax establishes the Vccmax and Vccmin socket load lines. Vccmax establishes the maximum DC socket load line boundary. Vccmin establishes the minimum AC and DC voltage boundary. Short transient bursts above the Vccmax load line are permitted; this condition is defined in Section 2.7.

Table 2-1. Socket Load Line Equations

Socket load line	Equation
Equation 2-1: Vccmax Socket load line	$Vcc = VID – (R_{LL} * I_{cc})$
Equation 2-2: Vcctyp Socket load line	$Vcc = VID – TOB - (R_{LL} * I_{cc})$
Equation 2-3: Vccmin Socket load line	$Vcc = VID – 2*TOB - (R_{LL} * I_{cc})$

Socket load line recommendations are established to provide guidance for satisfying processor die load line specifications, which are defined in processor datasheets. Die load line requirements must be satisfied at all times and may require adjustment in the socket load line value.

Table 2-2. Vcc Regulator Design Parameters

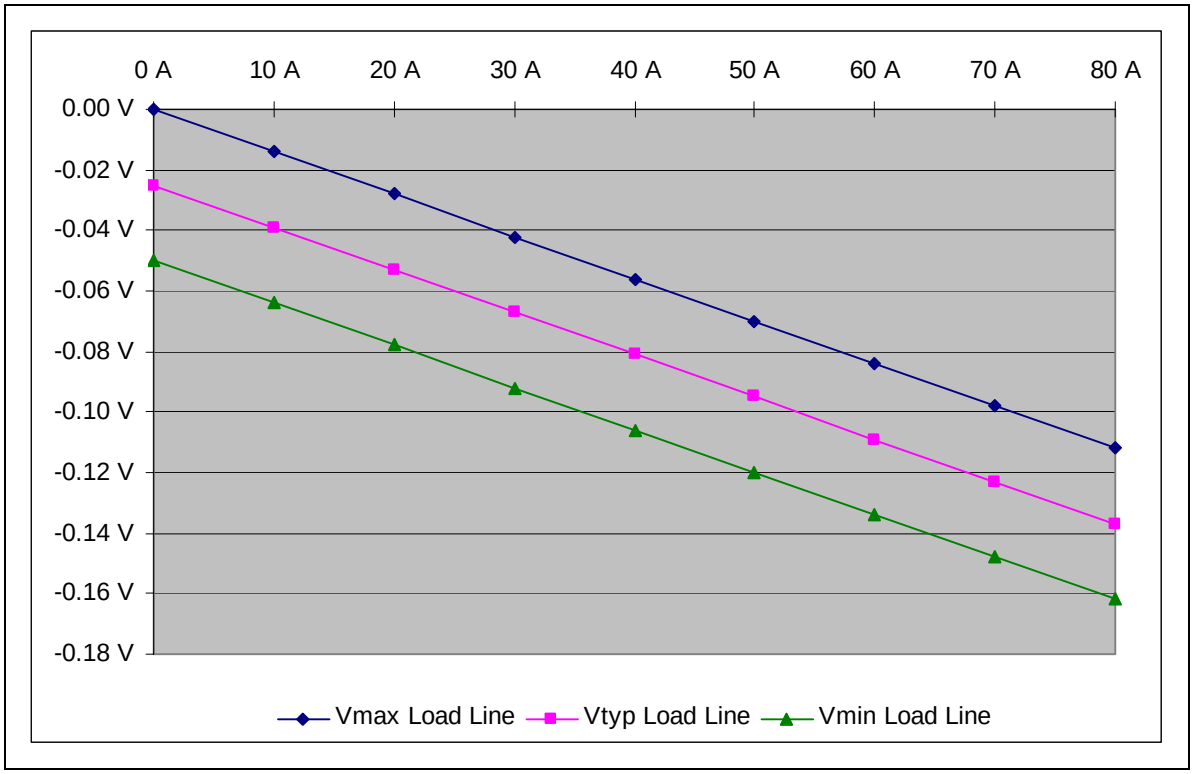
VR Configuration	Iccmax	VR TDC	Dynamic Icc	R_{LL}	TOB	Maximum VID
775_VR_CONFIG_04A	78 A	68 A	55 A	1.40 mΩ	±25 mV	1.4 V
775_VR_CONFIG_04B	119 A	101 A	95 A	1.00 mΩ	±19 mV	1.4 V
775_VR_CONFIG_05A	100A	85A	65A	1.00mΩ	+/-19mV	1.4V
775_VR_CONFIG_05B	125A	115A	95A	1.00mΩ	+/-19mV	1.4V

Refer to the relevant processor datasheet for mapping to the correct VR ConfigurationVRD transient socket load line circuits should be designed to meet or exceed rated conditions defined in Table 2-1. For example, 775_VR_CONFIG_04A requires a socket load line slope of 1.40 mΩ. A transient socket load line slope of 1.0 mΩ will satisfy this requirement without adversely impacting system performance or processor lifespan. This condition may be necessary when supporting multiple processors with a single VRD design. However, the static load line condition must be set to the recommended value unless explicitly stated otherwise in the processor datasheet. Operating at a low load line resistance will result in higher processor operating temperature, which may result in damage or a reduced processor life span. Processor temperature rise from higher functional voltages may lead to operation at low power states which directly reduces processor performance. Operating at a higher load line resistance will result in minimum voltage violations which may result in system lock-up, “blue screening”, or data corruption.

Table 2-1 provides a comprehensive list of VRD10 LGA775 voltage regulator design configurations. The configurations to be adopted by VRD hardware will depend on the specific processors the design is intended to support. It is common for a motherboard to support processors that require different VR configurations. In this case, the Vcc regulator design must meet the specifications of all processors supported by that board. For example, If a motherboard is targeted to support processors that require 775_VR_CONFIG_04A and 775_VR_CONFIG_04B, then the voltage regulator must have the ability to support 101A of VR TDC, 119A of electrical peak current, satisfy overshoot requirements of Section 2.7with a dynamic load step of 95 A, satisfy a VRD tolerance band of ±19 mV (see Section 2.3), and have the ability to detect the specific processor installed in the socket and automatically configure the load line slope (RLL) to the correct value. VR configuration requirements will be defined in processor datasheets.

The following tables and figures show minimum and maximum voltage boundaries for each socket load line design configuration defined in Table 2-1. V_{CCTYP} socket load lines are provided for design reference; designs should calibrate the socket load line to this case (centered in the load line window, at the mean of the tolerance band). Different processors discussed in this design guide can be shipped with different VID values. The reader should not assume that processors with similar characteristics will have the save VID value. Typical values will range from 1.1 V to 1.6 V in 12.5 mV increments. A single load line chart and figure for each VRD design configuration can represent functionality for each possible VID value. Tables and figures presented as voltage deviation from VID provide the necessary information to identify voltage requirements at any reference VID. This avoids the redundancy of publishing tables and figures for each of the multiple cases.

Figure 2-1. Socket Load Line Window for Design Configuration 775_VR_CONFIG_04A



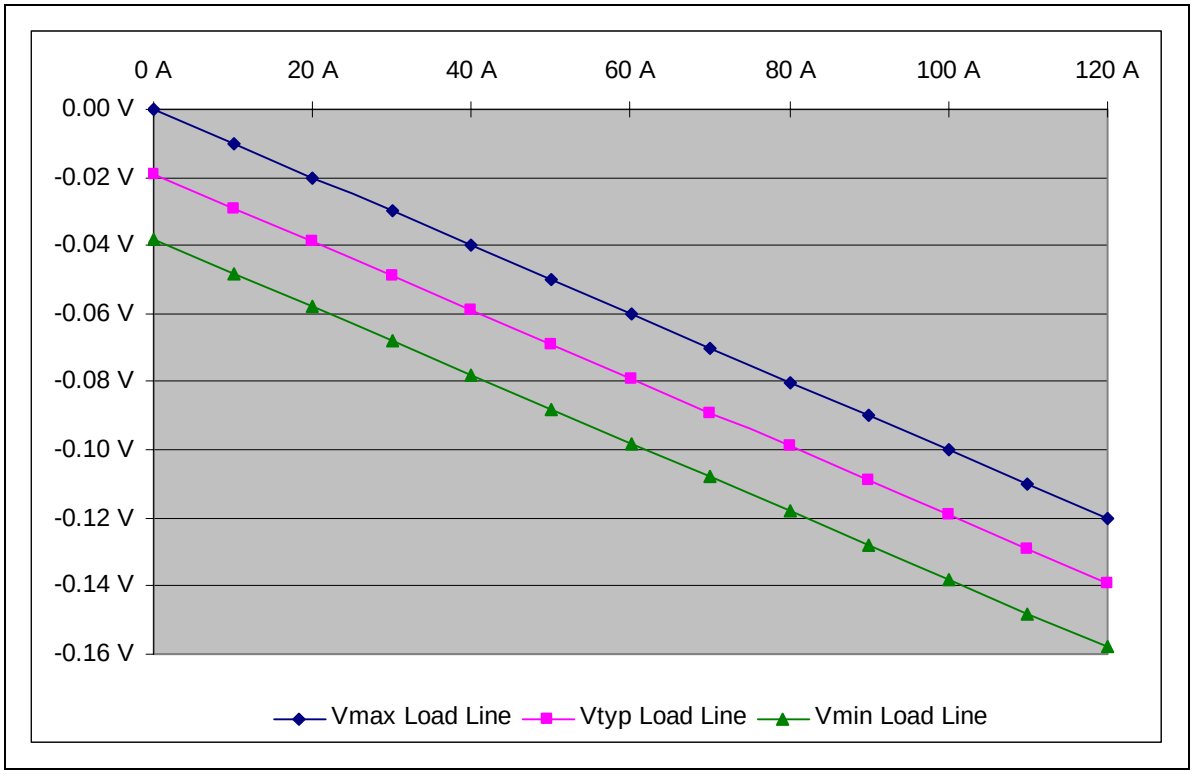
NOTES:
1. Presented as a deviation from VID.
2. Socket load line Slope = 1.4 mΩ, TOB = ±25 mV
3. Consult Table 2-1 for maximum current values

Table 2-3. Socket Load Line Window for Design Configuration 775_VR_CONFIG_04A

Icc	Maximum	Typical	Minimum
0 A	0.000 V	-0.025 V	-0.050 V
10 A	-0.014 V	-0.039 V	-0.064 V
20 A	-0.028 V	-0.053 V	-0.078 V
30 A	-0.042 V	-0.067 V	-0.092 V
40 A	-0.056 V	-0.081 V	-0.106 V
50 A	-0.070 V	-0.095 V	-0.120 V
60 A	-0.084 V	-0.109 V	-0.134 V
70 A	-0.098 V	-0.123 V	-0.148 V
80 A	-0.112 V	-0.137 V	-0.162 V

NOTES:
1. Presented as a deviation from VID.
2. Socket load line Slope = 1.4 mΩ, TOB = ±25 mV
3. Consult Table 2-1 for maximum current values

Figure 2-2. Socket Load Line Window for Design Configuration 775_VR_CONFIG_04B



NOTES:
1. Presented as a deviation from VID.
2. Socket load line Slope = 1.0 mΩ, TOB = ±19 mV
3. Consult Table 2-1 for maximum current values

Table 2-4. Socket Load Line Window for Design Configuration 775_VR_CONFIG_04B

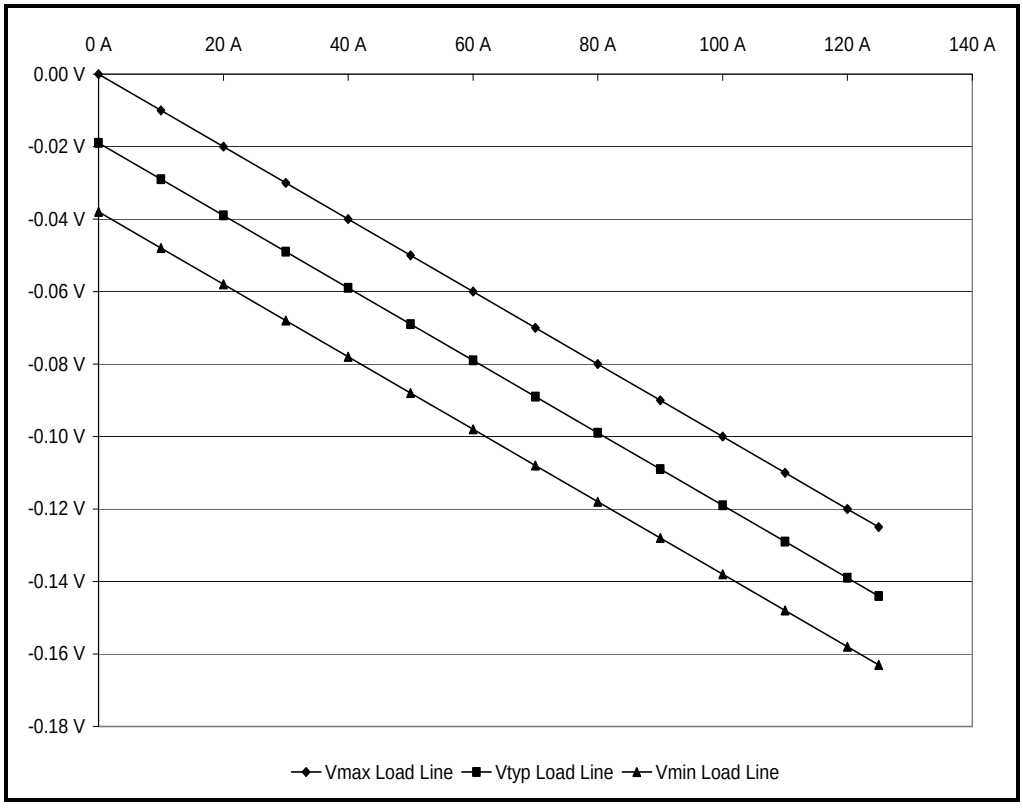
Icc	Maximum	Typical	Minimum
0 A	0.000 V	-0.019 V	-0.038 V
20 A	-0.020 V	-0.039 V	-0.058 V
40 A	-0.040 V	-0.059 V	-0.078 V
60 A	-0.060 V	-0.079 V	-0.098 V
80 A	-0.080 V	-0.099 V	-0.118 V
100 A	-0.100 V	-0.119 V	-0.138 V
120 A	-0.120 V	-0.139 V	-0.158 V

NOTES:
1. Presented as a deviation from VID.
2. Socket load line Slope = 1.0 mΩ, TOB = ±19 mV
3. Consult Table 2-1 for maximum current values

Reference nodes for socket load line measurements and voltage regulation are located in the land field between the socket cavity and the voltage regulator region with the highest phase count (see Figure 2-3); references for north and east phase configurations are identified in Table 2-5. It is recommended to place motherboard test points at these locations to enable load line calibration.

VRD layout studies indicate that the highest phase count is best located north of the processor with the controller to the southeast. This orientation is not suitable for routing sense lines to the location discussed above, so Intel has provided dedicated processor lands which jumper the VRD controller differential remote sense traces from a southeast connection to the center north land field. These lines are routed across the processor package and dropped down to the optimal regulation nodes of the motherboard power planes. The package traces are electrically isolated from all die and package electrical networks, simply providing the voltage at the desired motherboard sense node. In this configuration, the processor differential remote sense lands are also to be used as the socket load line measurement reference and all socket electrical specifications must be satisfied across these lands.

Figure 2-3. Socket Load Line Window for Design Configuration 775_VR_CONFIG_05A and 05B



NOTE: 1: Presented as a deviation from VID

2: Socket load line Slope = 1.0mOhms, TOB Tolerance = +/-19mV

3: Consult Table 1 for VR configuration parameter details

Table 2-5: Socket Load Line WindowSocket Load Line Window for Design Configurations 775_VR_CONFIG_05A and 775_VR_CONFIG_05B

Icc	Maximum	Typical	Minimum
0 A	0.000 V	-0.019 V	-0.038 V
20 A	-0.020 V	-0.039 V	-0.058 V
40 A	-0.040 V	-0.059 V	-0.078 V
60 A	-0.060 V	-0.079 V	-0.098 V
80 A	-0.080 V	-0.099 V	-0.118 V
100 A	-0.100 V	-0.119 V	-0.138 V
120 A	-0.120 V	-0.139 V	-0.158 V
125 A	-0.125 V	-0.144 V	-0.163 V

NOTE: 1: Presented as a deviation from VID

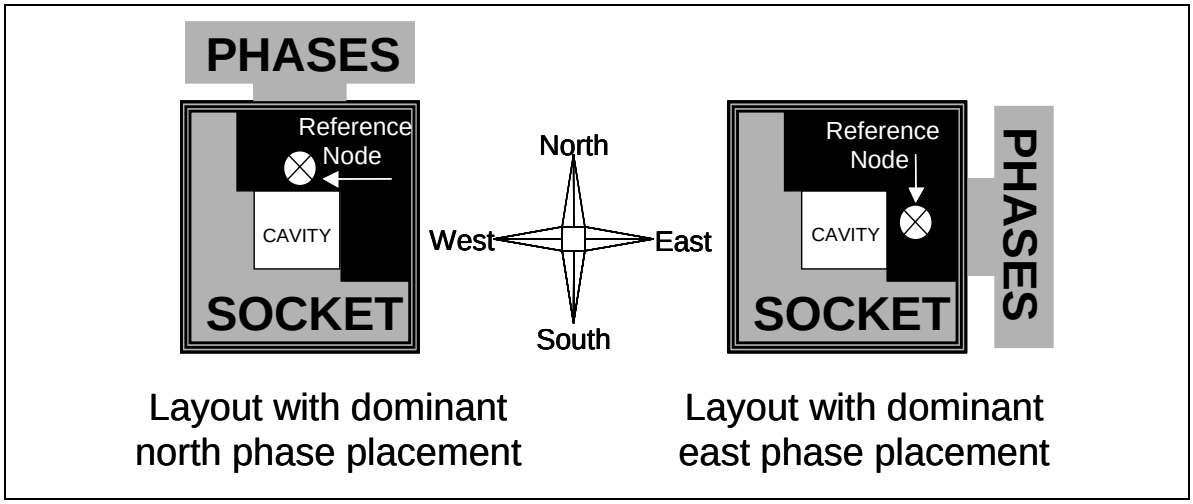
2: Socket load line Slope = 1.0mOhms, TOB Tolerance = +/-19mV

3: Consult Table 1 for VR configuration parameter details

Table 2-5. Socket Load Line Reference Lands

Orientation	Land
North Vcc	U27
North Vss	V27
East Vcc	AJ14
East Vss	AJ15
SE Vcc Jumper	AN5
SE Vss Jumper	AN6

Figure 2-3. VRD Phase Orientation



To properly calibrate the socket load line parameter, the VR designer must excite the processor socket with a current step that generates a voltage droop which must be checked against the load line window requirements. Table 2-8 identifies the steady state and transient current values to use for this calibration. For additional information, please consult the Socket Load Line Calculator for the appropriate Intel processor.

Table 2-6: Intel® Processor Current Step Values for Transient Socket Load Line Testing

VR Configuration	Starting Current	Ending Current	Dynamic Current Step
775_VR_CONFIG_04A	23 A	78 A	55 A
775_VR_CONFIG_04B	24 A	119 A	95 A
775_VR_CONFIG_05A	35A	100A	65A
775_VR_CONFIG_05B	30A	125A	95A

VRD designs must be socket load line compliant across the full tolerance band window to avoid data corruption, system lock-up, and reduced performance. When validating a system's socket load line, a single measurement is statistically insignificant and cannot represent the response variation seen across the entire high volume manufacturing population of VRD designs. A typical socket load line may fit in the specification window; however designs residing elsewhere in the tolerance band distribution may violate the specifications. For example, Figure 2-4. Example A shows a load line that is contained in the specification window and, in this single instance, complies with Vccmin and Vccmax specifications. The positioning of this socket load line will shift up and down as the tolerance drifts from typical to the design limits. Figure 2-4, Example B shows that Vccmax limits will be violated as the component tolerances shift the load line to the upper tolerance band limits. Figure 2-4, Example C shows that the Vccmin limits will be violated as the component tolerances shift the load line to the lower tolerance band limits.

To satisfy specifications across high volume manufacturing variation, a typical socket load line must be centered in the load line window and have a slope equal to the value specified in Table 2-1. Figure 2-4, Example A shows a socket load line that meets this condition. Under full 3-σ tolerance band variation, the load line slope will intercept the Vccmax load line (Figure 2-4 , Example B) or Vccmin load line (Figure 2-4, Example C) limits.

Figure 2-4. Examples of High Volume Manufacturing Load Line Violations

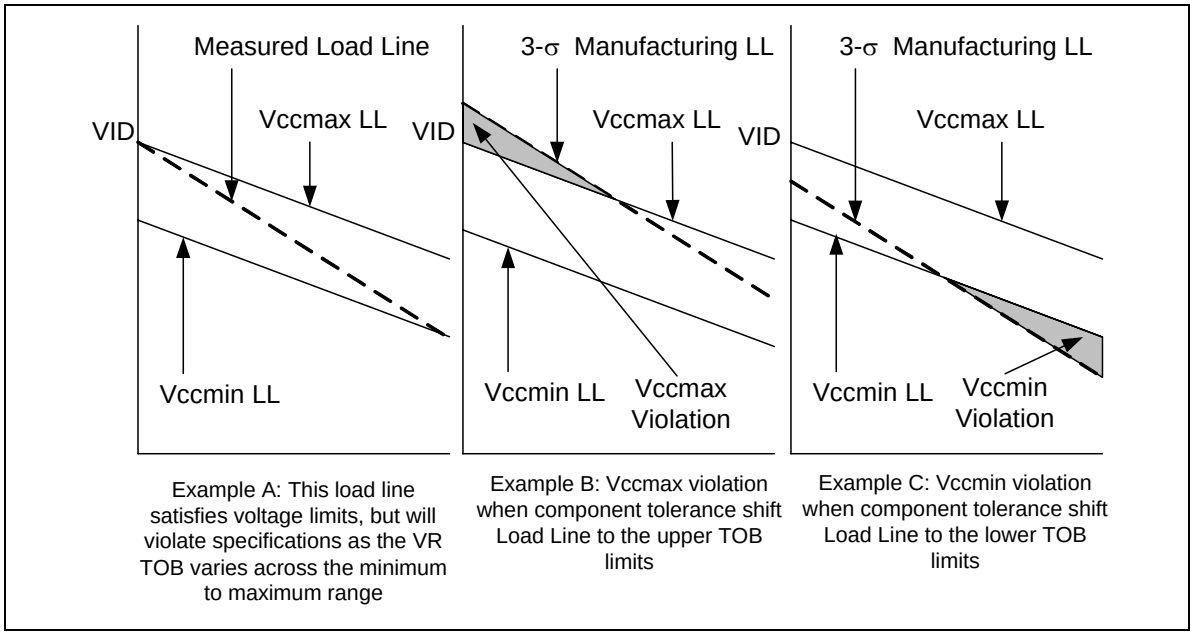
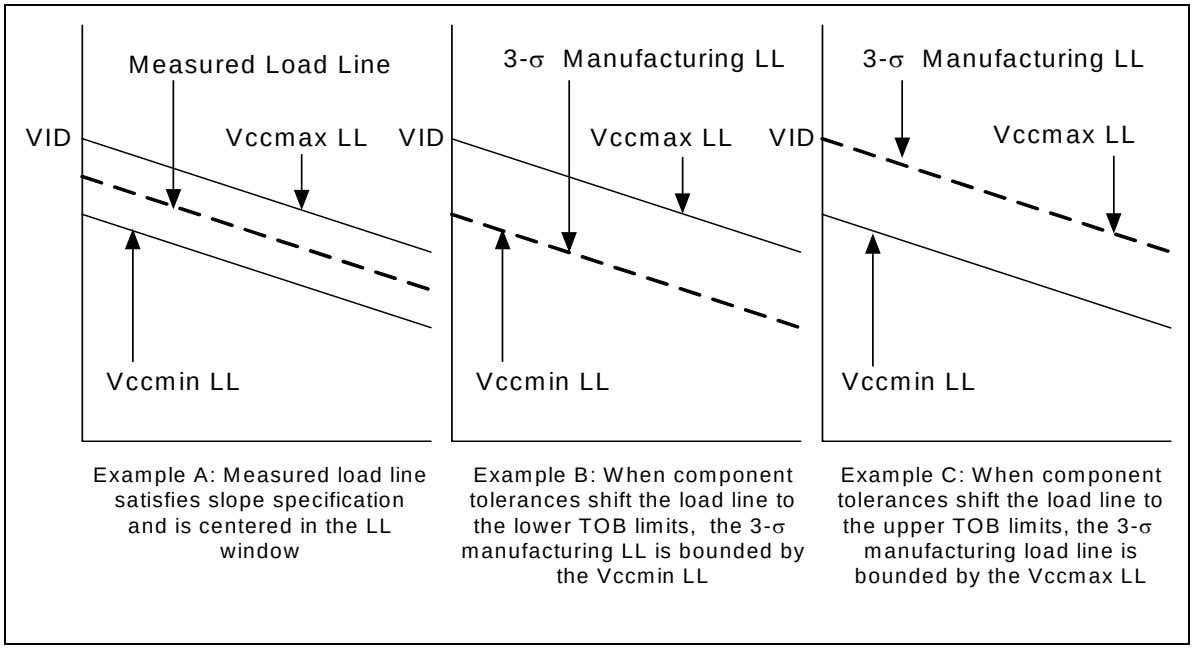


Figure 2-5. High Volume Manufacturing Compliant Load Line



2.3 TOB: Voltage Tolerance Band (REQUIRED)

Processor load line specifications must be guaranteed across component process variation, system temperature extremes, and age degradation limits. The VRD topology and component selection must maintain a 3-σ tolerance of the VRD Tolerance Band around the typical load line (see Section 2.2). The critical parameters include voltage ripple, VRD controller tolerance, and current sense tolerance under both static and transient conditions. Individual tolerance components will vary among designs; the processor requires only that the total error stack-up stay within the defined VR configuration tolerance band under the conditions defined in Table 2-1.

2.3.1 Sources of Voltage Deviation and Input Parameters

The standard VRD tolerance band (TOB) can be sliced into three main categories: controller tolerance, current sense variation, and voltage ripple.

Controller tolerance is determined by the DAC accuracy (digital to analog conversion) and DC offset of the internal controller circuitry (i.e., op amp offset). These tolerance parameters are functions of the operating voltage associated with the programmed VID (defined in Table 2-1). Internal controller circuitry also includes a tolerance associated with current sense signal conversion that must be included in the TOB calculation. Consult the controller datasheet or vendor for the particular component specifications.

VRD current sensing occurs by processing a sensed voltage across a component in the direct output current path. Current conversion occurs with knowledge of the device resistance and/or impedance. The tolerance of this sense method is directly aligned with the sense element's tolerance. For inductor, resistor, and FET sensing, the series resistance tolerance of the sense component is a critical factor for calculating the TOB. Integrating capacitors are part of the inductor current sense circuit and the manufacturing tolerance including thermal drift must be identified to ensure correct TOB calculations. For inductor and FET sensing, thermal compensation (see Section 2.4) is required to maintain a linear load line across the full, operational system temperature range.

Peak ripple should not exceed ±5 mV at the VRD measurement nodes. Ripple is typically suppressed by increasing the value of the output inductance or by increasing the value/quantity of ceramic capacitors in the high frequency filter (see Section 2.8).

Table 2-7. Input Parameters for VRD TOB Calculation

Parameter	Definition	Units
I_{dyn}	Maximum dynamic current step amplitude [1]	A
I_{max}	Maximum VR Configuration load current [1]	A
k_C	Tolerance of CS capacitance [2 3]	[±% @ 3-σ]
k_{ESR}	Tolerance of inductor DCR [4 6]	[±% @ 3-σ]
k_{gm}	Controller tolerance of current signal conversion	[±% @ 3-σ]
k_L	Tolerance of output inductance [4]	[±% @ 3-σ]
k_{RDS}	Tolerance of FET RDS-ON [4]	[±% @ 3-σ]
k_{rsense}	Tolerance of sense resistor [4]	[±% @ 3-σ]
k_{VID}	Controller reference voltage (VID) tolerance	[±% @ 3-σ]
n_{ph}	Number of independent phases in VRD	-
n_{rsense}	Number of sense resistors	-
R_{AVP}	AVP (Socket Load Line) resistance	[Ω]
V_{ripple}	Peak ripple voltage: Max = 5mV peak	[±V]
V_{TC}	Thermal compensation transient error	[±V]

NOTES:

1. See Table 2-1.
2. Statistical RSS may be applied if more than one component is used.
3. Tolerance is to include parameter thermal drift across operational temperature.
4. Thermal variation of parameter is included in VTC if thermal compensation is applied.
5. All parameter tolerances are defined at 3-σ. Many vendors define some common parameters, such as inductor tolerance and inductor DCR, at 6-σ. These numbers should be translated to 3-σ to obtain an accurate TOB calculation.
6. Vendors commonly refer to this parameter as RDC and it is generally a 6-σ tolerance value.

2.3.2 TOB: Tolerance Band Calculation

Reference TOB equations for each major current sense topology are provided in the next three subsections. Equations are presented in a manner for simple entry into a spreadsheet to simplify TOB calculation and design iterations.

2.3.3 Inductor RDC Current Sense TOB Calculations

Inductor sensing is the best general approach to satisfying the tolerance band requirements. TOB can be directly controlled by selecting output inductors and integrating capacitors of sufficient tolerance. Inductor thermal drift will require thermal compensation to keep the load line linear (see section 2.4). Capacitor thermal drift must also be considered in the tolerance and Intel recommends COG capacitors for their thermal stability. Understanding component variation is critical for calculating Inductor Sense TOB; many component tolerances are defined under 6-σ variation, which should be translated to 3-σ for calculation purposes.

$$TOB_{manuf} = \sqrt{(VID.k_{VID})^2 + V_{AVP}^2.(k_{gm}^2 + \frac{k_{ESR}^2}{n_{ph}}) + V_{AVPdyn}^2.(\frac{k_L^2 + k_C^2}{n_{ph}})}$$

$$V_{AVPdyn} = I_{dyn}.R_{AVP}$$

$$V_{AVP} = I_{max}.R_{AVP}$$

$$+/-TOB = TOB_{manuf} + V_{ripple} + V_{TC}$$

2.3.4 Resistor Current Sense TOB Calculations

Resistor sensing topologies have the capability to provide the tightest TOB solutions due to a wide industry selection of precision resistors. However, the accuracy comes at a price. Resistors are placed in series with the output current, which results in substantial power loss and heat generation. The resulting power dissipation requires large, expensive, high wattage resistors, which demand additional cooling to keep components and motherboard layers below maximum allowable temperature limits. Power loss may be mitigated by selecting a low value of resistance, however minimum signal amplitude must be considered for adequate current conversion (i.e., signal to noise ratio).

$$TOB_{manuf} = \sqrt{(VID.k_{VID})^2 + V_{AVP}^2.(k_{gm}^2 + \frac{k_{rsense}^2}{n_{rsense}})}$$

$$V_{AVP} = I_{max}.R_{AVP}$$

$$+/-TOB = TOB_{manuf} + V_{ripple}$$

2.3.5 FET RDS-ON Current Sense TOB Calculations

$$TOB_{manuf} = \sqrt{(VID.k_{VID})^2 + V_{AVP}^2.(k_{gm}^2 + k_{RDS}^2)}$$

$$V_{AVP} = I_{max}.R_{AVP}$$

$$+/-TOB = TOB_{manuf} + V_{ripple} + V_{TC}$$

Current can be determined by sensing the voltage across the VRD switching FET's drain to source 'on' resistance. While this provides a direct method of voltage to current conversion, the standard FET RDS-ON tolerance of 20% – 30% is not acceptable to satisfy Intel's tolerance band requirements. If RDS-ON sensing is to be applied, FET thermal compensation is required (see section 2.4) together with a tight FET RDS-ON distribution (approximately 5% at 3-σ). When this is applied, temperature differences between phases must be considered to ensure adequate load line linearity. Since boards are generally build with FETs from similar manufacturing lots, process to process variation is not random and the RDS-ON parameter may not be reduced through statistical analysis.

2.4 Voltage Regulator Thermal Compensation (REQUIRED)

VRD10.1 systems draw significant levels of current, resulting in a varying temperature gradient across electrical components. Electrical parameters of these components are functions of temperature and their values will drift with the thermal gradient. This drift will result in a load line violation. To ensure compliance to specifications, the voltage regulator requires thermal compensation.

Thermal compensation allows the processor Vcc VRD to respond to temperature drift in VRD electrical parameters. It is required to ensure that regulators using inductor or FET RDS current sensing maintain a stable voltage over the full range of load current and system temperatures.

If thermal compensation is not included, the output voltage of the regulator will droop as the resistance of the sense element increases with temperature. With the increased resistance, the regulator falsely detects an increase in load current and regulates to a lower voltage. Thermal compensation prevents this thermally induced voltage droop by adjusting the feedback path based on the temperature of the regulator. This is accomplished by placing a thermistor in the feedback network (tuned with a proper resistor configuration) to negate the effects of the increased resistance of the sense element.

The thermal compensation circuit is to be validated by running the regulator at VR TDC for 30 to 45 minutes. This is to ensure the board is thermally saturated and system temperatures have reached a maximum steady state condition. If the thermal compensation has been properly implemented, the output voltage will only drift 1-2 mV from its coolest temperature condition. If the thermal compensation has not been properly implemented, the voltage can droop in the 10s of mV range

2.5 Stability (EXPECTED)

The VRD must be unconditionally stable under all DC and transient conditions across the voltage and current ranges defined in Table 2-2 through Table 2-4 and Figure 2-1 and Figure 2-2. The VRD must also operate in a no-load condition: i.e., with no processor installed. Normally the no-processor VID code will be 11111, disabling the VRD (see Table 9-1).

2.6 Dynamic Voltage Identification (REQUIRED)

2.6.1 Dynamic-Voltage Identification Functionality

VRD10 architecture includes the Dynamic Voltage Identification (D-VID) feature set, which enables the processor to reduce power consumption and processor temperature. Reference VID codes are dynamically updated by the processor to the VRD controller via the VID bus when a low power state is initiated. VID codes are updated sequentially in 12.5 mV steps and are transmitted every 5 microseconds until the final voltage code is encountered. Processors are capable of transitioning from standard operational VID levels to the minimum table entry of 0.8375 V. They are also capable of returning to a higher VID code in a similar manner. The low voltage code will be held for a minimum of 50 microseconds prior to sequentially transitioning through the VID table to a new voltage reference which can be any higher VID code, but is generally the original reference VID.

Figure 2-6 illustrates processor-operating states as the VID level is lowered. The diagram assumes steady state, maximum current during the transition for ease of illustration. In this figure, the processor begins in a high-load condition. Upon entering D-VID, the processor will shift to a low power state and stop executing code (sequence 1 => 2). After reaching state 2, the processor encounters a brief delay to prepare for low power operation then re-initiates code, resulting in current draw and a load line IR drop to state 3. Sequencing from state 3 to 4 is a simplification of the multiple steps from the original VID load line window to the low-voltage VID window. Transition from state 4 to state 5 is an example of a load change during normal operation in the low voltage VID setting. Transition from a low to high VID reference follows the reverse sequence.

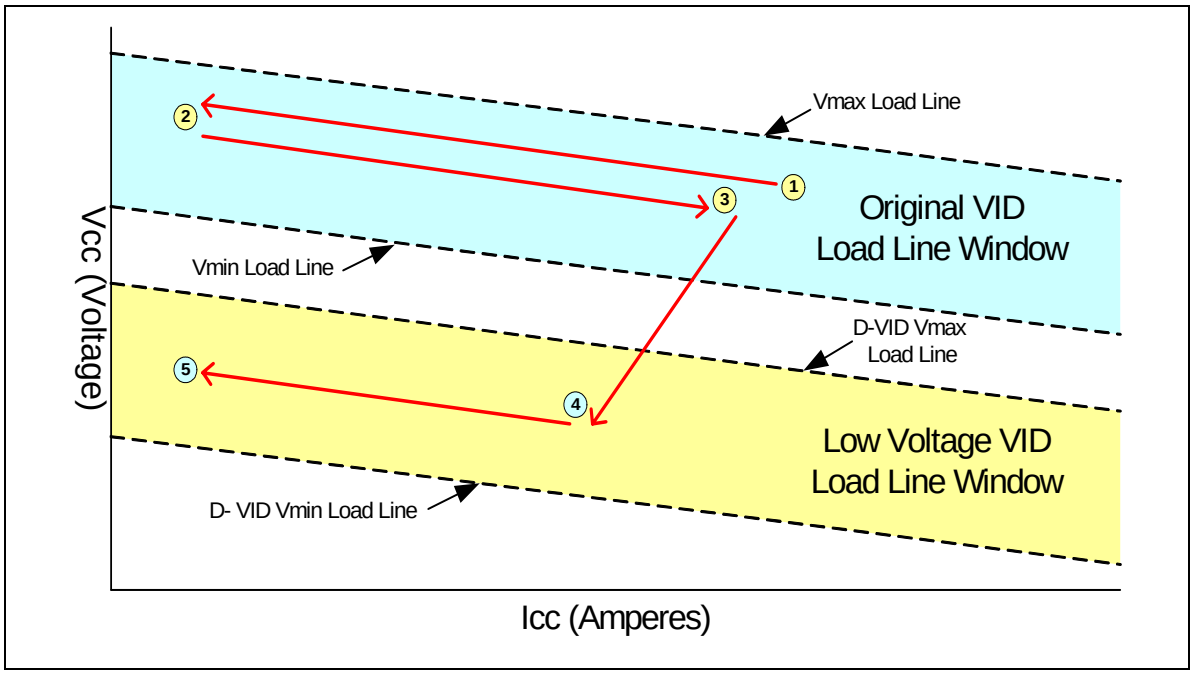
During a D-VID transition, Vcc must always reside above the minimum load line of the current VID setting (see Figure 2-6). The load line values of each VID increment are required to match the slope defined in Table 2-1. In addition, the voltage tolerance band and ripple specifications defined in Table 2-1and Section 2.3 must be satisfied in this state. To expedite power reduction and processor cooling, the VRD must lower the maximum Vcc value to reside within the low voltage VID window within 50 microseconds of the final VID code transmission (see Figure 2-1 and Figure 2-7). The VRD must respond to a transition from low VID to high VID by regulating the Vcc output to the range defined by the new VID code within 50 microseconds of the final code transmission. Note: the minimum VID is not constant among all processors; the value will vary with frequency and standard VID settings. This results in numerous possible D-VID states. A simple and direct D-VID validation method is defined at the end of this section.

During a D-VID event, the processor load may not be capable of absorbing output capacitor energy when the VID reference is lowered. As a result, reverse current may flow into the AC-DC regulator’s input filter, potentially charging the input filter to a voltage above the over voltage value. Upon detection of this condition, the AC-DC regulator will react by shutting down the AC-DC regulator supply voltage. The VRD and AC-DC filter must be designed to ensure this

condition does not occur. In addition, reverse current into the AC-DC regulator must not impair the operation of the VRD, the AC-DC supply, or any other part of the system.

Under all functional conditions, including D-VID, the Vcc supply must satisfy load line and overshoot constraints to avoid data corruption, system lock-up events, or system blue-screen failures.

Figure 2-6. Processor D-VID Load Line Transition States



2.6.2 D-VID Validation

Intel processors are capable of generating numerous D-VID states and the VRD must be designed to properly transition to and function at each possible VID voltage. However, exhaustive validation of each state is unnecessary and impractical. Validation can be simplified by verifying the VRD conforms to socket load line requirements, tolerance band specifications, and D-VID timing requirements. Then, by default, each processor D-VID state will be valid. The key variables for Vcc under D-VID conditions are processor loading, starting VID, ending VID, and Vcc slew rate. The Vcc slew rate is defined by VRD bulk decoupling, the output inductors, the switching FET resistance and the processor load. This indicates that the Vcc slewing will have an exponential behavior, where the response to code ‘n+1’ takes longer to settle than code ‘n’. As a result, a test from maximum to minimum and from minimum to maximum will be sufficient to guarantee slew rate requirements and VID code regulation.

To ensure support for any valid VID reference, testing should be performed from the maximum table entry of 1.6 V to the minimum value of 0.8375 V. The VRD must ensure that this 0.7625 V transition occurs within 50 microseconds of the final VID code, in 350 microseconds. Slew rate timing is referenced from 0.4 V on the rising edge of the initial VID code to the time the final voltage is settled within 5 mV of the final Vcc value. Intel testing has noted a 10% change to the

Vcc slew rate between VRD no load (5 A) and full load (VR TDC) conditions. For this reason, the Vcc slewing must be tested under both loading conditions.

During the D-VID test defined in the previous paragraph, Vcc droop and undershoot amplitudes must be limited to avoid processor damage and performance failures. If the processor experiences a voltage undershoot due to D-VID transitions, an application initiated di/dt droop can superimpose with this event and potentially violate minimum voltage specifications. Droop during this D-VID test must be limited to 5 mV. This value was derived by calculating VRD tolerance band improvements at the low D-VID current and voltage values. If the processor experiences an overshoot due to D-VID transitions, an application initiated di/dt overshoot can superimpose with this event and potentially violate overshoot specifications. Overshoot is permitted, but must be properly budgeted with respect to the specifications defined in Section 2.7. Superposition of the dynamic VID overshoot event and the overshoot resulting from the transient test defined in Section 2.7, must not exceed the amplitude and time requirements defined in the overshoot specification.

2.6.3 Validation Summary

Consult Figure 2-7 and Figure 2-8 for graphic representation of validation requirements.

1. Constraints:
    a. 762.5 mV ±5 mV transition must occur within 350 µs (see Figure 2-7)
    b. Start time is referenced to 0.4 V on the rising edge of the initial D-VID code
    c. End time is referenced to the steady state Vcc voltage after the final D-VID code
    d. Undershoot during maximum to minimum VID transition must be limited to 5 mV. This 5 mV is included within the ± 5 mV tolerance on the final VID value defined under test condition a.
    e. Overshoot observed when transitioning from minimum to maximum VID must conform to overshoot specifications. Specifically, superposition of the dynamic VID overshoot event and the overshoot resulting from the transient test defined in Section 2.7 must not exceed the overshoot amplitude and time requirements defined in the overshoot specification.
    f. Care must be taken to avoid motherboard and component heat damage resulting from extended operations with high current draw.
2. Validation exercises:
    a. D-VID transition must be validated against above constraints from a starting VID of 1.6 V to an ending VID of 0.8375 V with an applied 5 A Load.
    b. D-VID transition must be validated against above constraints from a starting VID of 1.6 V to an ending VID of 0.8375 V with an applied VR TDC Load.
    c. D-VID transition must be validated against above constraints from a starting VID of 0.8375 V to an ending VID of 1.6 V with an applied 5 A Load.

d. D-VID transition must be validated against above constraints from a starting VID of 0.8375 V to an ending VID of 1.6 V with an applied VR TDC Load.

Figure 2-7. D-VID Transition Timing States

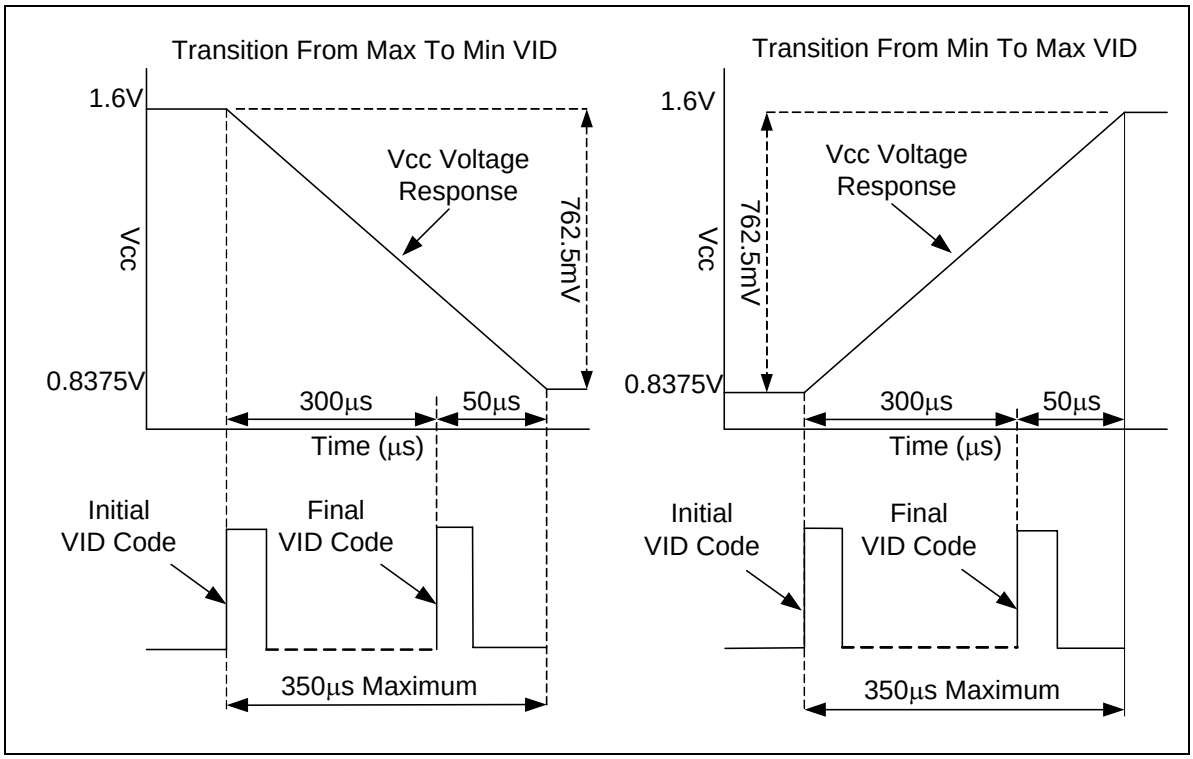


Figure 2-8. Overshoot and Undershoot during Dynamic VID Validation

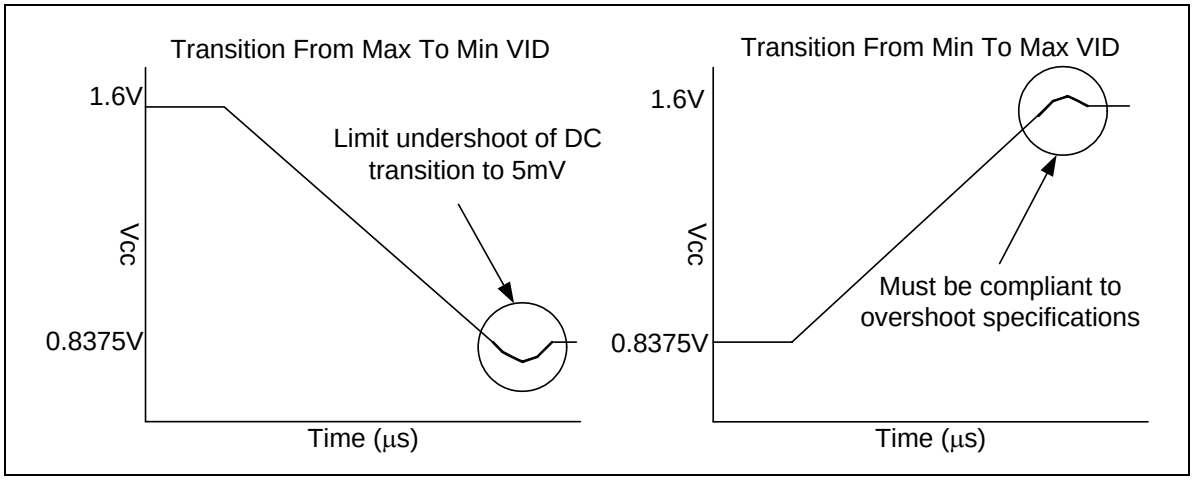


Table 2-8. D-VID Validation Summary Table

Parameter	Minimum	Typical	Maximum
VID	0.8375 V	-	1.6000 V
Voltage Transition	0.7575 V	0.762 5V	0.7675 V
Transition Time	-	-	350 µs[1]
Current Load	5 A	-	VR TDC

NOTES:
1. Time is measured from 0.4 V on rising edge of the first D-VID code to the convergent Vcc voltage value after the final D-VID code is transmitted

2.7 Processor Vcc Overshoot (REQUIRED)

2.7.1 Specification Overview

Intel desktop processors in VRD10.1 systems are capable of tolerating short transient overshoot events above VID on the Vcc supply that will not impact processor lifespan or reliability. Maximum processor Vcc overshoot, V_{OS}, cannot exceed VID+V_{OS_MAX}. Overshoot duration, T_{OS}, cannot stay above VID for a time more than T_{OS_MAX}. See Table 2-9 and Table 2-10 for details.

Table 2-9. Vcc Overshoot Terminology

Parameter	Definition
V_{OS}	Measured peak overshoot voltage
V_{OS_MAX}	Maximum specified overshoot voltage allowed above VID
T_{OS}	Measured overshoot time duration
T_{OS_MAX}	Maximum specified overshoot time duration above VID
Vzc	Zero current voltage: The voltage where the measured load line intercepts the voltage axis
Vzco	Zero current offset from VID: Vzco = VID – Vzc

Table 2-10. Vcc Overshoot Specifications

Parameter	Specification
VOS_MAX	50 mV
TOS_MAX	25 µs
VOS	Maximum = VID + VOS_MAX
TOS	Maximum = TOS_MAX

Maximum overshoot is validated by monitoring the voltage across the recommended test lands (defined in Section 2.2) while applying a current load release across the socket Vcc and Vss land field. Amperage values for performing this validation under each VRD design configuration are identified in Table 2-11. The platform voltage regulator output filter must be stuffed with a sufficient quality and number of capacitors to ensure that overshoot stays above VID for a time no longer than T_{OS_MAX} and never exceeds the maximum amplitude of $VID+V_{OS\_MAX}$. Measurements are to be taken using an oscilloscope with a 20 MHz bandwidth. Boards in violation must be redesigned for compliance to avoid processor damage.

Table 2-11. Intel Processor Current Release Values for Overshoot Testing

VR Configuration	Starting Current	Ending Current	Dynamic Current Step
775_VR_CONFIG_04A	5 A	60 A	55 A
775_VR_CONFIG_04B	5 A	100 A	95 A
775_VR_CONFIG_04C	5 A	94 A	89 A
775_VR_CONFIG_05A	35A	100A	65A
775_VR_CONFIG_05B	30A	125A	95A

To prevent processor damage, VRD designs should comply to overshoot specifications across the full socket load line tolerance band window (see Section 2.2). When validating a system's overshoot, a single measurement is statistically insignificant and cannot represent the response variation seen across the entire high volume manufacturing population of VRD designs. A typical design may fit in the socket load line window; however designs residing elsewhere in the tolerance band distribution may violate the Vcc overshoot specifications Figure 2-10 provides an illustration of this concept. A typical board will have the Vcc zero current voltage (Vzc) centered in the socket load line window at VID-TOB; for this example consider waveform A and assume TOB is 20 mV. Now assume that the VRD has maximum overshoot amplitude of VOS_MAX = 50 mV above VID. Under this single case, the overshoot aligns with the specification limit and there is zero margin to violation. Under manufacturing variation Vzc can drift to align with VID (waveform B). This drift will shift the overshoot waveform by the same voltage level. Since waveform A has zero overshoot amplitude margin, this increase in Vzc due to manufacturing drift will yield a 20 mV overshoot violation which will reduce the processor life span. To address this issue in validation, a voltage margining technique can be employed to ensure overshoot amplitudes stay below a safe value. This technique translates the specification baseline from VID to a VRD validation baseline of Vzc + VOS_MAX, which defines a test limit for specification compliance across the full TOB range:

Equation 2-4. Overshoot Voltage Limit

$$V_{OS} < Vzc + VOS\_MAX$$

This equation is to be used during validation to ensure overshoot is in compliance to specifications across high volume manufacturing variation. In addition, the overshoot duration must be reference to Vzc and cannot exceed this level by more than 25 µs.

Figure 2-9. Graphical Representation of Overshoot Parameters

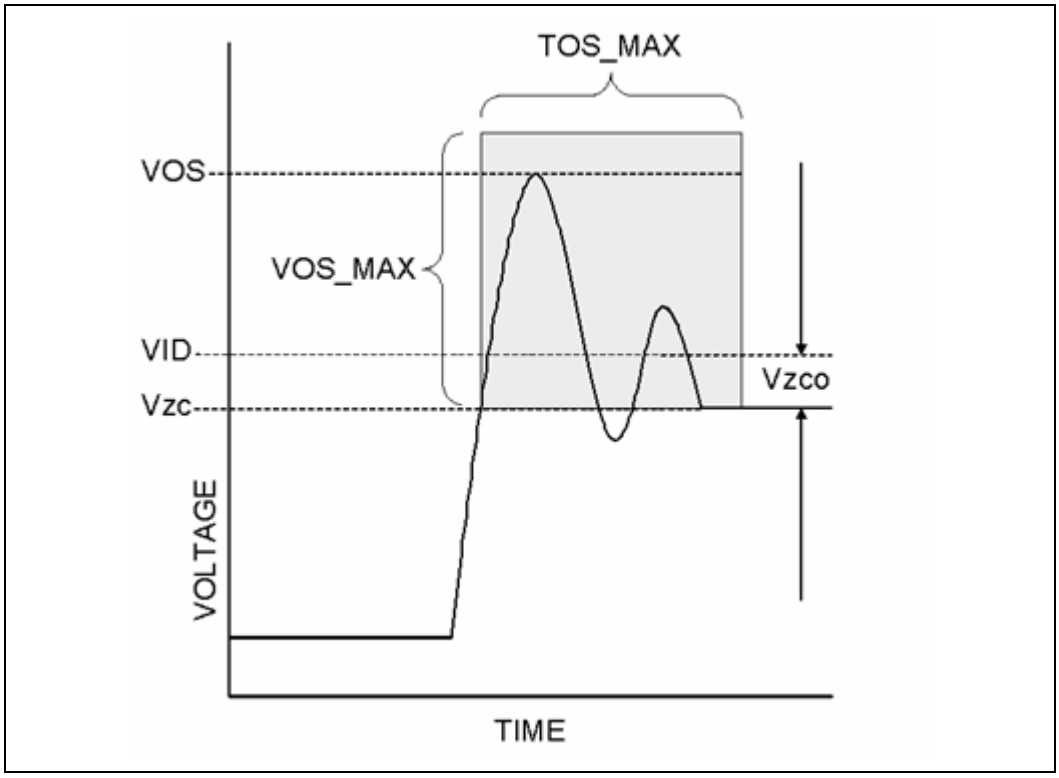


Figure 2-10. Processor Overshoot in High Volume Manufacturing

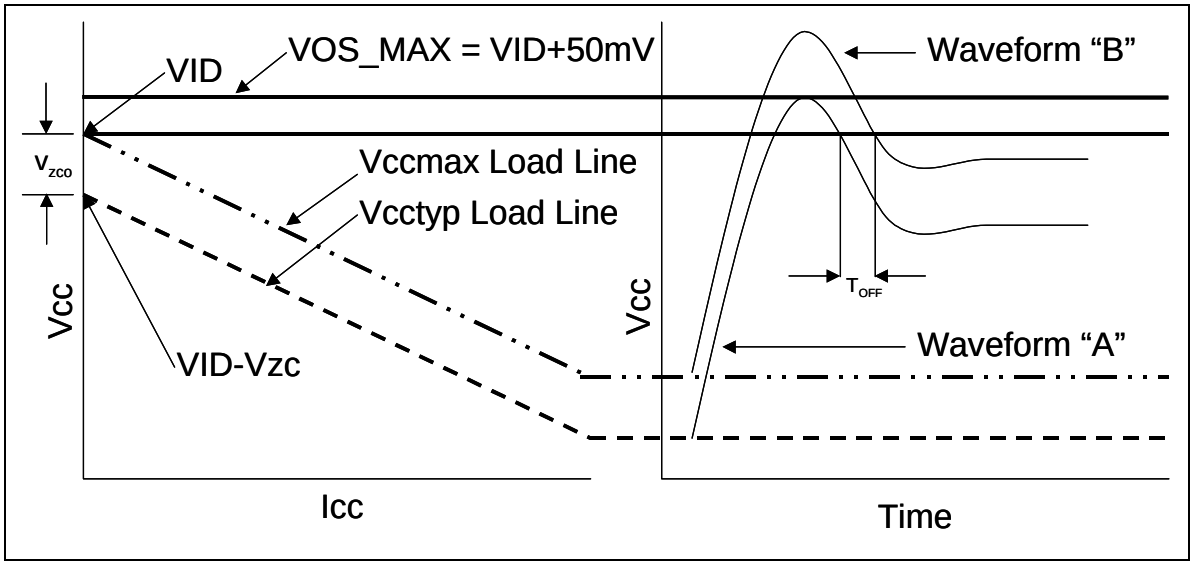
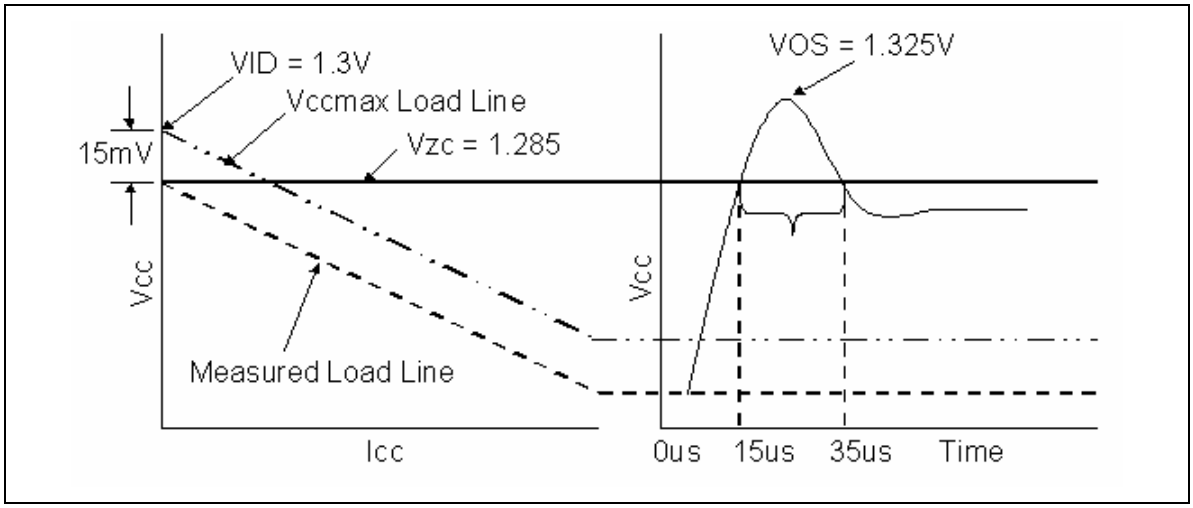


Figure 2-11. Example Socket Vcc Overshoot Waveform



2.7.2 Example: Socket Vcc Overshoot Test

To pass the overshoot specification, the amplitude constraint of Equation 2-4 and time duration requirement of TOS_MAX must be satisfied. This example references Figure 2-11.

Amplitude Test Constraint: Overshoot amplitude, VOS, must be less than Vzc + VOS_MAX

Input parameters

VOS= 1.325 V – Obtained from direct measurement

V_{ZC} = 1.285 V – Obtained from direct measurement

VOS_Max = 0.050 V – An Intel specified value

Amplitude Analysis:

V_{ZC} + VOS_MAX = 1.285 V + 0.050 V = 1.335 V

VOS = 1.325 < 1.335 V

Amplitude Test Satisfied

Time Duration Test Constraint: Overshoot duration above Vzc must be less than 25 µs

Input Parameters

Initial crossing of overshoot: 15 µs – Obtained from direct measurement

Final crossing of overshoot: 35 µs – Obtained from direct measurement

TOS_MAX = 25 µs – An Intel specified value

Overshoot Duration Analysis

TOS = Final Crossing of Vzc – Initial Crossing of Vzc

TOS = 35 µs – 15 µs = 20 µs < 25 µs = TOS_MAX

Time duration test passed

Amplitude and Time Duration Tests Passed => Overshoot specification is satisfied

2.8 VRD Output Filter (REQUIRED)

Desktop processor voltage regulators include an output filter consisting of large bulk decoupling capacitors to compensate for large transient voltage swings and small value ceramic capacitors to provide high frequency decoupling. This filter must be designed to stay within load line specifications (Table 2-3 — Table 2-4 and Figure 2-1—Figure 2-2) across tolerances due to age degradation, manufacturing variation, and temperature drift.

2.8.1 Bulk Decoupling

Bulk decoupling is necessary to maintain Vcc within load line limits prior to the VRD controller response. Design analysis shows that bulk decoupling greatly depends on number of VRD phases, the FET switching frequency. Design analysis determined that the most cost efficient filter solution incorporates bulk capacitors with low (5 mΩ) average ESR.

The D-VID mode of operation is directly impacted by the choice of bulk capacitors and output inductor value in the VRD output filter. It is necessary to minimize Vcc settling time during D-VID operation to hasten the speed of core temperature reduction. The speed of recovery is directly related to the RCL time constant of the output filter. To ensure an adequate thermal recovery time, it is recommended to design the output filter with a minimal output inductor value and a minimal amount of bulk capacitance with minimum ESR, while providing a sufficient amount of decoupling to maintain load line and ripple requirements. At this time, high-density aluminum poly capacitors with 5 mΩ average ESR have been identified as the preferred solution. Failure to satisfy the Vcc settling time requirements defined in section 2.6 may invalidate processor thermal modes; this may require a processor cooling solution (fan-heatsink) that is more robust than recommended.

It is common for a motherboard to support processors that require different VRD configurations (see Table 2-1). In this case, the Vcc regulator design must meet the specifications of all processors supported by that board. This requires the VRD to adopt an output filter design that satisfies the lowest socket load line value of all supported processors. For example, if a motherboard is to support processors requiring 775_VR_CONFIG_04A with a 1.4 mΩ socket load line slope and 775_VR_CONFIG_04B requiring a 1.0 mOhm socket load line slope, the VRD output filter must have a transient socket load line value of 1.0 mOhms to satisfy the noise requirements of each processor.

Consult the appropriate platform design guideline for an output filter design capable of satisfying load line and D-VID constraints.

2.8.2 High Frequency Decoupling

The output filter includes high frequency decoupling to ensure ripple and package noise is suppressed to specified levels. Ripple limits are defined in section 2.3 and package noise limits are defined in appropriate processor datasheets in the form of a processor die load line.

High frequency noise and ripple suppression are best minimized by 10 µF, 22 µF or 47 µF multi-layer ceramic capacitors (MLCC's). It is recommended to maximize the MLCC count in the socket cavity to help suppress transients induced by processor packaging hardware. Remaining MLCC's should be first placed adjacent to the socket edge in the region between the socket cavity and the voltage regulator.

Intel recommends a high frequency filter consisting of MLCC's distributed uniformly through the socket cavity region with an equivalent ESR of 0.16 mΩ and total capacitance of 180 µF. The cavity-capacitor ESL value is not a sensitive parameter, but Intel recommends minimizing the value to suppress noise. The parallel equivalent ESL on Intel reference boards is equivalent to 0.06 nH. To ensure functionality with all Intel processors, adoption of the reference solution (defined in the appropriate Platform Design Guidelines) accompanied by full processor load line validation is strongly recommended.

§

3 Vtt Requirements (REQUIRED)

The Vtt regulator provides power to the processor VID, the chipset - processor front side bus, and miscellaneous buffer signals. This rail must settle to the voltage defined in Table 3-1 and assert an active-high VIDPWRGD output when in regulation (see section 9.2). The Vtt regulator controller does not include an enable signal; valid output voltage of Table 3-1 must be guaranteed by the timing protocol defined in Figure 4-1.

3.1 Electrical Specifications

A linear regulator is recommended for the Vtt supply with adequate decoupling capacitors to ensure the sum of AC bus noise and DC tolerance satisfy limits identified in Table 3-1. The processor and chipset Vtt supply must be maintained within these tolerance limits across full operational thermal limits, part-to-part component variation, age degradation, and regulator accuracy. Full bandwidth bus noise amplitude must be guaranteed across all Vcc/Vss land pairs defined in Table 4-1.

Future generation processors may require lower Vtt voltages. To support multiple processor generations with different values, the Vtt regulator design must have the capability to identify the necessary voltage setting and configure the Vtt regulation voltage to the correct value. The processor communicates the required Vtt value to the regulator via the VTT_SELECT land. Table 3-2 lists each configuration with accompanying electrical requirements. At this time, 775_Vtt_CONFIG_B is PROPOSED and the electrical properties may change at any time.

The Vtt supply must be unconditionally stable under all DC and transient conditions across the voltage and current ranges defined in Table 3-1. The Vtt supply must also operate in a no-load condition: i.e., with no processor installed.

Table 3-1. Vtt Specifications

Processor	Vtt Min	Vtt Typ	Vtt Max	Itt Min	Itt Max	Itt TDC	Vtt_SELECT
775_Vtt_CONFIG_1	1.140 V	1.200 V	1.260 V	0.15 A	5 A	2.6 A	1
	1.045 V	1.100 V	1.155 V	0.15 A	5 A	2.6 A	0
775_Vtt_CONFIG_2	1.140 V	1.200 V	1.260 V	0.15 A	6.2 A	3.8 A	1
	1.045 V	1.100 V	1.155 V	0.15 A	6.2 A	3.8 A	0
All LGA775 Configurations	1.140V	1.200V	1.260V	0.15A	3.4A	5.25A	

NOTES:
1. This configuration is PROPOSED and may be changed at a later date.
2. See Section 3.2 for details regarding Vtt support for the Intel® Pentium® 4 processor Extreme Edition Supporting Hyper-Threading Technology on 0.13 micron process.
3. Combined DC and Transient voltage tolerance is 5%, with a maximum 2% DC tolerance.

4. TDC is the thermal design current with the maximum number of signals in a low, current consuming state. It includes processor and chipset i/o buffer draw.

Table 3-2. Vtt Measurement Lands

Device	Supply	Land
Processor	Vtt	D25
Processor	Vss	D26
865 MCH	Vtt	F29
865 MCH	Vss	E29
910 MCH	Vtt	F29
910 MCH	Vss	E29

3.2 Processor-MCH Vtt Mismatch

The Intel® Pentium® 4 processor Extreme Edition supporting Hyper-Threading Technology on 0.13 micron process requires the LGA775 Vtt regulator to sink and source current. This is a requirement because the processor's Vtt rail is connected to a reference core voltage on the die (equal to VID) and does not use the independent Vtt supply on the motherboard. Other LGA775 processors split the Vtt rail from the reference core voltage and only require a single source Vtt voltage regulator.

If the Extreme Edition processor is placed in a Vtt configuration without current sink capabilities, a voltage delta will appear on the Vtt rail due to the difference in the processor Vtt (equal to VID) and MCH Vtt (Typically 1.2 V) voltage values. When the bus is inactive, this voltage delta can create a condition where the higher processor Vtt voltage creates a back-drive current in the MCH termination. Since this current cannot be consumed by the MCH leakage current and the VR has no sink capability, the Vtt voltage will increase beyond the regulation limits. As a result, the Vtt VR may shut down due to OVP or may function with stability issues. Note, operating at Vtt voltages above specifications will impact the impedance calibration of the active MCH front side bus termination transistors and may lead to bus failures. The heightened voltage may also reduce the life span of the MCH.

Early Intel reference boards were designed with a Vtt circuit that did not include sink capabilities. If the target motherboard is to support the Pentium 4 processor Extreme Edition, additional circuitry must be added to ensure correct operation.

§

4 Power Sequencing (REQUIRED)

The VRD must correctly sequence power in accordance with Intel processor requirements. Figure 4-1 is a block diagram of the VRD connectivity with necessary signals and relevant power rails. Figure 4-2.provides the timing protocol for these signals and power rails in LGA775 platforms.

Figure 4-1. Power-on Sequencing Block Diagram

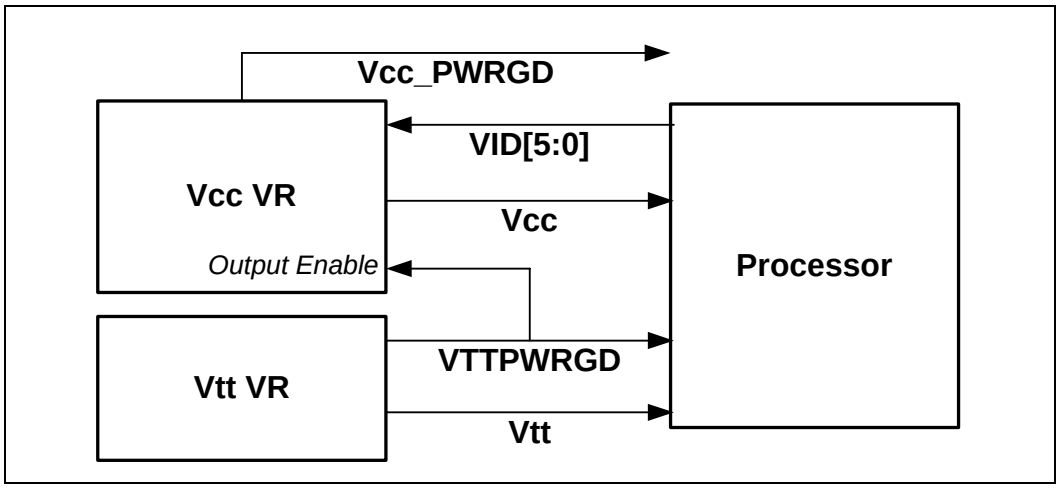
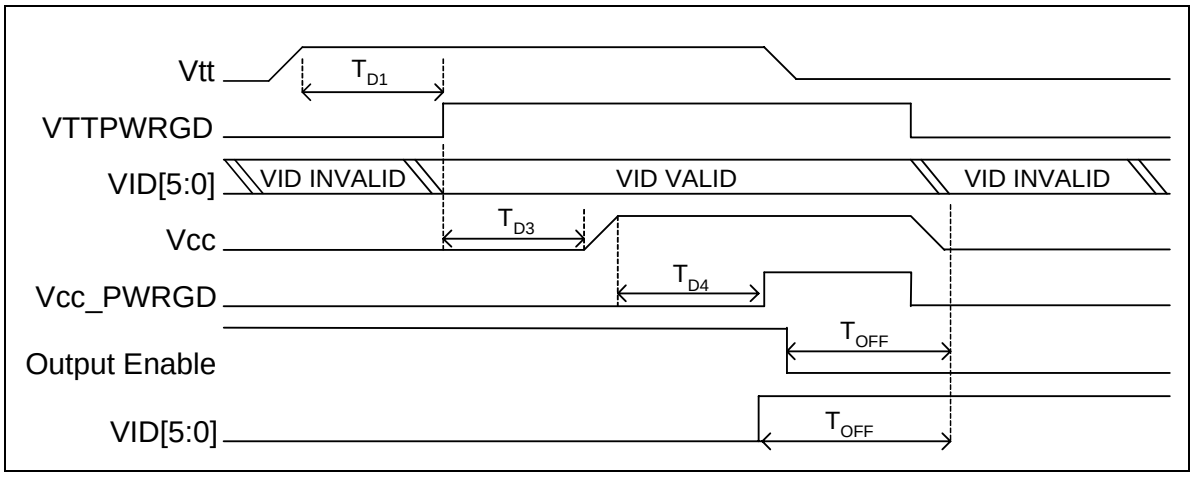


Figure 4-2. Power Sequence Timing Diagram



NOTES:

1. Vtt comes up at the application of system power to the Vtt VRD.
2. Vtt VRD generates VTTPWRGD to latch the processor's VID outputs and enable Vcc VRD, after the Vtt supply is valid. See Section 9.2.
3. Vcc_PWRGD is generated by the Vcc VRD and may be used elsewhere in the system.
4. VTTPWRGD may also be referenced as VIDPWRGD. Table 4-1. Power Sequence Timing Parameters
5. All power supply rails must be in regulator at the start of T_{D4}

Table 4-1. Power Sequence Timing Parameters

Parameter	Minimum	Typical	Maximum
TD1	1 ms	-	50 ms[1]
TD3	0 ms	-	-
TD4	0 ms	-	500 ms
TOFF	-	-	500 ms

NOTES:
1. . Applicable to all designs

When the VRD has been enabled and is delivering current to the processor, it should shut down power within 500 ms of receiving either a de-asserted Output Enable or an ‘OFF’ VID code (111111 or 011111). After an 'OFF' VID event, the processor will not provide an updated VID code to request current, so system power cycling must occur to restart the system.

Some VRD controllers sit idle (with no current delivered to the processor) waiting for a valid VID code and do not shut down. This is not the preferred operation, but is a valid state that will not cause functional failures.

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5 VRD Current Support (EXPECTED)

System boards supporting LGA775 socket processors must have voltage regulator designs compliant to electrical and thermal standards defined in Table 2-2. This includes full electrical support of Iccmax specifications and robust cooling solutions to support defined thermal design current (VR TDC) indefinitely within the envelope of system operating conditions. This includes regulator layout, processor fan selection, ambient temperature, chassis configuration, etc. Consult Table 2-2 and Table 3-1 for processor Vcc and Vtt current limits.

Intel processor VR TDC is the sustained (DC equivalent) current that is to be used for voltage regulator thermal design with supporting Thermal Monitor circuitry (see Section 9.4). At VR TDC, components such as switching FETs and inductors reach maximum temperature, heating the motherboard layers and neighboring components to the pass/fail boundary of thermal limits. Thermal analysis must include current contributions of both the Vcc and Vtt regulators. In some instances the PROCESSOR VRD will also power other motherboard components. Under this condition the VRD will supply current above the VR TDC limits; system designers must budget this additional current support in final VRD designs while remaining compliant to electrical and thermal specifications.

To avoid heat related failures, desktop computer systems should be validated for thermal compliance under the envelope of system operating for desktop systems.

§

6 Control Inputs

6.1 Vcc Output Enable (REQUIRED)

The VRD must include an input signal to enable the Vcc output. When disabled, the VRD output should be in a high-impedance state and should not source current. Once the VRD is operating after power-up, it should respond to a de-asserted output enable by turning off Vcc power within 500 ms. Consult Section 4 for Vcc power sequence information. When Output Enable is pulled low during the shutdown process, the VRD output must not exceed its previous voltage level regardless of the VID setting during the shutdown process. Voltage below –100 mV is not permitted at the output of the VRD.

Table 6-1. Output Enable Specifications

Design Parameter	Minimum	Typical	Maximum
Pull-Up Voltage Range		Vtt[1]	
Pull-Up Resistor	620 Ω[2]	680 Ω	750 Ω[3]
V_{IH}	0.8 V		-
V_{IL}	-		0.3 V

NOTES:
1. Consult Table 3-1 for Vtt specifications.
2. Value represents minimum resistance at tolerance limits.
3. Value represents maximum resistance at tolerance limits.
4. Voltage Identification (VID [5:0]) (REQUIRED)

The VRD must accept a six-bit code transmitted by the processor to establish the reference Vcc operating voltage as defined by Table 9-1.

While operating in the D-VID mode, Intel processors can transmit VID codes across the six bit bus with a 5 µs data transmission rate. To properly design this bus against timing and signal integrity requirements (Table 6-3), the following information is provided. The VID buffer circuit varies with processor generation and can be an open-drain or push-pull CMOS circuit configuration. The VID bus must be designed to be compatible with each circuit; therefore a pull-up resistor is required to bias the open drain configuration. The worst-case settling time requirement for code transmission at each load is 400 nanoseconds, including line-to-line skew. VRD controller VID inputs should contain circuitry to detect a change and prevent false tripping or latching of VID codes during this 400-nanosecond window.

Intel recommends use of the D-VID bus topology described in Figure 6-1 and Table 6-3. Under these conditions, traces can be routed with microstrip, stripline, or a combination with a maximum of Four-Layer transitions. The main trace length can vary between ½ inch and 15 inches with a maximum recommended line to line skew of 1 inch. The 680Ω ±10% pull-up resistor can be placed at any location on the trace with a maximum stub length of 1 inch.

Some designs may require additional VID bus loads. In this case, care should be taken to design the topology to avoid excessive undershoot and overshoot at each load. Failure to comply with these limits may lead to component damage or cause premature failure. The responsible engineer must identify minimum and maximum limits of each component and design a topology that ensures voltages stay within these limits at all times.

Figure 6-1. D-VID Bus Topology

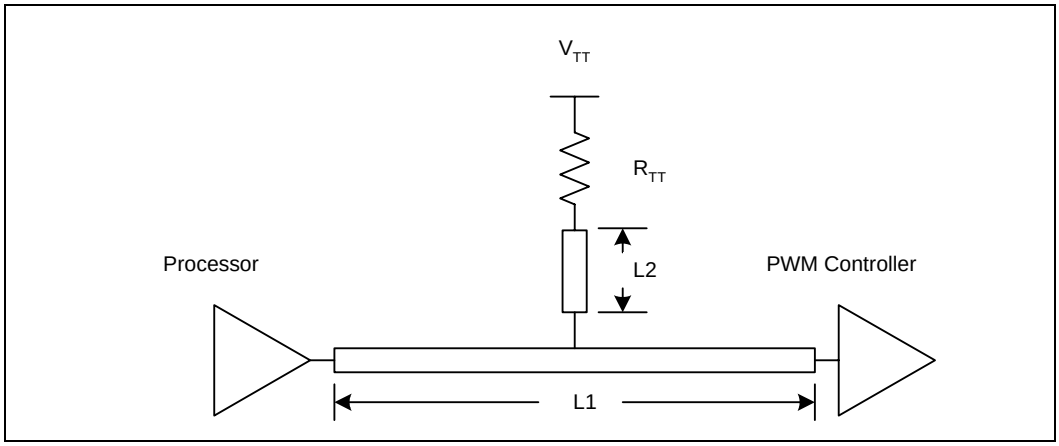


Table 6-2. VID Buffer and VID Bus Electrical Parameters

Design Parameter	Minimum	Typical	Maximum
VID Bus Voltage	-	Vtt[1]	-
Voltage Limits At Processor VID Lands	- 0.100	-	Vtt[2]
V_{IH}	0.8 V	-	-
V_{IL}	-	-	0.3 V
L_1, VID trace length	0.5 inch	-	15 inches
L_2, Vtt Stub Length	0 inch	-	1 inch
VID trace length skew	-	1.0 inch	-
VID trace width	5 mil	-	-
VID trace separation	5 mil	-	-
R_{TT}, Pull-Up Resistor	620 Ω[3]	680 Ω	750 Ω[4]

NOTES:
1. Consult Table 3-1 for Vtt specifications.
2. Consult the processor datasheet for signal overshoot limits.
3. Value represents minimum resistance at tolerance limits.
4. Value represents maximum resistance at tolerance limits.

Table 6-3. VRD10 Voltage Identification (VID) Table

Processor Lands (0 = low, 1 = high)						Vout (V)		Processor Lands (0 = low, 1 = high)						Vout(V)
VID5	VID4	VID3	VID2	VID1	VID0			VID5	VID4	VID3	VID2	VID1	VID0	
0	0	1	0	1	0	0.8375		0	1	1	0	1	0	1.2125
1	0	1	0	0	1	0.8500		1	1	1	0	0	1	1.2250
0	0	1	0	0	1	0.8625		0	1	1	0	0	1	1.2375
1	0	1	0	0	0	0.8750		1	1	1	0	0	0	1.2500
0	0	1	0	0	0	0.8875		0	1	1	0	0	0	1.2625
1	0	0	1	1	1	0.9000		1	1	0	1	1	1	1.2750
0	0	0	1	1	1	0.9125		0	1	0	1	1	1	1.2875
1	0	0	1	1	0	0.9250		1	1	0	1	1	0	1.3000
0	0	0	1	1	0	0.9375		0	1	0	1	1	0	1.3125
1	0	0	1	0	1	0.9500		1	1	0	1	0	1	1.3250
0	0	0	1	0	1	0.9625		0	1	0	1	0	1	1.3375
1	0	0	1	0	0	0.9750		1	1	0	1	0	0	1.3500
0	0	0	1	0	0	0.9875		0	1	0	1	0	0	1.3625
1	0	0	0	1	1	1.0000		1	1	0	0	1	1	1.3750
0	0	0	0	1	1	1.0125		0	1	0	0	1	1	1.3875
1	0	0	0	1	0	1.0250		1	1	0	0	1	0	1.4000
0	0	0	0	1	0	1.0375		0	1	0	0	1	0	1.4125
1	0	0	0	0	1	1.0500		1	1	0	0	0	1	1.4250
0	0	0	0	0	1	1.0625		0	1	0	0	0	1	1.4375
1	0	0	0	0	0	1.0750		1	1	0	0	0	0	1.4500
0	0	0	0	0	0	1.0875		0	1	0	0	0	0	1.4625
1	1	1	1	1	1	OFF[1]		1	0	1	1	1	1	1.4750
0	1	1	1	1	1	OFF[1]		0	0	1	1	1	1	1.4875
1	1	1	1	1	0	1.1000		1	0	1	1	1	0	1.5000
0	1	1	1	1	0	1.1125		0	0	1	1	1	0	1.5125
1	1	1	1	0	1	1.1250		1	0	1	1	0	1	1.5250
0	1	1	1	0	1	1.1375		0	0	1	1	0	1	1.5375
1	1	1	1	0	0	1.1500		1	0	1	1	0	0	1.5500
0	1	1	1	0	0	1.1625		0	0	1	1	0	0	1.5625
1	1	1	0	1	1	1.1750		1	0	1	0	1	1	1.5750
0	1	1	0	1	1	1.1875		0	0	1	0	1	1	1.5875
1	1	1	0	1	0	1.2000		1	0	1	0	1	0	1.6000

1. The Vcc output is disabled upon communication of an OFF VID code
   This is the same as de-asserting the output enable input (Section 6.1).
2. VID [4:0] are compatible with Intel desktop processors using five-bit VID codes.
3. VID [5:0] will be used on processors with six-bit codes.
4. Processors with seven or eight VID lines are not supported by VRD10

6.2 Differential Remote Sense Input (REQUIRED)

The PWM controller should include differential sense inputs to compensate for an output voltage offset of ≤ 300 mV in the power distribution path. The remote sense lines should draw no more than 10 mA, to minimize offset errors. Refer to Section 2.2 for the measurement location.

§

7 Input Voltage and Current

7.1 Input Voltages (EXPECTED)

VRD output voltage is supplied via DC-to-DC power conversion. To ensure proper operation, the input supplies to these regulators must satisfy the following conditions.

7.1.1 Desktop Input Voltages

The main power source for the Vcc VRD is 12 V ±15% and 3.3 V for the Vtt supply. These voltages are supplied by an AC-DC power supply through a cable to the motherboard. For input voltages outside the normal operating range, the VRD should either operate properly or shut down. The 1 A/µs slew rate specification for the input current is no longer a design requirement. Intel recommends a DC-DC regulator input filter with a minimum 1000 µF to ensure proper loading of the 12 V power source.

§

8 Output Protection

These are features built into the VRD to prevent damage to itself, the processor, and other system components.

8.1 Over-Voltage Protection (OVP) (PROPOSED)

An OVP circuit should monitor the output for an over-voltage condition. If the output is more than 200 mV above the maximum VID level, the VRD should shut off the Vcc supply to the processor.

8.2 Over-Current Protection (OCP) (PROPOSED)

The VRD must be capable of withstanding a continuous, abnormally low resistance on the output without overstressing the voltage regulator. Output current under this condition must be limited to avoid component damage and violation of the VRD thermal specifications (see Section 5).

§

9 Output Indicators

9.1 VCC_PWRGD: Vcc Power Good Output (PROPOSED)

The Vcc VRD is to provide a power-good signal, which satisfies timing requirements defined in section 4. The signal must remain asserted when the VRD is operating, except for fault or shutdown conditions. Vcc_PWRGD must not be de-asserted during the D-VID operation.

Table 9-1. Power Good Specifications

Design Parameter	Specification
Signal Type	Open-collector or equivalent
Voltage Range	5.5 V (maximum) in open state
Minimum IOL	4 mA
Maximum VOL	0.4 V

9.2 VTTPWRGD: Vtt Power Good Output (REQUIRED)

9.2.1 VTTPWRGD Electrical Specifications

The Vtt VRD is to provide a power-good signal to the processor and Vcc VRD, which satisfies timing requirements defined in Section 4 and electrical conditions defined in Table 9-2. The signal is to be asserted when Vtt reaches regulation and de-asserted after falling below tolerance limits. This signal is to remain asserted when the Vtt VRD is operating, except for fault or shutdown conditions. VTT_PWRGD must not be de-asserted during the D-VID operation. Each buffer attached to this signal must satisfy input Vil and Vih conditions defined in Table 9-2. See Section 6.1 for further information on the Vcc VRD Output Enable input.

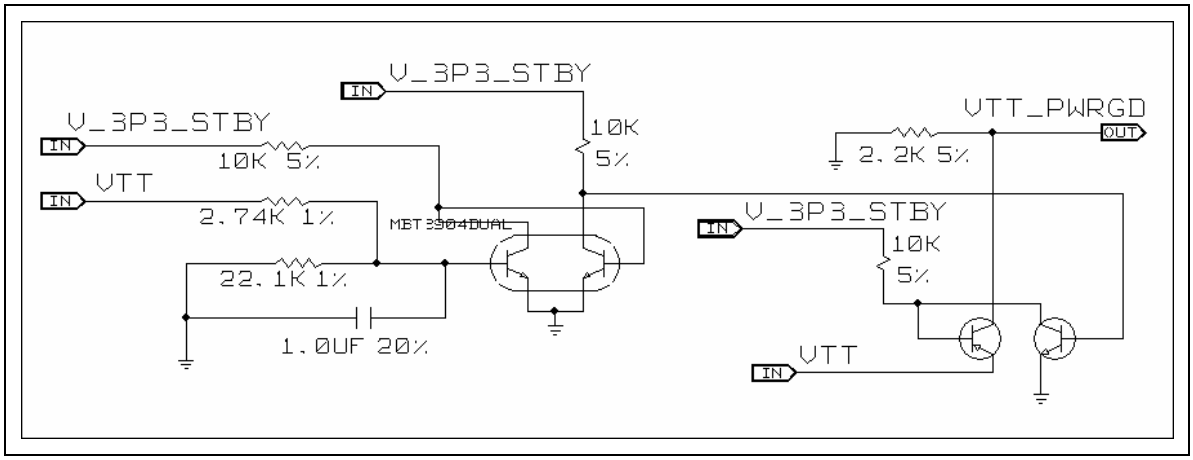
Table 9-2. VTT_PWRGD Electrical Parameters

Parameter	Minimum	Typical	Maximum
Pull-up voltage	-	Vtt[1]	-
Receiver Vih	0.8 V	-	-
Receiver Vil	-	-	0.3 V
Rise time (10% - 90%)	-	-	150 ns

NOTES:
1. Consult Table 3-1 for Vtt specifications

9.3 Example VTTPWRGD Circuit

Figure 9-1. VTTPWRGD Circuit



The circuit in Figure 9-1 satisfies the power sequence and rise time requirements of the VTTPWRGD signal as defined in Section 4 and 9.2.1. The circuit consists of two functional blocks. The first circuit block is centered around transistors A and B, which detect the Vtt threshold and triggers the VTTPWRGD signal. The second block consists of transistors D and C, which establish the necessary rise time and signal polarity. For this circuit, switching transistors are selected. As a result, the transistors are either cut-off or in full saturation. For the following discussion, please reference Figure 9-1.

At power-on, VTTPWRGD is tied low through the 2.2 kΩ transistor with transistor D OFF. For the benefit of the designer, the following passage describes the state of the circuit prior to Vtt regulation. At start-up, transistor A will be OFF since Vtt is below the base bias threshold. This establishes 0.7 V at the base of transistor B through the 10 k resistor tied to the 3.3 V stand-by. In this configuration, transistor B is in saturation and the collector voltage is below the base bias requirements of transistor C. As a result, Transistor C is OFF setting the collector of transistor C and base of transistor D to the 3.3 V standby voltage. Transistor D is a PNP with the emitter voltage tied to Vtt. With 3.3 V on the collector, transistor D is biased OFF in this configuration. This forces VTTPWRGD to ground through the 2.2 kΩ resistor. The 3.3 V supply provides a strong reference to avoid false triggering of this signal, however the 5 V standby can also be used. The 3.3 V standby supply was chosen for ease of routing.

Triggering of the VTTPWRGD signal occurs when the Vtt supply reaches regulation. The signal is toggled approximately 2.5 ms after the 90% Vtt threshold is reached. This functionality is established with an RC circuit connected to the base of transistor A. As Vtt rises to regulation, the RC network (the 2.74 kΩ resistor, 22.1 kΩ resistor, and 1.0 µF capacitor) will raise the base of transistor A to 0.7 V. This causes transistor A to conduct, thereby removing the base bias of transistor B. Removal of the base bias causes transistor B to switch off. This establishes a 0.7 V base bias for transistor C through the 10 kΩ resistor. With the existing collector bias, transistor C will switch-on. This collector voltage, connected to the base of transistor D, is sufficient to switch-on transistor D, thereby connecting VTTPWRGD to VTT.

This clever transistor network provides a low cost method of satisfying the VTTPWRGD trigger and rise-time specifications. General purpose switching NPN and PNP are chosen for design flexibility. Transistors A and B are contained in a single, 6-pin SOT-23 package; the

recommended part number is MBT3904Dual, which is provided by several vendors. Transistors C and D are also contained in a single, 6-pin SOT363 package; recommended part numbers are PUMZ1 (Philips Semiconductor*), MBT3964DW1(ON Semiconductor*) or equivalent.

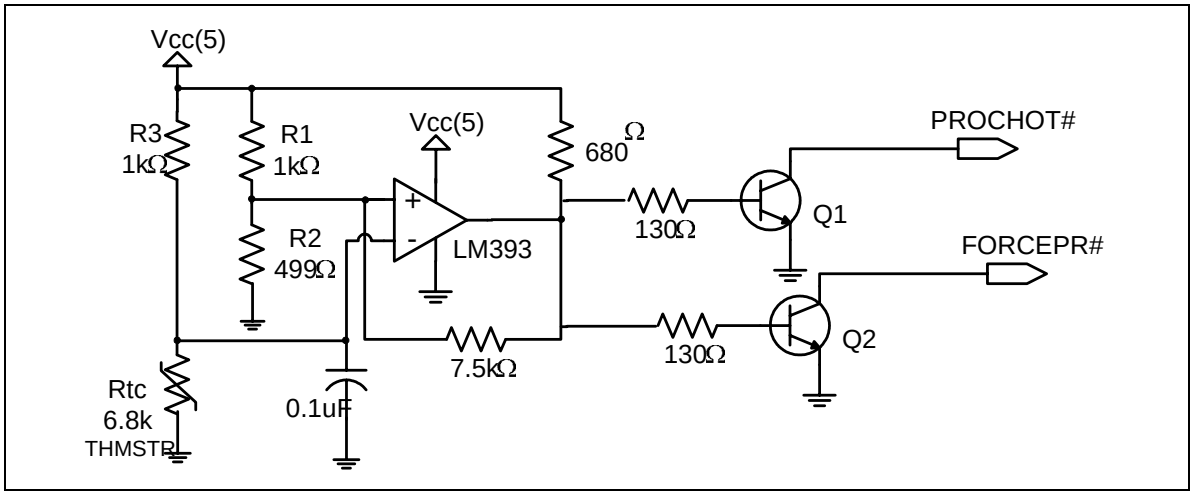
9.4 PROCHOT# and VRD Thermal Monitoring (EXPECTED)

This section describes how to protect the voltage regulator design from heat damage while supporting thermal design current (VR TDC). Intel does not recommend integrating thermal sensor features into Vcc PWM controller designs.

Each customer is responsible for identifying maximum temperature specifications for all components in the voltage regulator design and ensuring that these specifications are not violated while continuously drawing specified VR TDC levels. In the event of a catastrophic thermal failure, the thermal monitoring circuit is to assert the signal FORCEPR# and PROCHOT# immediately prior to exceeding maximum motherboard and component thermal ratings to prevent heat damage. Assertion of this signal will lower processor power consumption and reduce current draw through the voltage regulator, resulting in lower component temperatures. Assertion of these signals degrades system performance and must never occur when drawing less than specified thermal design current.

VRD temperature violations can be detected using a thermal sensor and associated control circuitry (see Figure 9-2). For this implementation, a thermistor (THMSTR) is placed in the temperature sensitive region of the voltage regulator. The location must be chosen carefully and is to represent the position where initial thermal violations are expected to occur. When exceeded, the thermal monitor circuit is to initiate FORCEPR# and PROCHOT# to protect the voltage regulator from heat damage.

Figure 9-2. Example VRD Thermal Monitor Circuit Design



NOTES: Where $R_2 = R_1/R_3 * R_{tc}$. Thermistor is NTHS0603N02N6801JR or equivalent. Where R_{tc} represents the thermistor resistance at maximum allowable temperature.

Assertion of PROCHOT# and FORCEPR# is governed by the comparator (LM393) using the sensor voltage (at the negative comparator terminal) and a trigger reference voltage (at the

positive comparator terminal). As the thermistor temperature increases due to system loading, the resistance will decrease. When the voltage drop across the thermistor falls below the trigger reference voltage, established by R1 and R2, the comparator will change state and bias the bipolar transistors. When biased, Q1 and Q2 provide the active low assertion of PROCHOT# and FORCEPR# compliant to Table 7 signaling specifications. Q1 and Q2 must be selected to adequately drive PROCHOT# and FORCEPR# VOL signaling values.

FORCEPR# is a processor signal with active-low input buffers terminated to the system Vtt (FSB termination voltage). PROCHOT# is a processor signal that can be configured as i/o using open-drain, output buffers terminated to the system Vtt (FSB termination voltage); This signal drives and receives with active low signaling. In some processor configurations, this buffer is configured as an output only signal To maintain reliable signaling, the bipolar transistor must be selected to operate with a collector bias established by motherboard, processor, or chipset on-die termination (See Figure 9-2). The bipolar transistors must be chosen to drive an the Vol levels identified in Table 9-3 with an effective termination range defined in Table 9-3. Note that the termination topology can take multiple forms; A generic representation is provided in Figure 9-3. PROCHOT# and FORCEPR# may see this full configuration, or a subset including any combination of the identified loads.

The values for R1, R2 and R3 in Figure 4 are included as an example and must be calculated using specific design parameters. The value of R2 is adjusted to calibrate the comparator's trigger reference voltage (and assertion of the output signals) against the sensor voltage representing a thermal violation.

Figure 9-3. Processor Load Schematic for PROCHOT# AND FORCEPR# termination (Single Load)

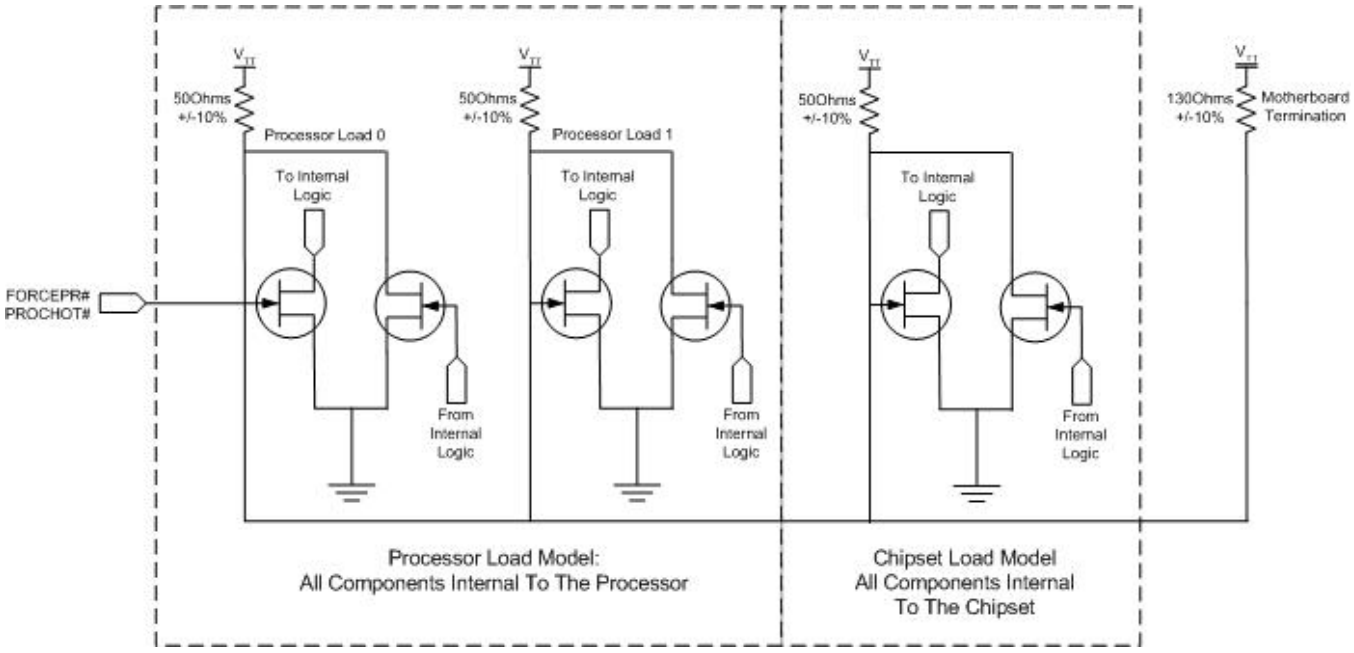


Table 9-3. Thermal Monitor Specifications

Parameter	Minimum	Typical	Maximum
Vtt	-	Vtt[1]	-
Vcc(5)	4.75 V	5.00 V	5.25 V
Q1 ‘on’ resistance	-	-	11 Ω
PROCHOT# leakage current	-	-	200 µA
PROCHOT# transition time	1.10 ns	100 ns	-
FORCEPR# leakage current			200 µA
FORCEPR# transition time	1.10 ns	100 ns	
PROCHOT# VOL (Maximum low voltage threshold)			0.4V
FORCEPR# VOL (Maximum low voltage threshold)			0.4V
FORCEPR# transition time	1.10 ns	100 ns	
Minimum time to toggle in and out of D-VID	0.5ms	-	-
RPU (Pull-up Resistor)[2]Equivalent Termination Tied to PROCHOT# OR/AND FORCEPR#	15 Ω	-	130 Ω

NOTES:
1. Consult Table 3-1 for Vtt specifications.
2. Bias for Q1and Q2 in the thermal monitor circuit is provided by the processor and chipset. Additional termination must not be integrated into the thermal monitoring circuit.

9.5 Load Indicator Output (EXPECTED)

To assist VRD circuit debug and validation, the PWM controller supplier may choose to include an output voltage that is a defined function of the VRD output current.

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10 Motherboard Power Plane Layout

The motherboard layer stack-up must be designed to ensure robust, noise-free power delivery to the processor. Failure to minimize and balance power plane resistance may result in non-compliance to the die load line specification. A poorly planned stack-up or excessive holes in the power planes may increase system inductance and generate oscillation on the rail at the processor. Both of these types of design errors can lead to processor failure and must be avoided by careful Vcc and Vss plane layout and stack-up. The types of noise introduced by these errors may not be immediately observed on the processor power lands or during system-board voltage transient validation, so issues must be resolved by design, prior to layout, to avoid unexpected failures.

Following basic layout rules can help avoid excessive power plane noise. All motherboard layers in the area surrounding the processor socket should be used for Vcc power delivery; copper shapes that encompass the power delivery region of the processor land field are required. A careful motherboard design will help ensure a well-functioning system that minimizes the noise profile at the processor die. The following subsections provide further guidance.

10.1 Minimize Power Path DC Resistance (EXPECTED)

Power path resistance can be minimized by ensuring that the copper layout area is balanced between Vcc and Vss planes. A good Four-Layer board design will have two Vcc layers and two Vss layers. Because there is generally more Vss copper in the motherboard stack-up, care should be taken to maximize the copper in Vcc floods. This includes care to minimize unnecessary plane splits and holes when locating through hole components, vias, and connection pads.

10.2 Minimize Power Delivery Inductance (EXPECTED)

At higher frequencies the ordering of the motherboard layers becomes critical as it is Vcc/Vss plane pairs which carry current and determine power plane inductance. The layer stack-up should maximize adjacent (layer-to-layer) planes at a minimized spacing to achieve the smallest possible inductance. Care must be taken to minimize unnecessary plane splits and holes when locating through-hole components, vias, and connection pads. Minimized inductance will ensure that the board does not develop low frequency noise which may cause the processor to fail (load line violation).

10.3 Four-Layer Boards (EXPECTED)

A well-designed 4-layer board will feature generous Vcc shapes on the outer layers and large Vss shapes on the inner layers. The Vss-reference requirements for the front side bus are best accommodated with this layer ordering. The power plane area should be maximized and cut-out areas should be carefully placed to minimize parasitic resistance and inductance. Examples power plane layout of Intel's reference board are provided in Table 11-1 and Figure 10-1 to Figure 10-5.

Figure 10-1. Reference Board Layer Stack-up

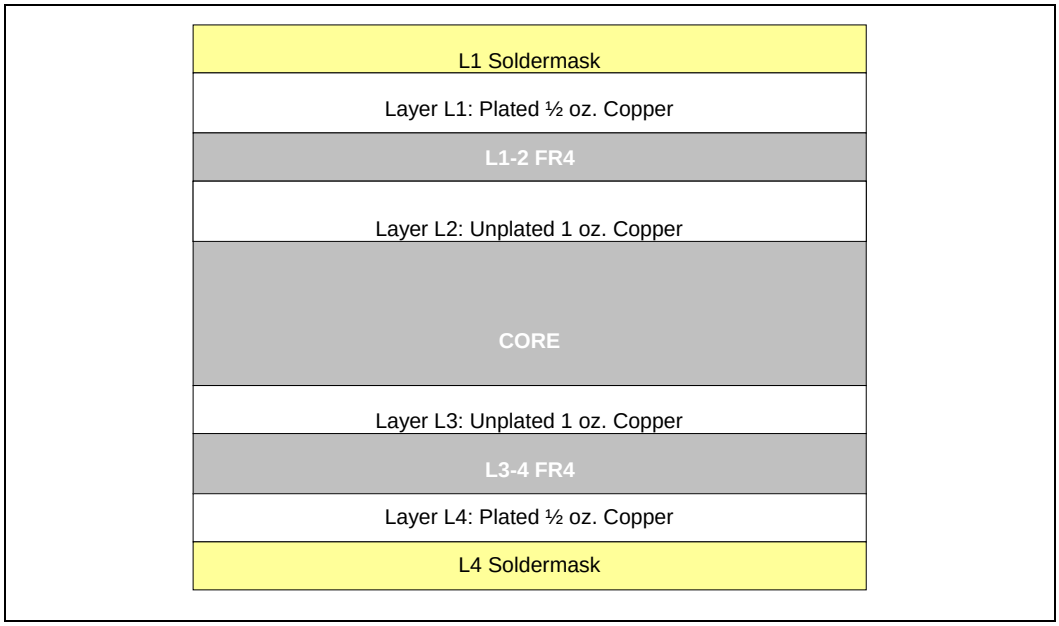


Table 10-1. Reference Board Layer Thickness

Layer	Minimum	Typical	Maximum
L1 Soldermask	0.15 mils	0.65 mils	1.16 mils
L1	1.08 mils	1.90 mils	2.72 mils
L1-2 FR4	3.90 mils	4.40 mils	4.80 mils
L2	1.00 mils	1.20 mils	1.40 mils
Core	57 mils	62 mils	70 mils
L3	1.00 mils	1.20 mils	1.40 mils
L3-4 FR4	3.90 mils	4.40 mils	4.80 mils
L4	1.08 mils	1.90 mils	2.72 mils
L4 Soldermask	0.15 mils	0.65 mils	1.16 mils

NOTE: Consult Figure 10-1 for layer definition

Figure 10-2. Layer 1 Vcc Shape for Intel's Reference Four-Layer Motherboard

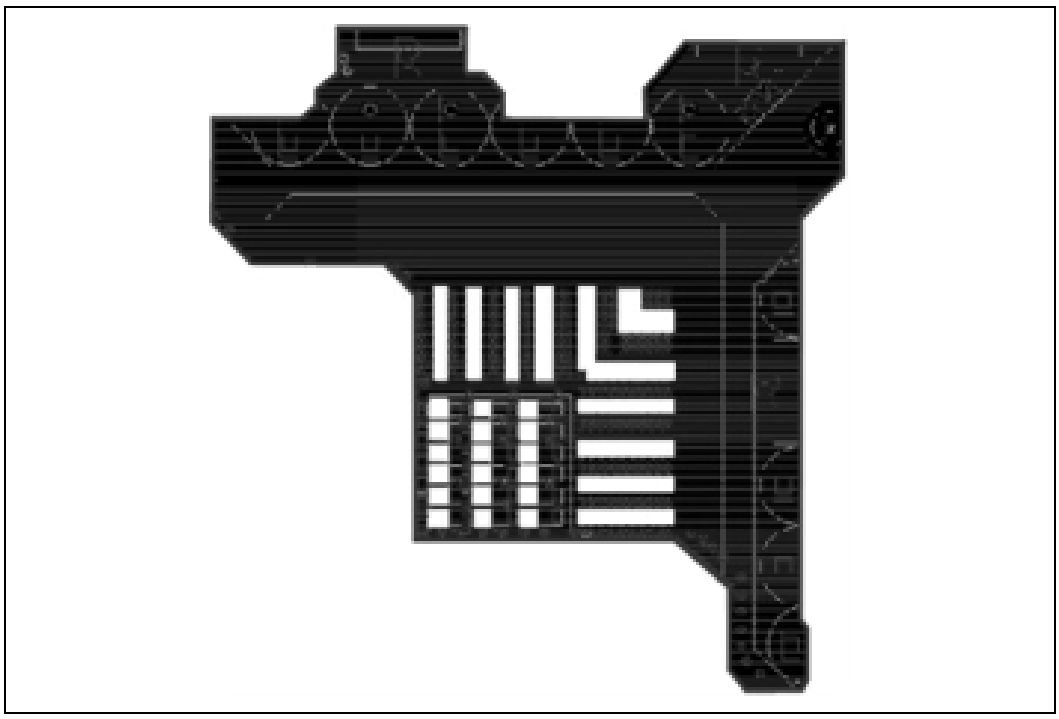


Figure 10-3. Layer 2 Vss Routing for Intel's Reference Four-Layer Motherboard

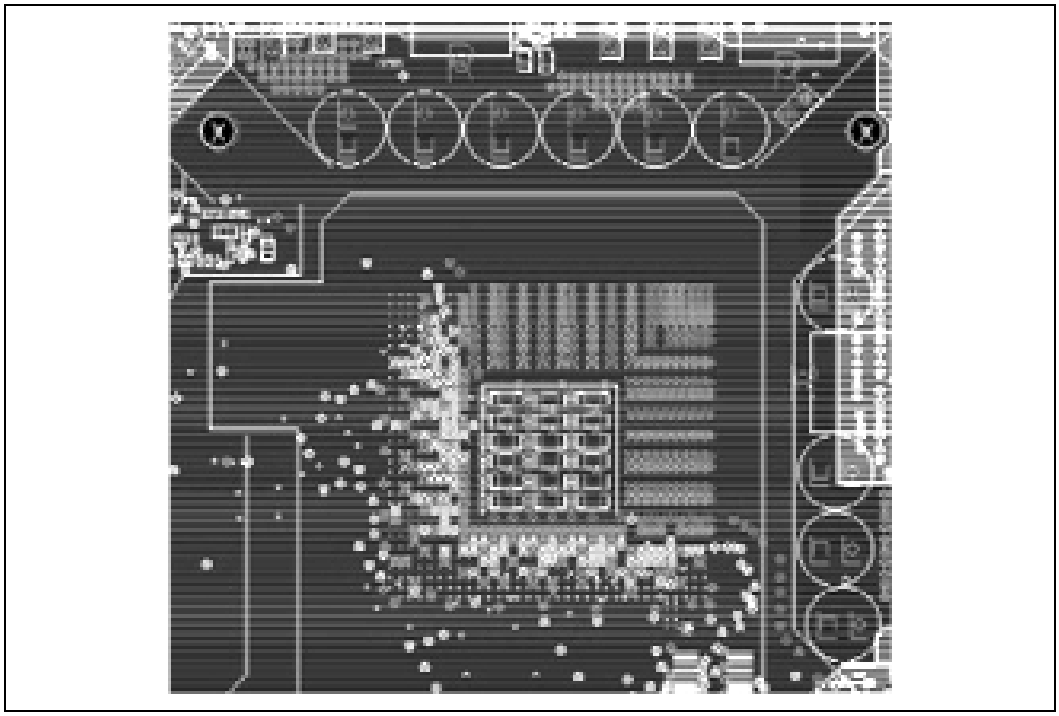


Figure 10-4. Layer 3 Vss Routing for Intel's Reference Four-Layer Motherboard

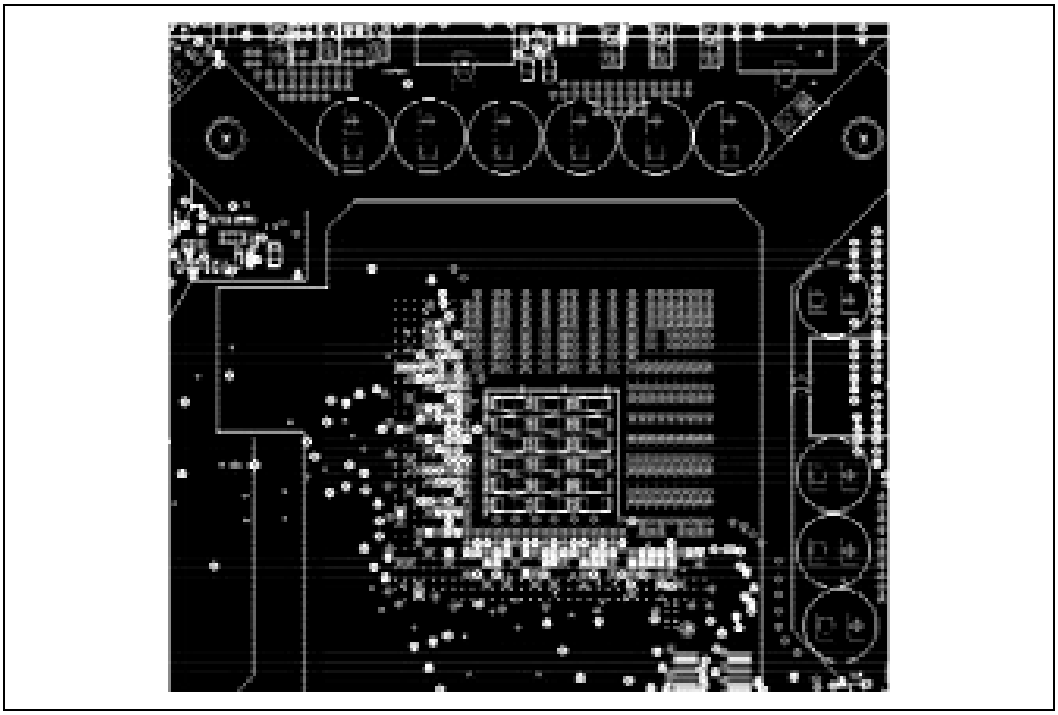
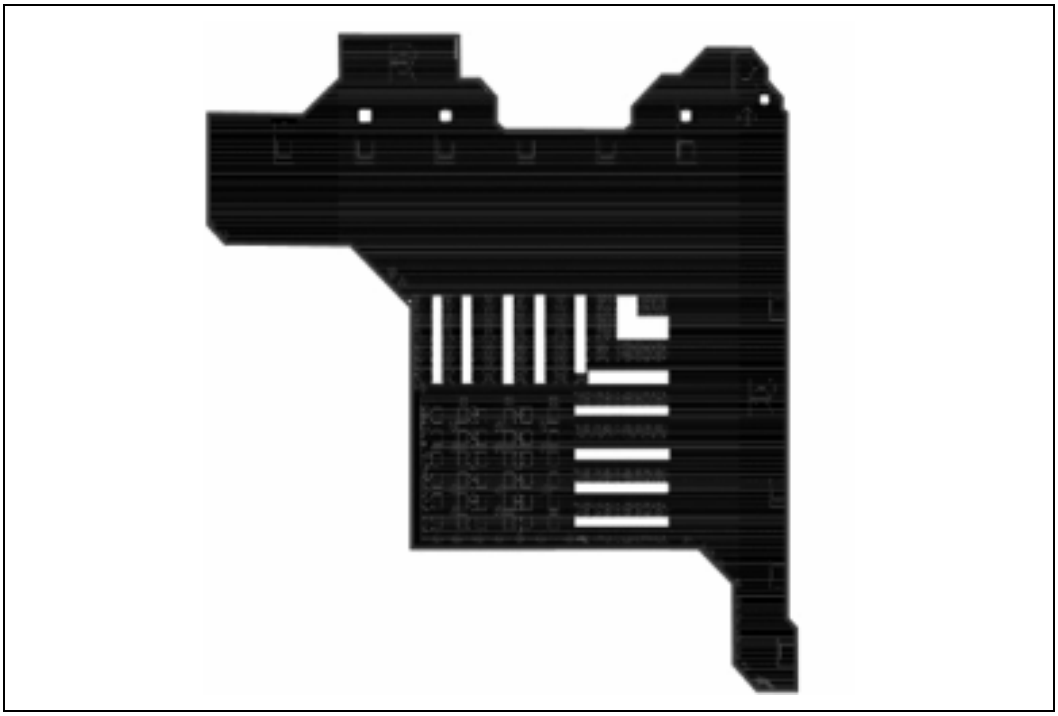


Figure 10-5. Layer 4 Vcc Shape for Intel's Reference Four-Layer Motherboard



10.4 Six-Layer Boards (EXPECTED)

Six layer boards provide layout engineers with greater design flexibility compared to the Four-Layer standard. Adjacent plane pairs of the same potential are not useful at higher frequencies, so the best approach is to maximize adjacent, closely spaced Vcc/Vss plane pairs. The plane pair separated by the PCB core material is of lesser importance since it is generally an order of magnitude larger in spacing than other plane pairs in the stack-up. Because the Vss planes are typically full floods of copper, an example of a well-designed 6-layer stack-up will have four Vcc layers and two layers for Vss. The DC resistive requirements (section 10.1) of the power delivery loop can still be met because the Vss floods are larger than the Vcc floods, and the higher frequency needs are considered as there are four Vcc/Vss plane pairs to deliver current and reduce inductance.

10.5 Resonance Suppression (EXPECTED)

Vcc power delivery designs can be susceptible to resonance phenomena capable of creating droop amplitudes in violation of load line specifications. This is due to the interleaved levels of inductively-separated decoupling capacitance. Furthermore, these resonances may not be detected through standard VTT validation and require engineering analysis to identify and resolve. If not identified and corrected in the design process, these resonant phenomena may yield droop amplitudes in violation of load line specifications by superimposing with standard VRD droop behavior. Frequency-dependent power delivery network impedance simulations and validation are strongly recommended to identify and resolve power delivery resonances before board are actually built. Careful modeling and validation can help to avoid voltage violations responsible for data corruption, system lock-up, or system ‘blue-screening’

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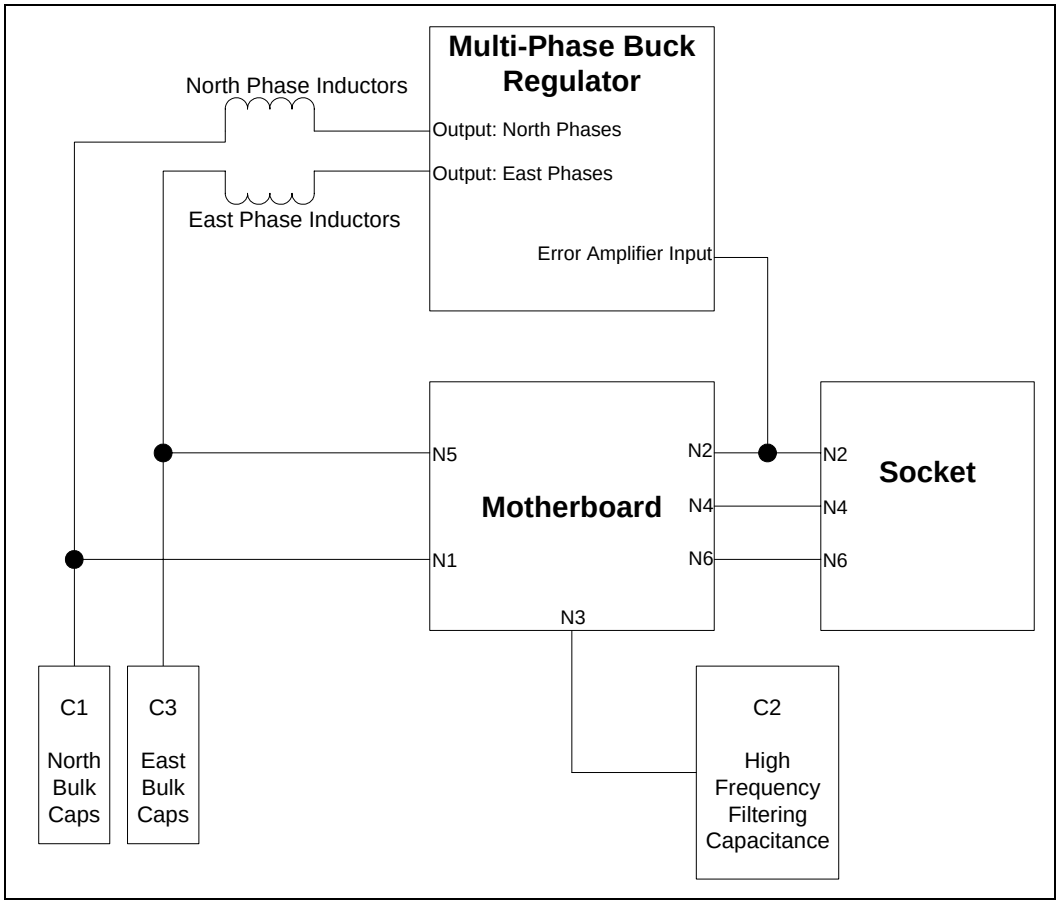
11 Electrical Simulation

The following electrical models are enclosed to assist with VRD design analysis and component evaluation for load line compliance. The block diagram shown in Figure 11-1 is a simplified representation of the Vcc power delivery network of the Intel four-layer reference board interfaced with the LGA775 socket. The board model, detailed in Figure 11-4, characterizes the power plane layout of Figure 10-2 to Figure 10-5. The socket, detailed in Figure 11-6, models the LGA775 electrical parasitics; it also provides a current load step model for exploring the system droop response. The multiphase buck regulator and capacitor models should be obtained from each selected vendor. When fully integrated into electrical simulation software, this model can be used to evaluate PWM controller, capacitor, and inductor performance against the load line and tolerance band requirements detailed in Section 2.2. To obtain accurate results, it is strongly recommended to create and use a custom model that represents the specific board design, PWM controller, and passive components that are under evaluation.

Figure 11-1. Simplified Block Diagram Representing Electrical Connectivity for the VRD on the Four-Layer Intel Reference Motherboard



NOTE: Consult Figure 10-2 to Figure 10-5 for reference layout.

The motherboard model of Figure 11-4 represents the power delivery path of Intel's reference four-layer motherboard design. Input and output node locations are identified in Figure 11-5. Feedback to the PWM controller error amplifier should be tied to node 'N2', the socket-motherboard interface. Node 'N1' is the location where the 'north' phase inductors of the buck regulator ties to the 'north' motherboard power plane. If the design incorporates more than one 'north' phase, the inductors of each should be tied to this node. 'North' bulk capacitors, C1, are also connected to node 'N1'. C1 represents the parallel combination of all capacitors and capacitor parasitics at this location. Node 'N5' is the location where the output inductors of the 'east' side phases tie to the 'east' motherboard power plane. If the design incorporates more than one 'east' phase, the inductors of each should be tied to this node. 'East' bulk capacitors, C3, are also connected to 'N5'. C3 represents the parallel combination of all capacitors and capacitor parasitics at this location. Node 'N3' represents the socket cavity and is connected to the high frequency filter, C2. C2 represents the parallel combination of all capacitors and capacitor parasitics at this location.

Typical capacitor models are identified in Figure 11-6. Each model represents the parallel combination of the local capacitor placement as identified in the previous paragraph. Recommended parallel values of each parameter are identified in Table 11-2. Consult Section 2.8 for further details regarding bulk and high frequency capacitor selection.

LGA775 electrical models are provided in Figure 11-7. The LGA775 socket is characterized by three impedance paths that connect to the motherboard at 'N2' ('north' connection), 'N4' ('south' cavity connection), and 'N6' ('east' connection). Current is fed to this branch network through the VTT Tool parasitic impedance (RVTT1, LVTT1, RVTT2, LVTT2), which is driven by current source I_PWL. I_PWL is a piece-wise linear current step that is used to stimulate the voltage droop as seen at the motherboard-socket interface and is defined in Figure 11-8 and Table 11-4. This load step approximates the low frequency current spectrum that is necessary to evaluate bulk capacitor and PWM controller performance. It does not provide high frequency content to excite package noise. The cavity capacitor solution, C2, is used as a reference for designing processor packaging material and should not be modified except to reduce ESR/ESL or increase total capacitance.

Caution: Failure to observe this recommendation may make the motherboard incompatible with some processor designs.

The primary purpose of the simulation model is to identify options in supporting the socket load line specification. Evaluation of the full power-path model will allow the designer to perform what-if analysis to determine the cost optimal capacitor and PWM controller configuration. This is especially useful in determining the capacitor configuration that can support load line specifications across variation such as manufacturing tolerance, age degradation, and thermal drift. The designer is encouraged to evaluate different bulk capacitor configurations and PWM controller designs. However, the designer should be aware that the feedback compensation network of most PWM controllers requires modification when the capacitor solution changes. Consult the PWM controller datasheet for further information.

Figure 11-2. Example Voltage Droop Observed at Node ‘N2’

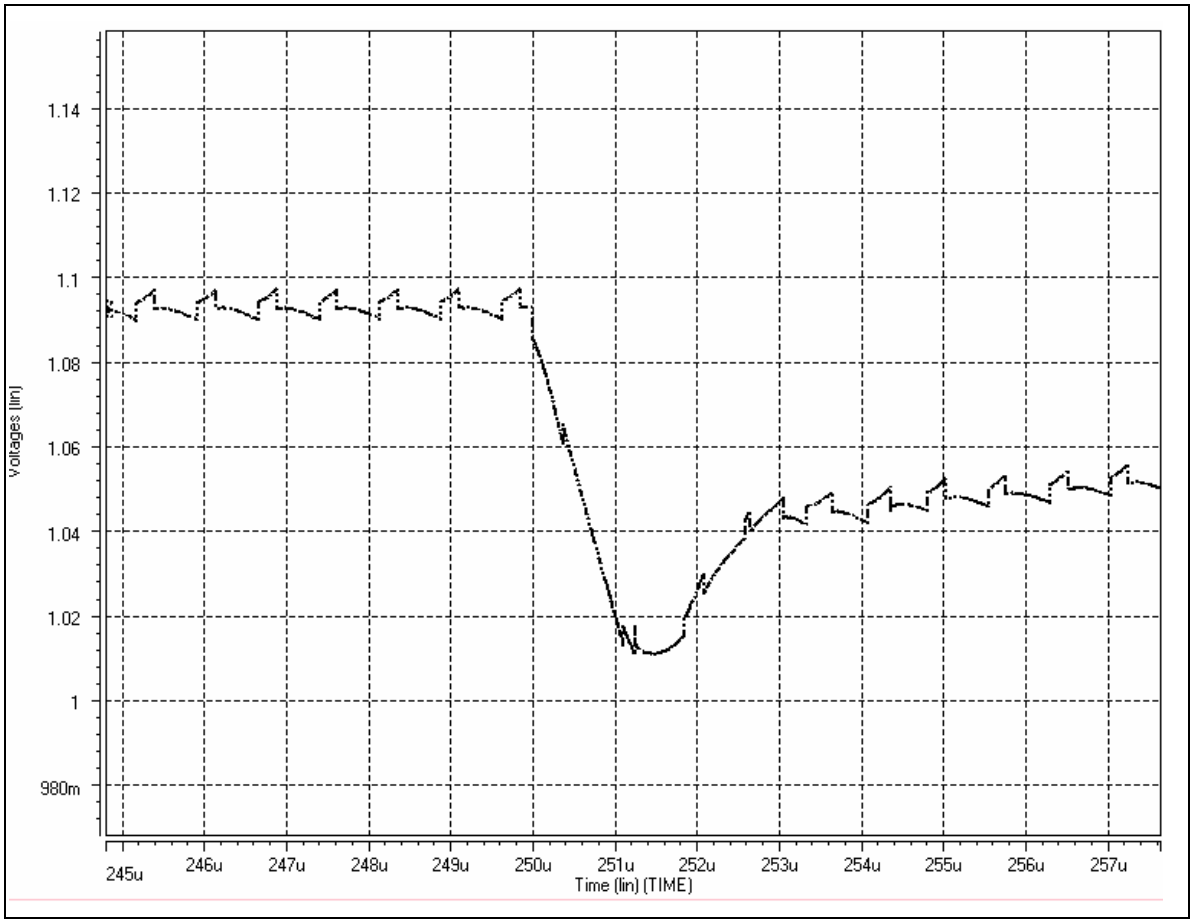
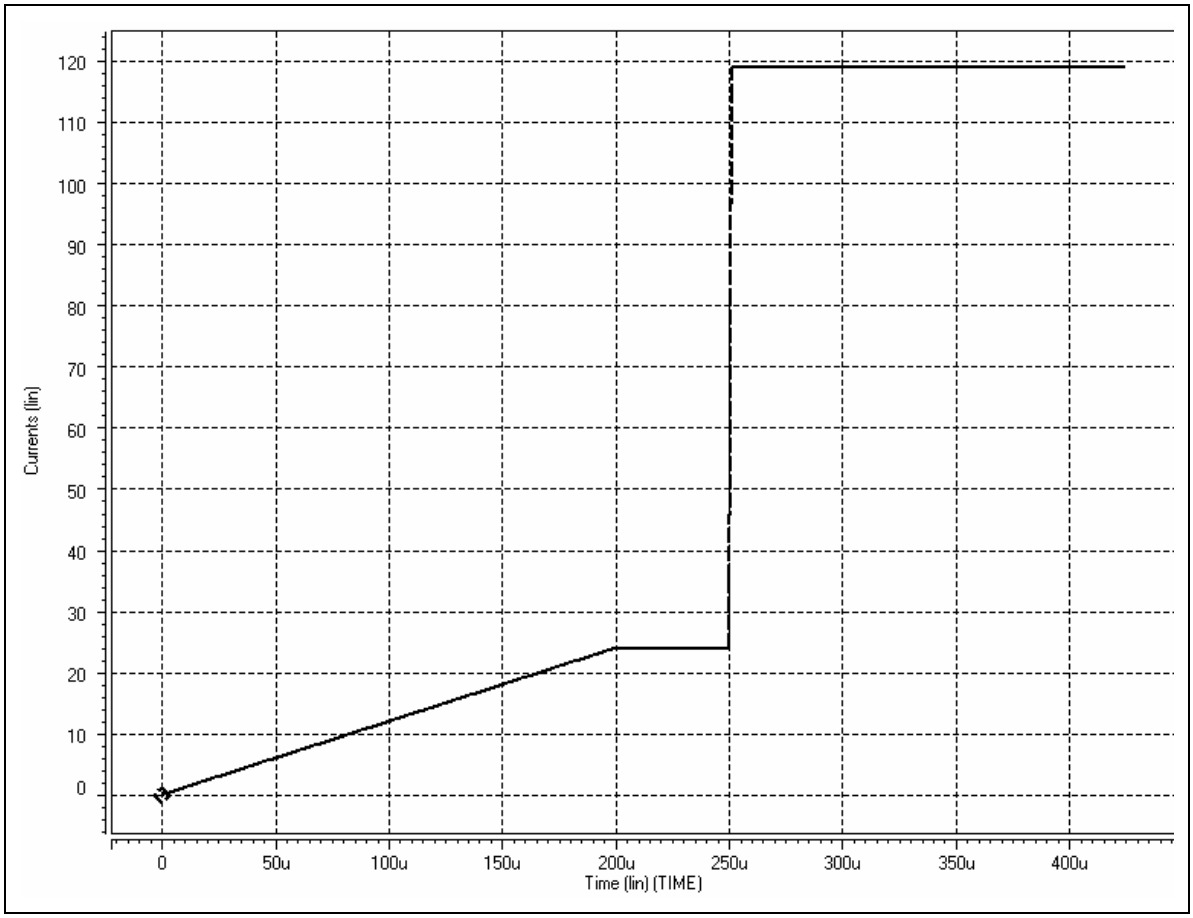


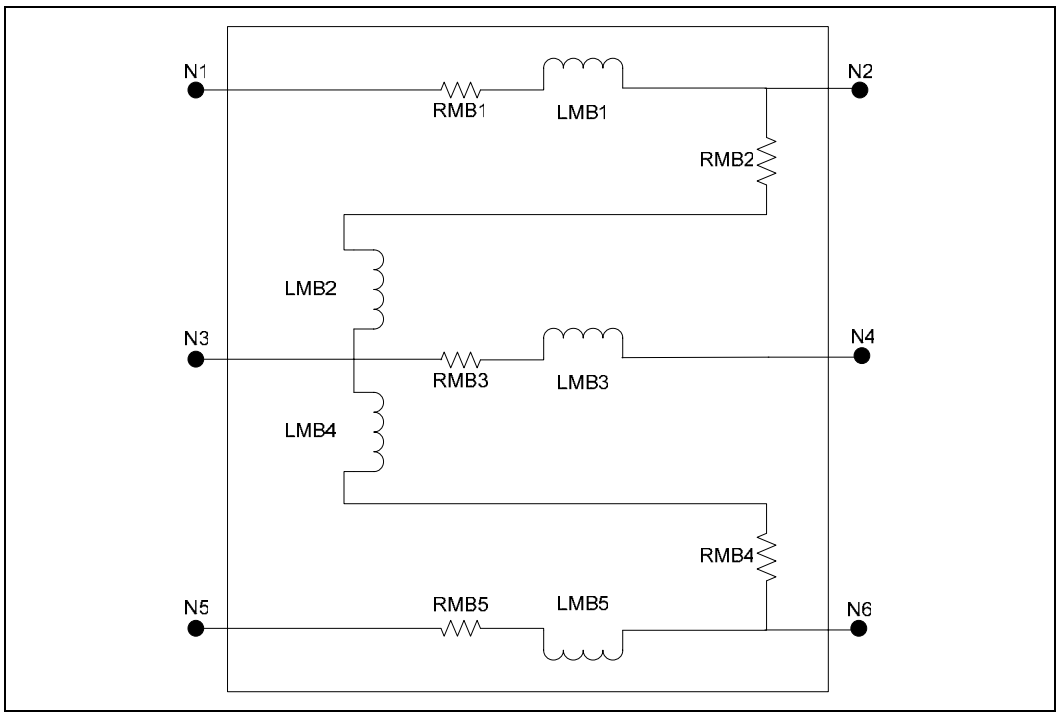
Figure 11-2 provides an example voltage droop waveform at node ‘N2’, the socket-motherboard interface. The load line value is defined as ΔV/ΔI with ΔV measured at this node and the current step observed through I_PWL (see Figure 11-7). The voltage amplitude is defined as the difference in the steady state voltage (prior to the transient) and the minimum voltage droop (consult Figure 11-2). Care must be taken to remove all ripple content in this measurement to avoid a pessimistic load line calculation that will require additional capacitors (cost) to correct. Figure 11-3provides an example current stimulus. The amplitude is measured as the difference in maximum current and steady state current prior to initiation of the current step. With ΔV and ΔI known, the load line slope is simply calculated using Ohm’s Law: $R_{LL} = \Delta V/\Delta I$.

Figure 11-3. Current Step Observed Through I_PWL



NOTE: To avoid excessive ringing in simulation, the system current should be slowly ramped from zero amps to the minimum recommended DC value prior to initiating the current step

Figure 11-4. Schematic Diagram for the Four-Layer Intel Reference Motherboard



NOTE: Consult Figure 10-2 to Figure 10-5 for reference layout.

Table 11-1. Parameter Values for the Schematic of Figure 11-4

Parameter	Value	Comments
RMB1	0.93 mΩ	'North' power plane parasitic resistance from the buck regulator output inductor to the LGA775 socket connection.
RMB2	0.85 mΩ	Power plane parasitic resistance from 'north' LGA775 motherboard connection to the center of the LGA775 cavity.
RMB3	0.70 mΩ	Power plane parasitic resistance from the center of the LGA775 cavity to the 'south' LGA775 socket connection.
RMB4	0.87 mΩ	Power plane parasitic resistance from the center of the LGA775 cavity to the 'east' LGA775 socket connection.
RMB5	0.97 mΩ	'East' power plane parasitic resistance from the buck regulator output inductor to the LGA775 connection.
LMB1	104 pH	'North' power plane parasitic inductance from the buck regulator output inductor to the LGA775 socket connection
LMB2	88 pH	Power plane parasitic inductance from 'north' LGA775 motherboard connection to the center of the LGA775 cavity.
LMB3	65 pH	Power plane parasitic inductance from the center of the LGA775 cavity to the 'south' LGA775 socket connection.
LMB4	92 pH	Power plane parasitic inductance from 'east' LGA775 motherboard connection to the center of the LGA775 cavity.
LMB5	106 pH	'East' power plane parasitic inductance from the buck regulator output inductor to the LGA775 connection.

Figure 11-5. Node Location for the Schematic of Figure 11-4

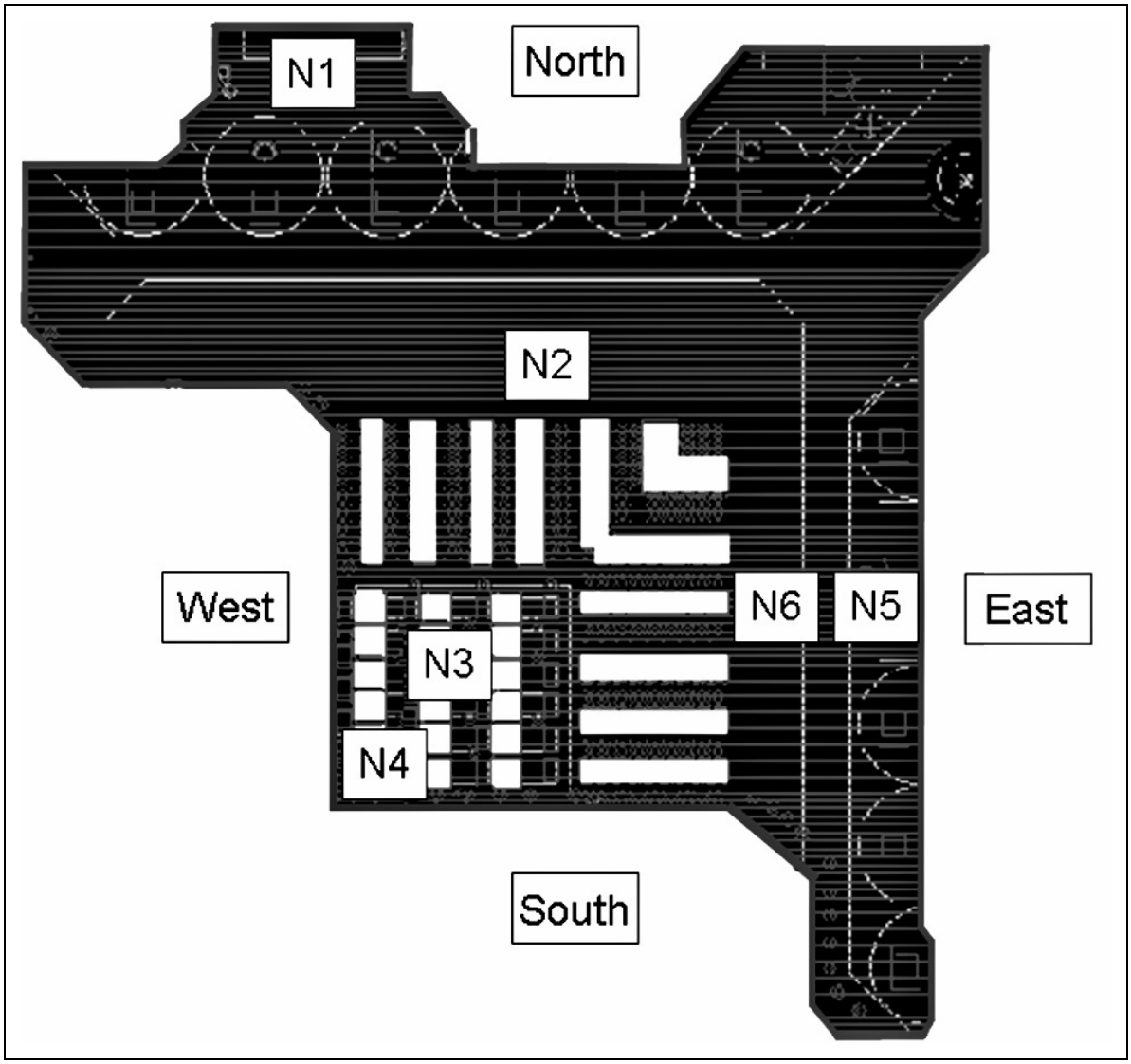
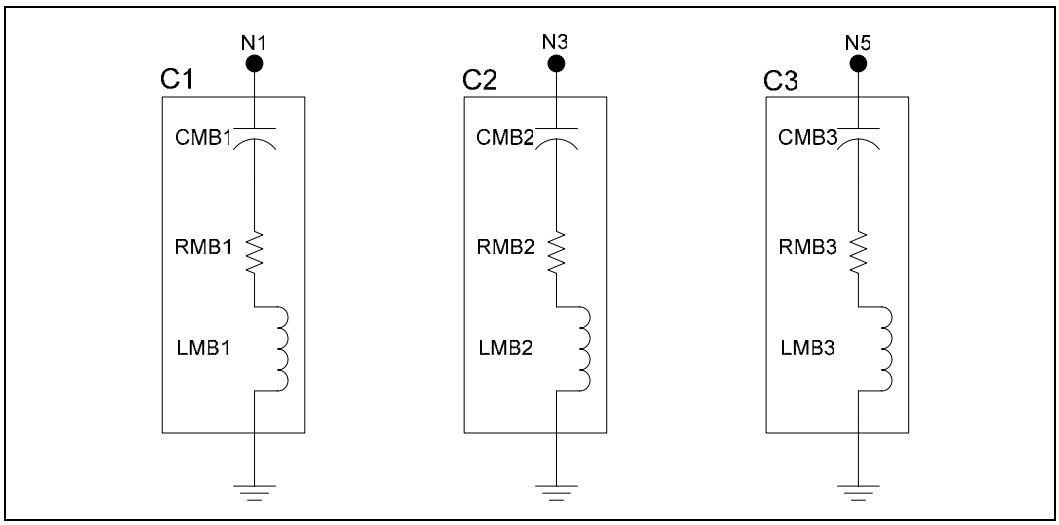


Figure 11-6. Schematic Representation of Bulk and High-Frequency Decoupling Capacitors



NOTES:

1. C1 represents the parallel model for 'north' location bulk decoupling
2. C2 represents the parallel model for high frequency decoupling located in the socket cavity
3. C3 represents the parallel model for 'east' location bulk decoupling

Table 11-2. Recommended Parameter Values for the Capacitors Models in Figure 11-6

Parameter	Value	Comments
CMB1	3360 μF[2]	Parallel equivalent for 'north' capacitors prior to age, thermal, & manufacturing degradation.
RMB1	1.0 mΩ	Parallel equivalent for 'north' capacitor maximum ESR.
LMB1	550 pH[1, 2]	Parallel equivalent for 'north' capacitor maximum ESL.
CMB2	180 μF[2]	Parallel equivalent for 'cavity' capacitors prior to age, thermal, & manufacturing degradation.
RMB2	0.16 mΩ[2]	Parallel equivalent for 'cavity' capacitor maximum ESR.
LMB2	60 pH[1, 2]	Parallel equivalent for 'cavity' capacitor maximum ESL.
CMB3	2240 μF[2]	Parallel equivalent for 'east' capacitors prior to age, thermal, and manufacturing degradation.
RMB3	1.5 mΩ[2]	Parallel equivalent for 'east' capacitor maximum ESR.
LMB3	712 pH[1, 2]	Parallel equivalent for 'east' capacitor maximum ESL.

NOTES: :

1. Higher values of ESL may satisfy design requirements.
2. Contact capacitor vendors to identify values for the specific components used in your design

Figure 11-7. Schematic Representation of the LGA775 Socket

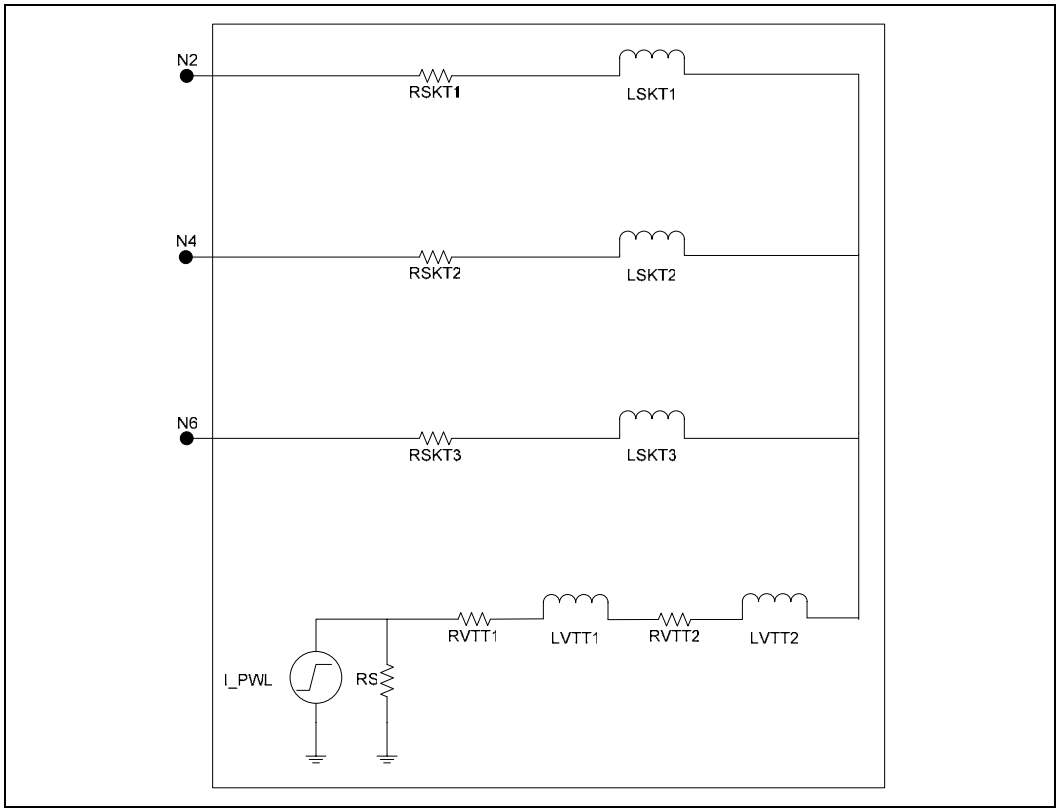


Table 11-3. Electrical Parameters for the Schematic of Figure 11-7

Parameter	Value	Comments
RSKT1	0.38 mΩ	LGA775 ‘north’ segment resistance
RSKT2	1.13 mΩ	LGA775 ‘center’ segment resistance
RSKT3	0.29 mΩ	LGA775 ‘east’ segment resistance
RVTT1	0.42 mΩ	Resistance of VTT Tool load board
RVTT2	0.91 mΩ	Resistance of VTT Tool socket adapter (interposer)
RS	100 kΩ	VTT Tool current source resistance
LSKT1	40 pH	LGA775 ‘north’ segment inductance
LSKT2	120pH	LGA775 ‘center’ segment inductance
LSKT3	30 pH	LGA775 ‘east’ segment inductance
LVTT1	240 pH	Inductance of VTT Tool load board
LVTT2	42 pH	Inductance of VTT Tool socket adapter (interposer)

Figure 11-8. Current Load Step Profile for I_PWL from the Schematic of Figure 11-7

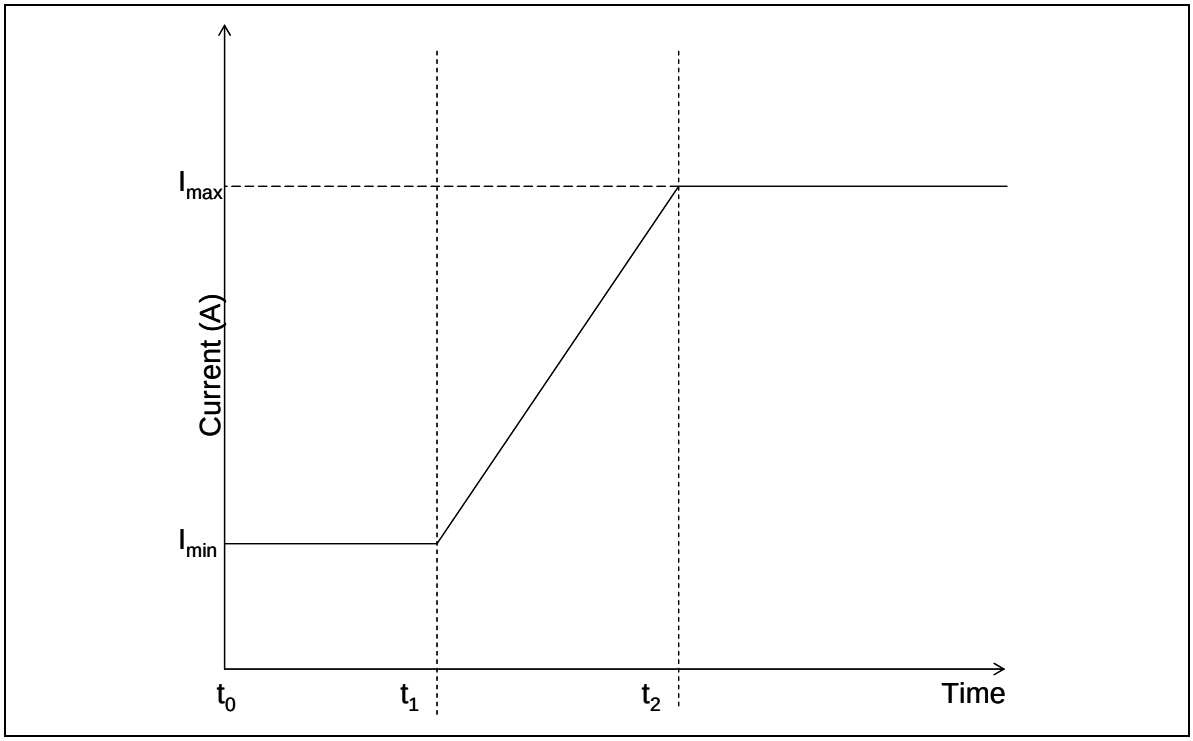


Table 11-4. I_PWL Current Parameters for Figure 11-7 and Figure 11-8

Parameter	Value	Comments
t_0	0 s	Simulation 'time zero'
t_1	250 µs	Time to initiate the current step. This parameter must be chosen at a time that the Vcc rail is residing at steady state.
t_2	t_1 + 1.25 µs	Time of maximum current
Istep	95 A	Current step for load line testing
Imin	24 A	Minimum current for simulation analysis
Imax	119 A	Maximum current for simulation analysis

§

12 Appendix: LGA775 Version 1 Pinmap

Land Name	Land #	Signal Buffer Type	Direction
A10#	U6	Source Synch	Input/Output
A11#	T4	Source Synch	Input/Output
A12#	U5	Source Synch	Input/Output
A13#	U4	Source Synch	Input/Output
A14#	V5	Source Synch	Input/Output
A15#	V4	Source Synch	Input/Output
A16#	W5	Source Synch	Input/Output
A17#	AB6	Source Synch	Input/Output
A18#	W6	Source Synch	Input/Output
A19#	Y6	Source Synch	Input/Output
A20#	Y4	Source Synch	Input/Output
A20M#	K3	Asynch GTL+	Input
A21#	AA4	Source Synch	Input/Output
A22#	AD6	Source Synch	Input/Output
A23#	AA5	Source Synch	Input/Output
A24#	AB5	Source Synch	Input/Output
A25#	AC5	Source Synch	Input/Output
A26#	AB4	Source Synch	Input/Output
A27#	AF5	Source Synch	Input/Output
A28#	AF4	Source Synch	Input/Output
A29#	AG6	Source Synch	Input/Output
A3#	L5	Source Synch	Input/Output
A30#	AG4	Source Synch	Input/Output
A31#	AG5	Source Synch	Input/Output
A32#	AH4	Source Synch	Input/Output
A33#	AH5	Source Synch	Input/Output
A34#	AJ5	Source Synch	Input/Output
A35#	AJ6	Source Synch	Input/Output
A4#	P6	Source Synch	Input/Output
A5#	M5	Source Synch	Input/Output
A6#	L4	Source Synch	Input/Output
A7#	M4	Source Synch	Input/Output
A8#	R4	Source Synch	Input/Output
A9#	T5	Source Synch	Input/Output
ADS#	D2	Common Clock	Input/Output
ADSTB0#	R6	Source Synch	Input/Output
ADSTB1#	AD5	Source Synch	Input/Output

Land Name	Land #	Signal Buffer Type	Direction
AP0#	U2	Common Clock	Input/Output
AP1#	U3	Common Clock	Input/Output
BCLK0	F28	Clock	Input
BCLK1	G28	Clock	Input
BINIT#	AD3	Common Clock	Input/Output
BNR#	C2	Common Clock	Input/Output
BOOTSELECT	Y1	Power/Other	Input
BPM0#	AJ2	Common Clock	Input/Output
BPM1#	AJ1	Common Clock	Input/Output
BPM2#	AD2	Common Clock	Input/Output
BPM3#	AG2	Common Clock	Input/Output
BPM4#	AF2	Common Clock	Input/Output
BPM5#	AG3	Common Clock	Input/Output
BPRI#	G8	Common Clock	Input
BR0#	F3	Common Clock	Input/Output
BSEL0	G29	Power/Other	Output
BSEL1	H30	Power/Other	Output
BSEL2	G30	Power/Other	Output
COMP0	A13	Power/Other	Input
COMP1	T1	Power/Other	Input
COMP2	G2	Power/Other	Input
COMP3	R1	Power/Other	Input
D0#	B4	Source Synch	Input/Output
D1#	C5	Source Synch	Input/Output
D10#	B10	Source Synch	Input/Output
D11#	C11	Source Synch	Input/Output
D12#	D8	Source Synch	Input/Output
D13#	B12	Source Synch	Input/Output
D14#	C12	Source Synch	Input/Output
D15#	D11	Source Synch	Input/Output
D16#	G9	Source Synch	Input/Output
D17#	F8	Source Synch	Input/Output
D18#	F9	Source Synch	Input/Output
D19#	E9	Source Synch	Input/Output
D2#	A4	Source Synch	Input/Output
D20#	D7	Source Synch	Input/Output
D21#	E10	Source Synch	Input/Output
D22#	D10	Source Synch	Input/Output
D23#	F11	Source Synch	Input/Output
D24#	F12	Source Synch	Input/Output
D25#	D13	Source Synch	Input/Output
D26#	E13	Source Synch	Input/Output
D27#	G13	Source Synch	Input/Output
D28#	F14	Source Synch	Input/Output
D29#	G14	Source Synch	Input/Output
D3#	C6	Source Synch	Input/Output

Land Name	Land #	Signal Buffer Type	Direction
D30#	F15	Source Synch	Input/Output
D31#	G15	Source Synch	Input/Output
D32#	G16	Source Synch	Input/Output
D33#	E15	Source Synch	Input/Output
D34#	E16	Source Synch	Input/Output
D35#	G18	Source Synch	Input/Output
D36#	G17	Source Synch	Input/Output
D37#	F17	Source Synch	Input/Output
D38#	F18	Source Synch	Input/Output
D39#	E18	Source Synch	Input/Output
D4#	A5	Source Synch	Input/Output
D40#	E19	Source Synch	Input/Output
D41#	F20	Source Synch	Input/Output
D42#	E21	Source Synch	Input/Output
D43#	F21	Source Synch	Input/Output
D44#	G21	Source Synch	Input/Output
D45#	E22	Source Synch	Input/Output
D46#	D22	Source Synch	Input/Output
D47#	G22	Source Synch	Input/Output
D48#	D20	Source Synch	Input/Output
D49#	D17	Source Synch	Input/Output
D5#	B6	Source Synch	Input/Output
D50#	A14	Source Synch	Input/Output
D51#	C15	Source Synch	Input/Output
D52#	C14	Source Synch	Input/Output
D53#	B15	Source Synch	Input/Output
D54#	C18	Source Synch	Input/Output
D55#	B16	Source Synch	Input/Output
D56#	A17	Source Synch	Input/Output
D57#	B18	Source Synch	Input/Output
D58#	C21	Source Synch	Input/Output
D59#	B21	Source Synch	Input/Output
D6#	B7	Source Synch	Input/Output
D60#	B19	Source Synch	Input/Output
D61#	A19	Source Synch	Input/Output
D62#	A22	Source Synch	Input/Output
D63#	B22	Source Synch	Input/Output
D7#	A7	Source Synch	Input/Output
D8#	A10	Source Synch	Input/Output
D9#	A11	Source Synch	Input/Output
DBI0#	A8	Source Synch	Input/Output
DBI1#	G11	Source Synch	Input/Output
DBI2#	D19	Source Synch	Input/Output
DBI3#	C20	Source Synch	Input/Output
DBR#	AC2	Power/Other	Output
DBSY#	B2	Common Clock	Input/Output

Land Name	Land #	Signal Buffer Type	Direction
DEFER#	G7	Common Clock	Input
DP0#	J16	Common Clock	Input/Output
DP1#	H15	Common Clock	Input/Output
DP2#	H16	Common Clock	Input/Output
DP3#	J17	Common Clock	Input/Output
DRDY#	C1	Common Clock	Input/Output
DSTBN0#	C8	Source Synch	Input/Output
DSTBN1#	G12	Source Synch	Input/Output
DSTBN2#	G20	Source Synch	Input/Output
DSTBN3#	A16	Source Synch	Input/Output
DSTBP0#	B9	Source Synch	Input/Output
DSTBP1#	E12	Source Synch	Input/Output
DSTBP2#	G19	Source Synch	Input/Output
DSTBP3#	C17	Source Synch	Input/Output
FC10	E24	Power/Other	Input
FC11	AM5	Power/Other	Output
FC12	AM7	Power/Other	Output
FC16	AN7	Power/Other	Output
FC17	Y3	Power/Other	Input
FC18	AE3	Power/Other	Input
FC3	J2	Power/Other	Input
FC4	T2	Power/Other	Input
FC5	F2	Common Clock	Input
FC7	G5	Source Synch	Output
FERR#/PBE#	R3	Asynch GTL+	Output
FORCEPR#	AK6	Asynch GTL+	Input
GTLREF_SEL	H29	Power/Other	Output
GTLREF0	H1	Power/Other	Input
GTLREF1	H2	Power/Other	Input
HIT#	D4	Common Clock	Input/Output
HITM#	E4	Common Clock	Input/Output
IERR#	AB2	Asynch GTL+	Output
IGNNE#	N2	Asynch GTL+	Input
IMPSEL	F6	Power/Other	Input
INIT#	P3	Asynch GTL+	Input
ITP_CLK0	AK3	TAP	Input
ITP_CLK1	AJ3	TAP	Input
LINT0	K1	Asynch GTL+	Input
LINT1	L1	Asynch GTL+	Input
LL_ID0	V2	Power/Other	Output
LL_ID1	AA2	Power/Other	Output
LOCK#	C3	Common Clock	Input/Output
MCERR#	AB3	Common Clock	Input/Output
MSID0	W1	Power/Other	Input
MSID1	V1	Power/Other	Input
PROCHOT#	AL2	Asynch GTL+	Output or

Land Name	Land #	Signal Buffer Type	Direction
			Input/Output
PWRGOOD	N1	Power/Other	Input
REQ0#	K4	Source Synch	Input/Output
REQ1#	J5	Source Synch	Input/Output
REQ2#	M6	Source Synch	Input/Output
REQ3#	K6	Source Synch	Input/Output
REQ4#	J6	Source Synch	Input/Output
RESERVED	A20		
RESERVED	AC4		
RESERVED	AE4		
RESERVED	AE6		
RESERVED	AH2		
RESERVED	C9		
RESERVED	D1		
RESERVED	D14		
RESERVED	D16		
RESERVED	E23		
RESERVED	E5		
RESERVED	E6		
RESERVED	E7		
RESERVED	F23		
RESERVED	F29		
RESERVED	G10		
RESERVED	B13		
RESERVED	J3		
RESERVED	N4		
RESERVED	N5		
RESERVED	P5		
RESERVED	G6		
RESET#	G23	Common Clock	Input
RS0#	B3	Common Clock	Input
RS1#	F5	Common Clock	Input
RS2#	A3	Common Clock	Input
RSP#	H4	Common Clock	Input
SKTOCC#	AE8	Power/Other	Output
SMI#	P2	Asynch GTL+	Input
STPCLK#	M3	Asynch GTL+	Input
TCK	AE1	TAP	Input
TDI	AD1	TAP	Input
TDO	AF1	TAP	Output
TESTHI0	F26	Power/Other	Input
TESTHI1	W3	Power/Other	Input
TESTHI10	H5	Power/Other	Input
TESTHI11	P1	Power/Other	Input
TESTHI12	W2	Power/Other	Input
TESTHI13	L2	Asynch GTL+	Input

Land Name	Land #	Signal Buffer Type	Direction
TESTHI2	F25	Power/Other	Input
TESTHI3	G25	Power/Other	Input
TESTHI4	G27	Power/Other	Input
TESTHI5	G26	Power/Other	Input
TESTHI6	G24	Power/Other	Input
TESTHI7	F24	Power/Other	Input
TESTHI8	G3	Power/Other	Input
TESTHI9	G4	Power/Other	Input
THERMDA	AL1	Power/Other	
THERMDC	AK1	Power/Other	
THERMTRIP#	M2	Asynch GTL+	Output
TMS	AC1	TAP	Input
TRDY#	E3	Common Clock	Input
TRST#	AG1	TAP	Input
VCC	AA8	Power/Other	
VCC	AB8	Power/Other	
VCC	AC23	Power/Other	
VCC	AC24	Power/Other	
VCC	AC25	Power/Other	
VCC	AC26	Power/Other	
VCC	AC27	Power/Other	
VCC	AC28	Power/Other	
VCC	AC29	Power/Other	
VCC	AC30	Power/Other	
VCC	AC8	Power/Other	
VCC	AD23	Power/Other	
VCC	AD24	Power/Other	
VCC	AD25	Power/Other	
VCC	AD26	Power/Other	
VCC	AD27	Power/Other	
VCC	AD28	Power/Other	
VCC	AD29	Power/Other	
VCC	AD30	Power/Other	
VCC	AD8	Power/Other	
VCC	AE11	Power/Other	
VCC	AE12	Power/Other	
VCC	AE14	Power/Other	
VCC	AE15	Power/Other	
VCC	AE18	Power/Other	
VCC	AE19	Power/Other	
VCC	AE21	Power/Other	
VCC	AE22	Power/Other	
VCC	AE23	Power/Other	
VCC	AE9	Power/Other	
VCC	AF11	Power/Other	
VCC	AF12	Power/Other	

Land Name	Land #	Signal Buffer Type	Direction
VCC	AF14	Power/Other	
VCC	AF15	Power/Other	
VCC	AF18	Power/Other	
VCC	AF19	Power/Other	
VCC	AF21	Power/Other	
VCC	AF22	Power/Other	
VCC	AF8	Power/Other	
VCC	AF9	Power/Other	
VCC	AG11	Power/Other	
VCC	AG12	Power/Other	
VCC	AG14	Power/Other	
VCC	AG15	Power/Other	
VCC	AG18	Power/Other	
VCC	AG19	Power/Other	
VCC	AG21	Power/Other	
VCC	AG22	Power/Other	
VCC	AG25	Power/Other	
VCC	AG26	Power/Other	
VCC	AG27	Power/Other	
VCC	AG28	Power/Other	
VCC	AG29	Power/Other	
VCC	AG30	Power/Other	
VCC	AG8	Power/Other	
VCC	AG9	Power/Other	
VCC	AH11	Power/Other	
VCC	AH12	Power/Other	
VCC	AH14	Power/Other	
VCC	AH15	Power/Other	
VCC	AH18	Power/Other	
VCC	AH19	Power/Other	
VCC	AH21	Power/Other	
VCC	AH22	Power/Other	
VCC	AH25	Power/Other	
VCC	AH26	Power/Other	
VCC	AH27	Power/Other	
VCC	AH28	Power/Other	
VCC	AH29	Power/Other	
VCC	AH30	Power/Other	
VCC	AH8	Power/Other	
VCC	AH9	Power/Other	
VCC	AJ11	Power/Other	
VCC	AJ12	Power/Other	
VCC	AJ14	Power/Other	
VCC	AJ15	Power/Other	
VCC	AJ18	Power/Other	
VCC	AJ19	Power/Other	

Land Name	Land #	Signal Buffer Type	Direction
VCC	AJ21	Power/Other	
VCC	AJ22	Power/Other	
VCC	AJ25	Power/Other	
VCC	AJ26	Power/Other	
VCC	AJ8	Power/Other	
VCC	AJ9	Power/Other	
VCC	AK11	Power/Other	
VCC	AK12	Power/Other	
VCC	AK14	Power/Other	
VCC	AK15	Power/Other	
VCC	AK18	Power/Other	
VCC	AK19	Power/Other	
VCC	AK21	Power/Other	
VCC	AK22	Power/Other	
VCC	AK25	Power/Other	
VCC	AK26	Power/Other	
VCC	AK8	Power/Other	
VCC	AK9	Power/Other	
VCC	AL11	Power/Other	
VCC	AL12	Power/Other	
VCC	AL14	Power/Other	
VCC	AL15	Power/Other	
VCC	AL18	Power/Other	
VCC	AL19	Power/Other	
VCC	AL21	Power/Other	
VCC	AL22	Power/Other	
VCC	AL25	Power/Other	
VCC	AL26	Power/Other	
VCC	AL29	Power/Other	
VCC	AL30	Power/Other	
VCC	AL8	Power/Other	
VCC	AL9	Power/Other	
VCC	AM11	Power/Other	
VCC	AM12	Power/Other	
VCC	AM14	Power/Other	
VCC	AM15	Power/Other	
VCC	AM18	Power/Other	
VCC	AM19	Power/Other	
VCC	AM21	Power/Other	
VCC	AM22	Power/Other	
VCC	AM25	Power/Other	
VCC	AM26	Power/Other	
VCC	AM29	Power/Other	
VCC	AM30	Power/Other	
VCC	AM8	Power/Other	
VCC	AM9	Power/Other	

Land Name	Land #	Signal Buffer Type	Direction
VCC	AN11	Power/Other	
VCC	AN12	Power/Other	
VCC	AN14	Power/Other	
VCC	AN15	Power/Other	
VCC	AN18	Power/Other	
VCC	AN19	Power/Other	
VCC	AN21	Power/Other	
VCC	AN22	Power/Other	
VCC	AN25	Power/Other	
VCC	AN26	Power/Other	
VCC	AN29	Power/Other	
VCC	AN30	Power/Other	
VCC	AN8	Power/Other	
VCC	AN9	Power/Other	
VCC	J10	Power/Other	
VCC	J11	Power/Other	
VCC	J12	Power/Other	
VCC	J13	Power/Other	
VCC	J14	Power/Other	
VCC	J15	Power/Other	
VCC	J18	Power/Other	
VCC	J19	Power/Other	
VCC	J20	Power/Other	
VCC	J21	Power/Other	
VCC	J22	Power/Other	
VCC	J23	Power/Other	
VCC	J24	Power/Other	
VCC	J25	Power/Other	
VCC	J26	Power/Other	
VCC	J27	Power/Other	
VCC	J28	Power/Other	
VCC	J29	Power/Other	
VCC	J30	Power/Other	
VCC	J8	Power/Other	
VCC	J9	Power/Other	
VCC	K23	Power/Other	
VCC	K24	Power/Other	
VCC	K25	Power/Other	
VCC	K26	Power/Other	
VCC	K27	Power/Other	
VCC	K28	Power/Other	
VCC	K29	Power/Other	
VCC	K30	Power/Other	
VCC	K8	Power/Other	
VCC	L8	Power/Other	
VCC	M23	Power/Other	

Land Name	Land #	Signal Buffer Type	Direction
VCC	M24	Power/Other	
VCC	M25	Power/Other	
VCC	M26	Power/Other	
VCC	M27	Power/Other	
VCC	M28	Power/Other	
VCC	M29	Power/Other	
VCC	M30	Power/Other	
VCC	M8	Power/Other	
VCC	N23	Power/Other	
VCC	N24	Power/Other	
VCC	N25	Power/Other	
VCC	N26	Power/Other	
VCC	N27	Power/Other	
VCC	N28	Power/Other	
VCC	N29	Power/Other	
VCC	N30	Power/Other	
VCC	N8	Power/Other	
VCC	P8	Power/Other	
VCC	R8	Power/Other	
VCC	T23	Power/Other	
VCC	T24	Power/Other	
VCC	T25	Power/Other	
VCC	T26	Power/Other	
VCC	T27	Power/Other	
VCC	T28	Power/Other	
VCC	T29	Power/Other	
VCC	T30	Power/Other	
VCC	T8	Power/Other	
VCC	U23	Power/Other	
VCC	U24	Power/Other	
VCC	U25	Power/Other	
VCC	U26	Power/Other	
VCC	U27	Power/Other	
VCC	U28	Power/Other	
VCC	U29	Power/Other	
VCC	U30	Power/Other	
VCC	U8	Power/Other	
VCC	V8	Power/Other	
VCC	W23	Power/Other	
VCC	W24	Power/Other	
VCC	W25	Power/Other	
VCC	W26	Power/Other	
VCC	W27	Power/Other	
VCC	W28	Power/Other	
VCC	W29	Power/Other	
VCC	W30	Power/Other	

Land Name	Land #	Signal Buffer Type	Direction
VCC	W8	Power/Other	
VCC	Y23	Power/Other	
VCC	Y24	Power/Other	
VCC	Y25	Power/Other	
VCC	Y26	Power/Other	
VCC	Y27	Power/Other	
VCC	Y28	Power/Other	
VCC	Y29	Power/Other	
VCC	Y30	Power/Other	
VCC	Y8	Power/Other	
VCC_MB_REGULATION	AN5	Power/Other	Output
VCC_SENSE	AN3	Power/Other	Output
VCCA	A23	Power/Other	
VCCIOPLL	C23	Power/Other	
VCCPLL	D23	Power/Other	Input
VID0	AM2	Power/Other	Output
VID1	AL5	Power/Other	Output
VID2	AM3	Power/Other	Output
VID3	AL6	Power/Other	Output
VID4	AK4	Power/Other	Output
VID5	AL4	Power/Other	Output
VSS	A12	Power/Other	
VSS	A15	Power/Other	
VSS	A18	Power/Other	
VSS	A2	Power/Other	
VSS	A21	Power/Other	
VSS	A24	Power/Other	
VSS	A6	Power/Other	
VSS	A9	Power/Other	
VSS	AA23	Power/Other	
VSS	AA24	Power/Other	
VSS	AA25	Power/Other	
VSS	AA26	Power/Other	
VSS	AA27	Power/Other	
VSS	AA28	Power/Other	
VSS	AA29	Power/Other	
VSS	AA3	Power/Other	
VSS	AA30	Power/Other	
VSS	AA6	Power/Other	
VSS	AA7	Power/Other	
VSS	AB1	Power/Other	
VSS	AB23	Power/Other	
VSS	AB24	Power/Other	
VSS	AB25	Power/Other	
VSS	AB26	Power/Other	

Land Name	Land #	Signal Buffer Type	Direction
VSS	AB27	Power/Other	
VSS	AB28	Power/Other	
VSS	AB29	Power/Other	
VSS	AB30	Power/Other	
VSS	AB7	Power/Other	
VSS	AC3	Power/Other	
VSS	AC6	Power/Other	
VSS	AC7	Power/Other	
VSS	AD4	Power/Other	
VSS	AD7	Power/Other	
VSS	AE10	Power/Other	
VSS	AE13	Power/Other	
VSS	AE16	Power/Other	
VSS	AE17	Power/Other	
VSS	AE2	Power/Other	
VSS	AE20	Power/Other	
VSS	AE24	Power/Other	
VSS	AE25	Power/Other	
VSS	AE26	Power/Other	
VSS	AE27	Power/Other	
VSS	AE28	Power/Other	
VSS	AE29	Power/Other	
VSS	AE30	Power/Other	
VSS	AE5	Power/Other	
VSS	AE7	Power/Other	
VSS	AF10	Power/Other	
VSS	AF13	Power/Other	
VSS	AF16	Power/Other	
VSS	AF17	Power/Other	
VSS	AF20	Power/Other	
VSS	AF23	Power/Other	
VSS	AF24	Power/Other	
VSS	AF25	Power/Other	
VSS	AF26	Power/Other	
VSS	AF27	Power/Other	
VSS	AF28	Power/Other	
VSS	AF29	Power/Other	
VSS	AF3	Power/Other	
VSS	AF30	Power/Other	
VSS	AF6	Power/Other	
VSS	AF7	Power/Other	
VSS	AG10	Power/Other	
VSS	AG13	Power/Other	
VSS	AG16	Power/Other	
VSS	AG17	Power/Other	
VSS	AG20	Power/Other	

Land Name	Land #	Signal Buffer Type	Direction
VSS	AG23	Power/Other	
VSS	AG24	Power/Other	
VSS	AG7	Power/Other	
VSS	AH1	Power/Other	
VSS	AH10	Power/Other	
VSS	AH13	Power/Other	
VSS	AH16	Power/Other	
VSS	AH17	Power/Other	
VSS	AH20	Power/Other	
VSS	AH23	Power/Other	
VSS	AH24	Power/Other	
VSS	AH3	Power/Other	
VSS	AH6	Power/Other	
VSS	AH7	Power/Other	
VSS	AJ10	Power/Other	
VSS	AJ13	Power/Other	
VSS	AJ16	Power/Other	
VSS	AJ17	Power/Other	
VSS	AJ20	Power/Other	
VSS	AJ23	Power/Other	
VSS	AJ24	Power/Other	
VSS	AJ27	Power/Other	
VSS	AJ28	Power/Other	
VSS	AJ29	Power/Other	
VSS	AJ30	Power/Other	
VSS	AJ4	Power/Other	
VSS	AJ7	Power/Other	
VSS	AK10	Power/Other	
VSS	AK13	Power/Other	
VSS	AK16	Power/Other	
VSS	AK17	Power/Other	
VSS	AK2	Power/Other	
VSS	AK20	Power/Other	
VSS	AK23	Power/Other	
VSS	AK24	Power/Other	
VSS	AK27	Power/Other	
VSS	AK28	Power/Other	
VSS	AK29	Power/Other	
VSS	AK30	Power/Other	
VSS	AK5	Power/Other	
VSS	AK7	Power/Other	
VSS	AL10	Power/Other	
VSS	AL13	Power/Other	
VSS	AL16	Power/Other	
VSS	AL17	Power/Other	
VSS	AL20	Power/Other	

Land Name	Land #	Signal Buffer Type	Direction
VSS	AL23	Power/Other	
VSS	AL24	Power/Other	
VSS	AL27	Power/Other	
VSS	AL28	Power/Other	
VSS	AL3	Power/Other	
VSS	AL7	Power/Other	
VSS	AM1	Power/Other	
VSS	AM10	Power/Other	
VSS	AM13	Power/Other	
VSS	AM16	Power/Other	
VSS	AM17	Power/Other	
VSS	AM20	Power/Other	
VSS	AM23	Power/Other	
VSS	AM24	Power/Other	
VSS	AM27	Power/Other	
VSS	AM28	Power/Other	
VSS	AM4	Power/Other	
VSS	AN1	Power/Other	
VSS	AN10	Power/Other	
VSS	AN13	Power/Other	
VSS	AN16	Power/Other	
VSS	AN17	Power/Other	
VSS	AN2	Power/Other	
VSS	AN20	Power/Other	
VSS	AN23	Power/Other	
VSS	AN24	Power/Other	
VSS	AN27	Power/Other	
VSS	AN28	Power/Other	
VSS	B1	Power/Other	
VSS	B11	Power/Other	
VSS	B14	Power/Other	
VSS	B17	Power/Other	
VSS	B20	Power/Other	
VSS	B24	Power/Other	
VSS	B5	Power/Other	
VSS	B8	Power/Other	
VSS	C10	Power/Other	
VSS	C13	Power/Other	
VSS	C16	Power/Other	
VSS	C19	Power/Other	
VSS	C22	Power/Other	
VSS	C24	Power/Other	
VSS	C4	Power/Other	
VSS	C7	Power/Other	
VSS	D12	Power/Other	
VSS	D15	Power/Other	

Land Name	Land #	Signal Buffer Type	Direction
VSS	D18	Power/Other	
VSS	D21	Power/Other	
VSS	D24	Power/Other	
VSS	D3	Power/Other	
VSS	D5	Power/Other	
VSS	D6	Power/Other	
VSS	D9	Power/Other	
VSS	E11	Power/Other	
VSS	E14	Power/Other	
VSS	E17	Power/Other	
VSS	E2	Power/Other	
VSS	E20	Power/Other	
VSS	E25	Power/Other	
VSS	E26	Power/Other	
VSS	E27	Power/Other	
VSS	E28	Power/Other	
VSS	E29	Power/Other	
VSS	E8	Power/Other	
VSS	F10	Power/Other	
VSS	F13	Power/Other	
VSS	F16	Power/Other	
VSS	F19	Power/Other	
VSS	F22	Power/Other	
VSS	F4	Power/Other	
VSS	F7	Power/Other	
VSS	G1	Power/Other	
VSS	H10	Power/Other	
VSS	H11	Power/Other	
VSS	H12	Power/Other	
VSS	H13	Power/Other	
VSS	H14	Power/Other	
VSS	H17	Power/Other	
VSS	H18	Power/Other	
VSS	H19	Power/Other	
VSS	H20	Power/Other	
VSS	H21	Power/Other	
VSS	H22	Power/Other	
VSS	H23	Power/Other	
VSS	H24	Power/Other	
VSS	H25	Power/Other	
VSS	H26	Power/Other	
VSS	H27	Power/Other	
VSS	H28	Power/Other	
VSS	H3	Power/Other	
VSS	H6	Power/Other	
VSS	H7	Power/Other	

Land Name	Land #	Signal Buffer Type	Direction
VSS	H8	Power/Other	
VSS	H9	Power/Other	
VSS	J4	Power/Other	
VSS	J7	Power/Other	
VSS	K2	Power/Other	
VSS	K5	Power/Other	
VSS	K7	Power/Other	
VSS	L23	Power/Other	
VSS	L24	Power/Other	
VSS	L25	Power/Other	
VSS	L26	Power/Other	
VSS	L27	Power/Other	
VSS	L28	Power/Other	
VSS	L29	Power/Other	
VSS	L3	Power/Other	
VSS	L30	Power/Other	
VSS	L6	Power/Other	
VSS	L7	Power/Other	
VSS	M1	Power/Other	
VSS	M7	Power/Other	
VSS	N3	Power/Other	
VSS	N6	Power/Other	
VSS	N7	Power/Other	
VSS	P23	Power/Other	
VSS	P24	Power/Other	
VSS	P25	Power/Other	
VSS	P26	Power/Other	
VSS	P27	Power/Other	
VSS	P28	Power/Other	
VSS	P29	Power/Other	
VSS	P30	Power/Other	
VSS	P4	Power/Other	
VSS	P7	Power/Other	
VSS	R2	Power/Other	
VSS	R23	Power/Other	
VSS	R24	Power/Other	
VSS	R25	Power/Other	
VSS	R26	Power/Other	
VSS	R27	Power/Other	
VSS	R28	Power/Other	
VSS	R29	Power/Other	
VSS	R30	Power/Other	
VSS	R5	Power/Other	
VSS	R7	Power/Other	
VSS	T3	Power/Other	
VSS	T6	Power/Other	

Land Name	Land #	Signal Buffer Type	Direction
VSS	T7	Power/Other	
VSS	U1	Power/Other	
VSS	U7	Power/Other	
VSS	V23	Power/Other	
VSS	V24	Power/Other	
VSS	V25	Power/Other	
VSS	V26	Power/Other	
VSS	V27	Power/Other	
VSS	V28	Power/Other	
VSS	V29	Power/Other	
VSS	V3	Power/Other	
VSS	V30	Power/Other	
VSS	V6	Power/Other	
VSS	V7	Power/Other	
VSS	W4	Power/Other	
VSS	W7	Power/Other	
VSS	Y2	Power/Other	
VSS	Y5	Power/Other	
VSS	Y7	Power/Other	
VSS_MB_REGULATION	AN6	Power/Other	Output
VSS_SENSE	AN4	Power/Other	Output
VSSA	B23	Power/Other	
VTT	A25	Power/Other	
VTT	A26	Power/Other	
VTT	A27	Power/Other	
VTT	A28	Power/Other	
VTT	A29	Power/Other	
VTT	A30	Power/Other	
VTT	B25	Power/Other	
VTT	B26	Power/Other	
VTT	B27	Power/Other	
VTT	B28	Power/Other	
VTT	B29	Power/Other	
VTT	B30	Power/Other	
VTT	C25	Power/Other	
VTT	C26	Power/Other	
VTT	C27	Power/Other	
VTT	C28	Power/Other	
VTT	C29	Power/Other	
VTT	C30	Power/Other	
VTT	D25	Power/Other	
VTT	D26	Power/Other	
VTT	D27	Power/Other	
VTT	D28	Power/Other	
VTT	D29	Power/Other	
VTT	D30	Power/Other	

Land Name	Land #	Signal Buffer Type	Direction
VTT_OUT_LEFT	J1	Power/Other	Output
VTT_OUT_RIGHT	AA1	Power/Other	Output
VTT_SEL	F27	Power/Other	Output
VTTPWRGD	AM6	Power/Other	Input