CK97 Clock Synthesizer Design Guidelines

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1. Introduction

This document is designed to provide the industry with the technical specifications required by clock drivers and synthesizers for present and future Intel Architecture platforms. Split power supply signaling to provide 2.5V and 3.3V clocks is a stated requirement for these products. Additionally, the clocking solution must provide processor and chipset clock frequencies of 66.6 Mhz (15.00 nS period) and 100 Mhz (10.00 nS period.) Certain applications may also require processor and chipset speeds of 60.00 Mhz (16.67 nS period.)

This document is intended to aid computer OEMs in defining and using the clock synthesizer components for all desktop system level clocking requirements.

The 3.3V power supply is used to power a portion of the I/O and the core, and 2.5V is used to power the remaining outputs. Because the two power supplies are independent, and because current PC technology does not control the power sequencing for turning on or turning off the system, latch-up and potentially damaging conditions can exist during these power sequencing phases. **Your design is required to operate properly and make no requirement of the system to sequence the power supplies.**

The 2.5V signaling specification follows the JEDEC standard 8-X. **It should be noted that the preferred implementation of the 2.5V supply will be a 2.5V ±5% voltage regulator. Processor and chipset clock voltages above the specified +5% variation are not allowed.** The 3.3V signaling specification follows the JEDEC standard for LVTTL signaling. The 3.3V power delivery specification follows the JEDEC standard range 3.3V ±5%.

These guidelined provide a baseline of development for Intel Architecture processor based platform clock driver requirements. It is not the only implementation that can be developed; however, this baseline functionality is required for most desktop platforms.

1.1 Clock Synthesizer Overview

Clock synthesizers are expected to source multiple clock types: e.g., Host clock, PCI clock, system clock, Super I/O and others as defined by system requirements. These guidelines deal with the CPU clock, other Host bus clocks, SDRAM (DIMM) clocks, PCI clocks, IOAPIC clocks, 48MHz, Serial Bus Clock, and copies of the reference clock. These products will not be required to generate the clock for the Accelerated Graphics Port (AGP) devices. The major technological challenge is seen to be the transition to 100 Mhz as a Host bus frequency.

There are no references to the number of clocks or the types of clocks any given clock driver chip will supply in the main body of the document. Examples of clock synthesizer designs are located in the appendix. The number of clocks and the types of clocks, package type and load conditions are also shown.

Timing and electrical requirements for all of the above mentioned clocks are provided. Information about the PCI CLK reflects the requirements as specified in the PCI specification Chapter 4. Examples of routing topologies, loading and signal quality specifications are outlined in Section 5.

1.2 Audio Codec 97 (AC97) support

Information on providing Audio clocks to support Audio Codec 97 (AC97) is defined in the latest revision of the Audio Codec specification. The Intel website address is listed in section 6.

1.3 Applicable Documents

The latest revision of the following are used as reference documents:

JEDEC Standard No. 8-1A, Interface Standard for 3.3±0.3 V Power Supply & Digital Integrated Circuits.
JEDEC Standard No. 8-X, 2.5V±0.2V (normal range), and 1.8V to 2.7V (wide range) Power supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuit.
PCI Specification 2.1
IBIS Modeling Specification
Audio Codec 97 Specification (AC97)
Philips I^2C Peripherals Data handbook IC12 1996

Other Intel Clock Design Guidelines:
CK25 Intel Clock Driver Design Guidelines for 440FX chipset support
CKDM66 Clock Driver Design Guidelines
Mixed Voltage Clock Synthesizer/Driver Design Guidelines with SDRAM support

See Section 6 on how to obtain copies of PCI, AC97 and IBIS specifications.

1.4 Drive Specification

The primary motivation for this document is to address the issues associated with split I/O voltage and the effects of it on system power delivery, signaling, timing and test. The signaling, timing, and test characteristics change with the different supply voltages and need to be thoroughly understood and simulated for optimal system performance.

The clock driver output buffers are specified in terms of their AC switching characteristics and their DC drive characteristics as such, the primary electrical parameters are the voltage to current relationship (V/I), the rise and fall time (Trise/Tfall) of the driver through its active switching range, and critical timing parameters.

2. Electrical Requirements

This section details the electrical parameters for two types of 2.5V clock output buffers, multiple types of 3.3V clock output buffers and a 5.0V compatible 3.3V PCI clock driver output buffer. The different types of 2.5V and 3.3V drivers are needed to compensate for corresponding board layout topologies.

Due to the low voltage (<3.0V) required by the CPU, TTL signaling levels are no longer useable. A signaling level to support 2.5V is being used for that portion of the design. The JEDEC standard called "2.5V±0.2V (normal range), and 1.8V to 2.7V (wide range) Power Supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuit", hereafter referred to as 2.5V signaling and 2.5V supply is being used. The 3.3V clocking requirements still support the TTL-level compatible requirements and will be called by their appropriate name, LVTTL, even though they are TTL signaling levels.

A clock driver designed to operate in the 2.5V Pentium® processor and Pentium II processor signaling environment will not necessarily operate correctly in the 3.3V LVTTL or the 5.0V PCI I/O bus signaling environment. Great care must be taken in this design environment to properly support the extremely tight timing requirements between clocks.

The clock driver for all clocks must generate monotonic edges through the input threshold regions as specified for each signaling environment. Many conditions exist in the design of the clock driver and the system that can affect the monotonic operation of the clock driver. Power supply noise, pin inductance and capacitance, ratio of clock signals to Vddq and Vss pins (SSO), and routing topology will affect the monotonicity of these clocks. The electrical requirements outlined here ensure components connect directly together without any external buffers or other "glue" logic. Series terminating resistors may be required to keep noise within limits on strong drivers under lightly loaded conditions. Components should be designed to operate within the "commercial" range of environmental parameters. However, this does not preclude the option of other operating environments at the vendor's and OEM's discretion.

Clock driver output buffers are specified in terms of their V/I curves and Trise/Tfall times. Limits on acceptable V/I curves provide for a maximum output impedance that can achieve acceptable timing in typical configurations, and for a minimum output impedance that keeps the reflected wave within reasonable bounds for signal quality. It is important to understand that drive strength and layout topology go hand in hand. Point-to-Point or multiple stubs at the receiver end will work with a weaker driver, whereas a route that splits at the driver requires a stronger buffer. The signal quality problems of a strong driver under light loads can be negated somewhat with a series termination resistor placed as close to the driver as possible. See Section 0 for more detail.

Examples of possible clock driver designs are contained in the appendices. These are not the only solutions that can be achieved, but are a good starting point to design a component to meet specific design requirements.

Due to the mixed power supplies now required for proper system operation, it is very important to understand that specific power supply sequencing is not supported. The clock synthesizer CAN'T force power sequencing requirements in the system.

2.1 DC Specifications (Clock Driver)

DC parameters must be sustainable under steady state (DC) conditions.

Table 2-1 Absolute Maximum DC Power Supply

Symbol	Parameter	Min.	Max.	Units	Notes
V_{DD3}	3.3V Core Supply Voltage	-0.5	4.6	V	
V_{DDQ2}	2.5V I/O Supply Voltage	-0.5	3.6	V	
V_{DDQ3}	3.3V I/O Supply Voltage	-0.5	4.6	V	
Ts	Storage Temperature	-65	150	°C	

Table 2-2 Absolute Maximum DC I/O

Symbol	Parameter	Min.	Max.	Units	Notes
V_{ih3}	3.3V Input High Voltage	-0.5	4.6	V	1
V_{il3}	3.3V Input Low Voltage	–0.5		V	
ESD prot.	Input ESD protection	2		kV	2

Notes:
1. Maximum Vih is not to exceed maximum VDD.
2. Human body model.

Table 2-3 DC Operating Requirements

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{DD3}	3.3V Core Supply Voltage	3.3V ±5%	3.135	3.465	V	4
V_{DDQ3}	3.3V I/O Supply Voltage	3.3V ±5%	3.135	3.465	V	4
V_{DDQ2}	2.5V I/O Supply Voltage	2.5V ±5%	2.375	2.625	V	4
$V_{DD\ 3}$= 3.3V±5%						
V_{ih3}	3.3V Input High Voltage	VDD3	2.0	V_{DD}+0.3	V	7
V_{il3}	3.3V Input Low Voltage		V_{SS}-0.3	0.8	V	7
I_{il}	Input Leakage Current	$0 < V_{in} < V_{DDQ3}$	-5	+5	µA	3, 7
V_{DDQ2} = 2.5V±5%						
V_{oh2}	2.5V Output High Voltage	Ioh = -1 mA	2.0		V	1
V_{ol2}	2.5V Output Low Voltage	Iol = 1 mA		0.4	V	1
V_{DDQ3}= 3.3V±5%						
V_{oh3}	3.3V Output High Voltage	Ioh = -1 mA	2.4		V	1
V_{ol3}	3.3V Output Low Voltage	Iol = 1 mA		0.4	V	1
V_{DDQ3}= 3.3V±5%						
V_{poh}	PCI Bus Output High Voltage	Ioh = -1 mA	2.4		V	1
V_{pol}	PCI Bus Output Low Voltage	Iol = 1 mA		0.55	V	1, 5
C_{in}	Input Pin Capacitance			5	pF	2
C_{xtal}	Xtal Pin Capacitance	1 MHz	13.5	22.5	pF	6
Cout	Output Pin Capacitance			6	pF	2
L_{pin}	Pin Inductance			7	nH	2
Ta	Ambient Temperature	No Airflow	0	70	°C	

Notes:

1. Signal edge is required to be monotonic when transitioning through this region.
2. This is a recommendation, not an absolute requirement as the package size and type are not being specified. The actual value should be provided with the component data sheet.
3. Input Leakage Current does not include inputs with Pull-Up or Pull-down resistors. Inputs with resistors should state current requirements.
4. No power sequencing is implied or allowed to be required in the system.
5. Conforms to 5V PCI Signaling specification.
6. As seen by the crystal. Device is intended to be used with a 17-20pF AT crystal. See next section for more details.
7. All inputs referenced to 3.3V power supply.

Load Capacitance As Seen By External Crystal:

Earlier clock definitions do not specify a target load capacitance for the clock synthesizer as seen by the crystal. Most clock vendors targeted 12-13 pF due to historical reasons, but few vendors specified the variation in their datasheets. However, the common crystals used today are in the 17-20 pF range. This requires the addition of two external capacitors for frequency compensation.

To reduce the ambiguity with this issue, we require that the clock driver load capacitance (as seen by the crystal, **not the capacitance of the individual XTAL_IN and XTAL_OUT pins**) be targeted **at 18pF ±- 25%.** This specification includes the clock driver component only and does not include any capacitance associated with board vias and traces.

Doing this:

- Directs vendors to design for the same target load capacitance.
- Requires testing/guarantee by design of the variation.
- May eliminate the external compensation capacitors if the frequency variation can be tolerated.

2.2 Buffer Specifications: 2.5 Volt, 3.3 Volt and PCI Clocks

The V/I curves, and Trise/Tfall specifications are targeted at achieving acceptable switching behavior under the load conditions as described in section 0 of this specification. Pull-up and pull-down sides for each of the buffers have separate V/I curves which are provided in the following sections. The DC drive curve specifies steady state conditions that must be maintained, but does not indicate real output drive strength.

AC parameters must be guaranteed under transient switching (AC) conditions. The sign on all current parameters (direction of current flow) is referenced to a ground inside the component; i.e. positive currents flow into the component while negative currents flow out of the component.

Buffer Name	VCC Range (V)	Impedance (Ohms)	Buffer Type
CPU	2.375 - 2.625	13.5 - 45	Type 1
IOAPIC	2.375 - 2.625	9 - 30	Type 2
48MHz, REF	3.135 - 3.465	20 - 60	Type 3
SDRAM	3.135 - 3.465	10 - 24	Type 4
PCI	3.135 - 3.465	12 - 55	Type 5

2.2.1 TYPE 1: CPU (2.5V) Buffer Characteristics

Table 2-4 TYPE 1: CPU Clock Buffer Operating Requirements

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
I_{ohmin}	Pull-Up Current	Vout = 1.0 V	-27			mA	1
I_{ohmax}	Pull-Up Current	V_{out} = 2.375 V			-27	mA	1
I_{olmin}	Pull-Down Current	V_{out} = 1.2 V	27			mA	1
I_{olmax}	Pull-Down Current	V_{out} = 0.3 V			30	mA	1
t_{rh}	2.5V Type 1 Output Rise Edge Rate	2.5V ±5% @ 0.4V - 2.0V	1/1		4/1	V/ns	2
t_{fh}	2.5V Type 1 Output Fall Edge Rate	2.5V ±5% @ 2.0V - 0.4V	1/1		4/1	V/ns	2

Notes:
1. Intended to approximate impedance curve below. Device should be checked against entire curve for characterization testing. Production testing is expected to be a subset of characterization testing.
2. Output rise and fall time. See Figure 4-1 CK100 Clock Waveform for calculation / measurement information.
3. Output rise and fall time must be guaranteed across VCC , process and temperature range.
4. Receiver logic thresholds are Vil=0.7 and Vih=1.7 Volts.
5. Ron 13.5-45 Ohm with a 29 Ohm nominal driver impedance.
6. Ron = Vout/Ioh, Vout/Iol measured at VCC/2.

Pull-Up			
Voltage (V)	I (mA) min	I (mA) typ	I (mA) max
0	-28	-61	-107
0.4	-28	-61	-107
0.6	-28	-61	-107
0.8	-28	-61	-107
1	-27	-60	-105
1.2	-26	-58	-101
1.4	-24	-53	-94
1.6	-21	-48	-85
1.8	-17	-40	-73
1.9	-15	-36	-67
2	-12	-31	-59
2.1	-9	-25	-51
2.2	-6	-20	-43
2.3	-3	-14	-34
2.375	0	-9	-27
2.5		0	-14
2.625			0

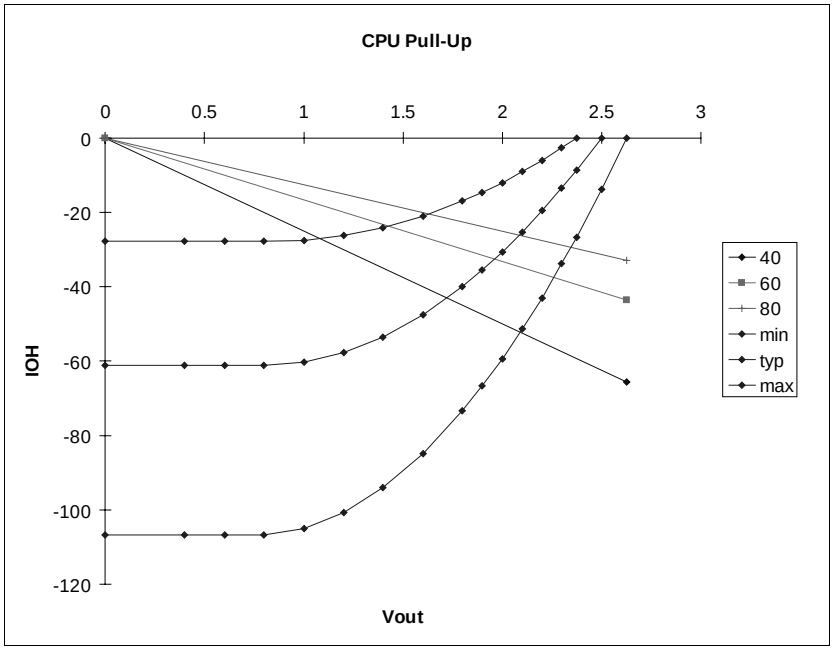


Figure 2-1 TYPE 1: CPU Clock Output Buffer Pull-Up Characteristics

Notes (Figure 2-1) **:**
1. Must meet the temperature and voltage range specified in Table 2-3 DC Operating Requirements
2. This drawing is not to scale. Comparisons should be made to the data provided in the table next this drawing and to Table 2-4 TYPE 1: CPU Clock Buffer Operating Requirements.

Pull-Down			
Voltage (V)	I (mA) min	I (mA) typ	I (mA) max
0	0	0	0
0.1	3	7	11
0.2	6	13	21
0.3	9	19	30
0.4	12	24	40
0.5	15	30	48
0.6	17	35	56
0.7	19	39	63
0.8	21	43	70
0.9	23	47	77
1	24	50	83
1.1	25	53	88
1.2	27	56	93
1.3	27	58	97
1.4	28	60	100
1.6	29	62	106
1.8	29	63	110
2	29	63	111
2.2	29	63	111
2.375	29	63	111
2.5		63	111
2.625			111

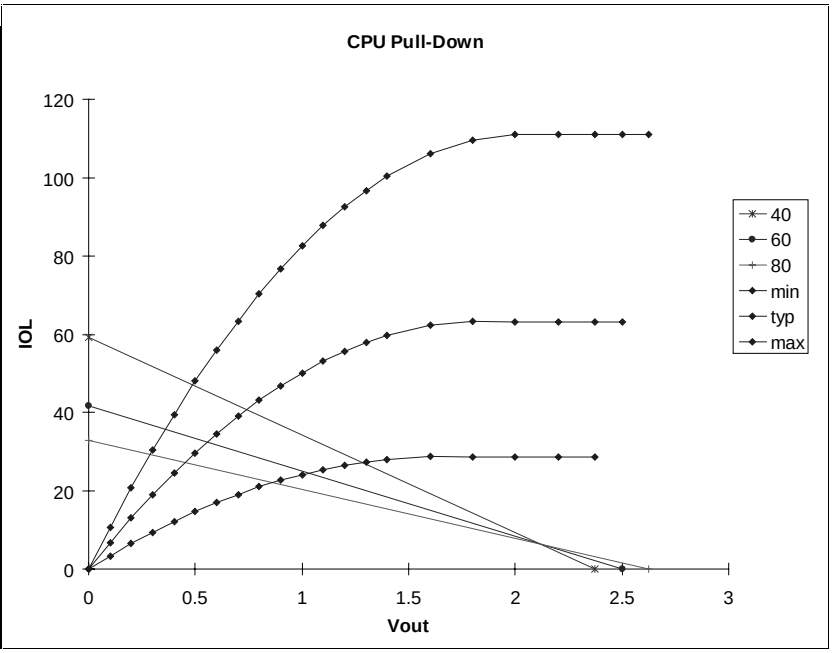


Figure 2-2 TYPE 1: CPU Clock Output Buffer Pull-Down Characteristics

Notes (Figure 2-2)**:**

1. Must meet the temperature and voltage range specified in Table 2-3 DC Operating Requirements
2. This drawing is not to scale. Comparisons should be made to the data provided in the table next to this drawing and to Table 2-4 TYPE 1: CPU Clock Buffer Operating Requirements.

2.2.2 TYPE 2: IOAPIC (2.5V) Buffer Characteristics

Table 2-5 IOAPIC Clock Buffer Operating Requirements

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
I_{ohmin}	Pull-Up Current	Vout = 1.4 V	-36			mA	1
I_{ohmax}	Pull-Up Current	V_{out} = 2.5V			-21	mA	1
I_{olmin}	Pull-Down Current	V_{out} = 1.0 V	36			mA	1
I_{olmax}	Pull-Down Current	V_{out} = 0.2 V			31	mA	1
t_{rh}	2.5V Type 2 Output Rise Edge Rate	2.5V ±5% @ 0.4V - 2.0V	1/1		4/1	V/ns	2
t_{fh}	2.5V Type 2 Output Fall Edge Rate	2.5V ±5% @ 2.0V - 0.4V	1/1		4/1	V/ns	2

Notes:

1. Intended to approximate impedance curve below. Device should be checked against entire curve for characterization testing. Production testing is expected to be a subset of characterization testing.
2. Output rise and fall time. See Figure 4-1 CK100 Clock Waveform for calculation / measurement information.
3. Output rise and fall time must be guaranteed across VCC , process and temperature range.
4. Receiver logic thresholds are Vil=0.7 and Vih=1.7 Volts.
5. Ron 9-30 Ohm with a 20 Ohm nominal driver impedance.
6. Ron = Vout/Ioh, Vout/Iol measured at VCC/2.

Pull-Up			
Voltage (V)	I (mA) min	I (mA) typ	I (mA) max
0	-42	-90	-159
0.4	-42	-90	-159
0.6	-42	-90	-159
0.8	-42	-90	-159
1	-41	-88	-157
1.2	-39	-85	-150
1.4	-36	-78	-140
1.6	-32	-70	-127
1.8	-25	-59	-109
1.9	-22	-52	-99
2	-18	-45	-89
2.1	-14	-37	-77
2.2	-9	-29	-64
2.3	-4	-20	-50
2.375	0	-13	-40
2.5		0	-21
2.625			0

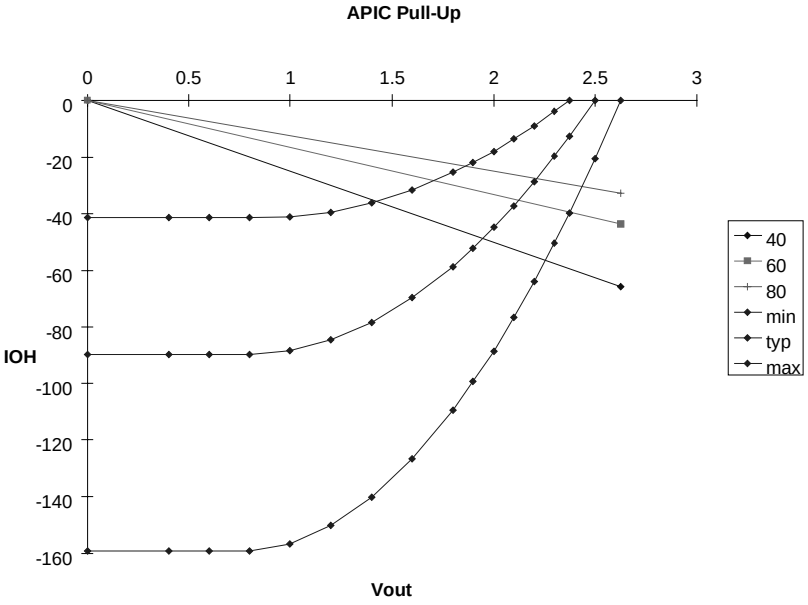


Figure 2-3 TYPE 2: IOAPIC Clock Output Buffer Pull-Up Characteristics

Notes (Figure 2-3)**:**

1. Must meet the temperature and voltage range specified in Table 2-3 DC Operating Requirements
2. This drawing is not to scale. Comparisons should be made to the data provided in the table next this drawing and to Table 2-5 IOAPIC Clock Buffer Operating Requirements.

Pull-Down			
Voltage (V)	I (mA) min	I (mA) typ	I (mA) max
0	0	0	0
0.1	5	10	16
0.2	10	19	31
0.3	14	28	45
0.4	18	36	59
0.5	22	44	72
0.6	25	51	84
0.7	29	57	95
0.8	31	63	105
0.9	34	69	114
1	36	73	123
1.1	38	78	131
1.2	40	82	138
1.3	41	85	144
1.4	42	88	150
1.6	43	91	158
1.8	43	93	163
2	43	93	165
2.2	43	93	165
2.375	43	93	165
2.5		93	165
2.625			165

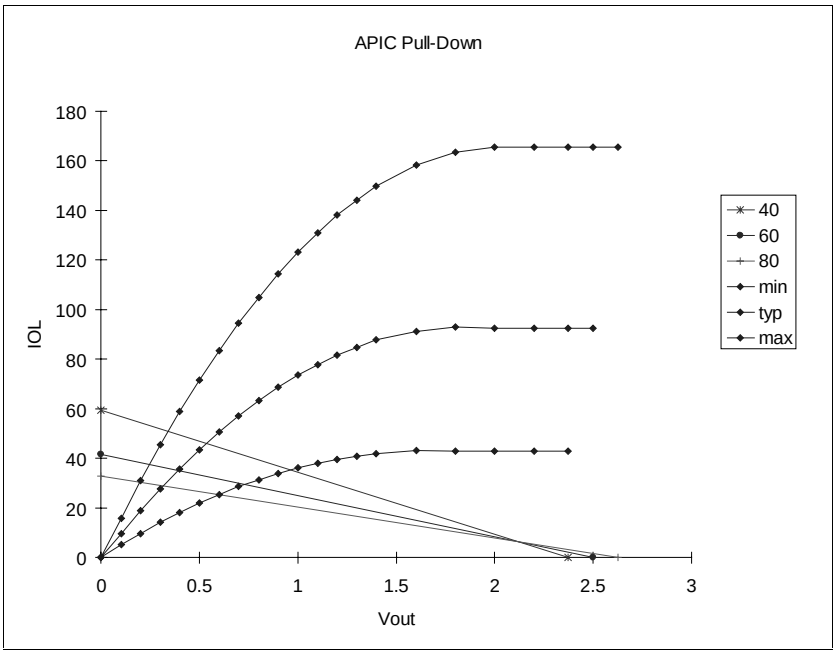


Figure 2-4 TYPE 2: IOAPIC Clock Output Buffer Pull-Down Characteristics

Notes (Figure 2-4)**:**
1. Must meet the temperature and voltage range specified in Table 2-3 DC Operating Requirements
2. This drawing is not to scale. Comparisons should be made to the data provided in the table next this drawing and to Table 2-5 IOAPIC Clock Buffer Operating Requirements.

2.2.3 TYPE 3: 3.3V 48Mhz, REF Buffer Characteristics

Table 2-6 3.3V Clock Operating Requirements

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
I_{ohmin}	Pull-Up Current	Vout = 1.0 V	-29			mA	1
I_{ohmax}	Pull-Up Current	V_{out} = 3.135 V			-23	mA	1
I_{olmin}	Pull-Down Current	V_{out} = 1.95V	29			mA	1
I_{olmax}	Pull-Down Current	V_{out} = 0.4 V			27	mA	1
t_{rh}	3.3V Type 3 Output Rise Edge Rate	3.3V ±5% @ 0.4V - 2.4V	0.5		2.0	V/ns	2
t_{fh}	3.3V Type 3 Output Fall Edge Rate	3.3V ±5% @ 2.4V - 0.4V	0.5		2.0	V/ns	2

Notes:
1. Intended to approximate impedance curve below. Device should be checked against entire curve for characterization testing. Production testing is expected to be a subset of characterization testing.
2. Output rise and fall time. See Figure 4-1 CK100 Clock Waveform for calculation / measurement information.
3. Output rise and fall time must be guaranteed across VCC , process and temperature range.
4. Receiver logic thresholds are Vil=0.8 and Vih=2.0 Volts.
5. Ron 20-60 Ohm with a 40 Ohm nominal driver impedance.
6. Ron = Vout/Ioh, Vout/Iol measured at VCC/2.

Pull-Up			
Voltage	I (mA)	I (mA)	I (mA)
(V)	min	typ	max
0	-29	-46	-99
1	-29	-46	-99
1.4	-27	-44	-94
1.5	-27	-43	-92
1.65	-25	-41	-89
1.8	-24	-39	-85
2	-22	-36	-79
2.4	-16	-28	-63
2.6	-12	-22	-53
3.135	0	-6	-23
3.3		0	-12
3.465			0

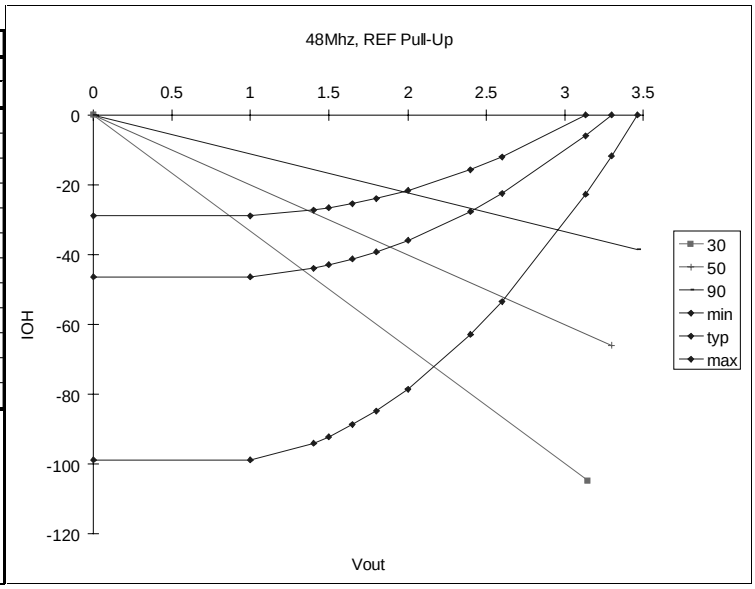


Figure 2-5 TYPE 3: 48Mhz, REF Clock Output Buffer Pull-Up Characteristics

Notes (Figure 2-5)**:**

1. Must meet the temperature and voltage range specified in Table 2-3 DC Operating Requirements
2. This drawing is not to scale. Comparisons should be made to the data provided in the table next to this drawing and to Table 2-6 3.3V Clock Operating Requirements.

Pull-Down			
Voltage	I (mA)	I (mA)	I (mA)
(V)	min	typ	max
0	0	0	0
0.4	9	13	27
0.65	14	21	41
0.85	17	26	52
1	20	29	59
1.4	25	37	76
1.5	26	39	79
1.65	27	41	84
1.8	28	43	88
1.95	29	45	92
3.135	29	45	102
3.6		45	102

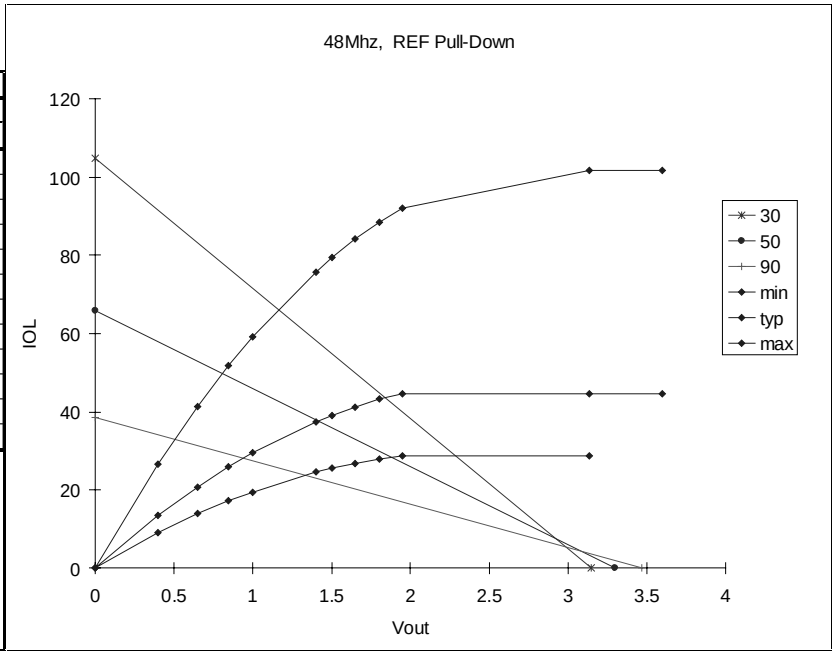


Figure 2-6 TYPE 3: 48Mhz, REF Clock Output Buffer Pull-Down Characteristics

Notes (Figure 2-6)**:**

1. Must meet the temperature and voltage range specified in Table 2-3 DC Operating Requirements
2. This drawing is not to scale. Comparisons should be made to the data provided in the table next this drawing and to Table 2-6 3.3V Clock Operating Requirements.

2.2.4 TYPE 4: SDRAM (3.3 V) Clock Buffer Characteristics

Table 2-7 SDRAM Clock Operating Requirements

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
I_{ohmin}	Pull-Up Current	Vout = 2.0 V	-54			mA	1
I_{ohmax}	Pull-Up Current	V_{out} = 3.135 V			-46	mA	1
I_{olmin}	Pull-Down Current	V_{out} = 1.0V	54			mA	1
I_{olmax}	Pull-Down Current	V_{out} = 0.4 V			53	mA	1
$t_{rhSDRAM}$	3.3V Type 4 Output Rise Edge Rate. SDRAM ONLY.	3.3V ±5% @ 0.4V - 2.4V	1.5		4/1	V/ns	2, 7
$t_{fhSDRAM}$	3.3V Type 4 Output Fall Edge Rate. SDRAM ONLY.	3.3V ±5% @ 2.4V - 0.4V	1.5		4/1	V/ns	2, 7

Notes:
1. Intended to approximate impedance curve below. Device should be checked against entire curve for characterization testing. Production testing is expected to be a subset of characterization testing.
2. Output rise and fall time. See Figure 4-1 CK100 Clock Waveform for calculation / measurement information.
3. Output rise and fall time must be guaranteed across VCC , process and temperature range.
4. Receiver logic thresholds are Vil=0.8 and Vih=2.0 Volts.
5. Ron 10-24 Ohm with a 16 Ohm nominal driver impedance.
6. Ron = Vout/Ioh, Vout/Iol measured at VCC/2.
7. 1.5V/nS component spec required to meet 1.0V/nS minimum rise/fall time at SDRAM input. This is required to guarantee PC100 component timings which are tested/specified with a maximum of 1.2nS from 0.8V to 2.0V threshold levels.

Pull-Up			
Voltage (V)	I (mA) min	I (mA) typ	I (mA) max
0	-72	-116	-198
1	-72	-116	-198
1.4	-68	-110	-188
1.5	-67	-107	-184
1.65	-64	-103	-177
1.8	-60	-98	-170
2	-54	-90	-157
2.4	-39	-69	-126
2.6	-30	-56	-107
3.135	0	-15	-46
3.3		0	-23
3.465			0

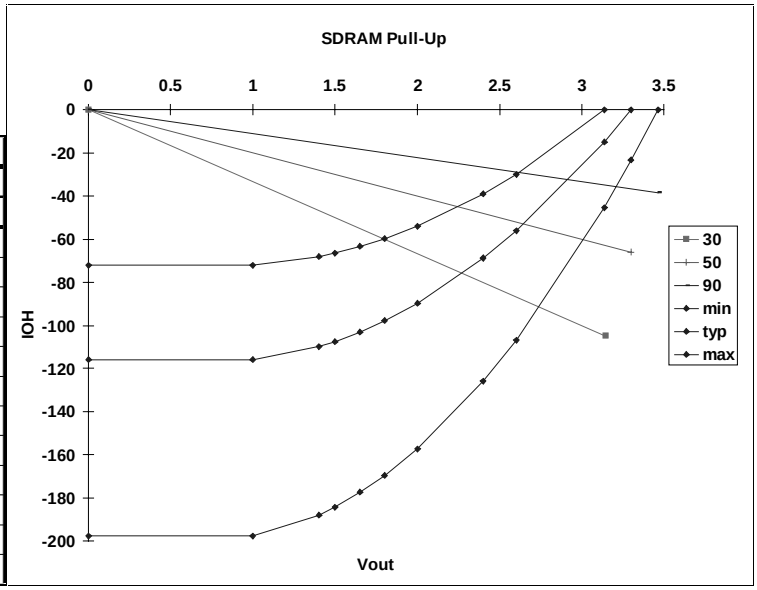


Figure 2-7 TYPE 4: SDRAM Clock Output Buffer Pull-Up Characteristics

Notes (Figure 2-7)**:**
1. Must meet the temperature and voltage range specified in Table 2-3 DC Operating Requirements
2. This drawing is not to scale. Comparisons should be made to the data provided in the table next to this drawing and to Table 2-6 3.3V Clock Operating Requirements.

Pull-Down			
Voltage (V)	I (mA) min	I (mA) typ	I (mA) max
0	0	0	0
0.4	23	34	53
0.65	35	52	83
0.85	43	65	104
1	49	74	118
1.4	61	93	152
1.5	64	98	159
1.65	67	103	168
1.8	70	108	177
1.95	72	112	184
3.135	72	112	204
3.6		112	204

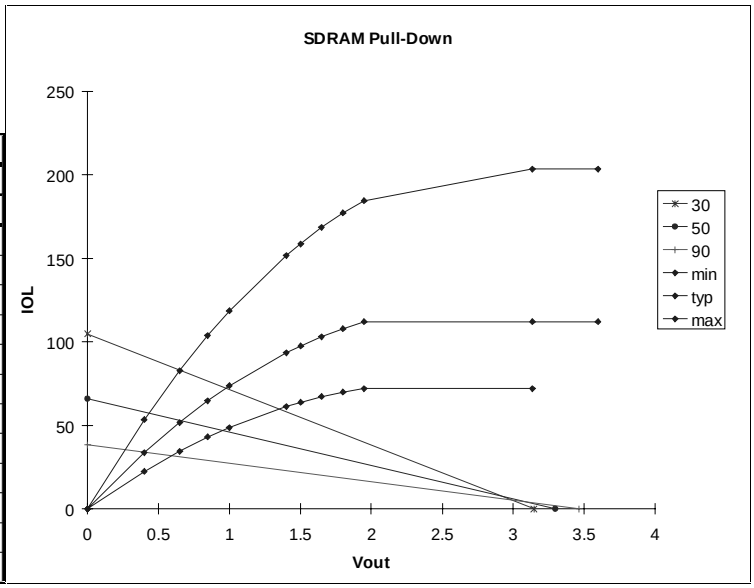


Figure 2-8 TYPE 4: SDRAM Clock Output Buffer Pull-Down Characteristics

Notes (Figure 2-8)**:**

1. Must meet the temperature and voltage range specified in Table 2-3 DC Operating Requirements
2. This drawing is not to scale. Comparisons should be made to the data provided in the table next this drawing and to Table 2-6 3.3V Clock Operating Requirements.

2.2.5 TYPE 5: PCI Clock Buffer Characteristics

Table 2-8 PCI Clock AC Operating Requirements

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
I_{ohmin}	Pull-Up Current	Vout = 1.0 V	-33			mA	1
I_{ohmax}	Pull-Up Current	V_{out} = 3.135 V			-33	mA	1
I_{olmin}	Pull-Down Current	V_{out} = 1.95V	30			mA	1
I_{olmax}	Pull-Down Current	V_{out} = 0.4 V			38	mA	1
t_{rh}	3.3V Type 4 Output Rise Edge Rate	3.3V ±5% @ 0.4V - 2.4V	1/1		4/1	V/ns	2
t_{fh}	3.3V Type 4 Output Fall Edge Rate	3.3V ±5% @ 2.4V - 0.4V	1/1		4/1	V/ns	2

Notes:

1. Intended to approximate impedance curve below. Device should be checked against entire curve for characterization testing. Production testing is expected to be a subset of characterization testing.
2. Output rise and fall time. See Figure 4-1 CK100 Clock Waveform for calculation / measurement information.
3. Output rise and fall time must be guaranteed across VCC , process and temperature range.
4. Receiver logic thresholds are Vil=0.8 and Vih=2.0 Volts.
5. Ron 12-55 Ohm with a 30 Ohm nominal driver impedance.
6. Ron = Vout/Ioh, Vout/Iol measured at VCC/2.
7. See PCI specification for additional PCI details

	Pull-Up		
Voltage (V)	I (mA) min	I (mA) typ	I (mA) max
0	-34	-59	-195
1	-33	-58	-194
1.4	-31	-55	-189
1.5	-30	-54	-184
1.65	-28	-52	-172
1.8	-25.5	-50	-159
2	-22	-46	-140
2.4	-14.5	-35	-100
2.6	-11	-28	-83
3.135	0	-6	-33
3.3		0	-19
3.6			0

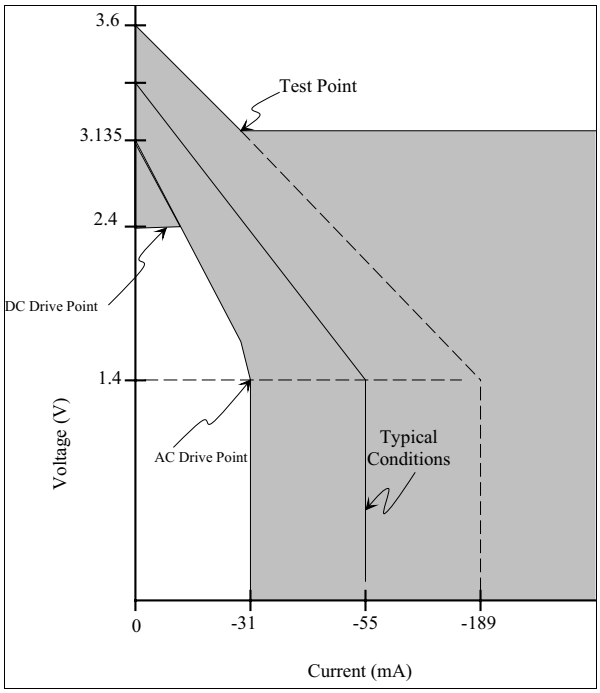


Figure 2-9 TYPE 5: PCI Clock Output Buffer Pull-Up Characteristics

Notes (Figure 2-9):

1. Must meet the temperature and voltage range specified in Table 2-3 DC Operating Requirements.

This drawing is not to scale. Comparisons should be made to the data provided in the table next to it and to Table 2-8 PCI Clock AC Operating Requirements

Pull-Down			
Voltage (V)	I (mA) min	I(mA) typ	I (mA) max
0	0	0	0
0.4	9.4	18	38
0.65	14	30	64
0.85	17.7	38	84
1	20	43	100
1.4	26.5	53	139
1.5	28	55	148
1.65	29	56	163
1.8	30	57	175
1.95	30	58	178
3.135	31	59	187
3.6	32	59	188

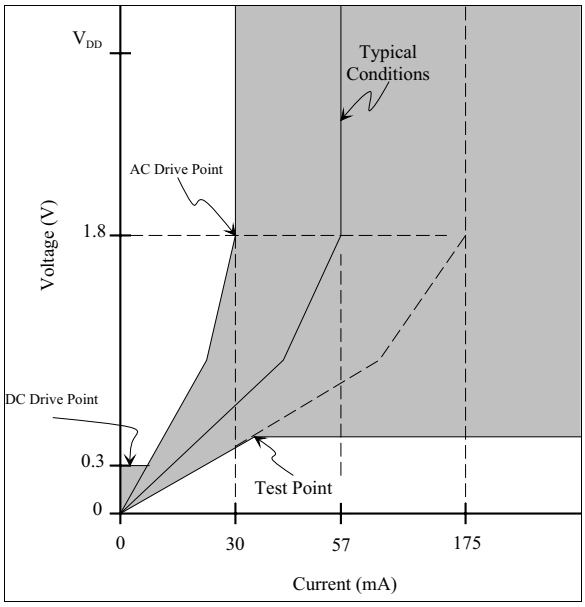


Figure 2-10 TYPE 5: PCI Clock Output Buffer Pull-Down Characteristics

Notes (Figure 2-10)**:**

1. Must meet the temperature and voltage range specified in Table 2-3 DC Operating Requirements
2. This drawing is not to scale. Comparisons should be made to the data provided in the table next to it and to Table 2-8 PCI Clock AC Operating Requirements

2.2.6 Vendor Provided Specifications

Vendors should make the following information available in their data sheets:

- Pin capacitance for all pins (min and max).
- Pin inductance for all pins (min and max).
- Output V/I curves under switching conditions. Two graphs/tables should be given for each output type used: one for driving high, the other for driving low. Both should show best-worst case conditions.
- Loaded rise/fall times for each output type for loads as specified in the test section of this specification.
- Absolute maximum data, including operating and non-operating temperature, DC maximums, etc.

Component vendors should make the following information electronically available in the IBIS model format. Include the following minimum information:

- Output V/I curves under switching conditions. Two curves should be supplied: one for driving high, the other for driving low. Both should show best-typical-worst curves.
- Unloaded rise/fall times for each output type as specified by IBIS.
- Package Resistance (R_pkg [min, max]); Package Inductance (L_pkg [min, max]); Package Capacitance (C_pkg [min, max]); Component Capacitance (C_comp [min, max]).

3. AC Timing

3.1 Timing Requirements

Table 3-1 Host Bus AC Timing Requirements

Symbol	Parameter	66 MHz		100 MHz		Units	Notes
		Min	Max	Min	Max		
tHKP	Host CLK period	15.0	15.5	10.0	10.5	ns	10
tHKH	Host CLK high time	5.2		3.0		ns	1, 5, 13
tHKL	Host CLK low time	5.0		2.8		ns	1, 6, 13
tHRISE	Host CLK rise time	0.4	1.6	0.4	1.6	ns	9
tHFALL	Host CLK fall time	0.4	1.6	0.4	1.6	ns	9
tJITTER	Host CLK Jitter		250		250	ps	
Duty Cycle	Measured at 1.25V	45	55	45	55	%	
tHSKW	Host Bus CLK Skew		175		175	ps	2
tIOSKW	IOAPIC Bus CLK Skew		250		250	ps	12
tpZL, tpZH	Output enable delay	1.0	8.0	1.0	8.0	ns	14
tpLZ, tpZH	Output disable delay	1.0	8.0	1.0	8.0	ns	14
tIOSKW	IOAPIC Bus CLK Skew		250		250	ps	12
tHSTB	Host CLK Stabilization from power-up		3		3	ms	7
tPKP	PCI CLK period	30.0	∞	30.0	∞	ns	3
tPKPS	PCI CLK period stability		500		500	ps	8
tPKH	PCI CLK high time	12.0		12.0		ns	1
tPKL	PCI CLK low time	12.0		12.0		ns	1
tPSKW	PCI Bus CLK Skew		500		500	ps	2
tHPOFFSET	Host to PCI Clock Offset	1.5	4.0	1.5	4.0	ns	2,4
tPSTB	PCI CLK Stabilization from power-up		3		3	ms	7

Notes:

1. Output drivers must have the characteristics noted in Section 2 above. See Figure 4.1 for measure points.
2. Period, jitter, offset and skew measured on rising edge @1.25V for 2.5V clocks and @ 1.5V for 3.3V clocks.
3. The PCI Clock is the Host clock divided by two at Host=66.6Mhz. PCI clock is the Host clock divided by three at Host = 100 Mhz.
4. The Host CLK must always lead the PCI CLK as shown in Figure 3-2. This must be guaranteed by design under the test load conditions.
5. tHKH is measured at 2.0V as shown in Figure 4-1.
6. tHKL is measured at 0.4V as shown in Figure 4-1.
7. The time specified is measured from when Vddq achieves its nominal operating level (typical condition Vddq = 3.3V) till the frequency output is stable and operating within specification.
8. Defined as once the clock is at its nominal operating frequency the adjacent period changes can not exceed the time specified.
9. tHRISE and tHFALL are measured as a transition through the threshold region Vol = 0.4V and Voh = 2.0V (1mA) JEDEC Specification.
10. The average period over any 1 uS period of time must be greater than the minimum specified period
11. There is no pin-pin skew requirement between individual outputs within the REF or 48Mhz banks.
12. Ideal specification would be to reduce to 175pS. However, 250pS is acceptable.
13. Calculated at minimum edge-rate (1V/nS) to guarantee 45/55% duty-cycle at 1.25 Volts. Pulsewidth is required to be wider at faster edge-rate to ensure duty-cycle specification is met.
14. Should be specified for completeness only. Specs can be modified If required.

Table 3-2A Main Memory Bus AC Timing Requirements

Symbol	Parameter	66 MHz		100 MHz		Units	Notes
		Min	Max	Min	Max		
tSDKP	SDRAM CLK period	15.0	15.5	10.0	10.5	ns	2, 8
tSDKH	SDRAM CLK high time	5.6		3.3		ns	3, 8, 12
tSDKL	SDRAM CLK low time	5.3		3.1		ns	4, 8, 12
tSDRISE	SDRAM CLK rise time	1.5	4.0	1.5	4.0	V/ns	6, 8
tSDFALL	SDRAM CLK fall time	1.5	4.0	1.5	4.0	V/ns	6, 8
tpLH	SDRAM Buffer LH prop delay	1.0	5.0	1.0	5.0	nS	8, 9
tpHL	SDRAM Buffer HL prop delay	1.0	5.0	1.0	5.0	nS	8, 9
tpZL, tpZH	SDRAM Buffer Enable delay	1.0	8.0	1.0	8.0	nS	8, 9, 10
tpLZ, tpHZ	SDRAM Buffer disable delay	1.0	8.0	1.0	8.0	nS	8, 9, 10
Duty Cycle	Measured at 1.5 V	45	55	45	55	%	7, 8, 9
tSDSKW	pin-to-pin CLK Skew		250		250	ps	2, 8

Notes:

1. Output drivers must have the characteristics noted in Section 2 above.
2. Clock period, and skew are measured on the rising edge at 1.5V for all 3.3V clocks.
3. tSDKH is measured at 2.4V as shown in Figure 4-1.
4. tSDKL is measured at 0.4V as shown in Figure 4-1.
5. Defined as once the clock is at its nominal operating frequency the adjacent period changes can not exceed the time specified.
6. tSDRISE and tSDFALL are measured as a transition through the threshold region Vol = 0.4V and Voh = 2.4V (1mA) JEDEC Specification. Measured with test loads described in Test and Measurement section
7. Duty cycle should be tested with a 50/50% input.
8. Over min (20pF) to max (30 pF) discrete load, process, voltage and temperature.
9. Input edge rate for these tests must be faster than 1 V/nS.
10. Should be specified for completeness only. Specs can be modified If required.
11. Part to part skew should be minimized and specified by vendor for completeness. Not a requirement to meet Intel yellow cover specification.
12. Calculated at minimum edge-rate (1.5nS) to guarantee 45/55% duty-cycle at 1.5 Volts. Pulsewidth is required to be wider at faster edge-rate to ensure duty-cycle specification is met.

3.2 Frequency Accuracy at 100 Mhz

Although the target Host clock frequency is 100 Mhz (10.0 nS minimum), it is known that the current generation of 14.318 Mhz-based clock drivers will not be able to produce an extremely accurate nominal frequency without having an effect on the jitter signature. Each vendor should be aware of the trade-offs between the counter values, PLL update rate and jitter. Sometimes a looser PPM device will have less jitter than a device with a low PPM variation. A maximum period has been defined as the minimum period plus 500 pS. The intent of this specification is to limit the variability within various platform clocking solutions.

3.3 Frequency Accuracy of 48Mhz outputs.

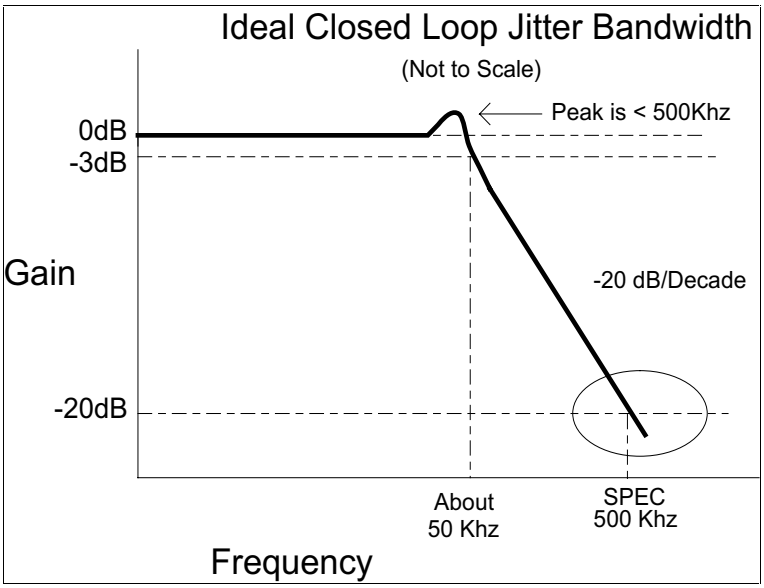
The 48 Mhz PPM of the nominal frequency is required to be +167 from 48.00Mhz to conform with the USB default. Failure to comply with this requirement requires a BIOS change and is deemed to be unacceptable.

3.4 Multiple PLL Jitter Tracking Specification.

The clock driver's closed loop jitter bandwidth must be set low to allow any PLL-based device to track the jitter created by the clock driver. This 1:1 relationship is critical when the clock driver drives two or more PLLs. A worst case timing issue would occur if one PLL attenuated the jitter and another device (PLL or nonPLL) tracked the jitter completely. To reduce the possibility of this we require that the -20dB attenuation point be less than or equal to 500Khz. Most clock vendors do not specify their jitter bandwidth characteristics or specify it only at the -3dB level. To allow for greatest flexibility in loop design we require the vendor to provide the -20dB point. This specification may be guaranteed by design and/or measured with a spectrum analyzer.

This specification is intended to replace and clarify the Pentium® specification which was stated as:

"To ensure a 1:1 jitter frequency relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 500 Khz and 1/3 of the clock operating frequency."



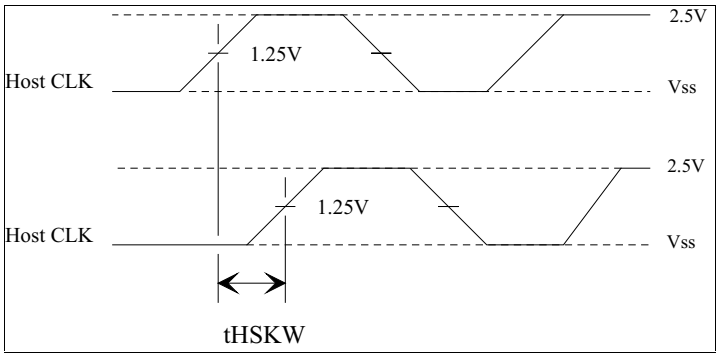


Figure 3-1 Host CLK to Host CLK Skew

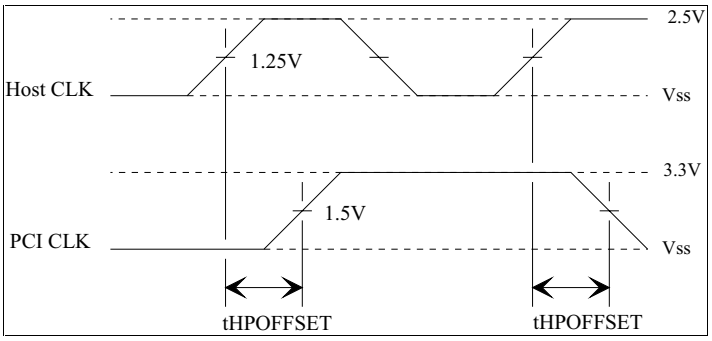


Figure 3-2 Host CLK to PCI CLK Offset

4. Test and Measurement

Board level simulations are usually done using ideal output buffer models which are defined/modeled with no output load. The typical source of these models comes from one or more silicon level simulators. Clock driver vendor validation of these models under a no load condition is extremely time consuming. The table below provides lumped load test loads over which the vendor is expected to test/guarantee all AC parameters for the clock driver. The vendor is encouraged to provide information on the correlation between the lumped load performance and the no-load performance as an applications exercise to fully describe the operation of the product.

Table 4-1 Minimum and Maximum Expected Capacitive Loads

Clock	Min Load	Max Load	Units	Notes
CPU Clocks (HCLK)	10	20	pF	1 device load, possible 2 loads.
PCI Clocks (PCLK)	30	30	pF	Must meet PCI 2.1 requirements
48 MHz Clock	10	20	pF	1 device load
SDRAM	20	30	pF	SDRAM DIMM spec.
REF	10	20	pF	1 device load
IOAPIC	10	20	pF	2 device loads

Notes:

1. Maximum rise/fall times are to be guaranteed at maximum specified load for each type of output buffer.
2. Minimum rise/fall times are to be guaranteed at minimum specified load for each type of output buffer
3. Rise/fall times are specified with pure capacitive load as shown. Testing may be done with an additional 500 ohm resistor in parallel if properly correlated with the capacitive load.
4. Minimum PCI load of 30 pF is legacy spec from previous clock driver platforms. Does not accurately reflect minimum PCI load.

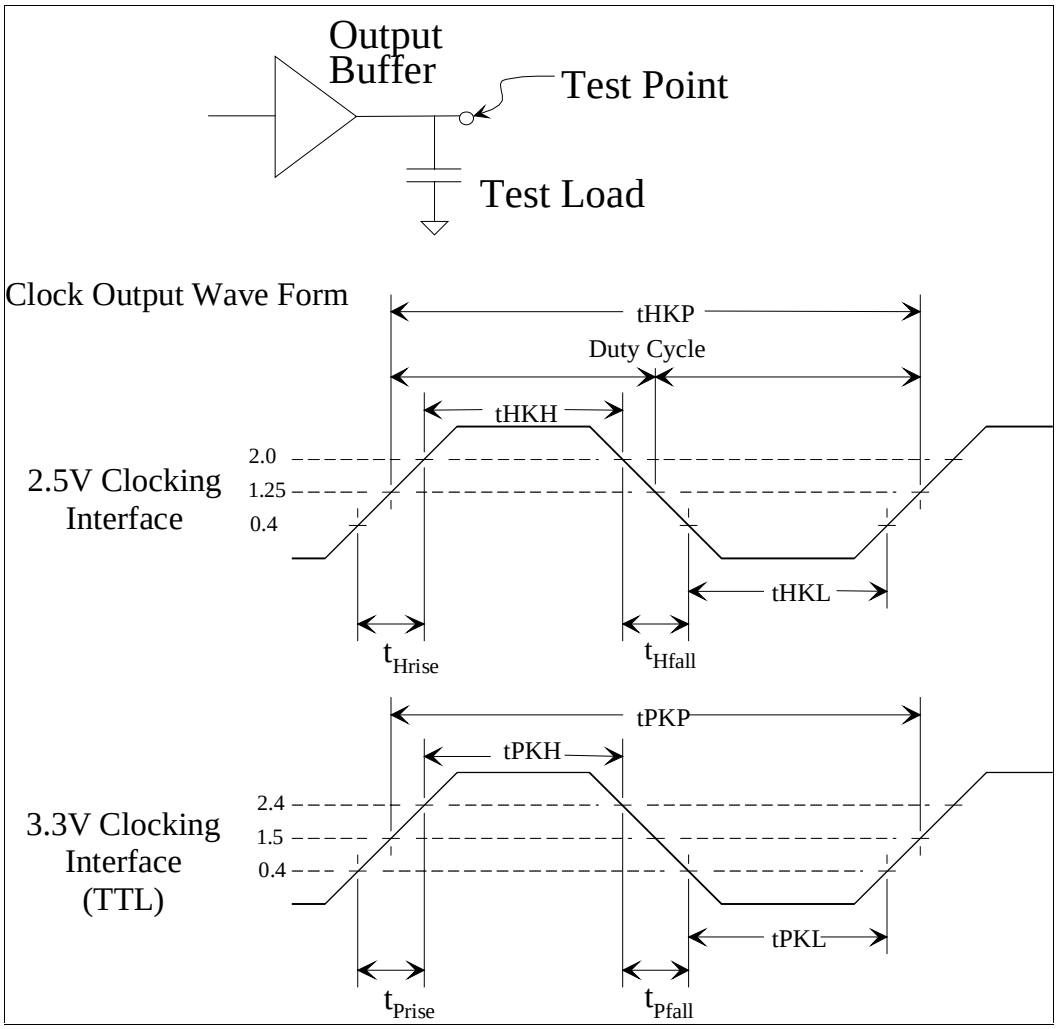


Figure 4-1 CK100 Clock Waveforms

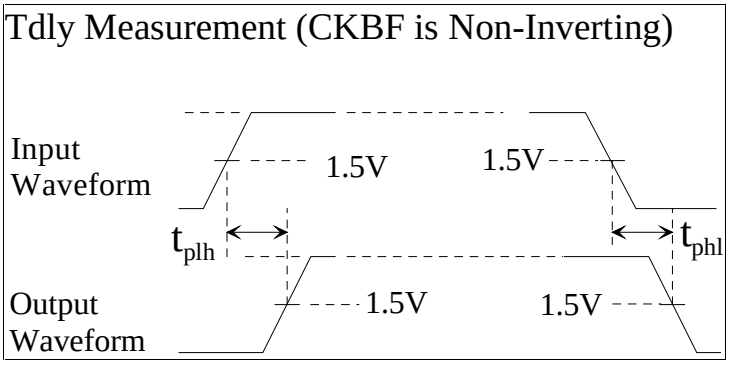


Figure 4-2A CKBF Clock Waveforms

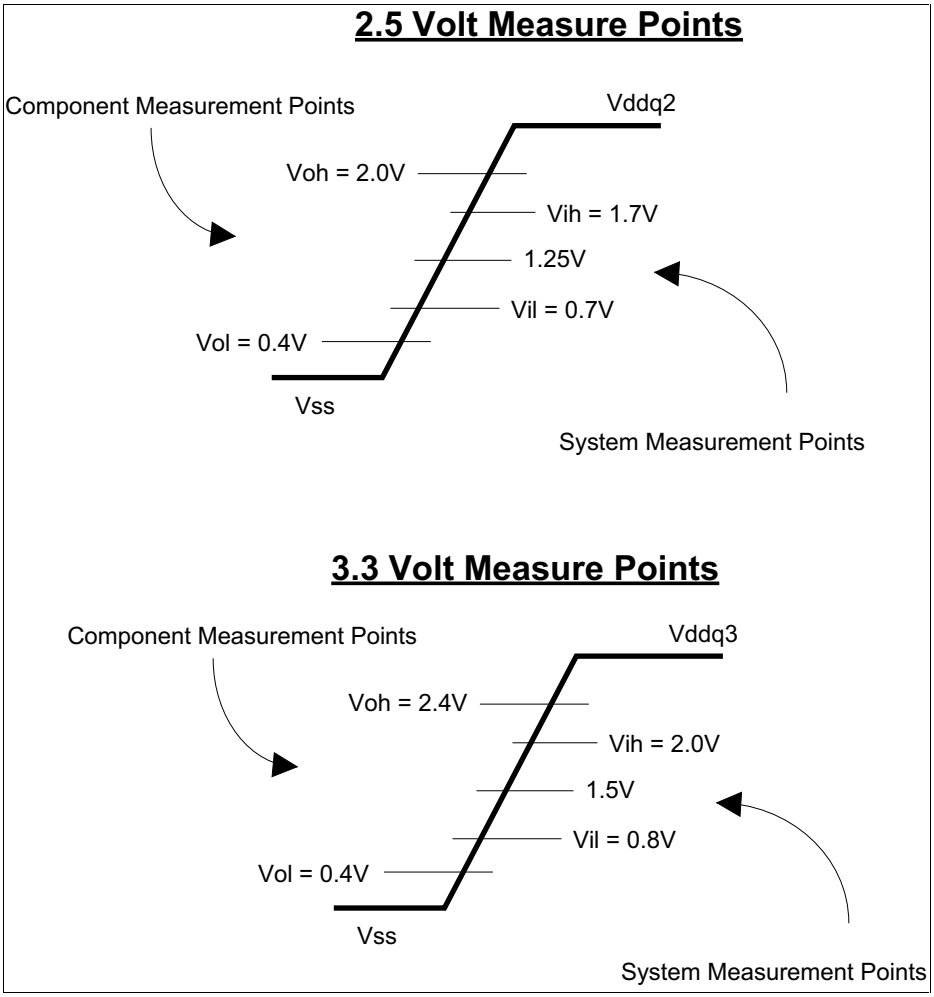


Figure 4-3B Component Versus System Measure Points

5. System Considerations

The diagrams shown below are typical clock routing topologies for the Pentium® II desktop platforms. These are meant as an aid to the OEM in laying out clocks for PC Desktop platforms. It is also meant as an aid to clock driver vendors to simulate and check their buffers.

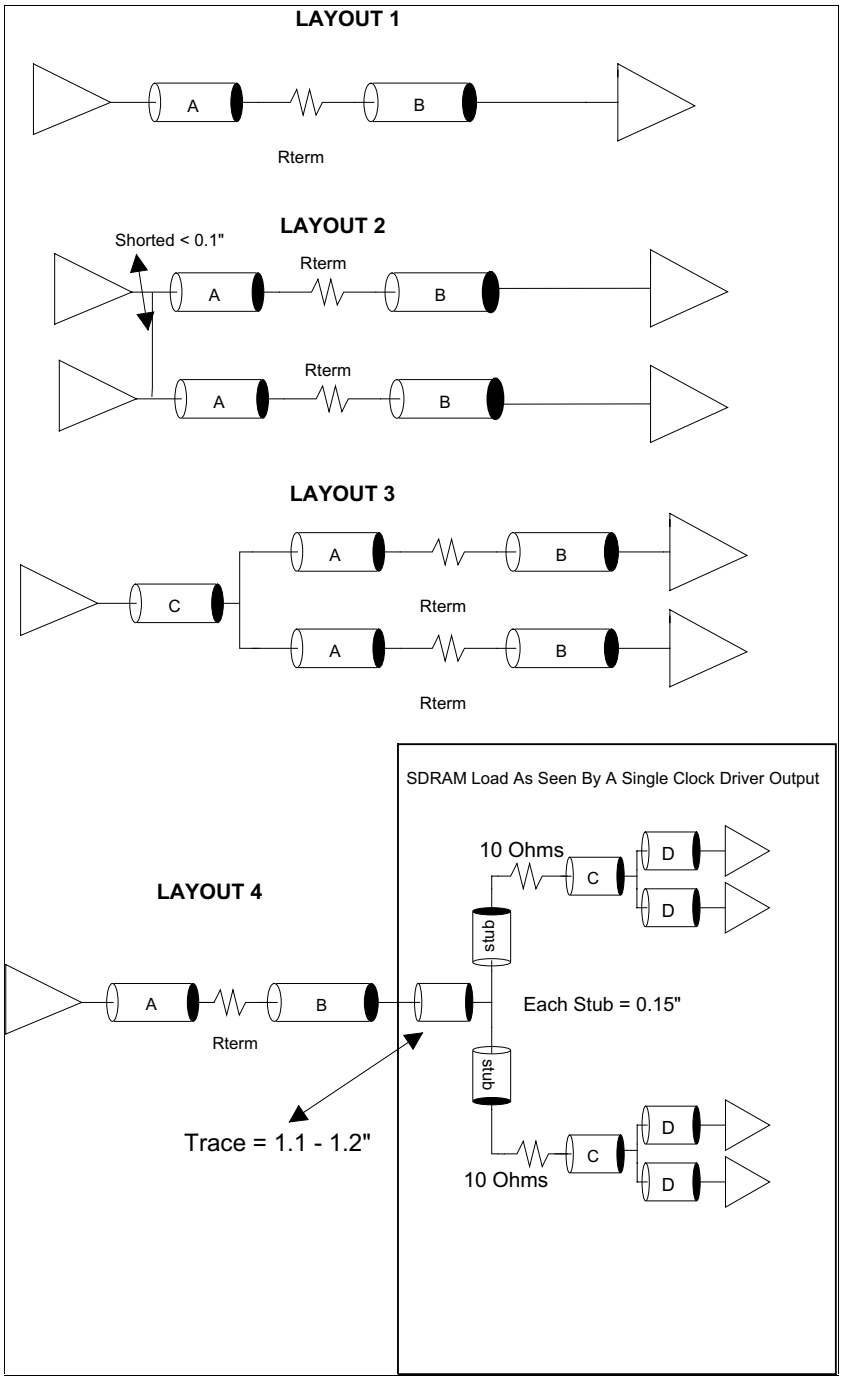


Figure 5-1 Standard Clock Layout Topologies

Table 5-1 Layout Dimensions

CLK	Topology	A	B	C	D	R_{TERM}	Notes
CPU	LAYOUT 1	0.25"- 0.5 "	3" - 7"	n/a	n/a	33	1
CPU	LAYOUT 2	0.1"- 0.25"	3" - 6"	n/a	n/a	33	2
IOAPIC	LAYOUT 3	0.25"- 0.5"	3" - 7"	0.25"- 0.5"	n/a	33	3
48MHz, REF	LAYOUT 1	0.25"- 0.5"	3" - 7"	n/a	n/a	22	4
SDRAM	LAYOUT 4	0.25" - 0.5"	4" - 7"	0.9" - 1.1"	0.6" - 0.8"	22	

Notes:
1. Primary topology for CPU outputs. One load.
2. Secondary topology for CPU outputs. Two loads.
3. REQUIRED to drive two loads, split at receiver.
4. Point-to-Point only

Table 5-2 Board Level Simulation Conditions

Symbol	*Parameter*	*Slow*	*Typ*	*Fast*
Z_O	Line Impedance	50 Ω	70 Ω	85 Ω
S	Line Velocity	2.2 ns/ft	1.9 ns/ft	1.6 ns/ft
V_{DD}	Core Supply Voltage	3.135 V	3.30V	3.465 V
V_{DDQ}	IO Supply Voltage	2.375 V	2.5 V	2.625 V
T	Ambient Temperature (no airflow)	70° C	25° C	0° C

The topologies listed above in Figure 5-1 are standard topologies for desktop PC clock routings. The parameters listed in Table 5-1 above give the minimum and maximum dimension ranges to be used for clock buffer driver simulation.

Series termination resistors will be required to control the output driver variation from platform to platform. Series termination should be placed as close to the driver as possible for best signal quality results.

The low impedance outputs for the IOAPIC clocks are required to reduce the sensitivity of the topology to output buffer edge-rate variation in the non point-to-point layout topologies shown in Figure 5-1.

Table 5-3 Typical DC Characteristics at Clock Destination

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{ih3}	3.3V Input High Voltage		2.0	V_{DDQ} + .3	V	1
V_{il3}	3.3V Input Low Voltage		-0.3	0.8	V	1
C_{in}	Input Pin Capacitance			6 - 9	pF	
$C_{insdram}$	SDRAM Input Pin Capacitance		3	5	pF	

Notes:
1. Signal edge is required to be monotonic when transitioning through this region.

The clock input to the processor and other system components must meet signal quality specifications to guarantee the clock signal is sensed properly and to ensure the clock signal does not affect the long term reliability of the components. There are two AC signal quality parameters defined: Overshoot/Undershoot and Ringback.

Typically, these values are determined by board designers as the result of multiple system level simulations. However, the data has been provided to allow the clock driver vendor to complete a first approximation of these system events. These simulations are encouraged and should be seen as a step in the validation of the IBIS models for the device. Each device will have a different sensitivity to the over and undershoot, due to various input capacitance and clamping circuits. Board impedance, termination and trace topology will dominate these measurements. The specifications should be taken as applications information and a design target for the clock driver vendor, but should be met by the board designer.

Current 100 Mhz SDRAM DIMM specifications call for input clamp diodes on all 100Mhz SDRAM components. This should help the signal quality of these devices and allow faster clock risetimes to be acceptable. However, backwards compatibility to 66Mhz SDRAM DIMMS (which may not have input clamp diodes) causes us to keep the driver specifications the same as previous generations of clock drivers.

Table 5-4 AC Signal Quality Requirements at Destination

Symbol	Parameter	Min	Max	Units	Notes
t_{over} SDRAM	Overshoot/Undershoot Voltage Duration		5.0	ns	1, 2
t_{ring} SDRAM	Ring back		Vih Vil	V	
t_{over} CPU/Chipset	Overshoot/Undershoot Voltage		Vddq +0.7 Vss - 0.7	V	4
t_{ring} CPU/Chipset	Ring back		Vih Vil	V	

Notes:

1. The maximum SDRAM overshoot and undershoot is specified to be 1.5 V above or below the power rails.
2. Settling time is defined at the point at which the output voltage remains within 10% of the clocks steady-state quiescent voltage. The t_{over} specification includes settling time.
3. These values are representative of the values for system level design targets for the current JEDEC SDRAM dimms.
4. Required to support future Intel Silicon.

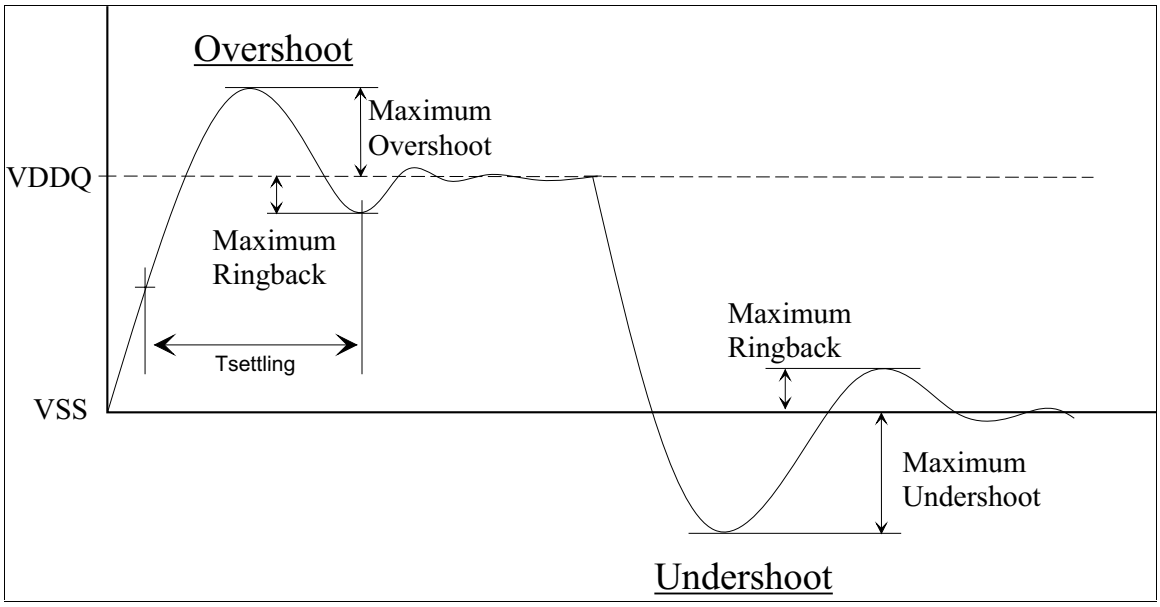


Figure 5-2 Overshoot & Undershoot

6. How To Obtain Reference Material

6.1 PCI Reference

The PCI Special Interest Group is an industry-wide group that controls the official PCI specification. You can obtain the latest copies of the PCI specification by contacting the PCI Special Interest Group at the following numbers:

(800)433-5177 - USA
(503)797-4297 - International
(503)234-6762 - Fax

There is a nominal fee for obtaining this specification.

6.2 IBIS Reference

The IBIS Open Forum is an industry-wide forum that controls the official IBIS specification. Minutes of IBIS meetings, email correspondence, proposals for specification changes, etc. are on-line at "vhdl.org". To join in the email discussions, send a message to "ibis-request@vhdl.org" and request that your name be added to the IBIS mail reflector. Be sure to include your email address.

The IBIS home page can be found at **http://www.eia.org/eig/ibis/ibis.htm**

6.3 Audio Codec 97 (AC97) Reference

The AC97 home page can be found at **http://www.intel.com/pc-supp/platform/ac97**

7. I²C Considerations

I²C has been chosen as the serial bus interface to control these clock drivers. I²C was chosen to support the JEDEC proposal JC-42.5 168 Pin Unbuffered SDRAM DIMM. All vendors are required to determine the intellectual property issues associated with the manufacture of I²C devices.

1) Address assignment: Any clock driver in this specification can use the single, 7 bit address shown below. All devices can use the address if only one master clock driver is used in a design. Intel believes that the address can be re-used for the CKBF device if no other conflicting I²C clock driver is used in the system.

The following address was confirmed by Philips on 09/04/96.

A6	A5	A4	A3	A2	A1	A0	R/W#
1	1	0	1	0	0	1	0

Note: The R/W# bit is used by the I2C controller as a data direction bit. A 'zero' indicates a transmission (WRITE) to the clock device. A 'one' indicates a request for data (READ) from the clock driver. Since the definition of the clock buffer only allows the controller to WRITE data; the R/W# bit of the address will always be seen as a 'zero.' Optimal address decoding of this bit is left to the vendor.

2) Options: It is our understanding that metal mask options and other pinouts of this type of clock driver will be allowed to use the same address as the original CKBF device. I²C addresses are defined in terms of function (master clock driver) rather than form (pinout, and option.)

3) Slave/Receiver: The clock driver is assumed to require only slave/receiver functionality. Slave/transmitter functionality is optional.

4) Data Transfer Rate: 100 kbits/s (standard mode) is the base functionality required. Fast mode (400 kbits/s) functionality is optional.

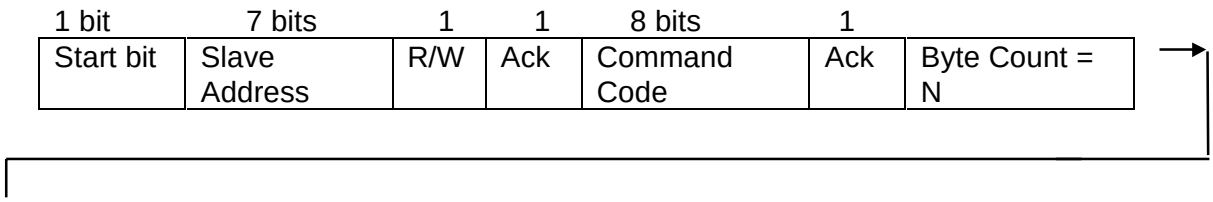
5) Logic Levels: I²C logic levels are based on a percentage of VDD for the controller and other devices on the bus. Assume all devices are based on a 3.3 Volt supply.

6) Data Byte Format: Byte format is 8 Bits as described in the following appendices.

7) Data Protocol:
To simplify the clock I²C interface, the clock driver serial protocol was specified to use only block writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. Indexed bytes are not allowed. However, the Intel controller has a more specific format than the generic I²C protocol.

The clock driver must meet this protocol which is more rigorous than previously stated I²C protocol. Treat the description from the viewpoint of controller. The controller "writes" to the clock driver and if possible would "read" from the clock driver (the clock driver is a slave/receiver only and is incapable of this transaction.)

"The block write begins with a slave address and a write condition. After the command code the host (controller) issues a byte count which describes how many more bytes will follow in the message. If the host had 20 bytes to send, the first byte would be the number 20 (14h), followed by the 20 bytes of data. The byte count may not be 0. A block write command is allowed to transfer a maximum of 32 data bytes."



Ack	Data Byte 1	Ack	Data Byte 2	Ack	...	Data Byte N	Ack	Stop
1 bit	8 bits	1	8 bits	1		8 bits	1	1

Note: The acknowledgment bit is returned by the slave/receiver (the clock driver).

Consider the command code and the byte count bytes required as the first two bytes of any transfer. The command code is software programmable via the controller, but will be specified as 0000 0000 in the clock specification. The byte count byte is the number of additional bytes required for the transfer, not counting the command code and byte count bytes. Additionally, the byte count byte is required to be a minimum of 1 byte and a maximum of 32 bytes to satisfy the above requirement.

For example:

Byte count byte MSB LSB	Notes:
0 0 0 0 0 0 0 0	Not allowed. Must have at least one byte.
0 0 0 0 0 0 0 1	Data for functional and frequency select register (currently byte 0 in spec)
0 0 0 0 0 0 1 0	Reads first two bytes of data. (byte 0 then byte 1)
0 0 0 0 0 0 1 1	Reads first three bytes (byte 0, 1, 2 in order)
0 0 0 0 0 1 0 0	Reads first four bytes (byte 0, 1, 2, 3 in order)
0 0 0 0 0 1 0 1	Reads first five bytes (byte 0, 1, 2, 3, 4 in order)
0 0 0 0 0 1 1 0	Reads first six bytes (byte 0, 1, 2, 3, 4, 5 in order)
0 0 0 0 0 1 1 1	Reads first seven bytes (byte 0, 1, 2, 3, 4, 5, 6 in order)
0 0 1 0 0 0 0 0	Max byte count supported = 32

A transfer is considered valid after the acknowledge bit corresponding to the byte count is read by the controller. The serial controller interface can be simplified by discarding the information in both the command code and the byte count bytes and simply reading all the bytes that are sent to the clock driver after being addressed by the controller. It is expected that the controller will not provide more bytes than the clock driver can handle. A clock vendor may choose to discard any number of bytes that exceed the defined byte count.

8) Clock Stretching: The clock device must not hold/stretch the SCLOCK or SDATA lines low for more than 10 mS. Clock stretching is discouraged and should only be used as a last resort. Stretching the clock/data lines for longer than this time puts the device in an error/time-out mode and may not be supported in all platforms. It is assumed that all data transfers can be completed as specified without the use of clock/data stretching.

9) General Call: It is assumed that the clock driver will not have to respond to the “general call.”

10) Electrical Characteristics: All electrical characteristics must meet the standard mode specifications found in section 15 of the I^2C specification.

a) Pull-Up Resistors: Any internal resistor pull-ups on the SDATA and SCLOCK inputs must be stated in the individual datasheet. The use of internal pull-ups on these pins of below 100K is discouraged. Assume that the board designer will use a single external pull-up resistor for each line and that these values are in the 5 - 6K Ohm range. Assume one I^2C device per DIMM (serial presence detect), one I^2C controller, one clock driver plus one/two more I^2C devices on the platform for capacitive loading purposes.

b) Input Glitch Filters: Only fast mode I^2C devices require input glitch filters to suppress bus noise. The clock driver is specified as a standard mode device and is not required to support this feature.

11) PWR_DWN#: If a clock driver is placed in PWR_DWN# mode, the SDATA and SCLK inputs must be Tri-Stated and the device must retain all programming information. Idd current due to the I^2C circuitry must be characterized and in the datasheet.

For specific I^2C information consult the Philips I^2C Peripherals Data Handbook ICI2 (1996)

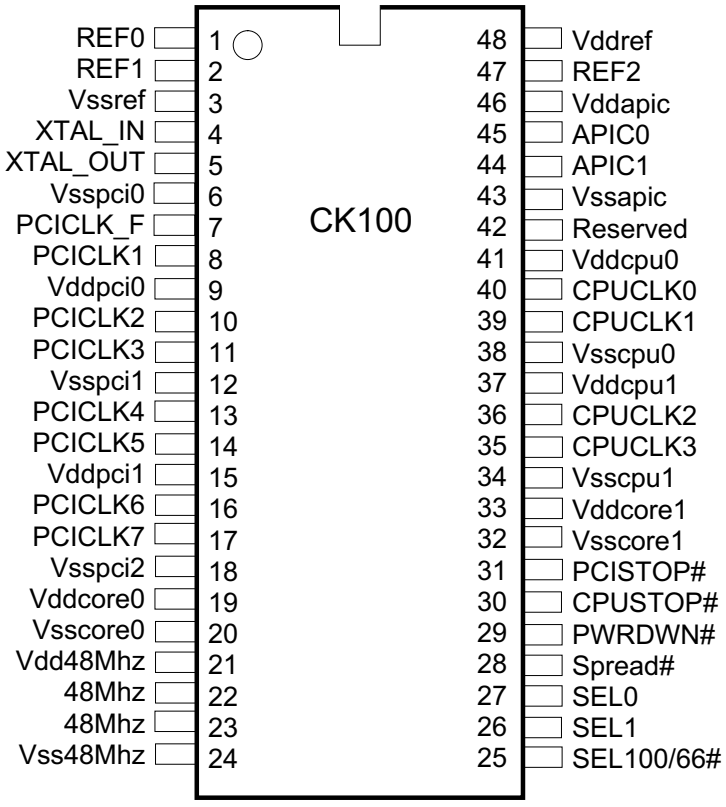
8. Appendices

8.1 Appendix A: CK100 28 and 48 SSOP Pinouts

The following Addendum defines generic pinouts and base requirements for Intel Architecture based desktop and mobile computing platforms. It is intended to be used with the 28 and 48 pin SSOP CKBF clock drivers described in Appendix B. This addendum can also be used as an example for development of other custom clock synthesizer/driver components. This is not the only solution that can be derived.

Features (48 SSOP Package):

- Four Copies of CPU Clock
- Eight Copies of PCI Clock (Synchronous w/CPU Clock)
- Two Copies of IOAPIC Clock @14.31818 MHz
- Two Copies of 48MHz Clock
- Three Copies of Ref. Clock @14.31818 MHz
- Ref. 14.31818MHz Xtal Oscillator Input
- 100MHz or 66MHz operation
- Power Management Control Input Pins
- Isolated core Vdd, Vss pins for noise reduction



Features (28 SSOP Package):

- Two Copies of CPU Clock
- Six Copies of PCI Clock (Synchronous w/CPU Clock)
- One Copy of Ref. Clock @14.31818 MHz
- Ref. 14.31818MHz Xtal Oscillator Input
- 100MHz or 66MHz operation
- Power Management Control Input Pins
- Isolated core Vdd, Vss pins for noise reduction

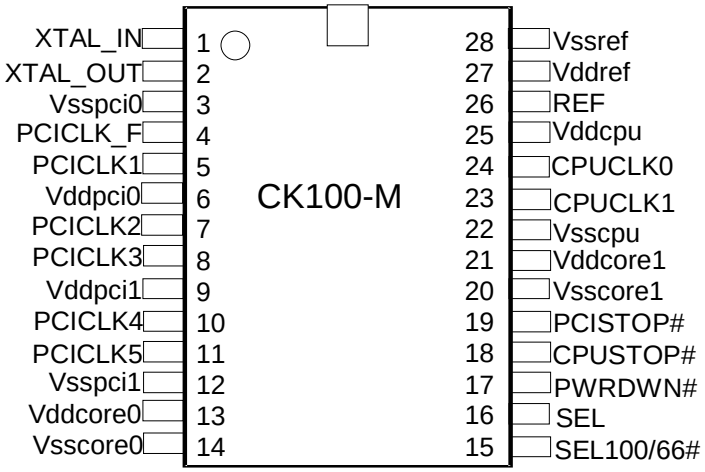


Table 8-1 CK100 Pin Description Table

28 Pin Package		48 Pin Package		Type	Symbol	Description
Pin	Qty	Pin	Qty			
26	1	1, 2, 47	3	output	REF [0-2]	14.318 MHz Clock output
28	1	3	1	ground	Vssref	Ground for Ref0-1 outputs
27	1	48	1	power	Vddref	Power for Ref0-1 outputs
1	1	4	1	input	XTAL_IN	14.318 MHz Crystal input
2	1	5	1	output	XTAL_OUT	14.318 MHz Crystal output
3, 12	2	6, 12, 18	3	ground	Vsspci [0-2]	Ground for PCI outputs
4	1	7	1	output	PCICLK_F	Free running PCI output
6, 9	2	9, 15	2	power	Vddpci [0-1]	Power for PCI outputs
5, 7, 8, 10, 11	5	8, 10, 11, 13, 14, 16, 17	7	output	PCICLK [1-7]	PCI Clock outputs. TTL compatible 3.3V
13, 21	2	19, 33	2	power	Vddcore [0-1]	Isolated power for core
14, 20	2	20, 32	2	ground	Vsscore [0-1]	Isolated ground for core
--	--	21	1	power	Vdd48MHz	Power for 48MHz outputs
--	--	24	1	ground	Vss48MHz	Ground for 48MHz outputs
--	--	22, 23	2	output	48MHz	48MHz outputs
--	--	26, 27	2	input	SEL[0-1]	Logic select pins. LVTTL levels
16	1	--	--	input	SEL	Logic select. LVTTL levels (note 3)
15	1	25	1	input	SEL100/66#	Select for enabling 100MHz or 66MHz H=100MHz, L=66MHz
17	1	29	1	input	PWRDWN#	Powers down device if held LOW
18	1	30	1	input	CPUSTOP#	Stops CPU clocks LOW if held LOW
19	1	31	1	input	PCISTOP#	Stops PCI clocks LOW if held LOW
25	1	37, 41	2	power	Vddcpu [0-1]	Power for CPU outputs
22	1	34, 38	2	ground	Vsscpu [0-1]	Ground for CPU outputs
23, 24	2	35, 36, 39, 40	4	outputs	CPUCLK0-3	CPU and Host clock outputs 2.5V
--	--	43	1	ground	Vssapic	Ground for Apic outputs
--	--	46	1	power	Vddapic	Power for Apic outputs
--	--	44, 45	2	outputs	APIC0-1	Apic output @2.5Volts. 14.31818 MHz
--	--	28	1	input	SPREAD#	OPTIONAL - Enables Spread Spectrum feature when LOW
--	--	42	1	reserved	reserved	Reserved for future modification

Notes:

1. Vdd and Vss names in the above table reflect a likely internal power and ground partition to reduce the effects of internal noise on the performance of the device. In reality, the platform will be configured with the Vddapic and Vddcpu pins tied to a 2.5V regulator, all remaining Vdd pins tied to a common 3.3V supply and all Vss pins being common. The Vdd/Vss naming convention above is done to show how the pinout is dominated by the need to isolate all the signals.

2. Reserved pins should be true no-connects. Can be treated as open circuit by current system platforms. There can be no external device requirements for these pins. Possible option includes additional IOAPIC or processor output.
3. SEL (pin 16 of the 28 pin package) does not map to either SEL[0-1] signals (pins 26 or 27 of the 48 pin package). Rather, SEL is the logical OR of SEL[0-1]. In order to maintain common silicon between both packages, the silicon pads of SEL[0-1] should both be connected to the package pin of SEL.

8.1.1 Spread Spectrum Clocking (SSC) Clarification:

Spread Spectrum functionality on the CK100 clock driver acts as an on/off switch for different forms of spread spectrum modulation techniques. Intel may or may not use this feature due to platform level timing issues. The following specifications are added to the current CK100 definition:

1. No external modulation frequency source is required by the CK100.
2. Vendor needs to synchronously modulate all the processor, and PCI output clocks. REF and fixed frequency 48MHz clock outputs are not modulated. If the APIC clocks are synchronous (16.6 MHz) to the processor they must be modulated. If the clocks are not synchronous (14.318 MHz) they must not be modulated.
3. All device timings (including jitter, skew, min-max clock period, output rise/fall time) MUST meet the existing non-spread spectrum specifications
4. All non-spread processor and PCI functionality must be maintained in the spread spectrum mode (includes all power management functions.)
5. The minimum clock period can't be violated. The preferred method is to adjust the spread technique to not allow for modulation above the nominal frequency. This technique is often called "down-spreading". An example triangular frequency modulation profile is shown in Figure 8-1. The modulation profile in a modulation period can be expressed as:

$$f = \begin{cases} (1-\delta) f_{nom} + 2 f_m \cdot \delta \cdot f_{nom} \cdot t & when \;\; 0 < t < \dfrac{1}{2 f_m}; \\ (1+\delta) f_{nom} - 2 f_m \cdot \delta \cdot f_{nom} \cdot t & when \;\; \dfrac{1}{2 f_m} < t < \dfrac{1}{f_m}, \end{cases}$$

where f_{nom} is the nominal frequency in the non-SSC mode, f_m is the modulation frequency, • is the modulation amount, and t is time.

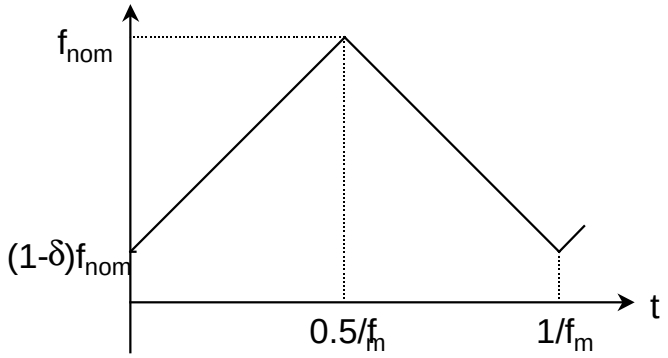


Figure 8-1 Triangular Frequency Modulation Profile.

6. The clock frequency deviation is required to be no more than the amount specified in the table below The absolute spread amount after fundamental frequency is shown below as the width of its spectral distribution (between the -3dB roll-off.) The ratio of this width to the fundamental frequency cannot exceed the maximum allowed below for each specific frequency and modulation profile. This parameter can be measured in the frequency domain using a spectrum analyzer. The amount of allowed spreading for any non-triangular modulation is determined by the induced downstream PLL tracking skew (see explanation in 8), which cannot exceed 140 pS.

Table 8-2 Maximum Allowed Spread Amount

Modulation Type	Fmod = 30 KHz	Fmod = 50 KHz
Linear (triangular)	0.8 %	0.6 %
Non-Linear	0.7 %	0.5 %

The maximum allowed spread values are intended to be met for both 100 and 66 MHz clocks. Variation from table 8-2 is the responsibility of the clock supplier and the user (see note 9 for more details.)

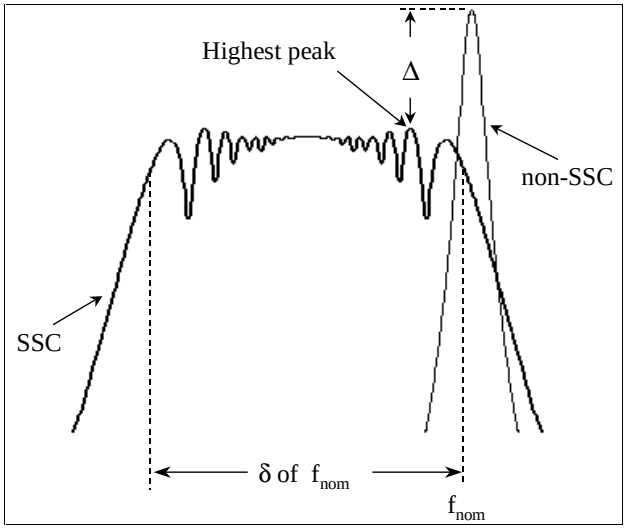


Figure 8-2 Spectral Fundamental Frequency Comparison

7. To achieve sufficient system-level EMI reduction, it is desired that SSC reduce the spectral peaks in the non-SSC mode by the amount specified below. The peak reduction is defined as shown in figure 8-2, as the difference between the spectral peaks in SSC and non-SSC modes at the specified measurement frequency.

Table 8-3 Desired Peak Amplitude Reduction by SSC.

CPU Clock Freq.	Peak Reduction Δ	Measurement Freq.
66 MHz	7 dB	600 MHz (9th harmonics)
100 MHz	7 dB	700 MHz (7th harmonics)

Notes:

a) The spectral peak reduction is not necessarily the same as the system EMI reduction. However, this relative measurement gives the component-level indication of SSC's EMI reduction capability at the system level.

b) It is recommended that a spectrum analyzer should be used for this measurement. The spectrum analyzer should have measurement capability out to 1 GHz. The measured SSC clock needs to be fed into the spectrum analyzer via a high-impedance probe compatible with the spectrum analyzer. The output clock should be loaded with 20 pF capacitance. The resolution bandwidth of the spectrum analyzer needs to be set at 120 KHz to comply with FCC EMI measurement requirements. The video band needs to be set at higher than 300 KHz for appropriate display. 100 KHz may be used as the resolution bandwidth in case of measurement equipment limitation. The display should be set with maximum hold. The corresponding harmonic peak readings should be recorded in both the non-SSC and the SSC modes, and be compared to determine the magnitude of the spectral peak reduction.

8. The modulation frequency of SSC is required to be in the range of 30-50 KHz to avoid audio band demodulation and to minimize system timing skew. The modulation frequency is desired to be in the range of 30-33 KHz for downstream PLLs to accurately track the frequency modulation. The downstream PLL tracking skew, i.e., the accumulative phase difference between the downstream PLL input and output clocks, is shown in Figure 8-3, as functions of modulation frequency, modulation profile, and spread amount. This plot is obtained through PLL behavior simulations assuming a jitter-free ideal modulated input clock to the PLL. The parameters of the simulated PLL are:

(VCO gain) * (charge-pump current) = 2800 (Hz/V)(A),
feedback divider•••••2nd-order filter:•C_1 = 11 pF; C2 = 356 pF; R = 9.75 k••

9. This skew should be minimized as it reduces system timing margins. Different system implementations have different requirements and PLL characteristics, and may require tighter/looser skew. It is always true that lower modulation frequency results in smaller tracking skew. The skew is proportional to the amount of spreading. **Any implemented modulation profile must induce less than 140-pS skew with the above PLL parameters by properly adjusting its spread amount. Sinusoidal modulation is discouraged due to its low peak reduction capability.**

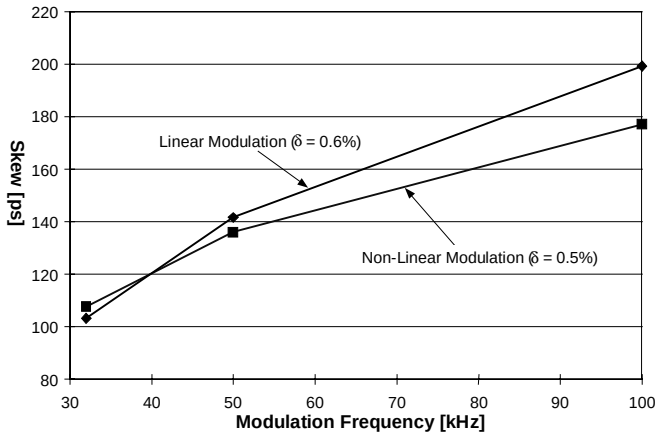


Figure 8-3 Downstream PLL tracking skew and modulation frequency

Table 8-4 CK100 Select Functions

SEL100/66 #	SEL1 (48 pin)	SEL0 (48 pin)	SEL (28 pin)	Function	Notes
0	0	0	0	Tri-State	1
0	0	1	-	(Reserved)	
0	1	0	-	(Reserved)	
0	1	1	1	Active 66MHz	
1	0	0	0	Test Mode	1
1	0	1	-	(Reserved)	
1	1	0	-	(Reserved)	
1	1	1	1	Active 100MHz	

Function Description	Outputs					
	CPU	PCI, PCI_F	48MHz	REF0:2	IOAPIC	Notes
Tri-State	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	
Test Mode	TCLK/2	TCLK/6	TCLK/2	TCLK	TCLK	2, 3

Notes:

1. Requires internal decode logic for all three select inputs for 48 pin device, two inputs for 28 pin device.
2. TCLK is a test clock over driven on the XTAL_IN input during test mode.
3. Range of reference frequency allowed is min = 14.316 nominal = 14.31818 MHz, max = 14.32 MHz.
4. Frequency accuracy of 48MHz must be +167PPM to match USB default. See Section 3.3 for details.

8.1.2 CK100 System Considerations:

The SEL100/66# frequency select pin requires a specific motherboard pull-up resistor to 3.3 Volts to allow the CK100 device to sense the maximum Host bus frequency of the processor to automatically configure the CK100 to either 100MHz or 66MHz. The nominal resistor value for desktop (slot one) applications is 200 Ohms with a maximum allowed tolerance of +/-5%. The power dissipation of the resistor is less than 1/16 Watts. For mobile applications this resistor value is not critical and the typical external resistor value is 10 - 100K Ohms.

No internal pull-up or pull-down resistors are allowed on the SEL100/66# pin.

Table 8-5 CK100 Driver types used

28 Pin Package	48 Pin Package	Driver Type	Symbol	Description
26	1, 2, 47	Type 2	REF0-2	14.318 MHz Clock outputs. 3.3V
4	7	Type 5	PCICLK_F	Free Running clock during PCICLK stopped. 3.3V
5, 7, 8, 10, 11	8, 10, 11, 13, 14, 16, 17	Type 5	PCICLK	PCI Clock outputs TTL compatible 3.3V.
23, 24	35, 36, 39, 40	Type 1	CPUCLK	CPU and Host clock outputs 2.5V
-	44, 45	Type 2	APIC	IOAPIC clock output 2.5V
-	22, 23	Type 3	48MHz	48MHz clock output 3.3V

8.1.3 CK100 Power Management

The following power consumption conditions for the device should be provided by each vendor. The values below are estimates of target specifications for the 48 SSOP pinouts. The power consumption should be clearly lower for the lower pincount devices.

CK100 Condition	Max 2.5V supply consumption Max discrete cap loads, Vddq2 = 2.625V All static inputs = Vddq3 or Vss	Max 3.3V supply consumption Max discrete cap loads Vddq3 = 3.465V All static inputs = Vddq3 or Vss.
Powerdown Mode (PWRDWN# = 0)	100uA	500uA
Active 66MHz SEL100/66# = 0	72mA	170mA
Active 100MHz SEL100/66# = 1	100mA	170mA

The powerdown controller provides a signal that is latched with its own copy of the free running PCI clock. In theory, this should be synchronous with the clock driver output IF the following is quantified:

a) The flight time of the clock trace from PCI_F to the controller
b) Input edge-rate at the controller, controller input load, set/hold time at controller.
c) Variance of output edge-rate from PCI_F of clock driver
d) Internal delay from output of PCI_F on clock driver to internal clock signal

However, the large number of platform level variables that must be taken into account for the input to be described as “synchronous” to the clock driver output is large and highly dependent on the board design. To simplify the platform design, the CPU_STOP# and the PCI_STOP# inputs are defined to be ASYNCHRONOUS from the clock driver external PCI_F clock. The clock driver must synchronize the input signal and resynchronize it with its own PCI_F clock output. This leaves the board timing issues up to the board designer rather than the clock vendor.

Clock sequencing must always guarantee full clock timing parameters at all times after the system has initially powered up except where noted. During power up and power down operations using the PWR_DWN# select pin, partial clocks are not allowed and all clock timing parameters must be met except for the following: It is understood that the first clock pulse coming out of a stopped clock condition could be slightly distorted due to clock network charging requirements. Allowable distortion parameters will be supplied at a later date. It is also understood that board routing and signal loading have a large impact on the initial clock distortion.

Table 8-6 CK100 Clock Enable Configuration

CPU_STOP#	PCI_STOP#	PWR_DWN#	CPUCLK	PCICLK	Other Clocks	Crystal	VCO's
X	X	0	low	low	Stopped	off	off
0	0	1	low	low	running	running	running
0	1	1	low	33 MHz	running	running	running
1	0	1	100/66 MHz	low	running	running	running
1	1	1	100/66 MHz	33 MHz	running	running	running

Table 8-7 CK100 Power Management Requirements

Signal	Signal State	Latency
		No. of rising edges of free running PCICLK
CPU_STOP#	0 (disabled)	1
	1 (enabled)	1
PCI_STOP#	0 (disabled)	1
	1 (enabled)	1
PWR_DWN#	1 (normal operation)	3 mS
	0 (power down)	2 max.

Notes:

1. Clock on/off latency is defined in the number of rising edges of free running PCICLKs between the clock disable goes low/high to the first valid clock comes out of the device.
2. Power up latency is when PWR_DWN# goes inactive (high) to when the first valid clocks are driven from the device.

CPU_STOP# is an input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CPU_STOP# is asserted asynchronously by the external clock control logic with the rising edge of free running PCI clock (and hence CPU clock) and must be internally synchronized to the external PCI_F output. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks must always be stopped in a low state and started in such a manner as to guarantee that the high pulse width is a full pulse. CPU clock on latency needs to be **2 or 3 CPU clocks** and CPU clock off latency needs to be **2 or 3 CPU clocks**.

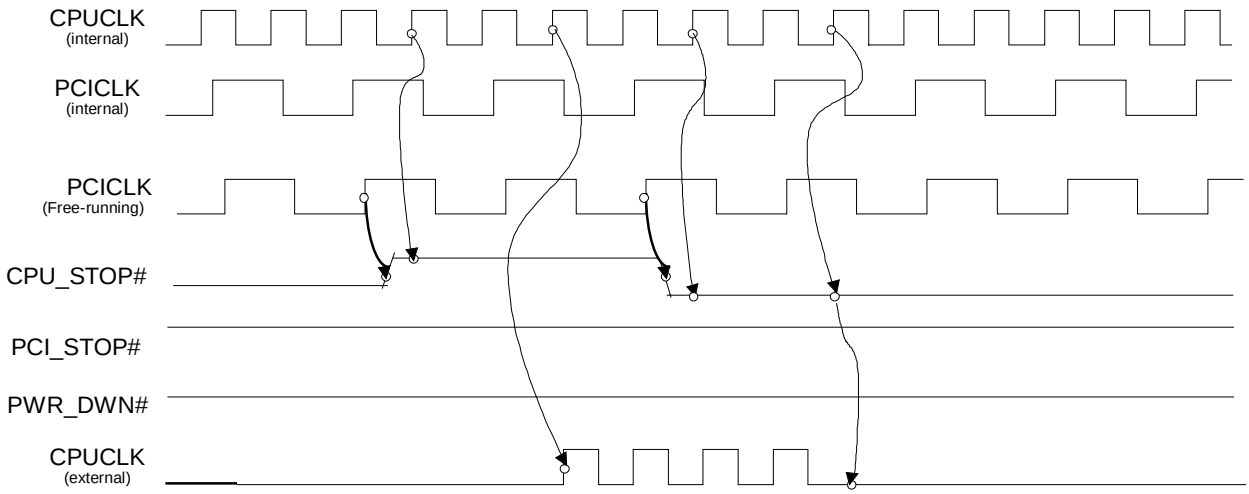


Figure 8-4 CK100 CPU_STOP# Timing Diagram

Notes:

1. All timing is referenced to the CPUCLK
2. The Internal label means inside the chip and is a reference only. This in fact may not be the way that the control is designed.
3. CPU_STOP# signal is an input signal that must be made synchronous to free running PCI_F
4. ON/OFF latency shown in the diagram is 2 CPU clocks.
5. All other clocks continue to run undisturbed.
6. PWR_DWN# and PCI_STOP# are shown in a high state.
7. Diagrams shown with respect to 66MHz. Similar operation as CPU=100MHz

PCI_STOP# is an input to the clock synthesizer and must be made synchronous to the clock driver PCI_F output. It is used to turn off the PCI clocks for low power operation. PCI clocks are required to be stopped in a low state and started such that a full high pulse width is guaranteed. There is **ONLY one rising edge of external PCICLK** after the clock control logic.

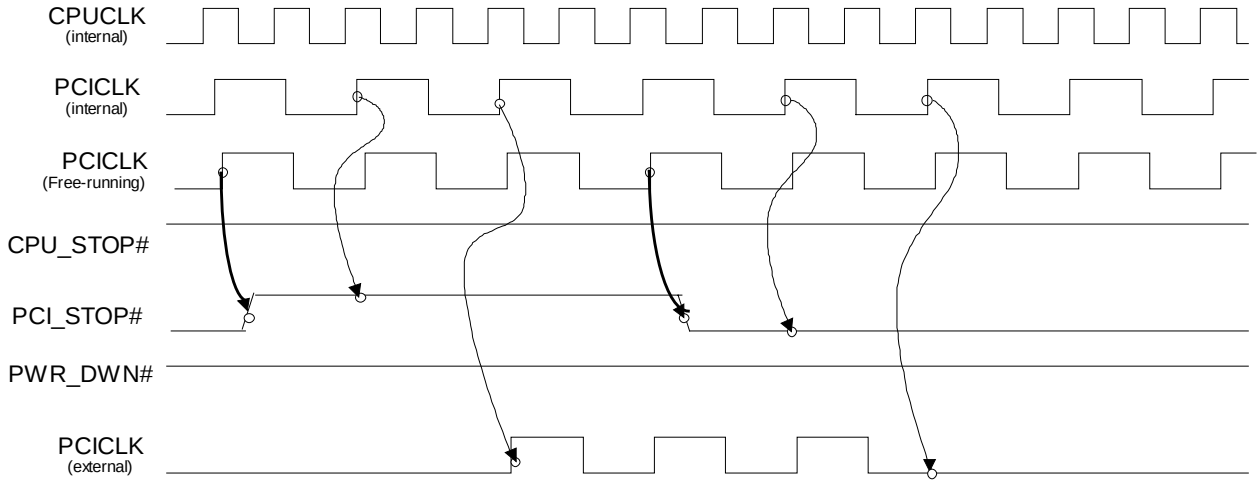


Figure 8-5 CK100 PCI_STOP# Timing Diagram

Notes:

1. All timing is referenced to the CPUCLK.
2. PCI_STOP# signal is an input signal which must be made synchronous to PCI_F output.
3. Internal means inside the chip.
4. All other clocks continue to run undisturbed.
5. PWR_DWN# and CPU_STOP# are shown in a high state.
6. Diagrams shown with respect to 66MHz. Similar operation as CPU=100MHz

The power down selection is used to put the part into a very low power state without turning off the power to the part. PWR_DWN# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer. PWR_DWN# is an asynchronous function for powering up the system. Internal clocks are not running after the device is put in power down. When PWR_DWN# is active low all clocks need to be driven to a low value and held prior to turning off the VCO's and the Crystal. The power on latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. PCI_STOP# and CPU_STOP# are considered to be don't cares during the power down operations. The REF0 clock is also expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF0 clock output in the LOW state may require more than one clock cycle to complete.

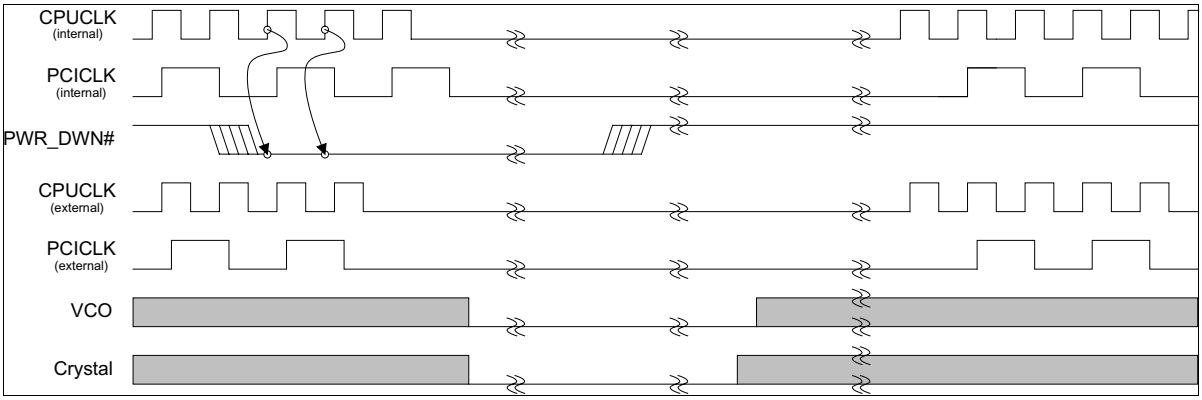


Figure 8-6 CK100 PWR_DWN# Timing Diagram

Notes:

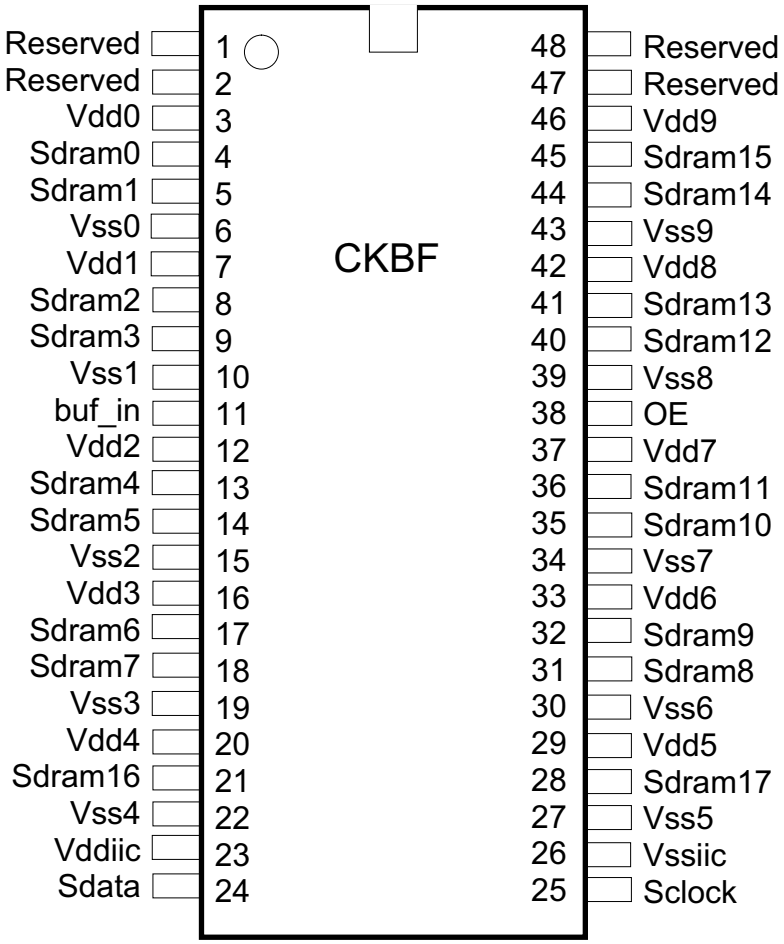
1. All timing is referenced to the CPUCLK
2. Internal means inside the chip
3. PWR_DWN# is an asynchronous input and metastable conditions could exist. This signal is required to be synchronized inside the part.
4. The Shaded sections on the VCO and the Crystal signals indicate an active clock
5. Diagrams shown with respect to 66MHz. Similar operation as CPU=100MHz

8.2 Appendix B: CKBF 28 and 48 SSOP Pinouts

The following Addendum defines generic pinouts and base requirements for Intel Architecture based desktop and mobile computing platforms. It is intended to be used with the 28 pin or 48 pin SSOP CK100 clock drivers described in Appendix A. This addendum can also be used as an example for development of other custom clock synthesizer/driver components. This is not the only solution that can be derived.

Features (48 SSOP Package):

- High speed, low noise non-inverting 1-18 buffer for SDRAM clock buffer applications
- Supports up to four SDRAM DIMMS
- I^2C Serial Configuration interface
- Multiple Vdd, Vss pins for noise reduction
- Separate Tri-State pin for testing



Features (28 SSOP Package):

- High speed, low noise non-inverting 1-10 buffer for SDRAM clock buffer applications
- Supports up to four SDRAM SO-DIMMS
- I^2C Serial Configuration interface
- Multiple Vdd, Vss pins for noise reduction
- Separate Tri-State pin for testing

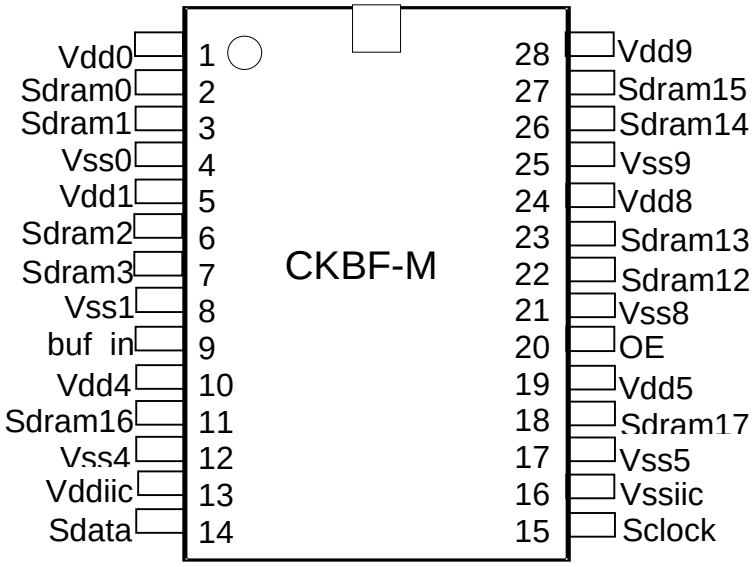


Table 8-8 CKBF Pin Description Table

28 Pin Package		48 Pin Package		Type	Symbol	Description
Pin	Qty	Pin	Qty			
2, 3, 6, 7	4	4, 5, 8, 9	4	output	SDRAM [0-3]	SDRAM Byte 0 clock output
--	--	13, 14, 17, 18	4	output	SDRAM [4-7]	SDRAM Byte 1 clock output
--	--	31, 32, 35, 36	4	output	SDRAM [8-11]	SDRAM Byte 2 clock output
22, 23, 26, 27	4	40, 41, 44, 45	4	output	SDRAM [12-15]	SDRAM Byte 3 clock output
11, 18	2	21, 28	4	output	SDRAM [16-17]	SDRAM clock outputs useable for feedback
9	1	11	1	input	buf_in	Input for 1-18 buffer
20	1	38	1	input	OE	Tri-States all outputs when held LOW
14	1	24	1	I/O	Sdata	Data pin for I^2C circuitry
15	1	25	1	I/O	Sclock	Clock pin for I^2C circuitry
1, 5, 10, 19, 24, 28	6	3, 7, 12, 16, 20, 29, 33, 37, 42, 46	10	power	Vdd [0-9]	3.3 Volt Power Supply for SDRAM buffer
4, 8, 12, 17, 21, 25	6	6, 10, 15, 19, 22, 27, 30, 34, 39, 43	10	ground	Vss [0-9]	Ground for SDRAM buffer
13	1	23	1	power	Vddiic	3.3 Volt Power Supply for I^2C circuitry
16	1	26	1	ground	Vssiic	Ground for I^2C circuitry
--	--	1, 2, 47, 48	4	Reserved	Reserved	Reserved for future modifications

Notes:

1. Vdd and Vss names in the above table reflect a likely internal power and ground partition to reduce the effects of internal noise on the performance of the device. In reality, the platform will be configured with all Vdd pins tied to a common 3.3V supply and all Vss pins common.
2. Reserved pins should be true no-connects. Can be treated as open circuit by current system platforms. There can be no external device requirements for these pins. Possible option includes additional control inputs for bank select capability.

Table 8-9 CKBF Functionality

OE	SDRAM[0-3]	SDRAM[4-7]	SDRAM[8-11]	SDRAM[12-15]	SDRAM[16-17]	Notes
0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	1
1	1 X buf_in	1 X buf_in	1 X buf_in	1 X buf_in	1 X buf_in	2

Notes:

1. Used for test purposes only.
2. Buffer is Non-inverting.

8.2.1 CKBF Default Conditions

At power up all SDRAM outputs are enabled and active. OE should have a >100 K Ohm internal pull-up resistor to keep all outputs active. The Sdata and Sclock inputs should both also have internal pull-up resistors with values above 100K Ohms as well for complete platform flexibility.

Table 8-10 CKBF Driver types used

Pin	Driver	Symbol	Description
All SDRAM	Type 4	SDRAM [0-17]	SDRAM outputs

8.2.2 CKBF Serial Configuration Map

A) The serial bits will be read by the clock driver in the following order:

Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0
Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0
.
Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0

B) All unused register bits (reserved and N/A) should be designed as don't care. It is expected that the controller will force all of these bits to a "0" level.

C) All register bits labeled "Initialize to 0" must be written to zero during initialization. Failure to do so may result in a higher then normal operating current. The controller will read back the last written value.

Byte 0 : SDRAM Active/Inactive Register (1 = enable, 0 = disable)

Bit	CKBF 28 Pin	CKBF 48 Pin	Name	48 Pin Description	28 Pin Description
Bit 7	--	18	SDRAM7	(Active/Inactive)	Initialize to 0
Bit 6	--	17	SDRAM6	(Active/Inactive)	Initialize to 0
Bit 5	--	14	SDRAM5	(Active/Inactive)	Initialize to 0
Bit 4	--	13	SDRAM4	(Active/Inactive)	Initialize to 0
Bit 3	7	9	SDRAM3	(Active/Inactive)	(Active/Inactive)
Bit 2	6	8	SDRAM2	(Active/Inactive)	(Active/Inactive)
Bit 1	3	5	SDRAM1	(Active/Inactive)	(Active/Inactive)
Bit 0	2	4	SDRAM0	(Active/Inactive)	(Active/Inactive)

Notes:

1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation,

Byte 1: SDRAM Active/Inactive Register (1 = enable, 0 = disable)

Bit	CKBF 28 Pin	CKBF 48 Pin	Name	48 Pin Description	28 Pin Description
Bit 7	27	45	SDRAM15	(Active/Inactive)	(Active/Inactive)
Bit 6	26	44	SDRAM14	(Active/Inactive)	(Active/Inactive)
Bit 5	23	41	SDRAM13	(Active/Inactive)	(Active/Inactive)
Bit 4	22	40	SDRAM12	(Active/Inactive)	(Active/Inactive)
Bit 3	--	36	SDRAM11	(Active/Inactive)	Initialize to 0
Bit 2	--	35	SDRAM10	(Active/Inactive)	Initialize to 0
Bit 1	--	32	SDRAM9	(Active/Inactive)	Initialize to 0
Bit 0	--	31	SDRAM8	(Active/Inactive)	Initialize to 0

Notes:

1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation,

Byte 2: Optional Register For Possible Future Requirements

Bit	CKBF 28 Pin	CKBF 48 Pin	Name	48 Pin Description	28 Pin Description
Bit 7	18	28	SDRAM17	(Active/Inactive)	(Active/Inactive)
Bit 6	11	21	SDRAM16	(Active/Inactive)	(Active/Inactive)
Bit 5	--	--	(Reserved)	(Reserved)	(Reserved)
Bit 4	--	--	(Reserved)	(Reserved)	(Reserved)
Bit 3	--	--	(Reserved)	(Reserved)	(Reserved)
Bit 2	--	--	(Reserved)	(Reserved)	(Reserved)
Bit 1	--	--	(Reserved)	(Reserved)	(Reserved)
Bit 0	--	--	(Reserved)	(Reserved)	(Reserved)

Notes:

1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.

8.3 CKBF Power Management

The following power-consumption conditions for the device should be provided by each vendor.
The values below are estimates of target specifications. Estimates are based upon 48 SSOP devices.

CKBF Condition	Max 3.3V supply consumption Max discrete cap loads Vddq3 = 3.465V All static inputs = Vddq3 or Vss.
No Clock Mode (buf_in = Vddq3 or Vss) Internal I^2C Circuitry Active	3mA
Active 66MHz (buf_in = 66.66 MHz)	230mA
Active 100MHz (buf_in = 100.00 MHz)	360mA

8.4 Appendix C: CK100-SM Pinout and Mobile Buffer Characteristic

8.5 CK100-SM 28 SSOP Pinout

The following Addendum defines generic pinout and base requirements for Intel Architecture based mobile computing platforms. It is intended to be an alternate solution for the 28 pin SSOP CK100-M clock drivers described in Appendix A. This solution contains spread spectrum functionality and 48 MHz outputs in a 28 pin package. The spread spectrum will apply only to those clocks that synchronize to the processor clocks (CPU, SDRAM and PCI clocks). The spread spectrum will not affect the asynchronous clocks (Reference and 48 MHz). This addendum can also be used as an example for development of other custom clock synthesizer/driver components. This is not the only solution that can be derived.

8.5.1 Features (28 SSOP Package):

- Two Copies of CPU Clock
- Five Copies of PCI Clock (Synchronous w/CPU Clock)
- One Copy of free running PCI Clock (Synchronous w/CPU Clock)
- Two Copies of Ref. Clock @14.31818 MHz
- One Copy of 48 MHz
- One Copy of selectable 48/24 MHz
- Ref. 14.31818MHz X'tal Oscillator Input
- 100MHz or 66MHz operation
- Power Management Control Input Pins
- Isolated core Vdd, Vss pins for noise reduction

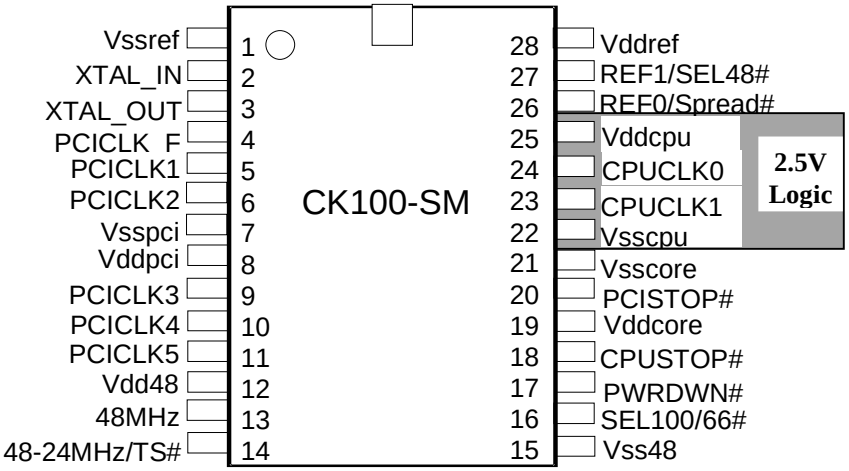


Table 8-11 CK100-SM Pin Description Table

28 Pin Package		Type	Symbol	Description
Pin	Qty			
1	1	Power	Vssref	Ground for 14.318 MHz reference clock outputs
2	1	Input	XTAL_IN	14.318 MHz Crystal input
3	1	Output	XTAL_OUT	14.318 MHz Crystal output
4	1	Output	PCICLK_F	3.3V free running PCI clock output
5, 6, 9, 10, 11	5	Output	PCICLK [1-5]	3.3V PCI Clock outputs
7	1	Power	Vsspci	Ground for PCI clock outputs
8	1	Power	Vddpci	3.3V power for PCI clock outputs
12	1	Power	Vdd48	3.3V power for 48/24 MHz clocks
13	1	Output	48MHz	3.3V 48MHz clock output
14	1	Output	48-24MHz/TS#	3.3V 48 or 24 MHz output and Tri-state strapping option (see note 2). Strap Low = Enter Tri-State mode for testing, Strap High = Normal operation.
15	1	Power	Vss48	Ground for 48/24MHz clocks
16	1	Input	SEL100/66#	Select for enabling 100MHz or 66MHz CPU clock High =100MHz, Low =66MHz
17	1	Input	PWRDWN#	Device enters power down mode when LOW
18	1	Input	CPUSTOP#	When signal Low, stop CPU clocks in LOW state
19	1	Power	Vddcore	Isolated 3.3V power for core
20	1	Input	PCISTOP#	When signal LOW, Stops all PCI clocks in LOW state except for PCICLK_F output
21	1	Power	Vsscore	Isolated ground for core
22	1	Power	Vsscpu	Ground for CPU clock outputs
23, 24	1	Output	CPUCLK[1-0]	2.5V CPU clock outputs
25	1	Power	Vddcpu	2.5V power for CPU clock outputs
26	1	Output	REF0/Spread#	3.3V 14.318 MHz reference clock output and power-on spread spectrum enable strap option (see note 3). Strap Low = Spread spectrum clocking enable, Strap High = Spread spectrum clocking disable.
27	1	Output	REF1/SEL48#	3.3V 14.318 MHz reference clock output and power-on 48/24 MHz select strap option (see note 4). Pin 14 output pin = 48 MHz when strapped Low, Pin 14 output pin = 24 MHz when strapped High.
28	1	Power	Vddref	3.3V power for 14.318 MHz reference clock outputs

Notes:

1. Vdd and Vss names in the above table reflect a likely internal power and ground partition to reduce the effects of internal noise on

the performance of the device. In reality, the platform will be configured with the same voltage Vdd pins tied to a common supply and all Vss pins being common. The Vdd/Vss naming convention above is done to show how the pinout is dominated by the need to isolate all the signals.

2. The output frequency at this pin is dependent on the power on strapping option at pin 27. A 48 MHz output when power on strapped Low and 24 MHz output when strapped High. This pin also serve as Tri-Sate strapping option during power on configuration. The CK100-SM will sample the value at this pin during power on. Strapped Low for Tri-State mode and high for normal operation. The pull up/down resistor value at this pin shall be 100K Ohms.
3. Pin 26 is a dual function pin. During power on, all clock outputs are disabled, the CK100-SM will sample the spread spectrum enable/disable strapping option. After the strapped value latches, all clock outputs will be enabled simultaneously and this pin will become a 14.318 MHz reference clock output. The Power on latency needs to be less than 3 mS after the supply voltage stabilized. The external pull up/down resistor value at this pin shall be 100K Ohms.
4. Pin 27 is a dual function pin. During power on, all clock outputs are disabled, the CK100-SM will sample the “48/24 MHz clock output frequency ” strapping option. After the strapped value latches, all clock outputs will be enabled simultaneously and this pin will become another 14.318 MHz reference clock output. The Power on latency needs to be less than 3 mS after the supply voltage stabilized. The external pull up/down resistor value at this pin shall be 100K Ohms.

8.5.2 Mobile Clock Buffer Specifications: 2.5 Volt, 3.3 Volt and PCI Clocks

The V/I curves, and Trise/Tfall specifications are targeted at achieving acceptable switching behavior under the load conditions as described in section 4 of this specification. Pull-up and pull-down sides for each of the buffers have separate V/I curves which are provided in the following sections. The DC drive curve specifies steady state conditions that must be maintained, but does not indicate real output drive strength.

AC parameters must be guaranteed under transient switching (AC) conditions. The sign on all current parameters (direction of current flow) is referenced to a ground inside the component; i.e. positive currents flow into the component while negative currents flow out of the component.

The mobile clock buffer characteristics are the same as the desktop version (CK100) with the exception of CPU and SDRAM clock buffers. Mobile platforms should use the buffer characteristic supplied in this appendix for simulation along with the Intel mobile layout guideline (document title: MOBILE PENTIUM® II PROCESSOR/440BX AGPSET ADVANCED PLATFORM RDDP-a) for PCB layout.

Buffer Name	VCC Range (V)	Impedance (Ohms)	Buffer Type
CPU (mobile)	2.375 - 2.625	6.8 - 17.3	Type 1
48MHz, REF	3.135 - 3.465	20 - 60	Type 3
SDRAM (mobile)	3.135 - 3.465	4.7- 12.3	Type 4
PCI	3.135 - 3.465	12 - 55	Type 5

8.5.3 Type 1: Mobile CPU (2.5V) Buffer Characteristics

Table 8-12 Type 1: Mobile CPU Clock Buffer Operating Requirements

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
I_{ohmin}	Pull-Up Current	Vout = 1.0 V	-82			mA	1
I_{ohmax}	Pull-Up Current	V_{out} = 2.375 V			-67	mA	1
I_{olmin}	Pull-Down Current	V_{out} = 1.2 V	81			mA	1
I_{olmax}	Pull-Down Current	V_{out} = 0.3 V			60	mA	1
t_{rh}	2.5V Type 1 Output Rise Edge Rate	2.5V ±5% @ 0.4V - 2.0V	1/1		4/1	V/ns	2
t_{fh}	2.5V Type 1 Output Fall Edge Rate	2.5V ±5% @ 2.0V - 0.4V	1/1		4/1	V/ns	2

Notes:
1. Intended to approximate impedance curve below. Device should be checked against entire curve for characterization testing. Production testing is expected to be a subset of characterization testing.
2. Output rise and fall time. See Figure 4-1 for calculation / measurement information.
3. Output rise and fall time must be guaranteed across VCC , process and temperature range.
4. Receiver logic thresholds are Vil=0.7 and Vih=1.7 Volts.
5. Ron 6.8-17.3 Ohm with a 12 Ohm nominal driver impedance.
6. Ron = Vout/Ioh, Vout/Iol measured at VCC/2.

Pull-Up			
Voltage (V)	I-min (mA)	I-typ (mA)	I-max (mA)
0	-84	-149.8	-214
0.4	-84	-149.8	-214
0.6	-84	-149.8	-214
0.8	-84	-149.8	-214
1	-82	-148	-210
1.2	-78.7	-143	-205
1.4	-73	-138	-196
1.6	-66	-128.1	-186
1.8	-58.3	-118.9	-173
1.9	-54	-113.9	-162.7
2	-46.3	-103.6	-147.9
2.1	-37	-91.5	-131.1
2.2	-27.4	-78.9	-113
2.28	-16.4	-60	-94.7
2.375	0	-39	-67
2.5		0	-34
2.625			0

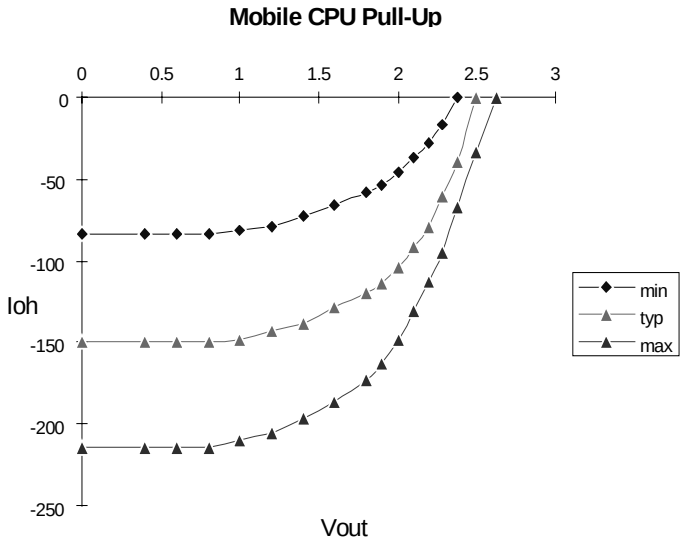


Figure 8-7 Type 1: Mobile CPU Clock Output Buffer Pull-Up Characteristics

Notes:
1. Must meet the temperature and voltage range specified in Table 2-3 DC Operating Requirements.
2. This drawing is not to scale. Comparisons should be made to the data provided in the table next to this drawing and to Table 8-12 Type 1: Mobile CPU Clock Buffer Operating Requirements.

Pull-Down			
Voltage	I-min	I-typ	I-max
(V)	(mA)	(mA)	(mA)
0	0	0	0
0.1	9	16	22
0.2	18	30	42
0.3	27	44	60
0.4	36	58	80
0.5	45	71	96
0.6	51	82	112
0.7	57	92	126
0.8	63	102	140
0.9	69	112	154
1	74	119	166
1.1	77.9	126	176
1.2	81	134	186
1.3	82.7	138	194
1.4	85.6	142	200
1.6	87	150	212.5
1.8	87	154.8	220
2	87	155	224
2.2	87	155	225
2.375	87	155	224
2.5		155	223.1
2.625			222

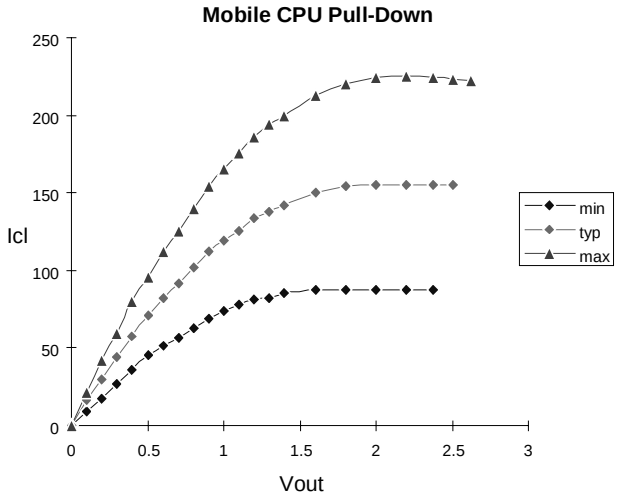


Figure 8-8 Type 1: Mobile CPU Clock Output Buffer Pull-Down Characteristics

Notes:

1. Must meet the temperature and voltage range specified in Table 2-3 DC Operating Requirements.
2. This drawing is not to scale. Comparisons should be made to the data provided in the table next to this drawing and to Table 8-12 Type 1: Mobile CPU Clock Buffer Operating Requirements.

8.5.4 Type 4: Mobile SDRAM (3.3 V) Clock Buffer Characteristics

Table 8-13 Type 4: Mobile SDRAM Clock Operating Requirements

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
I_{ohmin}	Pull-Up Current	Vout = 2.0 V	-79			mA	1
I_{ohmax}	Pull-Up Current	V_{out} = 3.135 V			-40	mA	1
I_{olmin}	Pull-Down Current	V_{out} = 1.0V	90			mA	1
I_{olmax}	Pull-Down Current	V_{out} = 0.4 V			85.5	mA	1
$t_{rhSDRAM}$	3.3V Type 4 Output Rise Edge Rate. Mobile SDRAM ONLY.	3.3V ±5% @ 0.4V - 2.4V	1.5		4/1	V/ns	2, 7
$t_{fhSDRAM}$	3.3V Type 4 Output Fall Edge Rate. Mobile SDRAM ONLY.	3.3V ±5% @ 2.4V - 0.4V	1.5		4/1	V/ns	2, 7

Notes:
1. Intended to approximate impedance curve below. Device should be checked against entire curve for characterization testing. Production testing is expected to be a subset of characterization testing.
2. Output rise and fall time. See Figure 4-1 for calculation / measurement information.
3. Output rise and fall time must be guaranteed across VCC , process and temperature range.
4. Receiver logic thresholds are Vil=0.8 and Vih=2.0 Volts.
5. Ron 4.7-12.3 Ohm with a 8.5 Ohm nominal driver impedance.
6. Ron = Vout/Ioh, Vout/Iol measured at VCC/2.
7. 1.5V/nS required to meet 1.2V/nS minimum rise/fall time at SDRAM input. This is required to guarantee SDRAM component timings which are tested/specified with a maximum of 1.2nS from 0.8V to 2.0V threshold levels.

Pull-Up			
Voltage	I-min	I-typ	I-max
(V)	(mA)	(mA)	(mA)
0	-113	-214.9	-330.6
1	-110.5	-190.2	-292.6
1.4	-104.1	-169.7	-261
1.5	-101.2	-164	-252.3
1.6	-98.3	-158.3	-243.6
1.7	-93.7	-152.7	-234.9
1.8	-89.3	-147	-226.2
1.9	-84	-141.4	-217.5
2	-79.1	-135.7	-208.8
2.4	-52.7	-101.8	-160
2.6	-41.1	-87.7	-130.5
3	-14.7	-44.8	-71.3
3.1	-8.7	-34	-54
3.18	0	-19.3	-40
3.3		0	-24.1
3.465			0

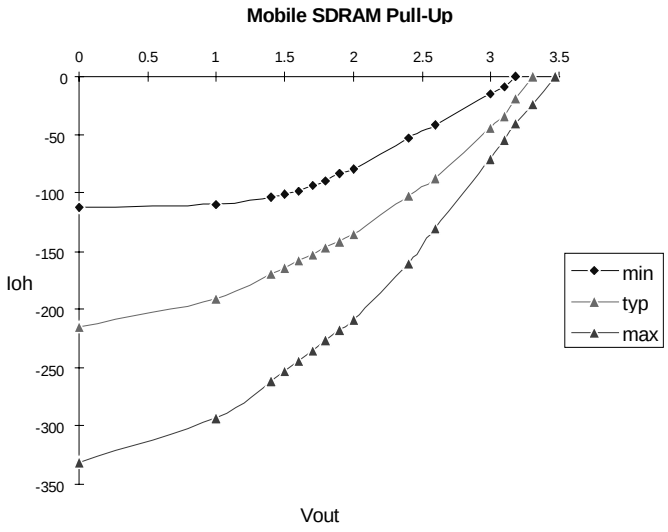


Figure 8-9 Type 4: Mobile SDRAM Clock Output Buffer Pull-Up Characteristics

Notes:
1. Must meet the temperature and voltage range specified in Table 2-3 DC Operating Requirements.
2. This drawing is not to scale. Comparisons should be made to the data provided in the table next to this drawing and to Table 8-13 Type 4: Mobile SDRAM Clock Operating Requirements.

Pull-Down			
Voltage (V)	I-min (mA)	I-typ (mA)	I-max (mA)
0	0	0	0
0.4	40	60	85.5
0.6	56.5	85.3	121.8
0.8	74	106.4	152
1	90	124.5	177.8
1.4	115	152.3	217.5
1.5	120	158.3	226.2
1.6	125	162.8	232.6
1.8	130	170.5	243.6
1.9	132	175.9	251.3
2	132	179.6	256.5
3	135.6	203.4	290.6
3.135	135.6	206.4	294.9
3.3		207.1	295.8
3.465			295.8

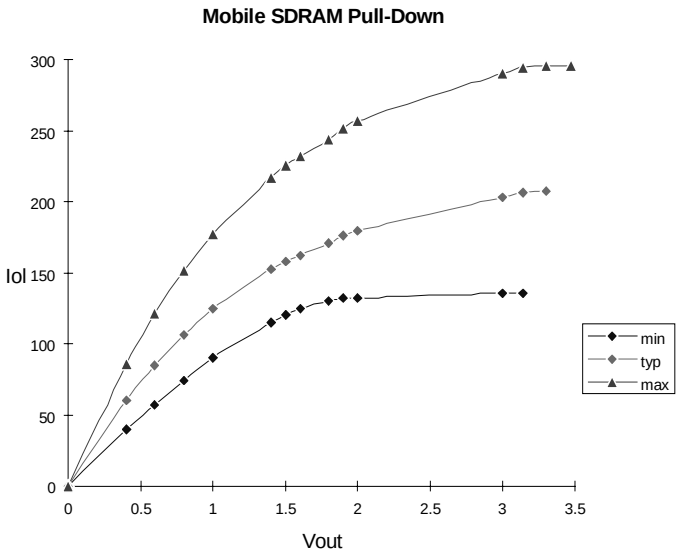
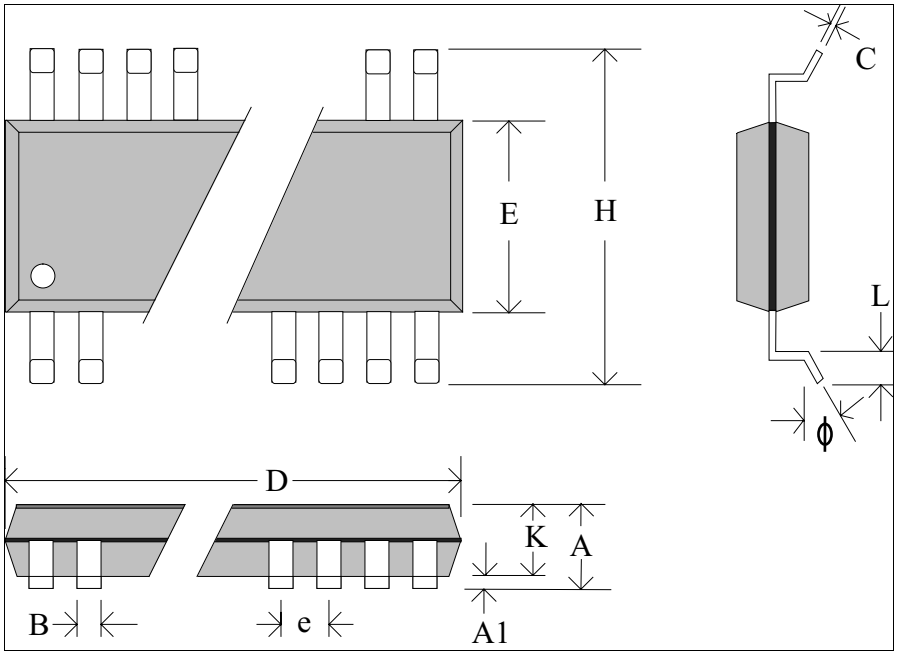


Figure 8-10 Type 4: Mobile SDRAM Clock Output Buffer Pull-Down Characteristics

Notes:

1. Must meet the temperature and voltage range specified in Table 2-3 DC Operating Requirements.
2. This drawing is not to scale. Comparisons should be made to the data provided in the table next to this drawing and to Table 8-13 Type 4: Mobile SDRAM Clock Operating Requirements.

8.6 Appendix D: SSOP Package Data



48 SSOP: Table of Dimensions (inches, unless otherwise specified)

Body		Symbol										
		E	H	C	L	ϕ	D	K	A	A1	e	B
48	Min	0.291	0.395	0.009	0.020	0°	0.620	-	0.095	0.008	0.025	0.008
(300mil)	Max	0.299	0.420	0.013	0.040	8°	0.630	-	0.110	0.016		0.012

EIAJ 28 SSOP: Table of Dimensions (inches, unless otherwise specified)

Body		Symbol										
		E	H	C	L	ϕ	D	K	A	A1	e	B
28	Min	0.197	0.291	0.009	0.025	0°	0.390	-	-	0.002	0.65 mm	0.009
(200mil)	Max	0.220	0.323	0.013	0.041	8°	0.413	-	0.079	-		0.015

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