Intel® Xeon™ Processor at 1.40 GHz, 1.50 GHz, 1.70 GHz and 2 GHz

Datasheet

Product Features

- Available at 1.40, 1.50, 1.70 and 2 GHz
- Dual processing server/workstation support
- Binary compatible with applications running on previous members of the Intel microprocessor line
- Intel® NetBurst™ micro-architecture
- System bus frequency at 400 MHz
  - —Bandwidth up to 3.2 Gbytes/sec
- Rapid Execution Engine: Arithmetic Logic Units (ALUs) run at twice the processor core frequency
- Hyper Pipelined Technology
- Advance Dynamic Execution
  - —Very deep out-of-order execution
  - —Enhanced branch prediction
- Level 1 Execution Trace Cache stores 12 K micro-ops and removes decoder latency from main execution loops
  - —Includes 8 KB Level 1 data cache
- 256 KB Advanced Transfer Cache (on-die, full speed Level 2 (L2) cache) with 8-way associativity and Error Correcting Code (ECC)
- Enables system support of up to 64 GB of physical memory
- 144 new Streaming SIMD Extensions 2 (SSE2) instructions
- Enhanced floating point and multimedia unit for enhanced video, audio, encryption, and 3D performance
- Power Management capabilities
  - —System Management mode
  - —Multiple low-power states
- Advanced System Management Features
  - —Processor Information ROM (PIROM)
  - —OEM Scratch EEPROM
  - —Machine Check Architecture (MCA)

The Intel® Xeon™ processor is designed for high-performance workstation and server applications. Based on the new Intel® NetBurst™ micro-architecture, it is binary compatible with previous Intel Architecture processors. The Intel Xeon processor is scalable to two processors in a multiprocessor system providing exceptional performance for applications running on advanced operating systems such as Windows* XP, Windows 2000 and UNIX*. The Intel Xeon processor extends the power of the Intel® Pentium® III Xeon™ processor with new features designed to make this processor the right choice for powerful workstation, advanced servers, and mission-critical applications. Advanced features simplify system management and meet the needs of a robust IT environment, resulting in maximized system up time, convenient system management, and optimal configuration.

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September 2001

Datasheet

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Revision History

Date of Release	Revision No.	Description
May 2001	-001	This is the first release of this datasheet.
August 2001	-002	- Included 2 GHz specifications - Added FC-BGA packaging details - Updated TAP Signal Group Signal Quality and DC Specifications

1.0 Introduction

The Intel® Xeon™ processor is based on the new Intel® NetBurst™ micro-architecture that operates at significantly higher clock speeds and delivers performance levels that are significantly higher than previous generations of IA-32 processors. While based on the new Intel NetBurst micro-architecture, it still maintains the tradition of compatibility with IA-32 software. The Intel NetBurst micro-architecture features include Hyper Pipelined Technology, a Rapid Execution Engine, a 400 MHz system bus, and an Execution Trace Cache. The Hyper Pipelined Technology doubles the pipeline depth in the processor, allowing the processor to reach much higher core frequencies. The Rapid Execution Engine allows the two integer ALUs in the processor to run at twice the core frequency, which allows many integer instructions to execute in one half the clock period. The 400 MHz system bus is a quad-pumped bus running off a 100 MHz system clock making 3.2 GB per second data transfer rates possible. The Execution Trace Cache is a level 1 cache that stores approximately twelve thousand decoded micro-operations, which removes the decoder from the main execution path, thereby increasing performance.

Improved features within the Intel NetBurst micro-architecture include Advanced Dynamic Execution, Advanced Transfer Cache, enhanced floating point and multi-media unit, and Streaming SIMD Extensions 2 (SSE2). Advanced Dynamic Execution improves speculative execution and branch prediction internal to the processor. The Advanced Transfer Cache is a 256Kbyte, on-die level 2 cache operating at the core speed which yields 64 GBytes/second of bandwidth at 2 GHz. The floating point and multi-media units have been improved by making the registers 128 bits wide and adding a separate register for data movement. Finally, SSE2 adds 144 new instructions for double-precision floating point, SIMD integer, and memory management.

The Intel Xeon processor is intended for high performance workstation and server systems with up to two processors on one bus. The Intel Xeon processor supports both dual- and uni-processor designs and includes manageability features. Components of the manageability features include an OEM EEPROM and Processor Information ROM which are accessed through a SMBus interface and contain information relevant to the particular processor and system in which it is installed. In addition, enhancements have been made to the Machine Check Architecture.

As a result of integrating the caches into the processor silicon, a return to PGA (Pin-Grid Array) style processor packaging is possible. The Intel Xeon processor is packaged in a 603-pin micro-PGA package and utilizes a surface mount ZIF socket with 603 pins. New heatsinks, heatsink retention mechanisms and sockets are required (versus previous processors in the Intel® Pentium® III Xeon™ processor family). Heatsinks and retention mechanisms have been designed with manufacturability as a high priority. Hence, mechanical assembly can be completed from the top of the motherboard.

The Intel Xeon processor uses a new scalable system bus protocol, referred to as the “system bus” in this document. The processor system bus utilizes a split-transaction, deferred reply protocol similar to that of the P6 processor family system bus, which is not compatible with the P6 processor family system bus. The system bus uses Source-Synchronous Transfer (SST) for address and data transfer to improve performance. Whereas the P6 processor family transfers data once per bus clock, the processor transfers data four times per bus clock (4X data transfer rate). Along with the 4X data bus, the address bus delivers addresses two times per bus clock and is referred to as a ‘double-clocked’ or 2X address bus. In addition, the Request Phase completes in one clock cycle. Working together, the 4X data bus and 2X address bus provide a data bus bandwidth of up to 3.2 Gbytes/second (3200 Mbytes/sec). Finally, the system bus also introduces transactions that are used to deliver interrupts.

Signals on the system bus use Assisted GTL+ (AGTL+) level voltages which are fully described in the appropriate platform design guide (refer to Section 1.3).

1.1 Terminology

A '#' symbol after a signal name refers to an active low signal, indicating a signal is in the asserted state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the '#' symbol implies that the signal is inverted. For example, D[3:0] = 'HLHL' refers to a hex 'A', and D[3:0]# = 'LHLH' also refers to a hex 'A' (H= High logic level, L= Low logic level).

"System bus" refers to the interface between the processor, system core logic (a.k.a. the chipset components), and other bus agents. The system bus is a multiprocessing interface to processors, memory, and I/O. For this document, "system bus" is used as the generic term for the Intel Xeon processor scalable system bus.

1.1.1 Processor Packaging Terminology

Commonly used terms are explained here for clarification:

- **603-pin socket** —The connector which mates the Intel® Xeon™ processor to the motherboard**.** The 603-pin socket is a surface mount technology (SMT), zero insertion force (ZIF) socket utilizing solder ball attachment to the platform. See the *603 Pin Socket Design Guidelines* for details regarding this socket.
- **FC-BGA (Flip Chip Ball Grid Array) package**— Microprocessor packaging using "flip chip" design, where the processor is attached to the substrate face-down, within a ball grid array package. This package is then mounted onto an interposer to interface with the platform.
- **Intel® Xeon™ processor** —The entire product including processor core in its OLGA or FC-BGA package, integrated heat spreader (IHS), and interposer.
- **Integrated Heat Spreader (IHS)** —The surface used to attach a heatsink or other thermal solution to the processor.
- **Interposer** —The structure on which the processor core package and I/O pins are mounted.
- **OLGA (Organic Land Grid Array) Package** —Microprocessor packaging using "flip chip" design, where the processor is attached to the substrate face-down for better signal integrity, more efficient heat removal and lower inductance, within an organic land grid array package.
- **Processor core** —The processor's execution engine. All AC timing and signal integrity specifications are to the pads of the processor core.
- **Processor Information ROM (PIR)**—A memory device located on the **Intel Xeon processor** and accessible via the System Management Bus (SMBus) which contains information regarding the processor's features. This device is shared with scratch EEPROM. The PIR is programmed during manufacturing and is write-protected. See **Section 7.4** for details on the PIR.
- **Retention mechanism** —The support pieces that are mounted through the motherboard and to the chassis wall to provide added support and retention for processor heatsinks.
- **Scratch EEPROM (Electrically Erasable, Programmable Read-Only Memory)**—A memory device located on the **Intel Xeon processor** and addressable via the SMBus which

can be used by the OEM to store information useful for system management. See **Section 7.4** for details on the Scratch EEPROM.

- **SMBus**—System Management Bus. A two-wire interface through which simple system and power management related devices can communicate with the rest of the system. It is based on the principals of the operation of the I^2C two-wire serial bus from Phillips Semiconductor*.

1.2 State of Data

The data contained within this document is subject to change. It is the best information that Intel is able to provide by the publication date of this document.

1.3 References

The reader of this specification should also be familiar with material and concepts presented in the following documents:

Document	Intel Order Number[1]
AP-485, *Intel Processor Identification and the CPUID Instruction*	241618
IA-32 Intel® Architecture Software Developer's Manual	
• *Volume I: Basic Architecture*	245470
• *Volume II: Instruction Set Reference Manual*	245471
• *Volume III: System Programming Guide*	245472
Intel® Xeon™ Processor and Intel® 860 Chipset Platform Design Guidelines	249671
Intel® Xeon™ Processor Family Thermal Design Guidelines	298348
603 Pin Socket Design Guidelines	249672
Intel® Xeon™ Processor Specification Update	developer.intel.com
CK00 Clock Synthesizer/Driver Design Guidelines	249206
VRM 9.0 DC-DC Converter Design Guidelines	249205
ITP700 Debug Port Design Guide	249679
Intel® Xeon™ Processor Thermal Solution Functional Specification	249673
Intel® Xeon™ Processor I/O Buffer Models	developer.intel.com[2]
Intel® Xeon™ Processor Enabled Components ProE Files*	developer.intel.com
Intel® Xeon™ Processor Enabled Components IGES Files	developer.intel.com
Intel® Xeon™ Processor FloTherm Model*	developer.intel.com
Intel® Xeon™ Processor Core Boundary Scan Descriptor Language (BSDL) Model	developer.intel.com
System Management Bus Specification, 2.0	www.sbs-forum.org
Wired for Management Baseline 2.0	developer.intel.com

NOTES:
1. Contact your Intel representative for the latest revision of the documents without order numbers.
2. The I/O Buffer Models are in IBIS format.

2.0 Electrical Specifications

2.1 System Bus and GTLREF

Most Intel® Xeon™ processor system bus signals use Assisted Gunning Transceiver Logic (AGTL+) signaling technology. This signaling technology provides improved noise margins and reduced ringing through low voltage swings and controlled edge rates. Unlike the Intel® Pentium® III Xeon™ processor family, the termination voltage level for the Intel® Xeon™ Processor AGTL+ signals is V_{CC}, the operating voltage of the processor core. P6 family processors utilize a fixed 1.5V termination voltage known as V_{TT} . The use of a termination voltage that is determined by the processor core allows better voltage scaling on the system bus for Intel® Xeon™ processors. Because of the speed improvements to data and address busses, signal integrity and platform design methods become more critical than with previous processor families. Design guidelines for the Intel Xeon processor system bus are detailed in the appropriate platform design guidelines (refer to Section 1.3).

The AGTL+ inputs require a reference voltage (GTLREF) which is used by the receivers to determine if a signal is a logical 0 or a logical 1. GTLREF must be generated on the system board (See Table 11 for GTLREF specifications). Termination resistors are provided on the processor silicon and are terminated to its core voltage (V_{CC}). The on-die termination resistors are a selectable feature and can be enabled or disabled via the ODTEN pin. For end bus agents, on-die termination can be enabled to control reflections on the transmission line. For middle bus agents, on-die termination must be disabled. The Intel 860 chipset provides on-die termination, thus eliminating the need to terminate the bus on the system board for most AGTL+ signals.

Note: Some AGTL+ signals do not include on-die termination and must be terminated on the system board. See Table 3 for details regarding these signals.

The AGTL+ bus depends on incident wave switching. Therefore timing calculations for AGTL+ signals are based on flight time as opposed to capacitive deratings. Analog signal simulation of the system bus, including trace lengths, is highly recommended when designing a system. Please refer to http//www.developer.intel.com to obtain the buffer electrical models, *Intel® Xeon™ Processor I/O Buffer Models.*

2.2 Power and Ground Pins

For clean on-chip power distribution, Intel® Xeon™ processors have 155 V_{CC} (power) and 155 V_{SS} (ground) inputs. All power pins must be connected to V_{CC}, while all V_{SS} pins must be connected to the system ground plane. The processor V_{CC} pins must be supplied the voltage determined by the VID (Voltage ID) pins.

2.3 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the Intel® Xeon™ processor is capable of generating large instantaneous current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Larger bulk storage (C_{BULK}), such as electrolytic capacitors, supply current during longer lasting changes in current demand by the component, such as coming out of an idle condition.

Similarly, they act as a storage well for current when entering an idle condition from a running condition. Care must be taken in the board design to ensure that the voltage provided to the processor remains within the specifications listed in Table 5. Failure to do so can result in timing violations or reduced lifetime of the component. For further information and guidelines, refer to the appropriate platform design guidelines.

2.3.1 V_{CC} Decoupling

Regulator solutions need to provide bulk capacitance with a low Effective Series Resistance (ESR) and maintain a low interconnect resistance from the regulator (or VRM pins) to the 603-pin socket. Bulk decoupling is provided on the voltage regulation module (VRM) to meet the needs of large current swings. The power delivery path must be capable of delivering enough current while maintaining the required tolerances (defined in Table 5). For further information regarding power delivery, decoupling, and layout guidelines, refer to the appropriate platform design guidelines.

2.3.2 System Bus AGTL+ Decoupling

The processor integrates a portion of the required high frequency decoupling capacitance on the processor package. However, additional high frequency capacitance must be added to the system board to properly decouple the return currents from the system bus. Bulk decoupling must also be provided by the system board for proper AGTL+ bus operation. Decoupling guidelines are described in the appropriate platform design guidelines.

2.4 System Bus Clock (BCLK[1:0]) and Processor Clocking

BCLK[1:0] directly controls the system bus interface speed as well as the core frequency of the processor. As in previous generation processors, the Intel® Xeon™ processor core frequency is a multiple of the BCLK[1:0] frequency. The processor bus ratio multiplier will have a maximum ratio set during manufacturing. Platforms will use the ratio-setting pins, as in previous generation Intel processors, to configure the processor to run at its maximum ratio or lower. This feature is provided to ensure that multiprocessing systems, which typically are not fully populated with processors at the time of purchase, may be upgraded at a later date and have all processors run at the same core frequency.

Clock multiplying within the processor is provided by the internal PLL, which requires a constant frequency BCLK[1:0] input with exceptions for spread spectrum clocking. Processor DC and AC specifications for the BCLK[1:0] inputs are provided in Table 6 and Table 12, respectively. These specifications must be met while also meeting signal integrity requirements as outlined in Chapter 3.0. Unlike previous processors, Intel® Xeon™ processors utilize differential clocks. Details regarding BCLK[1:0] driver specifications are provided in the *CK00 Clock Synthesizer/Driver Design Guidelines* document.

The BCLK[1:0] inputs directly control the operating speed of the system bus interface. The processor core frequency must be configured during Reset by using the A20M#, IGNNE#, LINT[1]/NMI, and LINT[0]/INTR pins (see Table 1). The value on these pins during Reset determines the multiplier that the Phase Lock Loop (PLL) will use for the internal core clock. The processor is limited to the maximum bus-to-core ratio and only the maximum or lower ratios are supported. If a ratio higher than the maximum is chosen, the processor will default to the maximum ratio. The maximum ratio for each processor is equal to the core frequency divided by the bus frequency marked on the processor.

2.4.1 Phase Lock Loop (PLL) Power and Filter

V_{CCA} and $V_{CCIOPLL}$ are power sources required by the PLL clock generators on the processor silicon. Since these PLLs are analog in nature, they require quiet power supplies for minimum jitter. Jitter is detrimental to the system: it degrades external I/O timings as well as internal core timings (i.e. maximum frequency). To prevent this degradation, these supplies must be low pass filtered from V_{CC}. A typical filter topology is shown in Figure 1.

The AC low-pass requirements, with input at V_{CC} and output measured across the capacitor (C_A or C_{IO} in Figure 1), is as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band < 1 Hz (see DC drop in next set of requirements)
- > 34 dB attenuation from 1 MHz to 66 MHz
- > 28 dB attenuation from 66 MHz to core frequency

The filter requirements are illustrated in Figure 2. For recommendations on implementing the filter refer to the appropriate platform design guidelines.

Figure 1. Typical $V_{CCIOPLL}$, V_{CCA} and V_{SSA} Power Distribution

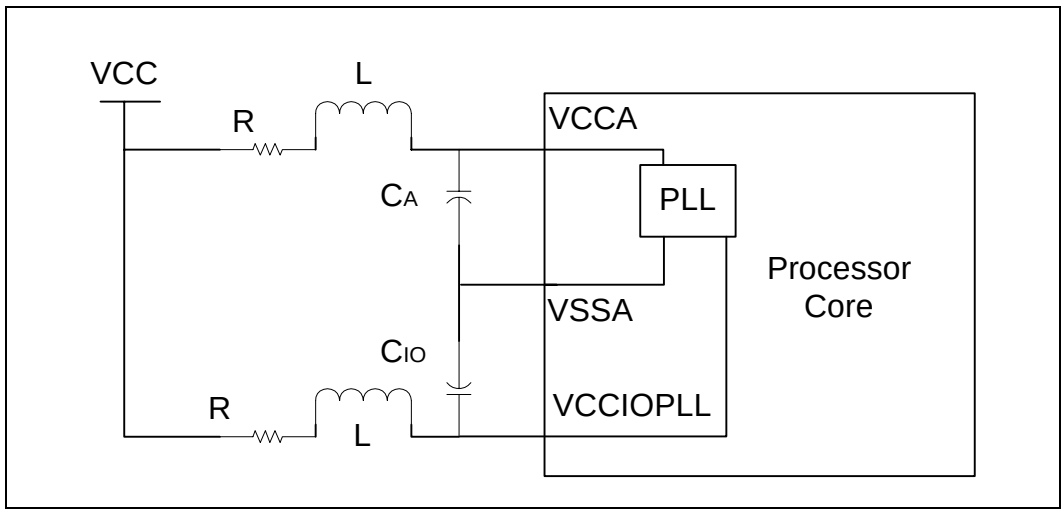
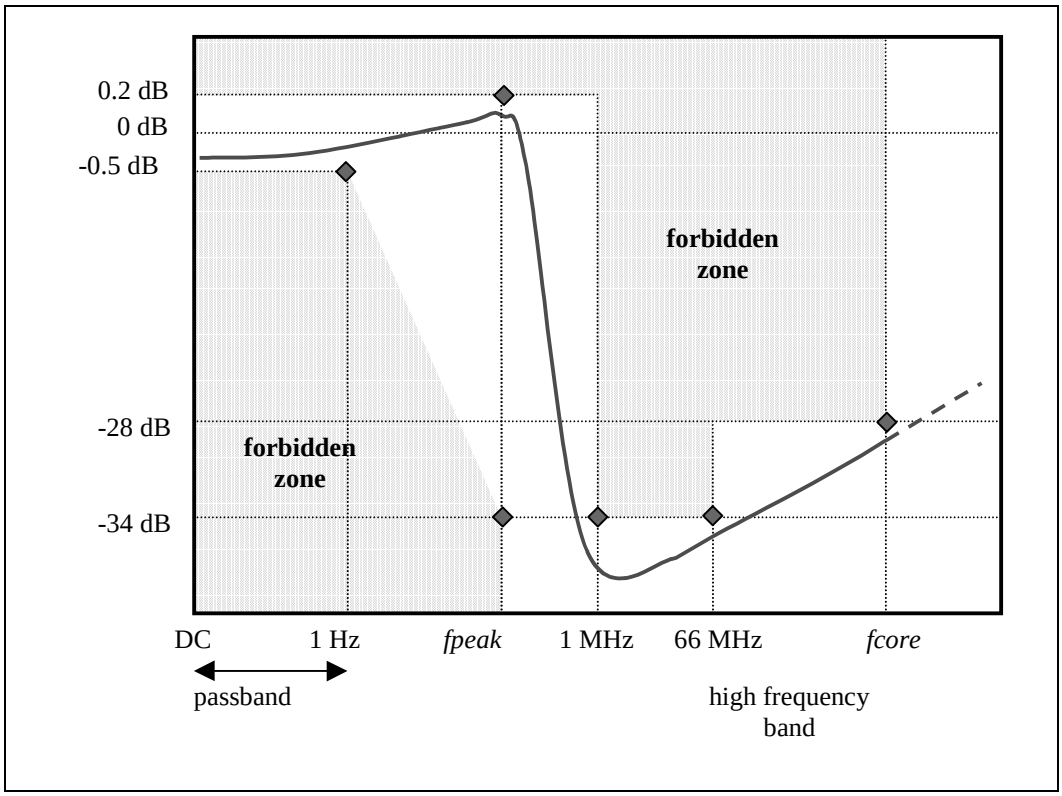


Figure 2. Phase Lock Loop (PLL) Filter Requirements



NOTES:
1. Diagram not to scale.
2. No specifications for frequencies beyond f_{core} (core frequency).
3. f_{peak}, if existent, should be less than 0.05MHz.

2.4.2 System Bus to Core Frequency Ratios

The frequency multipliers supported are shown in Table 1. Other combinations will not be validated nor supported by Intel. For a given processor, only the ratios which result in a core frequency equal to or less than the frequency marked on the processor are supported.

Table 1. Core Frequency to System Bus Multiplier Configuration

Multiplier for System Bus-to-Core Frequency[1]	Core Frequency	LINT[1]/ NMI	A20M#	IGNNE#	LINT[0]/ INTR
1/8	800 MHz	H	H	H	H
1/10	1.00 GHz	H	H	L	H
1/11	1.10 GHz	H	H	L	L
1/12	1.20 GHz	H	L	H	H
1/13	1.30 GHz	H	L	H	L
1/14	1.40 GHz	H	L	L	H
1/15	1.50 GHz	H	L	L	L
1/16	1.60 GHz	L	H	H	H
1/17	1.70 GHz	L	H	H	L
1/18	1.80 GHz	L	H	L	H
1/19	1.90 GHz	L	H	L	L
1/20	2.00 GHz	L	L	H	H

NOTES:
1. Refer to the *Intel® Xeon™ Processor Specification Update* for processor stepping details.

2.4.3 Mixing Processors

Mixing components operating at different internal clock frequencies is not supported and has not been validated by Intel. Not all operating systems can support multiple processors with mixed frequencies. Intel only supports and validates multi-processor configurations where all processors operate with the same system bus, core frequencies, and VID settings. Mixing of processors of different steppings (as per the CPUID) is supported in limited configurations (stepping IDs must not be separated by more than one stepping). For determining the level of support for mixed steppings, refer to the *Intel® Xeon™ Processor Specification Update*. Details on CPUID are provided in the AP-485, *Intel Processor Identification and the CPUID Instruction* application note.

2.5 Voltage Identification

The VID specification for Intel® Xeon™ processors is different from that of previous generations and is supported by the *VRM 9.0 DC-DC Convertor Design Guidelines*. The voltage set by the VID pins is the maximum voltage allowed by the processor. A minimum voltage is provided in Table 5 and changes with frequency. This allows processors running at a higher frequency to have a relaxed minimum voltage specification. The specifications have been set such that one voltage regulator can work with all supported frequencies.

The processor uses five voltage identification pins, VID[4:0], to support automatic selection of power supply voltages. Table 2 specifies the voltage level corresponding to the state of VID[4:0]. A ‘1’ in this table refers to a high voltage and a ‘0’ refers to low voltage level. The definition provided in Table 2 is not related in any way to previous processors or VRMs. If the processor socket is empty (VID[4:0] = 11111), or the voltage regulation circuit cannot supply the voltage that is requested, it must disable itself.

Table 2. Voltage Identification Definition

Processor Pins					
VID4	**VID3**	**VID2**	**VID1**	**VID0**	**V_{CC_MAX} (V)**
1	1	1	1	1	VRM output off
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	**0**	**1**	**1**	**0**	**1.700**
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850

2.5.1 Mixing Processors of Different Voltages

Mixing processors operating at different VID settings (voltages) is not supported and will not be validated by Intel.

2.6 Reserved Or Unused Pins

All Reserved pins must remain unconnected. Connection of these pins to V_{CC}, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future Intel® Xeon™ processor. See Section 5.0 for a pin listing of the processor and the location of all Reserved pins.

For reliable operation, always connect unused inputs or bidirectional signals to an appropriate signal level. In a system level design, on-die termination is provided by the processor to allow end agents to be terminated within the processor silicon. In this context, end agent refers to the bus agent that resides on either end of the daisy-chained system bus interface while a middle agent is any bus agent in between the two end agents. For end agents, most unused AGTL+ inputs should be left as no connects, as AGTL+ termination is provided on the processor silicon. However, see Table 3 for details on AGTL+ signals that do not include on-die termination. For middle agents, the on-die termination must be disabled, so the platform must ensure that unused AGTL+ input signals which do not connect to end agents are connected to V_{CC} via a pull-up resistor. Unused active high inputs, should be connected through a resistor to ground (V_{SS}). Unused outputs may be left unconnected, however this may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bidirectional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. For unused AGTL+ input or I/O signals, use pull-up resistors of the same value as the on-die termination resistors (R_{TT}). See Table 11.

TAP, Asynchronous GTL+ inputs, and Asynchronous GTL+ outputs do not include on-die termination. Inputs and utilized outputs must be terminated on the system board. Unused outputs may be terminated on the system board or left unconnected. Note that leaving unused outputs unterminated may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. Signal termination recommendations for these signal types is discussed in the platform design guidelines and the *ITP700 Debug Port Design Guide*.

For each processor, all TESTHI[6:0] pins must be connected to V_{CC} via a pull-up resistor of between 1 kΩ and 10 kΩ value. TESTHI[3:0] and TESTHI[6:5] may all be tied together at each processor and pulled up to V_{CC} with a single 1 kΩ – 4.7 kΩ resistor if desired. However, utilization of boundary scan test will not be functional if these pins are connected together. TESTHI4 must always be pulled up independently from the other TESTHI pins. The TESTHI pins must not be connected between system bus agents.

2.7 System Bus Signal Groups

In order to simplify the following discussion, the system bus signals have been combined into groups by buffer type. AGTL+ input signals have differential input buffers, which use GTLREF as a reference level. In this document, the term “AGTL+ Input” refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, “AGTL+ Output” refers to the AGTL+ output group as well as the AGTL+ I/O group when driving.

With the implementation of a source synchronous data bus comes the need to specify two sets of timing parameters. One set is for common clock signals whose timings are specified with respect to rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.) and the second set is for the source synchronous signals which are relative to their respective strobe lines (data and address) as well as rising edge of BCLK0. Asynchronous signals are still present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle. Table 3 identifies which signals are common clock, source synchronous and asynchronous.

Table 3. System Bus Signal Groups

Signal Group	Type	Signals [1]
AGTL+ Common Clock Input	Synchronous to BCLK[1:0]	BPRI#, BR[3:1]#[2,3], DEFER#, RESET#[2], RS[2:0]#, RSP#, TRDY#
AGTL+ Common Clock I/O	Synchronous to BCLK[1:0]	ADS#, AP[1:0]#, BINIT#[7], BNR#[7], BPM[5:0]#[2], BR0#[2], DBSY#, DP[3:0]#, DRDY#, HIT#[7], HITM#[7], LOCK#, MCERR#[7]
AGTL+ Source Synchronous I/O	Synchronous to assoc. strobe	**Signals** / **Associated Strobe**: REQ[4:0]#,A[16:3]#[6] / ADSTB0# A[35:17]#[6] / ADSTB1# D[15:0]#, DBI0# / DSTBP0#, DSTBN0# D[31:16]#, DBI1# / DSTBP1#, DSTBN1# D[47:32]#, DBI2# / DSTBP2#, DSTBN2# D[63:48]#, DBI3# / DSTBP3#, DSTBN3#
AGTL+ Strobes	Synchronous to BCLK[1:0]	ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#
Async GTL+ Input [4]	Asynchronous	A20M#[5], IGNNE#[5], INIT#[6], LINT0/INTR[5], LINT1/NMI[5], PWRGOOD, SMI#[6], SLP#, STPCLK#
Async GTL+ Output [4]	Asynchronous	FERR#, IERR#, THERMTRIP#, PROCHOT#
System Bus Clock	Clock	BCLK1, BCLK0
TAP Input [4]	Synchronous to TCK	TCK, TDI, TMS, TRST#
TAP Output [4]	Synchronous to TCK	TDO
SMBus Interface [8]	Synchronous to SM_CLK	SM_EP_A[2:0], SM_TS_A[1:0], SM_DAT, SM_CLK, SM_ALERT#, SM_WP
Power/Other	Power/Other	COMP[1:0], GTLREF, OTDEN, Reserved, SKTOCC#, TESTHI[6:0],VID[4:0], V_{CC}, SM_VCC, V_{CCA}, V_{SSA}, $V_{CCIOPLL}$, V_{SS}, $V_{CCSENSE}$, $V_{SSSENSE}$

NOTES:
1. Refer to Section 5.2 for signal descriptions.
2. These AGTL+ signals are not terminated by the processor. Refer to the *ITP700 Debug Port Design Guide* and the platform design guidelines for termination recommendations.They must be terminated at the end agent by the platform.
3. Intel® Xeon™ processors only utilize BR0# and BR1#. Use of BR2# and BR3# is reserved on Intel Xeon processors and must only be terminated to V_{CC}. For additional details regarding the BR[3:0]# signals, see Section 5.2 and Section 7.1.
4. These signal groups are not terminated by the processor. Refer to Section 2.6, the appropriate platform design guidelines and *ITP700 Debug Port Design Guide* for termination recommendations.
5. The value on these pins during the active-to-inactive edge of RESET# determines the multiplier that the Phase Lock Loop (PLL) will use for the internal core clock.
6. The value of these pins during the active-to-inactive edge of RESET# determine processor configuration options. See Section 7.1 for details.
7. These signals may be driven simultaneously by multiple agents (wired-OR).
8. These signals are not terminated by the processor's on-die termination. However, some signals in this group include termination on the processor interposer. See Section 7.4 for details.

2.8 Asynchronous GTL+ Signals

Intel® Xeon™ processors do not utilize CMOS voltage levels on any signals that connect to the processor. As a result, legacy input signals such as A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, SLP#, and STPCLK# utilize GTL+ input buffers. Legacy output FERR# and other non-AGTL+ signals IERR#, THERMTRIP# and PROCHOT# utilize GTL+ output buffers. All of these asynchronous GTL+ signals follow the same DC requirements as AGTL+ signals, however the outputs are not driven high (during the logical 0-to-1 transition) by the processor (the major difference between GTL+ and AGTL+). Asynchronous GTL+ signals do not have setup or hold time specifications in relation to BCLK[1:0]. However, all of the asynchronous GTL+ signals are required to be asserted for at least two BCLKs in order for the processor to recognize them. See Table 8 and Table 15 for the DC and AC specifications for the asynchronous GTL+ signal group. See Section 7.2 for additional timing requirements for entering and leaving low power states.

2.9 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, it is recommended that the processor be first in the TAP chain and followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage. Similar considerations must be made for TCK, TMS, and TRST#. Two copies of each signal may be required with each driving a different voltage level. See Table 9 and Table 17 for the DC and AC specifications for the TAP signal group. Refer to Section 9.0 for more detailed information.

2.10 Maximum Ratings

Table 4 lists the processor's maximum environmental stress ratings. Functional operation at the absolute maximum and minimum is neither implied nor guaranteed. The processor should not receive a clock while subjected to these conditions. Functional operating parameters are listed in the AC and DC tables. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the processor contains protective circuitry to resist damage from electro-static discharge, one should always take precautions to avoid high static voltages or electric fields.

Table 4. Processor Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
$T_{STORAGE}$	Processor storage temperature	–40	85	°C	1
V_{CC}	Any processor supply voltage with respect to V_{SS}	–0.5	2.1	V	2
$V_{inAGTL+}$	AGTL+ buffer DC input voltage with respect to V_{SS}	–0.3	2.1	V	
V_{inGTL+}	Async GTL+ buffer DC input voltage with respect to Vss	-0.3	2.1	V	
$V_{inSMBus}$	SMBus buffer DC input voltage with respect to Vss	-0.3	6.0	V	
I_{VID}	Max VID pin current		5	mA	

NOTE:
1. Please contact Intel for storage requirements in excess of one year.
2. This rating applies to any pin of the processor.

2.11 Processor DC Specifications

The processor DC specifications in this section are defined at the processor core (pads) unless noted otherwise. See Section 5.1 for the pin listings and Section 5.2 for the signal definitions. The voltage and current specifications of the processor are detailed in Table 5. The DC specifications for the AGTL+ signals are listed in Table 7.

The system bus clock signal group and the SMBus interface signal group are detailed in Table 6 and Table 10, respectively. Previously, legacy signals (CMOS) and Test Access Port (TAP) signals to the processor used low-voltage CMOS buffer types. However, these interfaces now follow DC specifications similar to GTL+. The DC specifications for the asynchronous GTL+ signal group are listed in Table 8 and the TAP signal group Table 9.

Table 5 through Table 10 list the DC specifications for the processor and are valid only while meeting specifications for case temperature (T_{CASE} as specified in Chapter 6.0), clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Table 5. Voltage and Current Specifications

Symbol	Parameter	Core Freq	Min	Typ	Max	Unit	Notes[1]
V_{CC}	V_{CC} for processor core	1.40 GHz 1.50 GHz 1.70 GHz 2 GHz	1.590 1.585 1.575 1.560		1.70 1.70 1.70 1.70	V V V V	2, 3, 4 2, 3, 4 2, 3, 4 2, 3, 4
V_{CC_MID}	V_{CC} of processor at max. I_{CC}	All freq.		(V_{CC_MAX}+V_{CC_MIN})/ 2		V	4
V_{CC_SMBus}	SMBus supply voltage	All freq.	3.135	3.30	3.465	V	
I_{CC}	I_{CC} for processor core	1.40 GHz 1.50 GHz 1.70 GHz 2 GHz			41.7 44.2 49.4 57.2	A A A A	4, 5 4, 5 4, 5 4, 5
I_{CC_SMBus}	Icc for SMBus power supply	All freq.		3.0	22.5	mA	
I_{CC_PLL}	I_{CC} for PLL power pins	All freq			30	mA	8
I_{CC_GTLREF}	I_{CC} for GTLREF pins	All freq			15	µA	9
I_{SGnt}/I_{SLP}	I_{CC} Stop-Grant/Sleep	All freq			14.6	A	6
I_{TCC}	I_{CC} TCC active	All freq			14.6	A	7

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processors.
2. A variable voltage source should exist on systems in the event that a different voltage is required. See Section 2.5 and Table 2 for more information.
3. The voltage specification requirements are measured across vias on the platform for the V_{CC_SENSE} and V_{SS_SENSE} pins close to the socket with a 100MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
4. The processor should not be subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MID} + 0.200 * (1-I_{CC}/I_{CC_MAX}) [V]. Moreover, Vcc should never exceed V_{CC_MAX} (VID). Failure to adhere to this specification can shorten the processor lifetime.
5. Maximum current is defined at V_{CC_MID}.
6. The current specified is also for AutoHALT State.
7. The instantaneous current the processor will draw while the thermal control circuit is active as indicated by the assertion of PROCHOT#.
8. This specification applies to the PLL power pins VCCA and VCCIOPLL. See Section 2.4.1 for details. This parameter is based on design characterization and is not tested.
9. This specification applies to each GTLREF pin.

Table 6. System Bus Differential BCLK DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Figure	Notes [1]
V_L	Input Low Voltage		0		V	5	
V_H	Input High Voltage	0.660	0.710	V_{CC} - 0.30	V	5	7
V_{CROSS}	Crossing Voltage	0.45 * (V_H-V_L)	0.5 * (V_H-V_L)	0.55 * (V_H-V_L)	V	5	2, 7
V_{OV}	Overshoot	N/A	N/A	0.300	V	5	3
V_{US}	Undershoot	N/A	N/A	0.300	V	5	4
V_{RBM}	Ringback Margin	0.200	N/A	N/A	V	5	5
V_{TH}	Threshold Region	V_{CROSS} -0.100		V_{CROSS}+0.100	V	5	6

NOTES:.
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Crossing Voltage is defined as absolute voltage where rising edge of BCLK0 is equal to the falling edge of BCLK1. V_H and V_L are the voltages observed at the processor.
3. Overshoot is defined as the absolute value of the maximum voltage allowed above the V_H level.
4. Undershoot is defined as the absolute value of the maximum voltage allowed below the V_{SS} level.
5. Ringback Margin is defined as the absolute voltage difference between the maximum Rising Edge Ringback and the maximum Falling Edge Ringback.
6. Threshold Region is defined as a region centered about the crossing voltage in which the differential receiver switches. It includes input threshold hysteresis.
7. The V_{CC} referred to in these specifications refers to instantaneous V_{CC}.

Table 7. AGTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes [1]
V_{IL}	Input Low Voltage	-0.150	GTLREF - 0.100	V	2, 6
V_{IH}	Input High Voltage	GTLREF + 0.100	V_{CC}	V	3, 4, 6
V_{OL}	Output Low Voltage	-0.150	V_{CC} * R_{ON}_max/ (R_{ON}_max + 0.50 * Rtt_min)	V	6
V_{OH}	Output High Voltage	GTLREF + 0.100	V_{CC}	V	4, 6
I_{OL}	Output Low Current	N/A	V_{CC} / (0.50 * Rtt_min + R_{ON}_min)	mA	6
I_{LI}	Input Leakage Current	N/A	± 100	µA	
I_{LO}	Output Leakage Current	N/A	± 100	µA	
R_{ON}	Buffer On Resistance	5	11	Ω	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{OH} may experience excursions above V_{CC}. However, input signal drivers must comply with the signal quality specifications in Chapter 3.0.
5. Refer to *Intel® Xeon™ Processor I/O Buffer Models* for I/V characteristics.
6. The V_{CC} referred to in these specifications refers to instantaneous V_{CC}.

Table 8. Asynchronous GTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes [1]
V_{IL}	Input Low Voltage	-0.150	GTLREF - (0.1 * V_{CC}/1.3)	V	5
V_{IH}	Input High Voltage	GTLREF + (0.1 * V_{CC}/1.3)	V_{CC}	V	4, 5
V_{OL}	Output Low Voltage	-0.150	0.400	V	2
V_{OH}	Output High Voltage	N/A	V_{CC}	V	3, 4, 5
I_{OL}	Output Low Current		56	mA	6
I_{LI}	Input Leakage Current	N/A	± 100	µA	
I_{LO}	Output Leakage Current	N/A	± 100	µA	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Parameter will be measured at 56 mA (for use with system inputs).
3. All outputs are open-drain.
4. V_{IH} and V_{OH} may experience excursions above V_{CC}. However, input signal drivers must comply with the signal quality specifications in Chapter 3.0.
5. The V_{CC} referred to in these specifications refers to instantaneous V_{CC}.
6. The maximum output current for asynch GTL+ is not specified into the test load shown in Figure 3.

Table 9. TAP Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1,2]
V_{HYS}	TAP Input Hysteresis	200	300	V	8
V_{T+}	TAP input low to high threshold voltage	0.5 * (V_{CC} + V_{HYS_MIN})	0.5 * (V_{CC} + V_{HYS_MAX})	V	5
V_{T-}	TAP input high to low threshold voltage	0.5 * (V_{CC} - V_{HYS_MAX})	0.5 * (V_{CC} - V_{HYS_MIN})	V	5
V_{OH}	Output High Voltage	N/A	V_{CC}	V	3, 5
I_{OL}	Output Low Current		45	mA	6, 7
I_{LI}	Input Leakage Current		+/- 100	mA	
I_{LO}	Output Leakage Current		+/- 100	uA	
R_{ON}	Buffer On Resistance	6.25	13.25	Ω	4

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. All outputs are open drain.
3. TAP signal group must meet system signal quality specifications in Chapter 3.0.
4. Refer to *Intel® Xeon™ Processor I/O Buffer Models* for I/V characteristics.
5. The V_{CC} referred to in these specifications refers to instantaneous V_{CC}.
6. The maximum output current is based on maximum current handling capability of the buffer and is not specified into the test load.
7. V_{OL_MAX} of 360 mV is guaranteed when driving into a test load as depicted in Figure 3.
8. V_{HYS} represents the amount of hysteresis, nominally centered about 0.5 * V_{CC} for all TAP inputs.

Table 10. SMBus Signal Group DC Specifications (Page 1 of 2)

Symbol	Parameter	Min	Max	Unit	Notes [1,2,3]
V_{IL}	Input Low Voltage	-0.30	0.30 * SM_V_{CC}	V	
V_{IH}	Input High Voltage	0.70 * SM_V_{CC}	3.465	V	

Table 10. SMBus Signal Group DC Specifications (Page 2 of 2)

V_{OL}	Output Low Voltage	0	0.400	V	
I_{OL}	Output Low Current	N/A	3.0	mA	
I_{LI}	Input Leakage Current	N/A	± 10	µA	
I_{LO}	Output Leakage Current	N/A	± 10	µA	
C_{SMB}	SMBus Pin Capacitance		15.0	pF	4

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. These parameters are based on design characterization and are not tested.
3. All DC specifications for the SMBus signal group are measured at the processor pins.
4. Platform designers may need this value to calculate the maximum loading of the SMBus and to determine maximum rise and fall times for SMBus signals.

2.12 AGTL+ System Bus Specifications

Routing topologies are dependent on the number of processors supported and the chipset used in the design. Please refer to the appropriate platform design guidelines. In most cases, termination resistors are not required as these are integrated into the processor silicon, see Table 3 for details on which AGTL+ signals do not include on-die termination.The termination resistors are enabled or disabled through the ODTEN pin. To enable termination, this pin should be pulled up to V_{CC} through a resistor and to disable termination, this pin should be pulled down to V_{SS} through a resistor. The processor's on-die termination must be enabled for the end agent only. Please refer to Table 11 for termination resistor values.

Valid high and low levels are determined by the input buffers via comparing with a reference voltage called GTLREF (known as V_{REF} in previous documentation).

Table 11 lists the GTLREF specifications. The AGTL+ reference voltage (GTLREF) should be generated on the system board using high precision voltage divider circuits. It is important that the system board impedance is held to the specified tolerance, and that the intrinsic trace capacitance for the AGTL+ signal group traces is known and well-controlled. For more details on platform design see the appropriate platform design guidelines.

Table 11. AGTL+ Bus Voltage Definitions

Symbol	Parameter	Min	Typ	Max	Units	Notes [1]
GTLREF	Bus Reference Voltage	2/3 VCC - 2%	2/3 VCC	2/3 VCC + 2%	V	2, 3, 6
R_{TT}	Termination Resistance	36	41	46	Ω	4
COMP[1:0]	COMP Resistance	42.77	43.2	43.63	Ω	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The tolerances for this specification have been stated generically to enable system designer to calculate the minimum values across the range of V_{CC}.
3. GTLREF is generated from V_{CC} on the baseboard by a voltage divider of 1% resistors. Refer to the appropriate platform design guidelines for implementation details.
4. R_{TT} is the on-die termination resistance measured at V_{OL} of the AGTL+ output driver. Refer to the *Intel® Xeon™ Processor I/O Buffer Models* for I/V characteristics.
5. COMP resistors are provided by the baseboard with 1% resistors. See the appropriate platform design guidelines for implementation details.
6. The V_{CC} referred to in these specifications refers to instantaneous V_{CC}.

2.13 System Bus AC Specifications

The processor system bus timings specified in this section are defined at the processor core (pads). See Chapter 5.0 for the processor pin listing and signal definitions.

Table 12 through Table 18 list the AC specifications associated with the processor system bus.

All AGTL+ timings are referenced to GTLREF for both ‘0’ and ‘1’ logic levels unless otherwise specified.

The timings specified in this section should be used in conjunction with the I/O buffer models provided by Intel. These I/O buffer models, which include package information, are available for the processor in IBIS format. AGTL+ layout guidelines are also available in the appropriate platform design guidelines.

Note: Care should be taken to read all notes associated with a particular timing parameter.

Table 12. System Bus Differential Clock AC Specifications

T# Parameter	Min	Nom	Max	Unit	Figure	Notes[1]
System Bus Frequency			100.0	MHz		2
T1: BCLK[1:0] Period	10.00		10.20	ns	5	3
T2: BCLK[1:0] Period Stability	N/A		150	ps		4, 5
T3: T_{PH} BCLK[1:0] Pulse High Time	3.94	5	6.12	ns	5	
T4: T_{PL} BCLK[1:0] Pulse Low Time	3.94	5	6.12	ns	5	
T5: BCLK[1:0] Rise Time	175		700	ps	5	6
T6: BCLK[1:0] Fall Time	175		700	ps	5	6

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The processor core clock frequency is derived from BCLK. The bus clock to processor core clock ratio is determined during initialization as described in Section 2.4. Table 1 shows the supported ratios for the processor. Also refer to Chapter 10.0.
3. The period specified here is the average period. A given period may vary from this specification as governed by the period stability specification (T2).
4. For the clock jitter specification, refer to the *CK00 Clock Synthesizer/Driver Design Guidelines*.
5. In this context, period stability is defined as the worst case timing difference between successive crossover voltages. In other words, the largest absolute difference between adjacent clock periods must be less than the period stability.
6. Slew rate is measured between the 35% and 65% points of the clock swing (V_L and V_H).

Table 13. System Bus Common Clock AC Specifications

T# Parameter	Min	Max	Unit	Figure	Notes[1, 2, 3]
T10: Common Clock Output Valid Delay	0.20	1.45	ns	6	4
T11: Common Clock Input Setup Time	0.65	N/A	ns	6	5
T12: Common Clock Input Hold Time	0.40	N/A	ns	6	5
T13: RESET# Pulse Width	1.00	10.00	ms	9	6, 7, 8

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Not 100% tested. Specified by design characterization.
3. All common clock AC timings for AGTL+ signals are referenced to the Crossing Voltage (V_{CROSS}) of the BCLK[1:0] at rising edge of BCLK0. All common clock AGTL+ signal timings are referenced at GTLREF at the processor core.
4. Valid delay timings for these signals are specified into the test circuit described in Figure 3 and with GTLREF at 2/3 V_{CC} ± 2%.
5. Specification is for a minimum swing defined between AGTL+ V_{IL_MAX} to V_{IH_MIN} . This assumes an edge rate of 0.4 V/ ns to 4.0V/ns.
6. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously.
7. This should be measured after V_{CC} and BCLK[1:0] become stable.
8. Maximum specification applies only while PWRGOOD is asserted.

Table 14. System Bus Source Synchronous AC Specifications

T# Parameter	Min	Max	Unit	Figure	Notes 1,2,3,4
T20: Source Sync. Output Valid Delay (first data/ address only)	0.20	1.30	ns	7, 8	5
T21: T_{VBD} Source Sync. Data Output Valid Before Data Strobe	0.85		ns	8	5, 8
T22: T_{VAD} Source Sync. Data Output Valid After Data Strobe	0.85		ns	8	5, 8
T23: T_{VBA} Source Sync. Address Output Valid Before Address Strobe	1.88		ns	7	5, 8
T24: T_{VAA} Source Sync. Address Output Valid After Address Strobe	1.88		ns	7	5, 9
T25: T_{SUSS} Source Sync. Input Setup Time	0.21		ns	7, 8	6
T26: T_{HSS} Source Sync. Input Hold Time	0.21		ns	7, 8	6
T27: T_{SUCC} Source Sync. Input Setup Time to BCLK	0.65		ns	7, 8	7
T28: T_{FASS} First Address Strobe to Second Address Strobe		1/2	BCLKs	7	10, 14
T29: T_{FDSS}: First Data Strobe to Subsequent Strobes		n/4	BCLKs	8	11, 12, 14
T30: Data Strobe ‘n’ (DSTBN#) Output Valid Delay	8.80	10.20	ns	8	13
T31: Address Strobe Output Valid Delay	2.27	4.23	ns	7	

NOTE:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Not 100% tested. Specified by design characterization.
3. All source synchronous AC timings are referenced to their associated strobe at GTLREF. Source synchronous data signals are referenced to the falling edge of their associated data strobe. Source synchronous address signals are referenced to the rising and falling edge of their associated address strobe. All source synchronous AGTL+ signal timings are referenced at GTLREF at the processor core.
4. Unless otherwise noted, these specifications apply to both data and address timings.
5. Valid delay timings for these signals are specified into the test circuit described in Figure 3 and with GTLREF at 2/3 $V_{CC} \pm 2\%$.
6. Specification is for a minimum swing defined between AGTL+ V_{IL_MAX} to V_{IH_MIN}. This assumes an edge rate of 0.3 V/ns to 4.0V/ns.
7. All source synchronous signals must meet the specified setup time to BCLK as well as the setup time to each respective strobe.
8. This specification represents the minimum time the data or address will be valid before its strobe. Refer to the appropriate platform design guidelines for more information on the definitions and use of these specifications.
9. This specification represents the minimum time the data or address will be valid after its strobe. Refer to the appropriate platform design guidelines for more information on the definitions and use of these specifications.
10. The rising edge of ADSTB# must come approximately 1/2 BCLK period (5 ns) after the falling edge of ADSTB#.
11. For this timing parameter, n = 1, 2, and 3 for the second, third, and last data strobes respectively.
12. The second data strobe (falling edge of DSTBn#) must come approximately 1/4 BCLK period (2.5 ns) after the first falling edge of DSTBp#. The third data strobe (falling edge of DSTBp#) must come approximately 2/4 BCLK period (5 ns) after the first falling edge of DSTBp#. The last data strobe (falling edge of DSTBn#) must come approximately 3/4 BCLK period (7.5 ns) after the first falling edge of DSTBp#.
13. This specification applies only to DSTBN[3:0]# and is measured to the second falling edge of the strobe.
14. This specification reflects a typical value, not a minimum or maximum.

Table 15. Asynchronous GTL+ AC Specifications

T# Parameter	Min	Max	Unit	Figure	Notes 1, 2, 3, 4
T35: Async GTL+ input pulse width, except PWRGOOD	2	N/A	BCLKs		
T36: PWRGOOD to RESET# de-assertion time	1	10	ms	10	
T37: PWRGOOD inactive pulse width	10	N/A	BCLKs	10	5
T38: PROCHOT# pulse width	500		us	12	6
T39: THERMTRIP# to power down sequence	0	0.5	sec	13	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. All AC timings for the Asynchronous GTL+ signals are referenced to the BCLK0 rising edge at Crossing Voltage (V_{CROSS}). All Asynchronous GTL+ signal timings are referenced at GTLREF.
3. These signals may be driven asynchronously.
4. Refer to Section 7.2 for additional timing requirements for entering and leaving low power states.
5. Refer to the PWRGOOD signal definition in Section 5.2 for more detail information on behavior of the signal.
6. Length of assertion for PROCHOT# does not equal internal clock modulation time. Time is allocated after the assertion of PROCHOT# for the processor to complete current instruction execution.

Table 16. System Bus AC Specifications (Reset Conditions)

T# Parameter	Min	Max	Unit	Figure	Notes[1]
T45: Reset Configuration Signals (A[31:3]#, BR[1:0]#, INIT#, SMI#) Setup Time	4		BCLKs	9	2
T46: Reset Configuration Signals (A[31:3]#, BR[1:0]#, INIT#, SMI#, A20M#, IGNNE#, LINT[1:0]) Hold Time	2	20	BCLKs	9, 10	3
T47: Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]) Setup Time	1		ms	9	2
T48: Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]) Delay Time		5	BCLKs	9	4

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Before the de-assertion of RESET#
3. After the clock that de-asserts RESET#.
4. After the assertion of RESET#.

Table 17. TAP Signal Group AC Specifications

T# Parameter	Min	Max	Unit	Figure	Notes 1,2,3,9
T55: TCK Period	60.0		ns	4	
T56: TCK Rise Time		9.5	ns	4	4
T57: TCK Fall Time		9.5	ns	4	4
T58: TMS, TDI Rise Time		8.5	ns	4	4
T59: TMS, TDI Fall Time		8.5	ns	4	4
T61: TDI, TMS Setup Time	0		ns	11	5,8
T62: TDI, TMS Hold Time	3.0		ns	11	5,8
T63: TDO Clock to Output Delay	0.5	3.5	ns	11	6
T64: TRST# Assert Time	2		T_{TCK}	12	7

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Not 100% tested. Specified by design characterization.
3. All AC timings for the TAP signals are referenced to the TCK signal at 0.5 * V_{CC} at the processor pins. All TAP signal timings (TMS, TDI, etc) are referenced at 0.5 * V_{CC} at the processor pins.
4. Rise and fall times are measured from the 20% to 80% points of the signal swing.
5. Referenced to the rising edge of TCK.
6. Referenced to the falling edge of TCK.
7. TRST# must be held asserted for 2 TCK periods to guarantee that it is recognized by the processor.
8. Specification for a minimum swing defined between TAP V_{T+} to V_{T-}. This assumes a minimum edge rate of 0.5V/ns.
9. It is recommended that TMS be asserted while TRST# is being deasserted.

Table 18. SMBus Signal Group AC Specifications

T# Parameter	Min	Max	Unit	Figure	Notes 1,2,3
T70: SM_CLK Frequency	10	100	KHz		
T71: SM_CLK Period	10	100	us		
T72: SM_CLK High Time	4.0	N/A	us	14	
T73: SM_CLK Low Time	4.7	N/A	us	14	
T74: SMBus Rise Time	0.02	1.0	us	14	5
T75: SMBus Fall Time	0.02	0.3	us	14	5
T76: SMBus Output Valid Delay	0.1	4.5	us	15	
T77: SMBus Input Setup Time	250	N/A	ns	14	
T78: SMBus Input Hold Time	300	N/A	ns	14	
T79: Bus Free Time	4.7	N/A	us	14	4, 6
T80: Hold Time after Repeated Start Condition	4.0	N/A	us	14	
T81: Repeated Start Condition Setup Time	4.7	N/A	us	14	
T82: Stop Condition Setup Time	4.0	N/A	us	14	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. These parameters are based on design characterization and are not tested.
3. All AC timings for the SMBus signals are referenced at V_{IL_MAX} or V_{IL_MIN} and measured at the processor pins. Refer to Figure 14.
4. Minimum time allowed between request cycles.
5. Rise time is measured from (V_{IL_MAX} - 0.15V) to (V_{IH_MIN} + 0.15V). Fall time is measured from (0.9 * SM_VCC) to (V_{IL_MAX} - 0.15V). DC parameters are specified in Table 10.

6. Following a write transaction, an internal write cycle time of 10ms must be allowed before starting the next transaction.

2.14 Processor AC Timing Waveforms

The following figures are used in conjunction with the AC timing tables, Table 12 through Table 18.

Note: For Figure 4 through Figure 12, the following apply:

1. All common clock AC timings for AGTL+ signals are referenced to the Crossing Voltage (V_{CROSS}) of the BCLK[1:0] at rising edge of BCLK0. All common clock AGTL+ signal timings are referenced at GTLREF at the processor core (pads).
2. All source synchronous AC timings for AGTL+ signals are referenced to their associated strobe (address or data) at GTLREF. Source synchronous data signals are referenced to the falling edge of their associated data strobe. Source synchronous address signals are referenced to the rising and falling edge of their associated address strobe. All source synchronous AGTL+ signal timings are referenced at GTLREF at the processor core (pads).
3. All AC timings for AGTL+ strobe signals are referenced to BCLK[1:0] at V_{CROSS}. All AGTL+ strobe signal timings are referenced at GTLREF at the processor core (pads).
4. All AC timings for the TAP signals are referenced to the TCK signal at 0.5 * V_{CC} at the processor pins. All TAP signal timings (TMS, TDI, etc) are referenced at 0.5 * V_{CC} at the processor core (pads).
5. All AC timings for the SMBus signals are referenced to the SM_CLK signal at 0.5 * SM_VCC at the processor pins. All SMBus signal timings (SM_DAT, SM_ALERT#, etc) are referenced at V_{IL_MAX} or V_{IL_MIN} at the processor pins.

Figure 3. Electrical Test Circuit

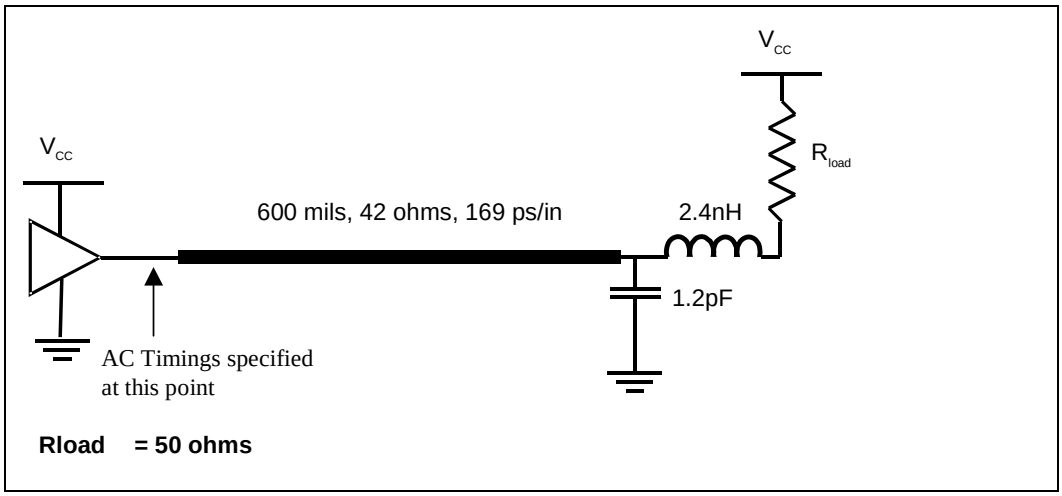
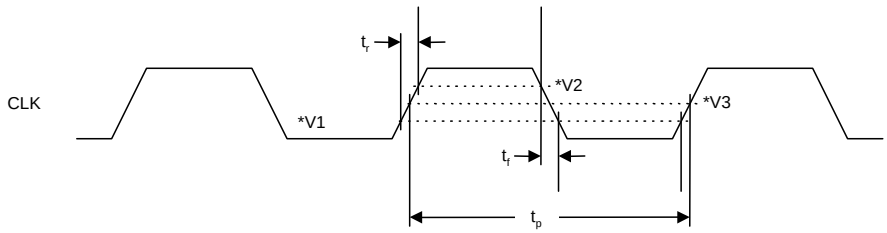


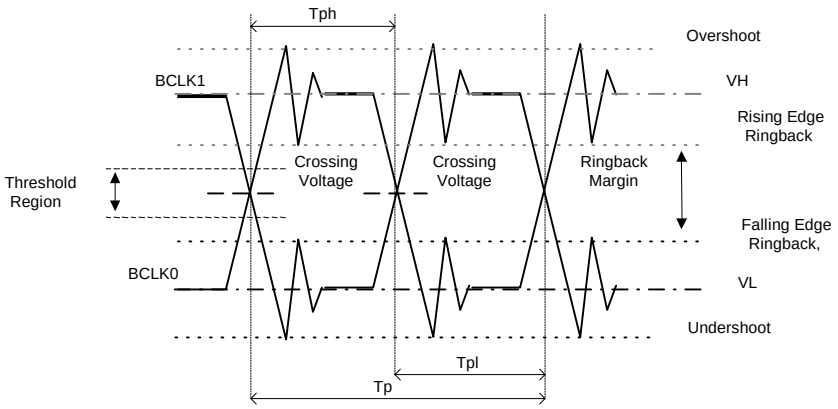
Figure 4. TCK Clock Waveform



T_r = T56, T58 (Rise Time)
T_f = T57, T59 (Fall Time)
T_p = T55 (Period)

V1, V2: For rise and fall times, TCK is measured between V_{t-} to V_{t+}.
V3: TCK is referenced to 0.5 * V_{CC}.

Figure 5. Differential Clock Waveform



Tp = T1 (BCLK[1:0] period)
T2 = BCLK[1:0] Period stability (not shown)
Tph =T3 (BCLK[1:0] pulse high time)
Tpl = T4 (BCLK[1:0] pulse low time)
T5 = BCLK[1:0] rise time through the threshold region
T6 = BCLK[1:0] fall time through the threshold region

Figure 6. System Bus Common Clock Valid Delay Timing Waveform

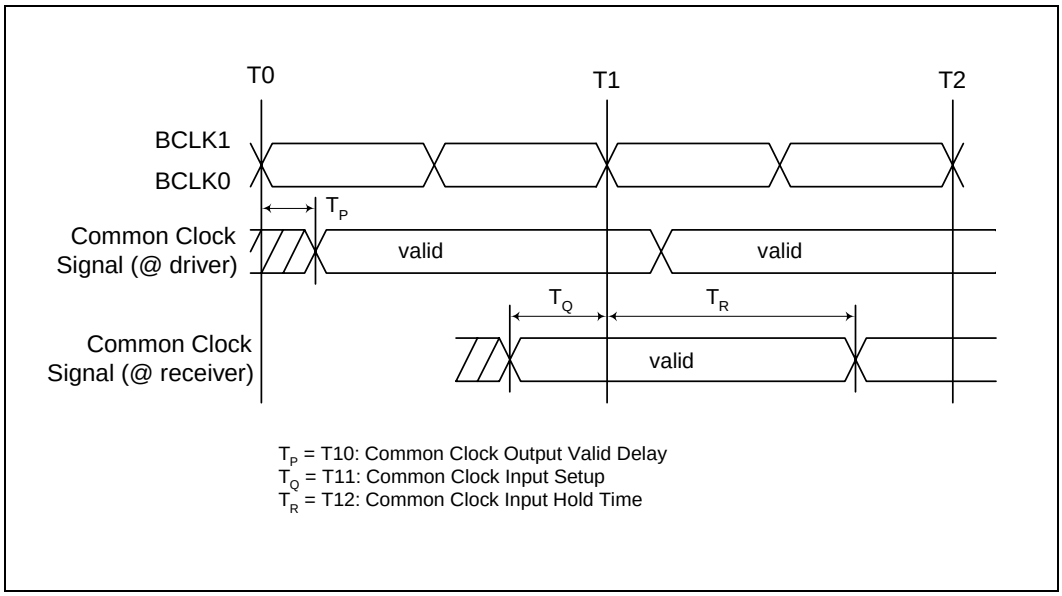


Figure 7. System Bus Source Synchronous 2X (Address) Timing Waveform

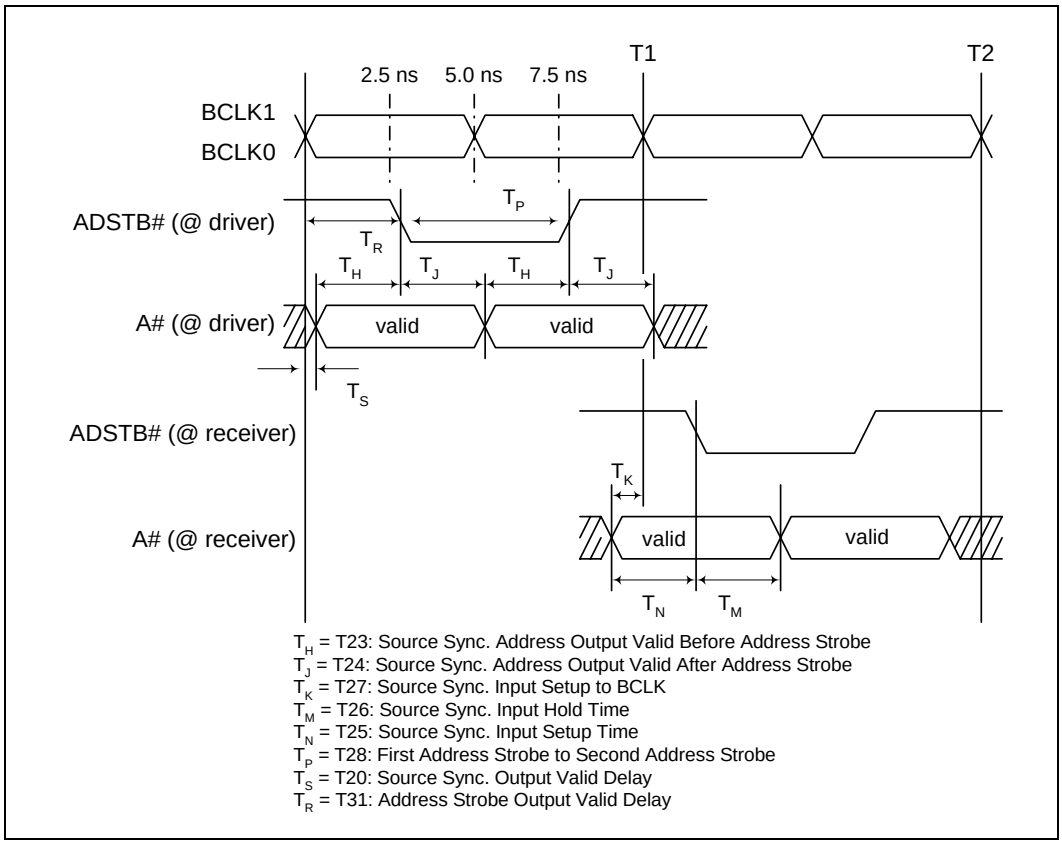
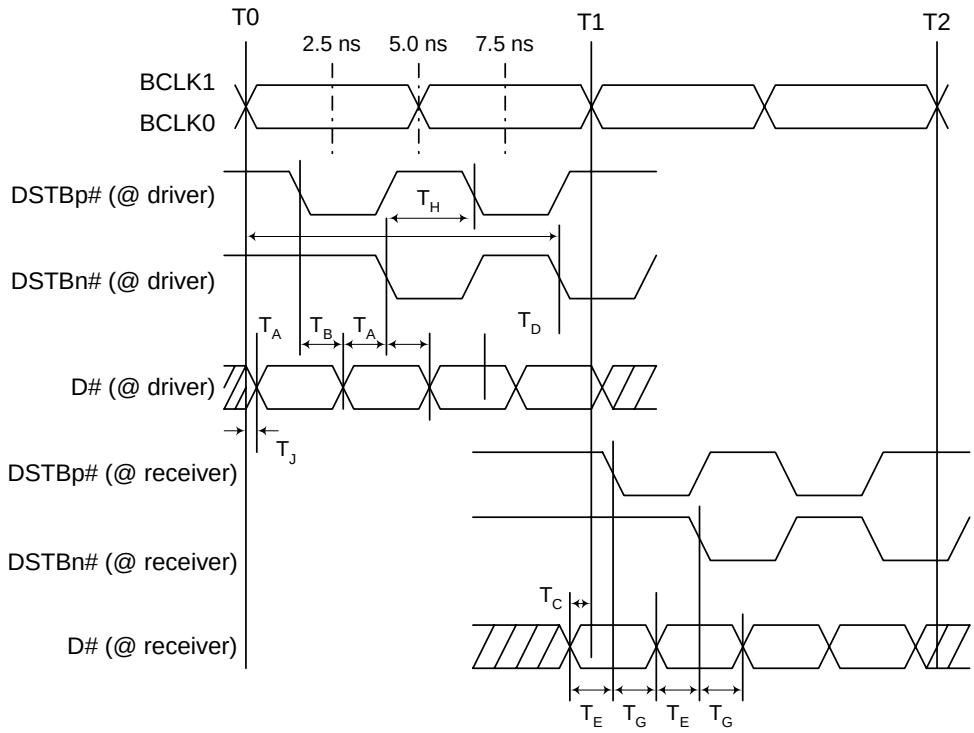


Figure 8. System Bus Source Synchronous 4X (Data) Timing Waveform



T_A = T11: Source Sync. Data Output Valid Delay Before Data Strobe
T_B = T12: Source Sync. Data Output Valid Delay After Data Strobe
T_C = T17: Source Sync. Setup Time to BCLK
T_D = T30: Source Sync. Data Strobe 'N' (DSTBN#) Output Valid Delay
T_E = T15: Source Sync. Input Setup Time
T_G = T16: Source Sync. Input Hold Time
T_H = T29: First Data Strobe to Subsequent Strobes
T_J = T20: Source Sync. Data Output Valid Delay

Figure 9. System Bus Reset and Configuration Timing Waveform

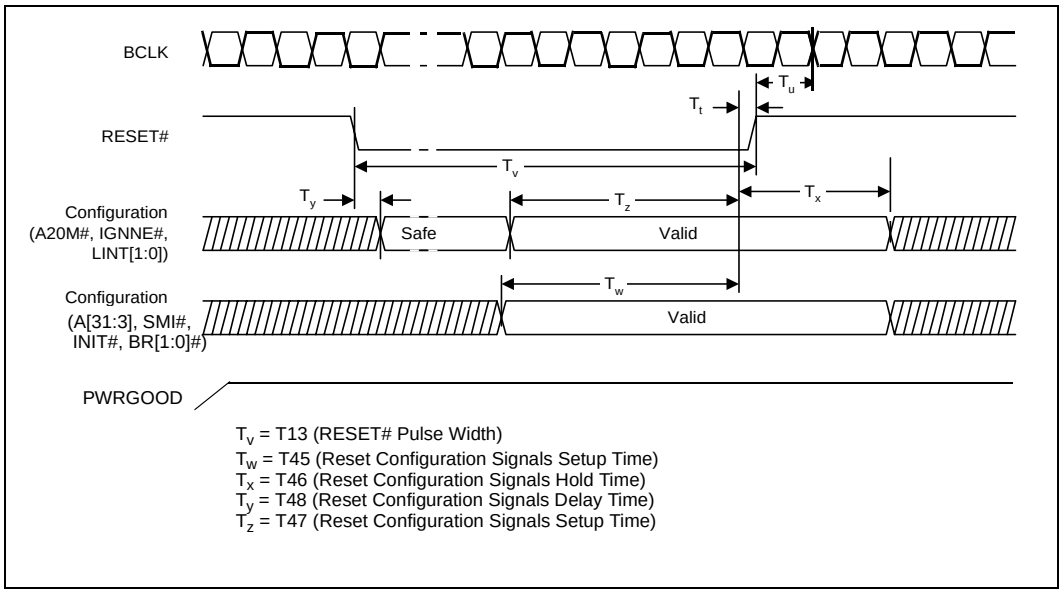


Figure 10. Power-On Reset and Configuration Timing Waveform

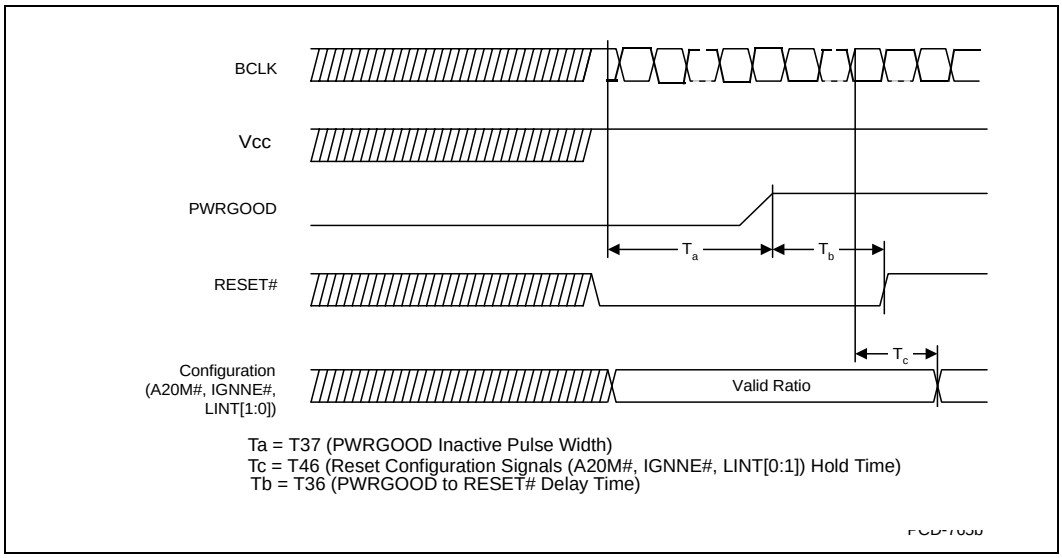


Figure 11. TAP Valid Delay Timing Waveform

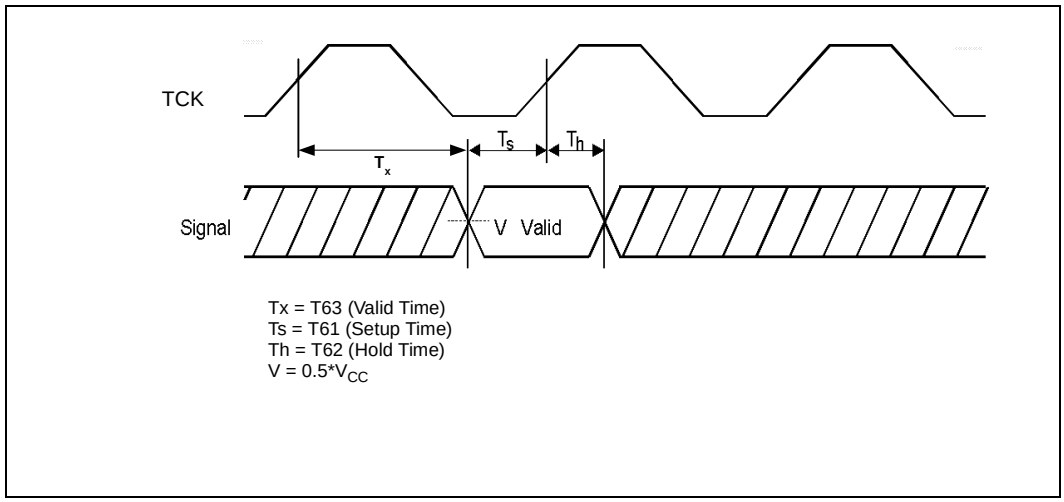


Figure 12. Test Reset (TRST#), Async GTL+ Input, and PROCHOT# Timing Waveform

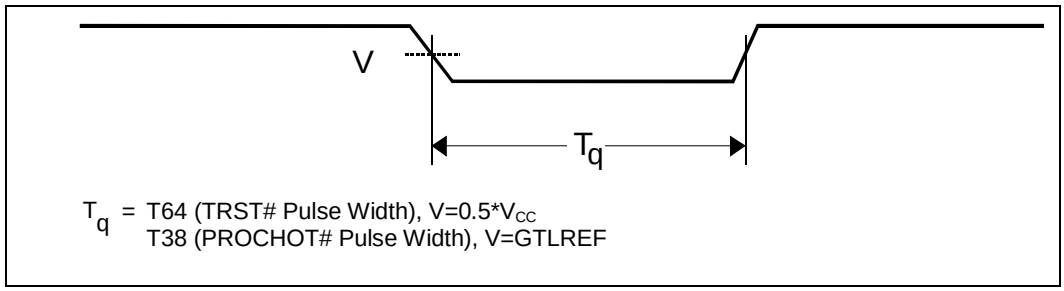


Figure 13. THERMTRIP# Power Down Waveform

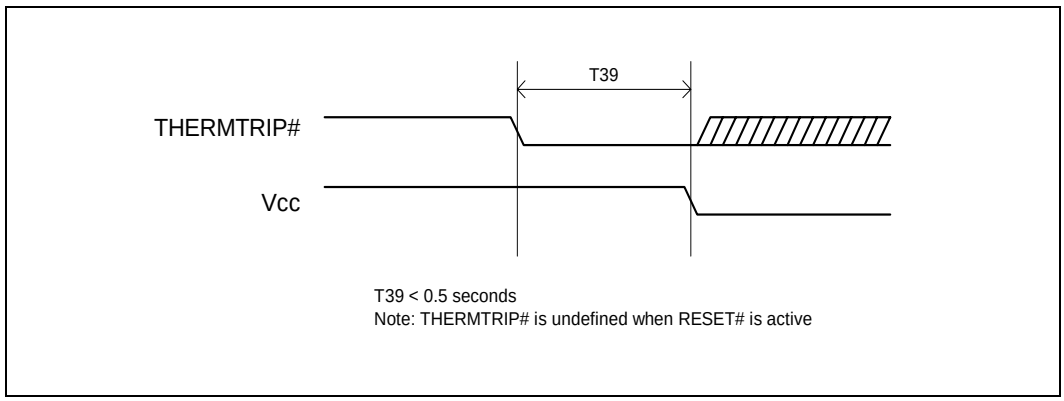


Figure 14. SMBus Timing Waveform

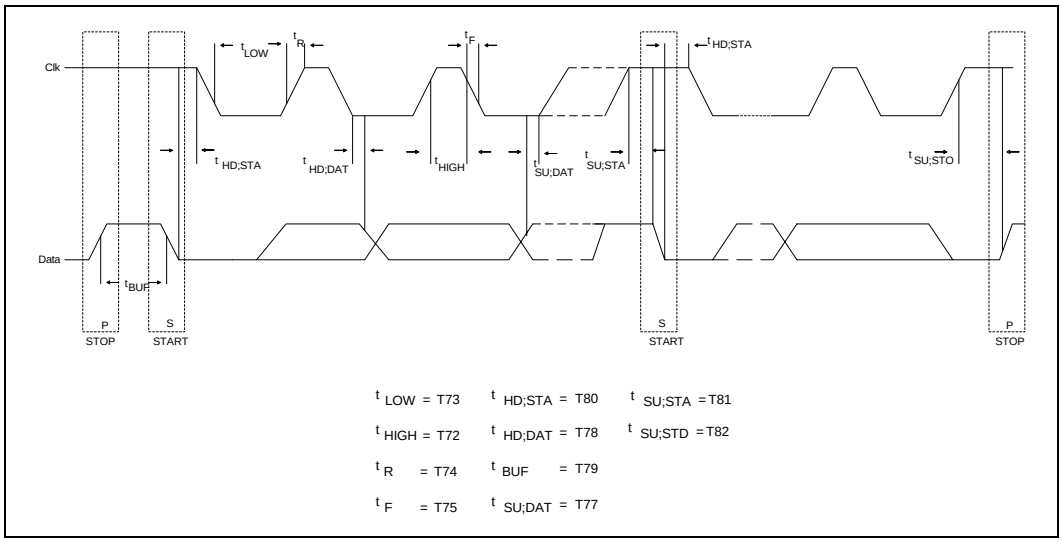
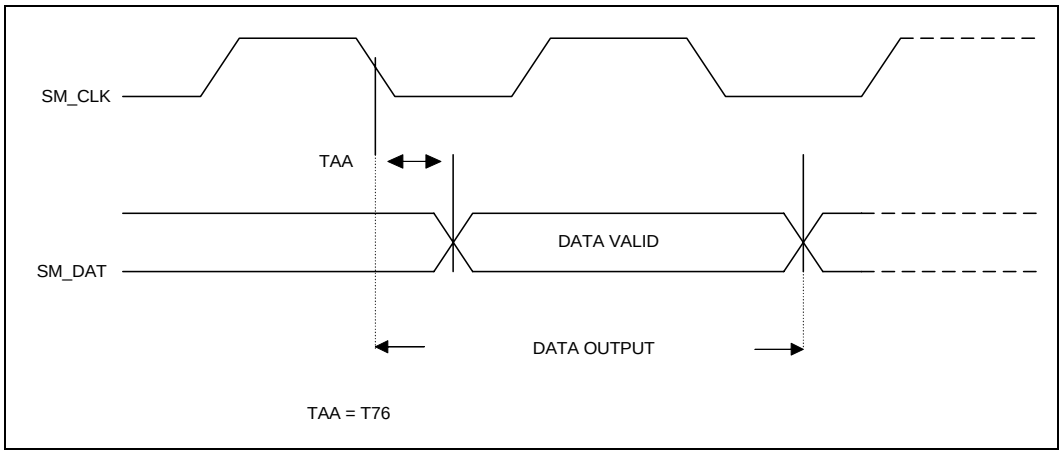


Figure 15. SMBus Valid Delay Timing Waveform



3.0 System Bus Signal Quality Specifications

Source synchronous data transfer requires the clean reception of data signals and their associated strobes. Ringing below receiver thresholds, non-monotonic signal edges, and excessive voltage swing will adversely affect system timings. Ringback and signal non-monotinicity cannot be tolerated since these phenomena may inadvertently advance receiver state machines. Excessive signal swings (overshoot and undershoot) are detrimental to silicon gate oxide integrity, and can cause device failure if absolute voltage limits are exceeded. Additionally, overshoot and undershoot can cause timing degradation due to the build up of inter-symbol interference (ISI) effects.

For these reasons, it is crucial that the designer work towards a solution that provides acceptable signal quality across all systematic variations encountered in volume manufacturing.

This section documents signal quality metrics used to derive topology and routing guidelines through simulation and all specifications are specified at the processor core (pad measurements).

Specifications for signal quality are for measurements at the processor core only and are only observable through simulation. The same is true for all system bus AC timing specifications in Section 2.13. Therefore, proper simulation of the processor system bus is the only means to verify proper timing and signal quality metrics.

3.1 System Bus Clock (BCLK) Signal Quality Specifications and Measurement Guidelines

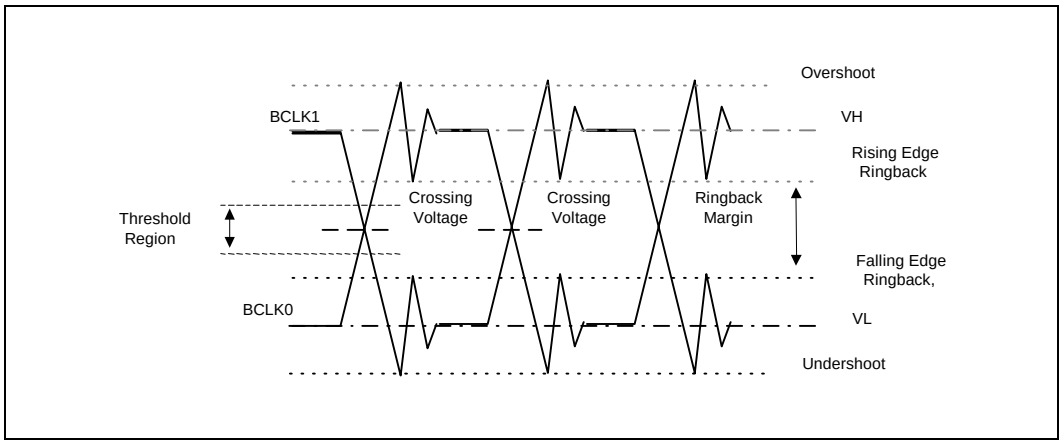
Table 19 describes the signal quality specifications at the processor pads for the processor system bus clock (BCLK) signals. Figure 16 describes the signal quality waveform for the system bus clock at the processor pads.

Table 19. BCLK Signal Quality Specifications

Parameter	Min	Max	Unit	Figure	Notes[1]
BCLK[1:0] Overshoot	N/A	0.30	V	16	
BCLK[1:0] Undershoot	N/A	0.30	V	16	
BCLK[1:0] Ringback Margin	0.20	N/A	V	16	
BCLK[1:0] Threshold Region	N/A	0.10	V	16	2

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the BCLK signal can dip back to after passing the V_{IH} (rising) or V_{IL} (falling) voltage limits. This specification is an absolute value.

Figure 16. BCLK[1:0] Signal Integrity Waveform



3.2 System Bus Signal Quality Specifications and Measurement Guidelines

3.2.1 Ringback Guidelines

Many scenarios have been simulated to generate a set of system bus layout guidelines which are available in the appropriate platform design guidelines.

Table 20 provides the signal quality specifications for the AGTL+ and asynchronous GTL+ signal groups. Table 21 demonstrates the signal quality specification for the TAP signals. These specifications are for use in simulating signal quality at the processor core pads.

Maximum allowable overshoot and undershoot specifications for a given duration of time are detailed in Table 22 through Table 25. System bus ringback tolerance for AGTL+ and asynchronous GTL+ signal groups are shown in Figure 17 (low-to-high transitions) and Figure 18 (high-to-low transitions).

The TAP signal group includes hysteresis on the input buffers and thus has relaxed ringback requirements when compared to the other buffer types. Figure 19 shows the system bus ringback tolerance for low-to-high transitions and Figure 20 for high-to-low transitions. The hysteresis values V_{t+} and V_{t-} can be found in Table 9.

Table 20. Ringback Specifications for AGTL+ and Asynchronous GTL+ Signal Groups

Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Unit	Figure	Notes
All Signals	0 → 1	GTLREF + 0.100	V	17	1,2,3,4,5,6,7
All Signals	1 → 0	GTLREF - 0.100	V	18	1,2,3,4,5,6,7

NOTES:
1. All signal integrity specifications are measured at the processor core (pads).
2. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
3. Specifications are for the edge rate of 0.3 - 4.0V/ns.
4. All values specified by design characterization.
5. Please see Section 3.2.3 for maximum allowable overshoot.

6. Ringback between GTLREF + 100 mV and GTLREF - 100 mV is not supported.
7. Intel recommends simulations not exceed a ringback value of GTLREF +/- 200 mV to allow margin for other sources of system noise.

Figure 17. Low-to-High Receiver Ringback Tolerance for AGTL+ and Async GTL+ Signals

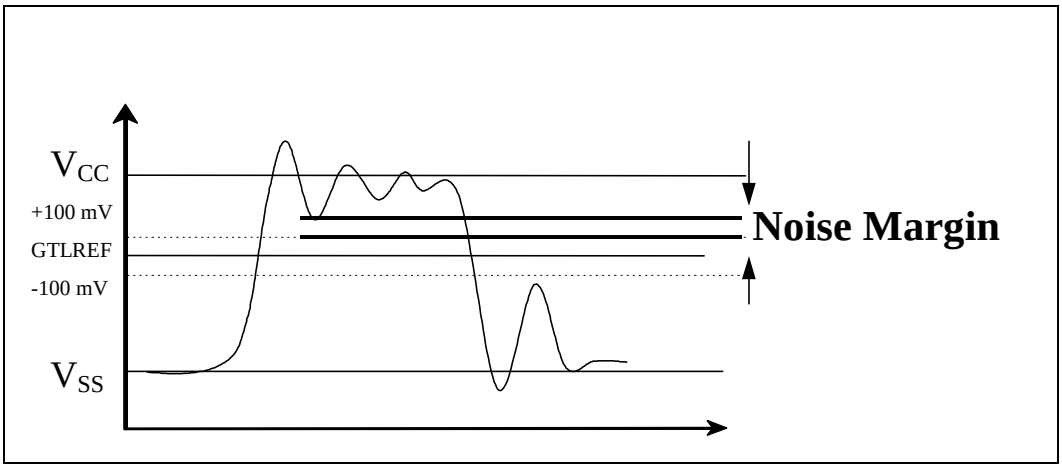


Figure 18. High-to-Low Receiver Ringback Tolerance for AGTL+ and Async GTL+ Signals

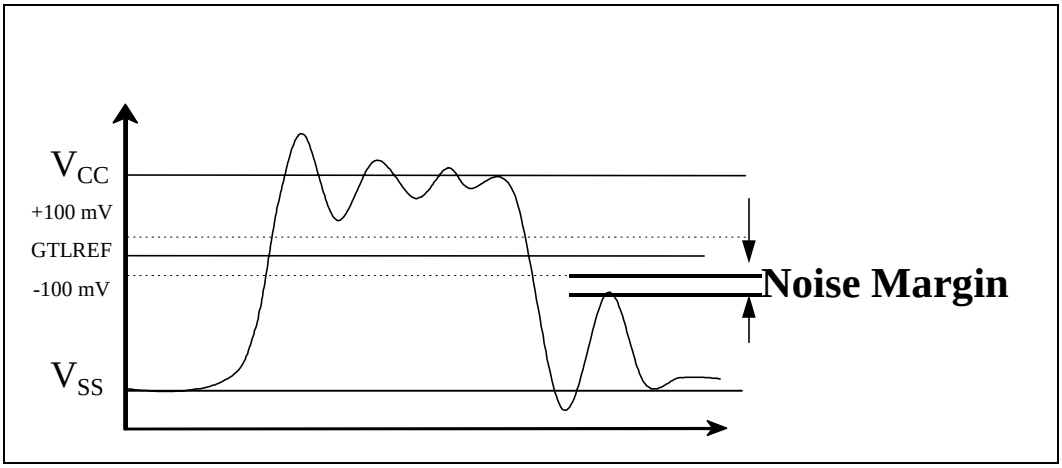


Table 21. Ringback Specifications for TAP Signal Group

Signal Group	Transition	Maximum Ringback (with input diodes present)	Units	Figure	Notes
TAP	0 → 1	V_{T+}(max) to V_{T-}(max)	V	19	1,2,3,4,5
TAP	1 → 0	V_{T-}(max) to V_{T+}(max)	V	20	1,2,3,4,5

NOTES:
1. All signal integrity specifications are measured at the processor core (pads).
2. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
3. Specifications are for the edge rate of 0.3 - 4.0V/ns.
4. All values specified by design characterization.
5. Please see Section 3.2.3 for maximum allowable overshoot.

Figure 19. Low-to-High Receiver Ringback Tolerance for TAP Buffers

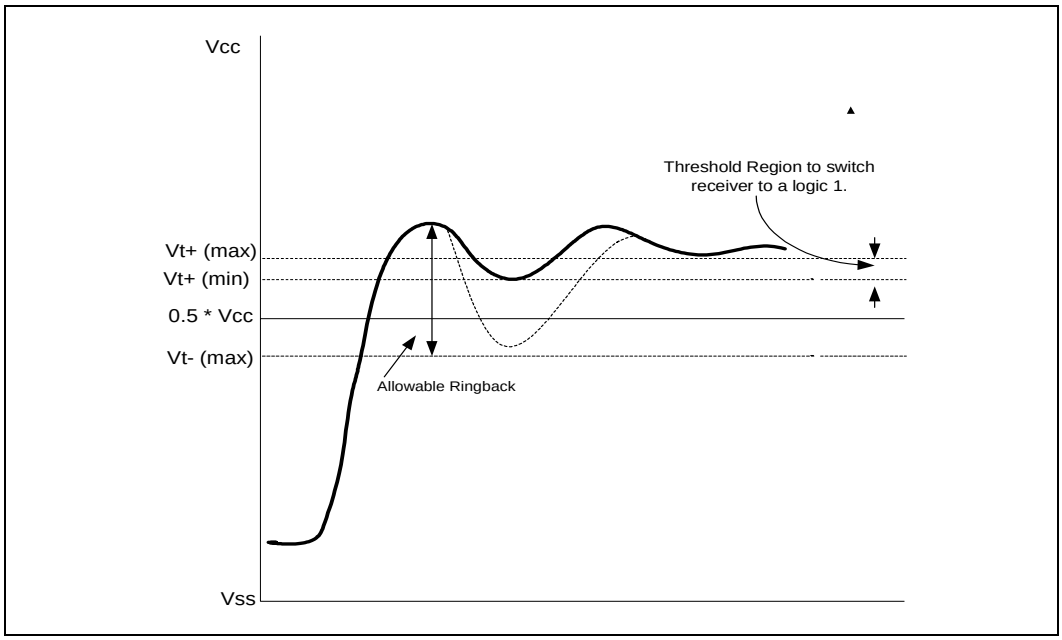
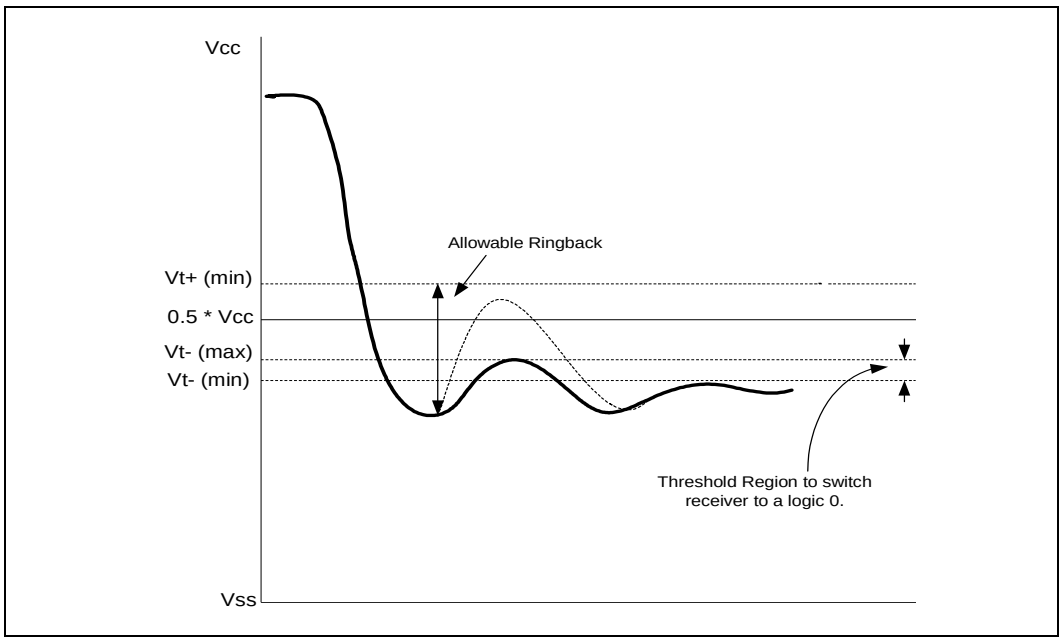


Figure 20. High-to-Low Receiver Ringback Tolerance for TAP Buffers



3.2.2 Overshoot/Undershoot Guidelines

Overshoot (or undershoot) is the absolute value of the maximum voltage above or below V_{SS}. The overshoot/undershoot specifications limit transitions beyond V_{CC} or V_{SS} due to the fast signal edge rates. The processor can be damaged by repeated overshoot or undershoot events on any input, output, or I/O buffer if the charge is large enough (i.e., if the over/undershoot is great enough). Determining the impact of an overshoot/undershoot condition requires knowledge of the magnitude, the pulse direction, and the activity factor (AF). Permanent damage to the processor is the likely result of excessive overshoot/undershoot.

When performing simulations to determine impact of overshoot and undershoot, ESD diodes must be properly characterized. ESD protection diodes do not act as voltage clamps and will not provide overshoot or undershoot protection. ESD diodes modelled within Intel I/O buffer models do not clamp undershoot or overshoot and will yield correct simulation results. If other I/O buffer models are being used to characterize the processor system bus, care must be taken to ensure that ESD models do not clamp extreme voltage levels. Intel I/O buffer models also contain I/O capacitance characterization. Therefore, removing the ESD diodes from an I/O buffer model will impact results and may yield excessive overshoot/undershoot.

3.2.3 Overshoot/Undershoot Magnitude

Magnitude describes the maximum potential difference between a signal and its voltage reference level. For the Intel® Xeon™ processor, both are referenced to V_{SS}. It is important to note that overshoot and undershoot conditions are separate and their impact must be determined independently.

Overshoot/undershoot magnitude levels must observe the absolute maximum specifications listed in Table 22 through Table 25. These specifications must not be violated at any time regardless of bus activity or system state. Within these specifications are threshold levels that define different allowed pulse durations. Provided that the magnitude of the overshoot/undershoot is within the absolute maximum specifications (2.3V for overshoot and -0.65V for undershoot), the pulse magnitude, duration and activity factor must all be used to determine if the overshoot/undershoot pulse is within specifications.

3.2.4 Overshoot/Undershoot Pulse Duration

Pulse duration describes the total time an overshoot/undershoot event exceeds the overshoot/undershoot reference voltage (V_{CC}). The total time could encompass several oscillations above the reference voltage. Multiple overshoot/undershoot pulses within a single overshoot/undershoot event may need to be measured to determine the total pulse duration.

Note 1: Oscillations below the reference voltage can not be subtracted from the total overshoot/undershoot pulse duration.

3.2.5 Activity Factor

Activity Factor (AF) describes the frequency of overshoot (or undershoot) occurrence relative to a clock. Since the highest frequency of assertion of any common clock signal is every other clock, an AF = 1 indicates that the specific overshoot (or undershoot) waveform occurs every other clock cycle. Thus, an AF = 0.01 indicates that the specific overshoot (or undershoot) waveform occurs one time in every 200 clock cycles.

For source synchronous signals (address, data, and associated strobes), the activity factor is in reference to the strobe edge. The highest frequency of assertion of any source synchronous signal is every active edge of its associated strobe. So, an AF = 1 indicates that the specific overshoot (or undershoot) waveform occurs every strobe cycle.

The specifications provided in Table 22 through Table 25 show the maximum pulse duration allowed for a given overshoot/undershoot magnitude at a specific activity factor. Each table entry is independent of all others, meaning that the pulse duration reflects the existence of overshoot/undershoot events of that magnitude ONLY. A platform with an overshoot/undershoot that just meets the pulse duration for a specific magnitude where the AF < 1, means that there can be no other overshoot/undershoot events, even of lesser magnitude (note that if AF = 1, then the event occurs at all times and no other events can occur).

Note 1: Activity factor for common clock AGTL+ signals is referenced to BCLK[1:0] frequency.

Note 2: Activity factor for source synchronous (2x) signals is referenced to ADSTB[1:0]#.

Note 3: Activity factor for source synchronous (4x) signals is referenced to DSTBP[3:0]# and DSTBN[3:0]#.

3.2.6 Reading Overshoot/Undershoot Specification Tables

The overshoot/undershoot specification for the processor is not a simple single value. Instead, many factors are needed to determine what the over/undershoot specification is. In addition to the magnitude of the overshoot, the following parameters must also be known: the width of the overshoot and the activity factor (AF). To determine the allowed overshoot for a particular overshoot event, the following must be done:

1. Determine the *signal group* that particular signal falls into. For AGTL+ signals operating in the 4x source synchronous domain, use Table 22. For AGTL+ signals operating in the 2x source synchronous domain, use Table 23. If the signal is an AGTL+ signal operating in the common clock domain, use Table 24. Finally, all other signals reside in the 33MHz domain (asynchronous GTL+, TAP, etc.) and are referenced in Table 25.
2. Determine the *magnitude* of the overshoot or the undershoot (relative to V_{SS}).
3. Determine the *activity factor* (how often does this overshoot occur?).
4. Next, from the appropriate specification table, determine the *maximum pulse duration* (in nanoseconds) allowed.
5. Compare the specified maximum pulse duration to the signal being measured. If the pulse duration measured is less than the pulse duration shown in the table, then the signal meets the specifications.

Undershoot events must be analyzed separately from overshoot events as they are mutually exclusive.

3.2.7 Determining if a System Meets the Overshoot/Undershoot Specifications

The overshoot/undershoot specifications listed in the following tables specify the allowable overshoot/undershoot for a single overshoot/undershoot event. However most systems will have multiple overshoot and/or undershoot events that each have their own set of parameters (duration,

AF and magnitude). While each overshoot on its own may meet the overshoot specification, when you add the total impact of all overshoot events, the system may fail. A guideline to ensure a system passes the overshoot and undershoot specifications is shown below.

1. Ensure no signal ever exceeds V_{CC} or -0.25V OR
2. If only one overshoot/undershoot event magnitude occurs, ensure it meets the over/undershoot specifications in the following tables OR
3. If multiple overshoots and/or multiple undershoots occur, measure the worst case pulse duration for each magnitude and compare the results against the AF = 1 specifications. If all of these worst case overshoot or undershoot events meet the specifications (measured time < specifications) in the table (where AF=1), then the system passes.

The following notes apply to Table 22 through Table 25.

- Absolute Maximum Overshoot magnitude of 2.3V must never be exceeded.
- Absolute Maximum Overshoot is measured referenced to V_{SS}, Pulse Duration of overshoot is measured relative to V_{CC}.
- Absolute Maximum Undershoot and Pulse Duration of undershoot is measured relative to V_{SS}.
- Ringback below V_{CC} cannot be subtracted from overshoots/undershoots.
- Lesser undershoot does not allocate overshoot with longer duration or greater magnitude .
- OEM's are strongly encouraged to follow Intel layout guidelines.
- All values specified by design characterization.

Table 22. Source Synchronous (400MHz) AGTL+ Signal Group Overshoot/Undershoot Tolerance

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF = 1	Pulse Duration (ns) AF = 0.1	Pulse Duration (ns) AF = 0.01	Notes [1,2,3]
2.30	-0.65	0.07	0.65	5.00	
2.25	-0.60	0.12	1.22	5.00	
2.20	-0.55	0.23	2.25	5.00	
2.15	-0.50	0.42	4.15	5.00	
2.10	-0.45	0.74	5.00	5.00	
2.05	-0.40	1.38	5.00	5.00	
2.00	-0.35	2.50	5.00	5.00	
1.95	-0.30	4.50	5.00	5.00	
1.90	-0.25	5.00	5.00	5.00	
1.85	-0.20	5.00	5.00	5.00	
1.80	-0.15	5.00	5.00	5.00	
1.75	-0.10	5.00	5.00	5.00	

NOTES:
1. These specifications are measured at the processor pad.
2. Assumes a BCLK period of 10 ns.
3. AF is referenced to associated source synchronous strobes.

Table 23. Source Synchronous (200MHz) AGTL+ Signal Group Overshoot/Undershoot Tolerance

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF = 1	Pulse Duration (ns) AF = 0.1	Pulse Duration (ns) AF = 0.01	Notes [1,2,3]
2.30	-0.65	0.13	1.30	10.0	
2.25	-0.60	0.24	2.44	10.0	
2.20	-0.55	0.45	4.50	10.0	
2.15	-0.50	0.83	8.30	10.0	
2.10	-0.45	1.48	10.0	10.0	
2.05	-0.40	2.76	10.0	10.0	
2.00	-0.35	5.00	10.0	10.0	
1.95	-0.30	5.00	10.0	10.0	
1.90	-0.25	10.0	10.0	10.0	
1.85	-0.20	10.0	10.0	10.0	
1.80	-0.15	10.0	10.0	10.0	
1.75	-0.10	10.0	10.0	10.0	

NOTES:
1. These specifications are measured at the processor pad.
2. Assumes a BCLK period of 10 ns.
3. AF is referenced to associated source synchronous strobes.

Table 24. Common Clock (100MHz) AGTL+ Signal Group Overshoot/Undershoot Tolerance

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF = 1	Pulse Duration (ns) AF = 0.1	Pulse Duration (ns) AF = 0.01	Notes [1,2,3]
2.30	-0.65	0.26	2.60	20.0	
2.25	-0.60	0.49	4.88	20.0	
2.20	-0.55	0.90	9.00	20.0	
2.15	-0.50	1.66	16.60	20.0	
2.10	-0.45	2.96	20.0	20.0	
2.05	-0.40	5.52	20.0	20.0	
2.00	-0.35	10.0	20.0	20.0	
1.95	-0.30	18.0	20.0	20.0	
1.90	-0.25	20.0	20.0	20.0	
1.85	-0.20	20.0	20.0	20.0	
1.80	-0.15	20.0	20.0	20.0	
1.75	-0.10	20.0	20.0	20.0	

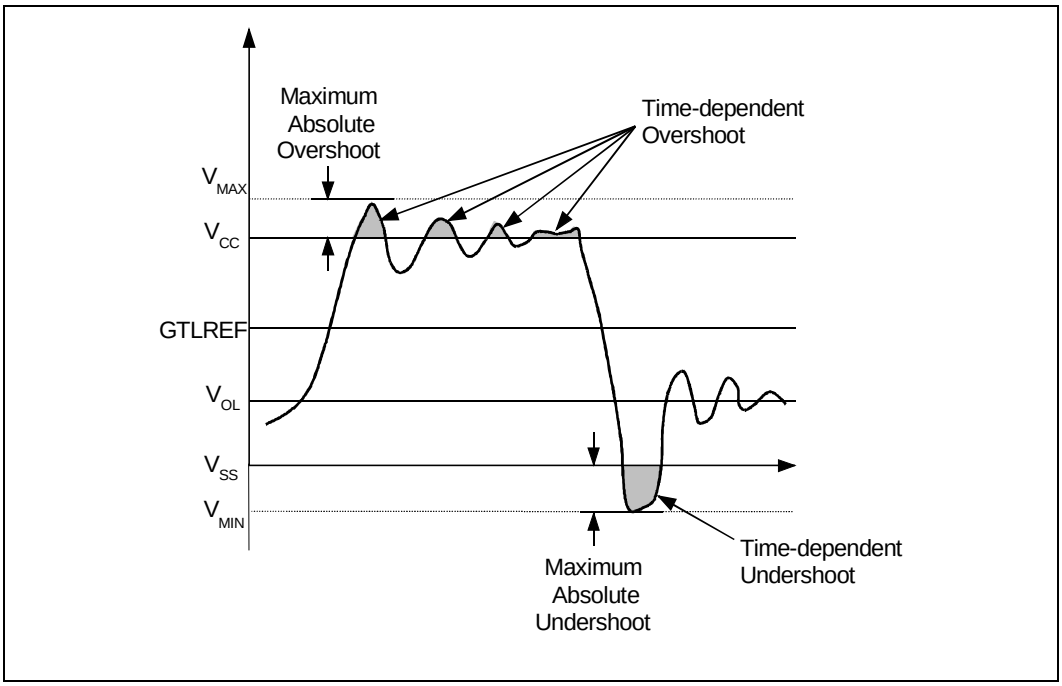
NOTES:
1. These specifications are measured at the processor pad.
2. BCLK period is 10 ns.
3. AF is referenced to BCLK[1:0].

Table 25. Asynchronous GTL+ and TAP Signal Groups Overshoot/Undershoot Tolerance

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF = 1	Pulse Duration (ns) AF = 0.1	Pulse Duration (ns) AF = 0.01	Notes [1,2]
2.30	-0.65	0.78	7.80	60.0	
2.25	-0.60	1.46	14.64	60.0	
2.20	-0.55	2.70	27.0	60.0	
2.15	-0.50	4.98	49.8	60.0	
2.10	-0.45	8.88	60.0	60.0	
2.05	-0.40	16.56	60.0	60.0	
2.00	-0.35	30.0	60.0	60.0	
1.95	-0.30	54.0	60.0	60.0	
1.90	-0.25	60.0	60.0	60.0	
1.85	-0.20	60.0	60.0	60.0	
1.80	-0.15	60.0	60.0	60.0	
1.75	-0.10	60.0	60.0	60.0	

NOTES:
1. These specifications are measured at the processor pad.
2. These signals are assumed in a 33MHz time domain.

Figure 21. Maximum Acceptable Overshoot/Undershoot Waveform



4.0 Mechanical Specifications

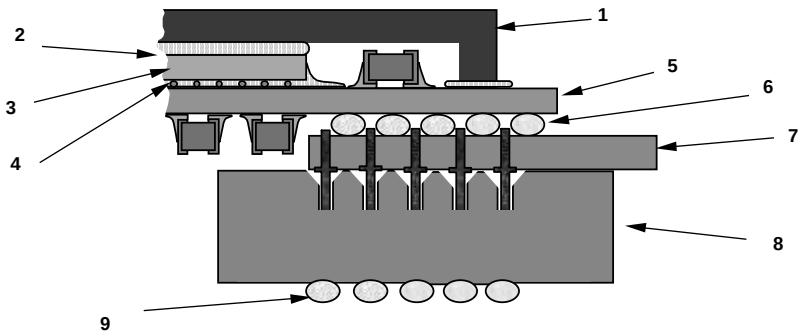
The Intel® Xeon™ processor uses Pin Grid Array (PGA) package technology. Components of the package include the integrated heat spreader (IHS), an organic land grid array (OLGA) package or flip chip ball grid array (FC-BGA) package containing the processor die and a pinned FR4 interposer. Mechanical specifications for the processor are given in this section. See Section 1.1 for terminology listing. Figure 22 provides a basic processor assembly drawing to better understand the components which make up the entire processor. In addition to the package components, the processor also includes several passive components, an EEPROM, and a thermal sensor.

The Intel Xeon processor utilizes a surface mount 603 pin zero-insertion force (ZIF) socket for installation into the system board. See the *603 Pin Socket Design Guidelines* for further details on the socket.

Note: For Figure 22 through Figure 28, the following notes apply:

1. Unless otherwise specified, the following drawings are dimensioned in millimeters.
2. All dimensions are not tested, but guaranteed by design characterization.
3. Figures and drawings labeled as “Reference Dimensions” are provided for informational purposes only. Reference Dimensions are extracted from the mechanical design database and are nominal dimensions with no tolerance information applied. Reference Dimensions are NOT checked as part of the processor manufacturing process. Unless noted as such, dimensions in parentheses without tolerances are Reference Dimensions.
4. Drawings are not to scale.

Figure 22. Processor Assembly Drawing (Including Socket)



NOTE: This drawing is not to scale and is for reference only. The 603-pin socket is supplied as a reference only.

KEY:
1. Integrated Heat Spreader (IHS)
2. Thermal Interface Material (TIM) between processor die and IHS
3. Processor die
4. Flip Chip interconnect
5. OLGA (Organic Land Grid Array) package or FC-BGA (Flip Chip Ball Grid Array) package
6. OLGA package or FC-BGA package solder joints
7. Processor interposer
8. 603-pin socket
9. 603-pin socket solder joints

4.1 Processor Mechanical Specifications

Figure 23. Top View Component Placement Detail

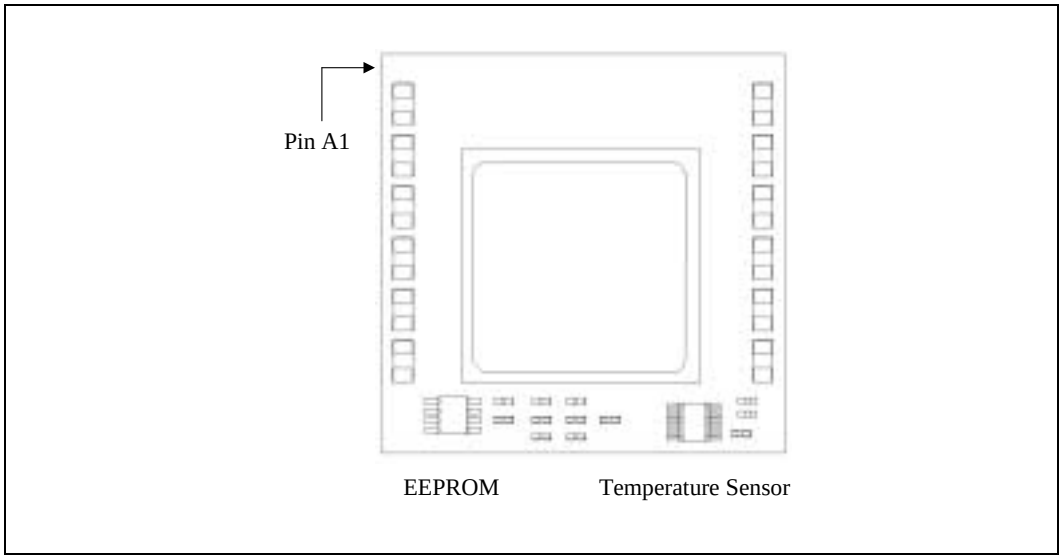


Figure 24. Processor Package Drawing

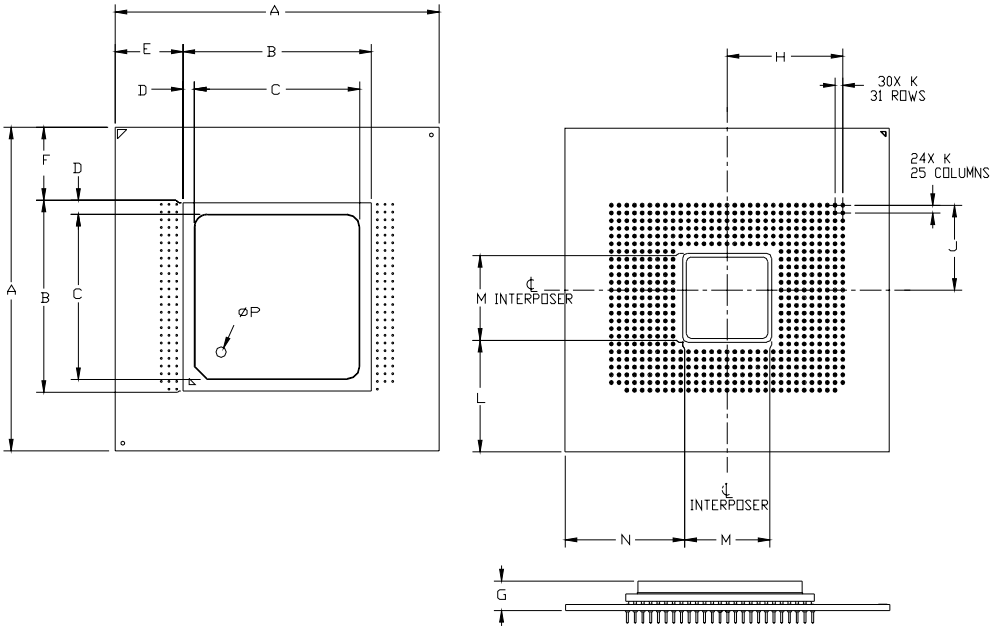


Table 26. Package Dimensions

Symbol	Millimeters			Notes
	Min	Nominal	Max	
A	53.190	53.340	53.490	
B	30.900	31.000	31.100	
C	26.900	27.000	27.100	
D	1.365	2.000	2.635	
E	11.018	11.170	11.322	
F	12.288	12.440	12.592	
G	4.200	4.700	5.200	
H	18.821	19.050	19.279	
J	13.741	13.970	14.199	
K		1.270		Nominal
L	17.831	18.085	18.339	
M	14.503	14.630	14.757	
N	19.101	19.355	19.609	
∅P	1.400	1.700	2.000	Diameter

Figure 25 details the keep-in zone for components mounted to the top side of the processor interposer. The components include the EEPROM, thermal sensor, resistors and capacitors.

Figure 25. Top View - Component Height Keep-in

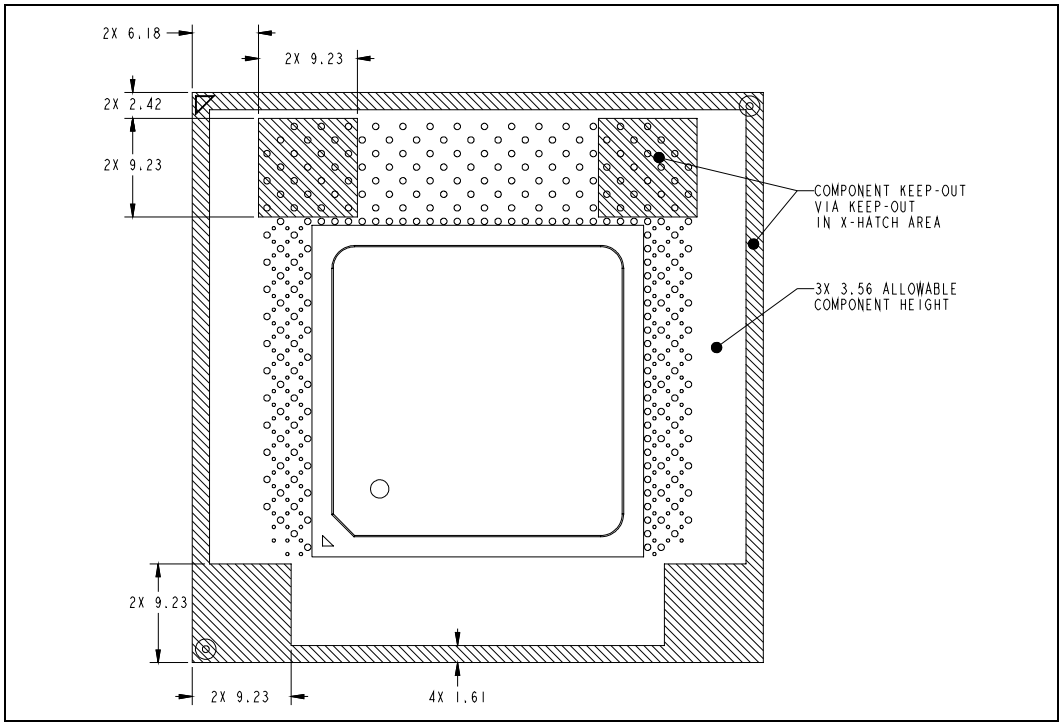


Figure 26 details the keep in specification for pin-side components. The processor may contain pin side capacitors mounted to the processor package. The capacitors will be exposed within the opening of the interposer cavity. This keep-in specification applies to both packages.

Figure 26. Processor Cross Section View - Pin Side Component Keep-in

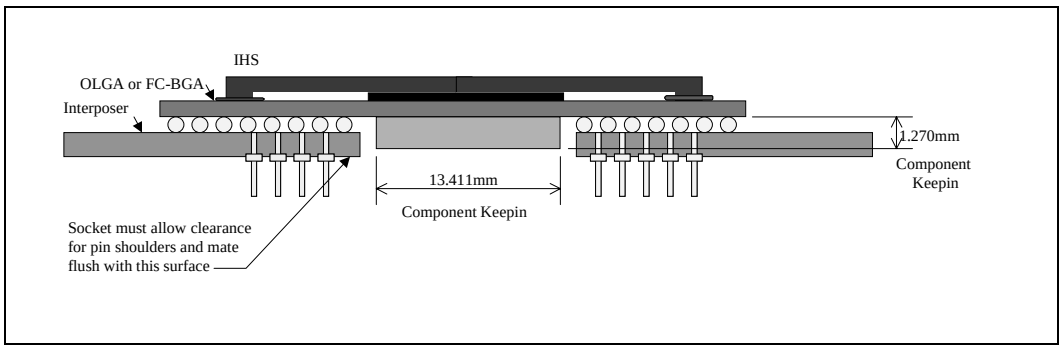
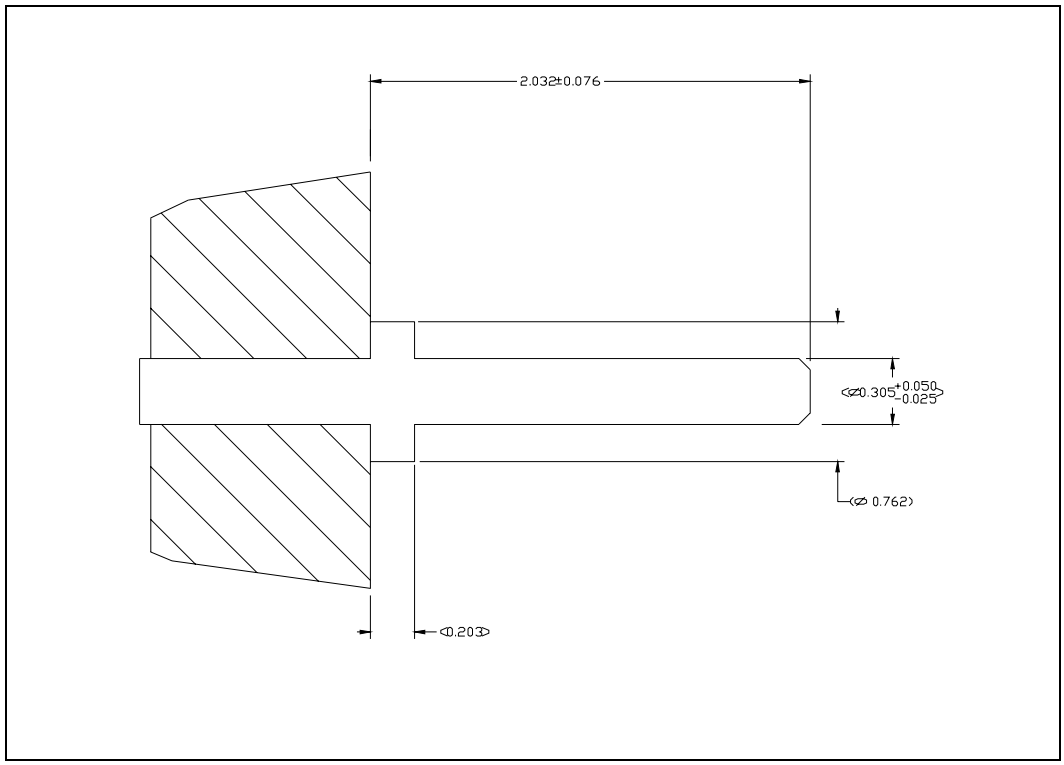


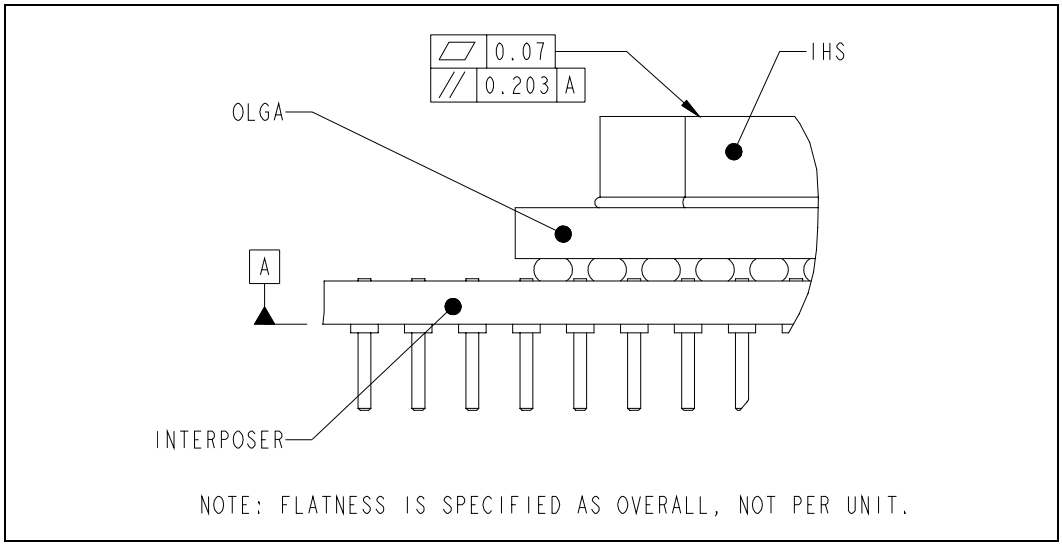
Figure 27. Processor Pin Detail



NOTES:
1. Pin plating consists of 0.2 micrometers Au over 2.0 micrometer Ni.
2. 0.254 Diametric true position, pin to pin.

Figure 28 details the flatness and tilt specifications for the IHS. Tilt is measured with the reference datum set to the bottom of the processor interposer.

Figure 28. IHS Flatness and Tilt Drawing



4.2 Package Load Specifications

Table 27 provides dynamic and static load specifications for the processor IHS. These mechanical load limits should not be exceeded during heat sink assembly, mechanical stress testing, or standard drop and shipping conditions. The heat sink attach solutions must not induce continuous stress onto the processor with the exception of a uniform load to maintain the heat sink-to-processor thermal interface. It is not recommended to use any portion of the processor interposer as a mechanical reference or load bearing surface for thermal solutions.

Table 27. Package Dynamic and Static Load Specifications

Parameter	Max	Unit	Notes
Static	25	lbf	1, 2, 3
Dynamic	100	lbf	1, 3, 4

NOTES:
1. This specification applies to a uniform compressive load.
2. This is the maximum static force that can be applied by the heatsink and clip to maintain the heatsink and processor interface.
3. These parameters are based on design characterization and not tested.
4. Dynamic loading specifications are defined assuming a maximum duration of 11ms.

4.3 Insertion Specifications

The processor can be inserted and removed 30 times from a 603-pin socket meeting the *603-Pin Socket Design Guidelines* document. Note that this specification is based on design characterization and is not tested.

4.4 Mass Specifications

Table 28 specifies the processors mass. This includes all components which make up the entire processor product.

Table 28. Processor Mass

Processor	Mass (grams)
Intel® Xeon™ processor	23.70

4.5 Processor Materials

The processor is assembled from several components. The basic material properties are described in Table 29.

Table 29. Processor Material Properties

Component	Material	Notes
Integrated Heat Spreader	Nickel plated copper	
OLGA package	BT Resin	
FC-BGA	BT Resin	
Interposer	FR4	
Interposer pins	Gold over nickel	

4.6 Processor Markings

The following section details the processor top-side and bottom-side laser markings. It is provided to aid in the identification of the processor.

Figure 29. Processor Top-Side Markings

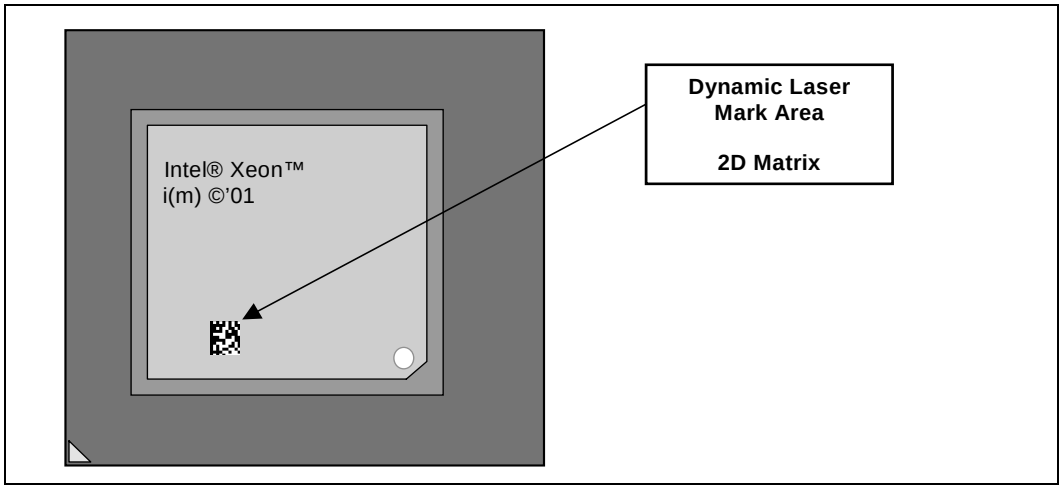
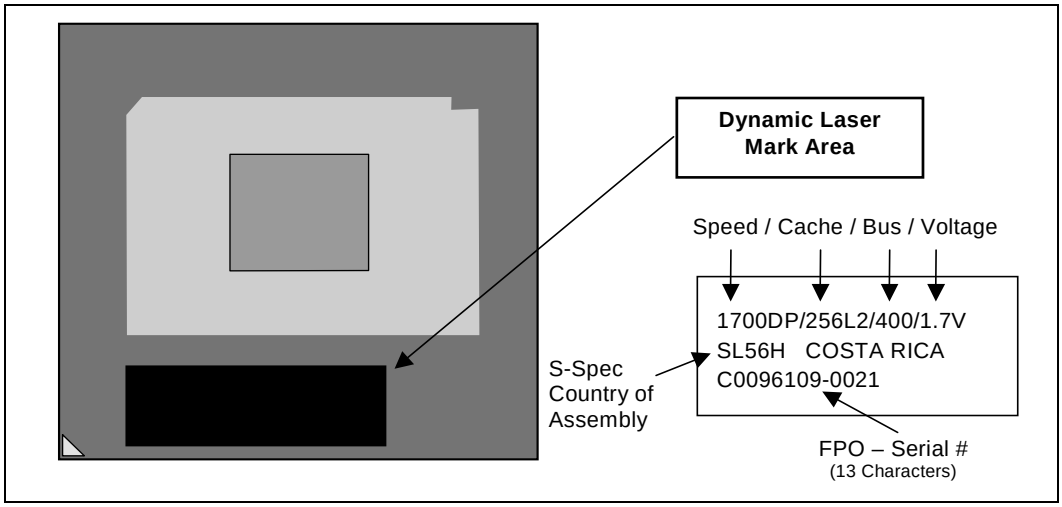


Figure 30. Processor Bottom-Side Markings



NOTES:
1. Approximate character size for laser markings are: height 1.27mm (0.050") , width 0.81 - 1.27mm (0.032 - 0.050").
2. All characters will be in upper case.

4.7 Pin-Out Diagrams

This section provides two views of the processor pin grid. Figure 31 and Figure 32 detail the coordinates of the 603 processor pins.

Figure 31. Processor Pin-out Diagram -- Top View

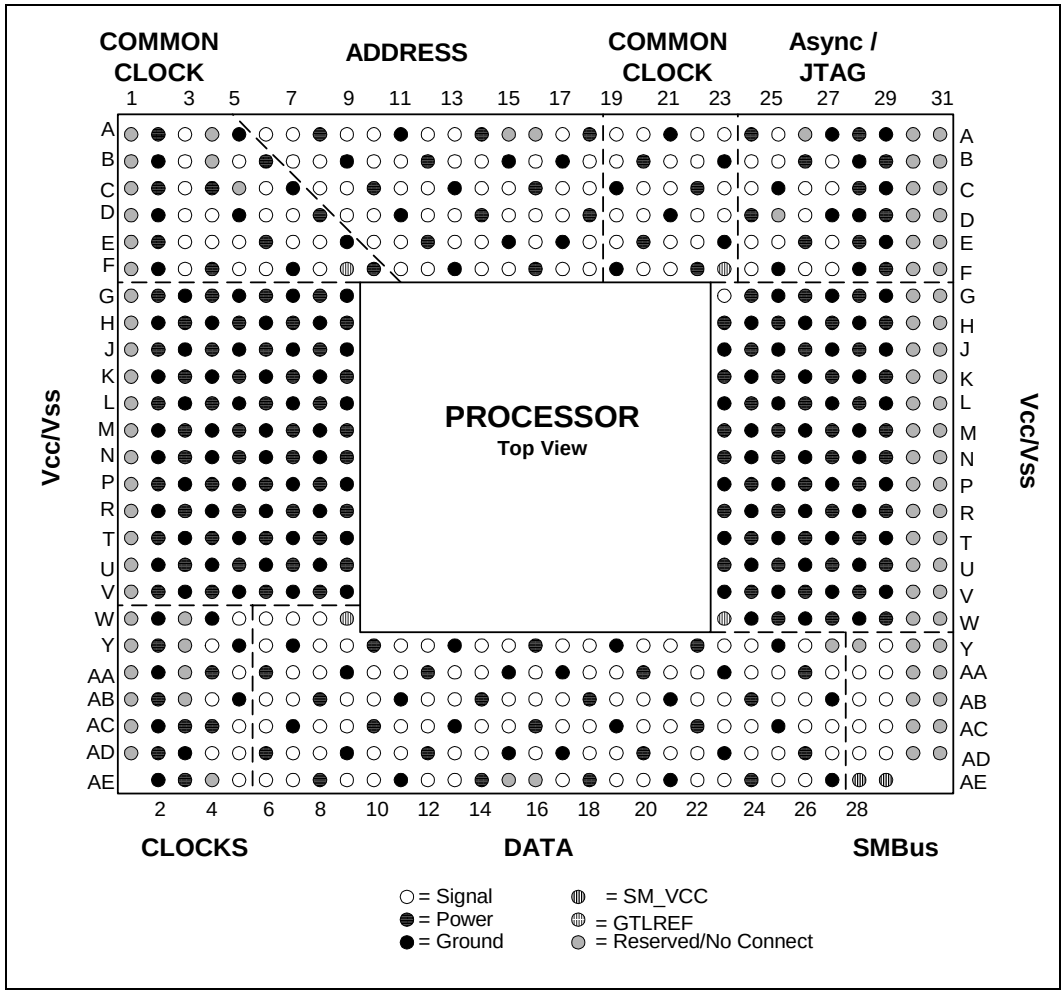
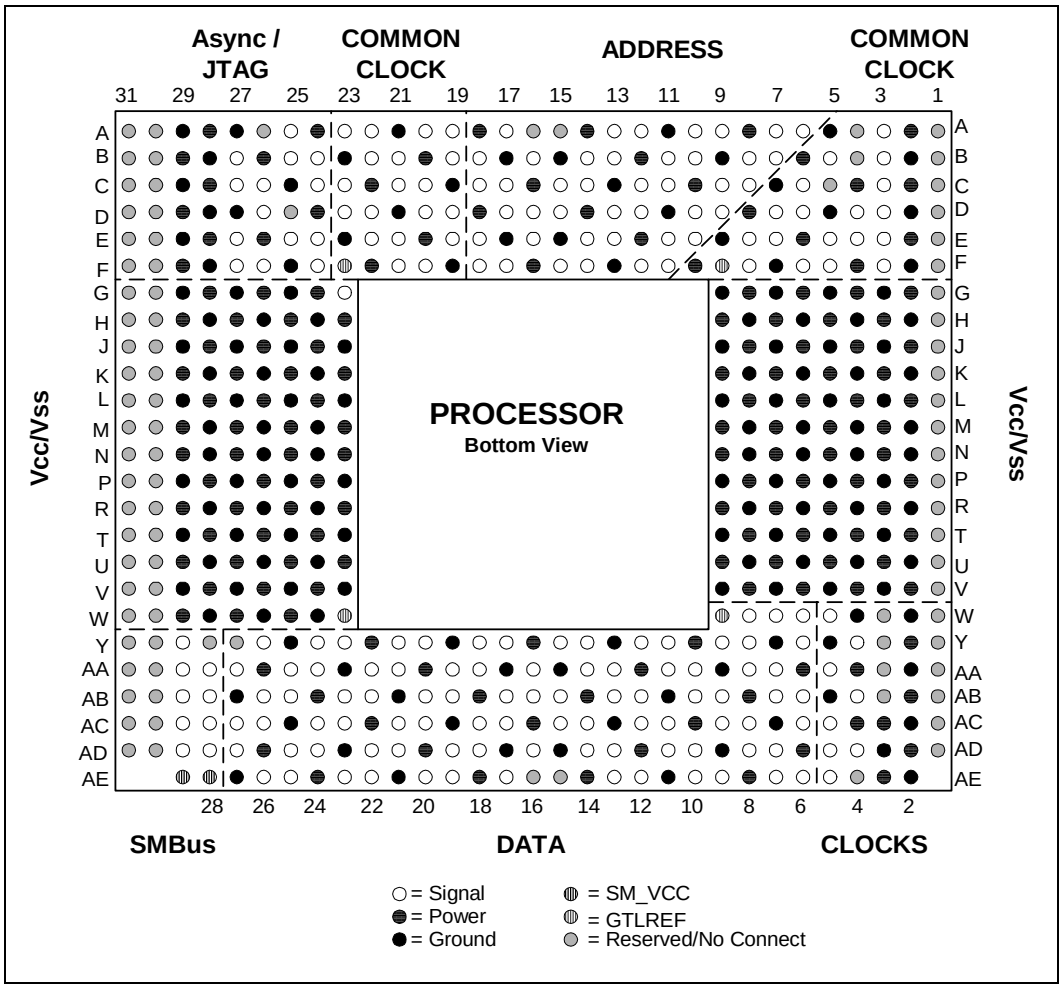


Figure 32. Processor Pin-out Diagram -- Bottom View



5.0 Pin Listing and Signal Definitions

5.1 Processor Pin Assignments

Section 2.7 contains the system bus signal groups in Table 3 for the Intel® Xeon™ processor. This section provides a sorted pin list in Table 30 and Table 31. Table 30 is a listing of all processor pins ordered alphabetically by pin name. Table 31 is a listing of all processor pins ordered by pin number.

Note: Note that "N/C" (no connect) indicates the associated pin is not connected to the processor silicon, however these pins may be utilized by future processors intended for the 603-pin socket. "Reserved" pins must never be utilized by the platform, they are to remain unconnected.

5.1.1 Pin Listing by Pin Name

Table 30. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
A3#	A22	Source Sync	Input/Output
A4#	A20	Source Sync	Input/Output
A5#	B18	Source Sync	Input/Output
A6#	C18	Source Sync	Input/Output
A7#	A19	Source Sync	Input/Output
A8#	C17	Source Sync	Input/Output
A9#	D17	Source Sync	Input/Output
A10#	A13	Source Sync	Input/Output
A11#	B16	Source Sync	Input/Output
A12#	B14	Source Sync	Input/Output
A13#	B13	Source Sync	Input/Output
A14#	A12	Source Sync	Input/Output
A15#	C15	Source Sync	Input/Output
A16#	C14	Source Sync	Input/Output
A17#	D16	Source Sync	Input/Output
A18#	D15	Source Sync	Input/Output
A19#	F15	Source Sync	Input/Output
A20#	A10	Source Sync	Input/Output
A21#	B10	Source Sync	Input/Output
A22#	B11	Source Sync	Input/Output
A23#	C12	Source Sync	Input/Output
A24#	E14	Source Sync	Input/Output
A25#	D13	Source Sync	Input/Output
A26#	A9	Source Sync	Input/Output
A27#	B8	Source Sync	Input/Output

Table 30. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
A28#	E13	Source Sync	Input/Output
A29#	D12	Source Sync	Input/Output
A30#	C11	Source Sync	Input/Output
A31#	B7	Source Sync	Input/Output
A32#	A6	Source Sync	Input/Output
A33#	A7	Source Sync	Input/Output
A34#	C9	Source Sync	Input/Output
A35#	C8	Source Sync	Input/Output
A20M#	F27	Async GTL+	Input
ADS#	D19	Common Clk	Input/Output
ADSTB0#	F17	Source Sync	Input/Output
ADSTB1#	F14	Source Sync	Input/Output
AP0#	E10	Common Clk	Input/Output
AP1#	D9	Common Clk	Input/Output
BCLK0	Y4	Sys Bus Clk	Input
BCLK1	W5	Sys Bus Clk	Input
BINIT#	F11	Common Clk	Input/Output
BNR#	F20	Common Clk	Input/Output
BPM0#	F6	Common Clk	Input/Output
BPM1#	F8	Common Clk	Input/Output
BPM2#	E7	Common Clk	Input/Output
BPM3#	F5	Common Clk	Input/Output
BPM4#	E8	Common Clk	Input/Output
BPM5#	E4	Common Clk	Input/Output
BPRI#	D23	Common Clk	Input

Table 30. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
BR0#	D20	Common Clk	Input/Output
BR1#	F12	Common Clk	Input
BR2# [1]	E11	Reserved	Reserved
BR3# [1]	D10	Reserved	Reserved
COMP0	AD16	Power/Other	Input
COMP1	E16	Power/Other	Input
D0#	Y26	Source Sync	Input/Output
D1#	AA27	Source Sync	Input/Output
D2#	Y24	Source Sync	Input/Output
D3#	AA25	Source Sync	Input/Output
D4#	AD27	Source Sync	Input/Output
D5#	Y23	Source Sync	Input/Output
D6#	AA24	Source Sync	Input/Output
D7#	AB26	Source Sync	Input/Output
D8#	AB25	Source Sync	Input/Output
D9#	AB23	Source Sync	Input/Output
D10#	AA22	Source Sync	Input/Output
D11#	AA21	Source Sync	Input/Output
D12#	AB20	Source Sync	Input/Output
D13#	AB22	Source Sync	Input/Output
D14#	AB19	Source Sync	Input/Output
D15#	AA19	Source Sync	Input/Output
D16#	AE26	Source Sync	Input/Output
D17#	AC26	Source Sync	Input/Output
D18#	AD25	Source Sync	Input/Output
D19#	AE25	Source Sync	Input/Output
D20#	AC24	Source Sync	Input/Output
D21#	AD24	Source Sync	Input/Output
D22#	AE23	Source Sync	Input/Output
D23#	AC23	Source Sync	Input/Output
D24#	AA18	Source Sync	Input/Output
D25#	AC20	Source Sync	Input/Output
D26#	AC21	Source Sync	Input/Output
D27#	AE22	Source Sync	Input/Output
D28#	AE20	Source Sync	Input/Output
D29#	AD21	Source Sync	Input/Output
D30#	AD19	Source Sync	Input/Output

Table 30. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
D31#	AB17	Source Sync	Input/Output
D32#	AB16	Source Sync	Input/Output
D33#	AA16	Source Sync	Input/Output
D34#	AC17	Source Sync	Input/Output
D35#	AE13	Source Sync	Input/Output
D36#	AD18	Source Sync	Input/Output
D37#	AB15	Source Sync	Input/Output
D38#	AD13	Source Sync	Input/Output
D39#	AD14	Source Sync	Input/Output
D40#	AD11	Source Sync	Input/Output
D41#	AC12	Source Sync	Input/Output
D42#	AE10	Source Sync	Input/Output
D43#	AC11	Source Sync	Input/Output
D44#	AE9	Source Sync	Input/Output
D45#	AD10	Source Sync	Input/Output
D46#	AD8	Source Sync	Input/Output
D47#	AC9	Source Sync	Input/Output
D48#	AA13	Source Sync	Input/Output
D49#	AA14	Source Sync	Input/Output
D50#	AC14	Source Sync	Input/Output
D51#	AB12	Source Sync	Input/Output
D52#	AB13	Source Sync	Input/Output
D53#	AA11	Source Sync	Input/Output
D54#	AA10	Source Sync	Input/Output
D55#	AB10	Source Sync	Input/Output
D56#	AC8	Source Sync	Input/Output
D57#	AD7	Source Sync	Input/Output
D58#	AE7	Source Sync	Input/Output
D59#	AC6	Source Sync	Input/Output
D60#	AC5	Source Sync	Input/Output
D61#	AA8	Source Sync	Input/Output
D62#	Y9	Source Sync	Input/Output
D63#	AB6	Source Sync	Input/Output
DBSY#	F18	Common Clk	Input/Output
DEFER#	C23	Common Clk	Input
DBI0#	AC27	Source Sync	Input/Output
DBI1#	AD22	Source Sync	Input/Output

Table 30. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
DBI2#	AE12	Source Sync	Input/Output
DBI3#	AB9	Source Sync	Input/Output
DP0#	AC18	Common Clk	Input/Output
DP1#	AE19	Common Clk	Input/Output
DP2#	AC15	Common Clk	Input/Output
DP3#	AE17	Common Clk	Input/Output
DRDY#	E18	Common Clk	Input/Output
DSTBN0#	Y21	Source Sync	Input/Output
DSTBN1#	Y18	Source Sync	Input/Output
DSTBN2#	Y15	Source Sync	Input/Output
DSTBN3#	Y12	Source Sync	Input/Output
DSTBP0#	Y20	Source Sync	Input/Output
DSTBP1#	Y17	Source Sync	Input/Output
DSTBP2#	Y14	Source Sync	Input/Output
DSTBP3#	Y11	Source Sync	Input/Output
FERR#	E27	Async GTL+	Output
GTLREF	W23	Power/Other	Input
GTLREF	W9	Power/Other	Input
GTLREF	F23	Power/Other	Input
GTLREF	F9	Power/Other	Input
HIT#	E22	Common Clk	Input/Output
HITM#	A23	Common Clk	Input/Output
IERR#	E5	Async GTL+	Output
IGNNE#	C26	Async GTL+	Input
INIT#	D6	Async GTL+	Input
LINT0	B24	Async GTL+	Input
LINT1	G23	Async GTL+	Input
LOCK#	A17	Common Clk	Input/Output
MCERR#	D7	Common Clk	Input/Output
ODTEN	B5	Power/Other	Input
PROCHOT#	B25	Async GTL+	Output
PWRGOOD	AB7	Async GTL+	Input
REQ0#	B19	Source Sync	Input/Output
REQ1#	B21	Source Sync	Input/Output
REQ2#	C21	Source Sync	Input/Output
REQ3#	C20	Source Sync	Input/Output
REQ4#	B22	Source Sync	Input/Output

Table 30. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
Reserved	A1	Reserved	Reserved
Reserved	A4	Reserved	Reserved
Reserved	A15	Reserved	Reserved
Reserved	A16	Reserved	Reserved
Reserved	A26	Reserved	Reserved
N/C	A30[2]	N/C	N/C
N/C	A31[3]	N/C	N/C
Reserved	B1	Reserved	Reserved
N/C	B4[2]	N/C	N/C
N/C	B30[3]	N/C	N/C
N/C	B31[2]	N/C	N/C
N/C	C1[3]	N/C	N/C
Reserved	C5	Reserved	Reserved
N/C	C30[2]	N/C	N/C
N/C	C31[3]	N/C	N/C
N/C	D1[2]	N/C	N/C
Reserved	D25	Reserved	Reserved
N/C	D30[3]	N/C	N/C
N/C	D31[2]	N/C	N/C
N/C	E1[3]	N/C	N/C
N/C	E30[2]	N/C	N/C
N/C	E31[3]	N/C	N/C
N/C	F1[2]	N/C	N/C
N/C	F30[3]	N/C	N/C
N/C	F31[2]	N/C	N/C
N/C	G1[3]	N/C	N/C
N/C	G30[2]	N/C	N/C
N/C	G31[3]	N/C	N/C
N/C	H1[2]	N/C	N/C
N/C	H30[3]	N/C	N/C
N/C	H31[2]	N/C	N/C
N/C	J1[3]	N/C	N/C
N/C	J30[2]	N/C	N/C
N/C	J31[3]	N/C	N/C
N/C	K1[2]	N/C	N/C
N/C	K30[3]	N/C	N/C
N/C	K31[2]	N/C	N/C

Table 30. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
N/C	L1[3]	N/C	N/C
N/C	L30[2]	N/C	N/C
N/C	L31[3]	N/C	N/C
N/C	M1[2]	N/C	N/C
N/C	M30[3]	N/C	N/C
N/C	M31[2]	N/C	N/C
N/C	N1[2]	N/C	N/C
N/C	N30[3]	N/C	N/C
N/C	N31[2]	N/C	N/C
N/C	P1[3]	N/C	N/C
N/C	P30[2]	N/C	N/C
N/C	P31[3]	N/C	N/C
N/C	R1[2]	N/C	N/C
N/C	R30[3]	N/C	N/C
N/C	R31[2]	N/C	N/C
N/C	T1[3]	N/C	N/C
N/C	T30[2]	N/C	N/C
N/C	T31[3]	N/C	N/C
N/C	U1[2]	N/C	N/C
N/C	U30[3]	N/C	N/C
N/C	U31[2]	N/C	N/C
N/C	V1[3]	N/C	N/C
N/C	V30[2]	N/C	N/C
N/C	V31[3]	N/C	N/C
N/C	W1[2]	N/C	N/C
Reserved	W3	Reserved	Reserved
N/C	W30[3]	N/C	N/C
N/C	W31[2]	N/C	N/C
N/C	Y1[3]	N/C	N/C
Reserved	Y3	Reserved	Reserved
Reserved	Y27	Reserved	Reserved
Reserved	Y28	Reserved	Reserved
N/C	Y30[2]	N/C	N/C
N/C	Y31[3]	N/C	N/C
N/C	AA1[2]	N/C	N/C
Reserved	AA3	Reserved	Reserved
N/C	AA30[3]	N/C	N/C

Table 30. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
N/C	AA31[2]	N/C	N/C
N/C	AB1[3]	N/C	N/C
Reserved	AB3	Reserved	Reserved
N/C	AB30[2]	N/C	N/C
N/C	AB31[3]	N/C	N/C
Reserved	AC1	Reserved	Reserved
N/C	AC30[3]	N/C	N/C
N/C	AC31[2]	N/C	N/C
Reserved	AD1	Reserved	Reserved
N/C	AD30[2]	N/C	N/C
N/C	AD31[3]	N/C	N/C
Reserved	AE4	Reserved	Reserved
Reserved	AE15	Reserved	Reserved
Reserved	AE16	Reserved	Reserved
RESET#	Y8	Common Clk	Input
RS0#	E21	Common Clk	Input
RS1#	D22	Common Clk	Input
RS2#	F21	Common Clk	Input
RSP#	C6	Common Clk	Input
SKTOCC#	A3	Power/Other	Output
SLP#	AE6	Async GTL+	Input
SM_ALERT#	AD28	SMBus	Output
SM_CLK	AC28	SMBus	Input
SM_DAT	AC29	SMBus	Input/Output
SM_EP_A0	AA29	SMBus	Input
SM_EP_A1	AB29	SMBus	Input
SM_EP_A2	AB28	SMBus	Input
SM_TS_A0	AA28	SMBus	Input
SM_TS_A1	Y29	SMBus	Input
SM_VCC	AE28	Power/Other	
SM_VCC	AE29	Power/Other	
SM_WP	AD29	SMBus	Input
SMI#	C27	Async GTL+	Input
STPCLK#	D4	Async GTL+	Input
TCK	E24	TAP	Input
TDI	C24	TAP	Input
TDO	E25	TAP	Output

Table 30. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
TESTHI0	W6	Power/Other	Input
TESTHI1	W7	Power/Other	Input
TESTHI2	W8	Power/Other	Input
TESTHI3	Y6	Power/Other	Input
TESTHI4	AA7	Power/Other	Input
TESTHI5	AD5	Power/Other	Input
TESTHI6	AE5	Power/Other	Input
THERMTRIP#	F26	Async GTL+	Output
TMS	A25	TAP	Input
TRDY#	E19	Common Clk	Input
TRST#	F24	TAP	Input
VCC	A2	Power/Other	
VCC	A8	Power/Other	
VCC	A14	Power/Other	
VCC	A18	Power/Other	
VCC	A24	Power/Other	
VCC	A28	Power/Other	
VCC	B6	Power/Other	
VCC	B12	Power/Other	
VCC	B20	Power/Other	
VCC	B26	Power/Other	
VCC	B29	Power/Other	
VCC	C2	Power/Other	
VCC	C4	Power/Other	
VCC	C10	Power/Other	
VCC	C16	Power/Other	
VCC	C22	Power/Other	
VCC	C28	Power/Other	
VCC	D8	Power/Other	
VCC	D14	Power/Other	
VCC	D18	Power/Other	
VCC	D24	Power/Other	
VCC	D29	Power/Other	
VCC	E2	Power/Other	
VCC	E6	Power/Other	
VCC	E12	Power/Other	
VCC	E20	Power/Other	

Table 30. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
VCC	E26	Power/Other	
VCC	E28	Power/Other	
VCC	F4	Power/Other	
VCC	F10	Power/Other	
VCC	F16	Power/Other	
VCC	F22	Power/Other	
VCC	F29	Power/Other	
VCC	G2	Power/Other	
VCC	G4	Power/Other	
VCC	G6	Power/Other	
VCC	G8	Power/Other	
VCC	G24	Power/Other	
VCC	G26	Power/Other	
VCC	G28	Power/Other	
VCC	H3	Power/Other	
VCC	H5	Power/Other	
VCC	H7	Power/Other	
VCC	H9	Power/Other	
VCC	H23	Power/Other	
VCC	H25	Power/Other	
VCC	H27	Power/Other	
VCC	H29	Power/Other	
VCC	J2	Power/Other	
VCC	J4	Power/Other	
VCC	J6	Power/Other	
VCC	J8	Power/Other	
VCC	J24	Power/Other	
VCC	J26	Power/Other	
VCC	J28	Power/Other	
VCC	K3	Power/Other	
VCC	K5	Power/Other	
VCC	K7	Power/Other	
VCC	K9	Power/Other	
VCC	K23	Power/Other	
VCC	K25	Power/Other	
VCC	K27	Power/Other	
VCC	K29	Power/Other	

Table 30. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
VCC	L2	Power/Other	
VCC	L4	Power/Other	
VCC	L6	Power/Other	
VCC	L8	Power/Other	
VCC	L24	Power/Other	
VCC	L26	Power/Other	
VCC	L28	Power/Other	
VCC	M3	Power/Other	
VCC	M5	Power/Other	
VCC	M7	Power/Other	
VCC	M9	Power/Other	
VCC	M23	Power/Other	
VCC	M25	Power/Other	
VCC	M27	Power/Other	
VCC	M29	Power/Other	
VCC	N3	Power/Other	
VCC	N5	Power/Other	
VCC	N7	Power/Other	
VCC	N9	Power/Other	
VCC	N23	Power/Other	
VCC	N25	Power/Other	
VCC	N27	Power/Other	
VCC	N29	Power/Other	
VCC	P2	Power/Other	
VCC	P4	Power/Other	
VCC	P6	Power/Other	
VCC	P8	Power/Other	
VCC	P24	Power/Other	
VCC	P26	Power/Other	
VCC	P28	Power/Other	
VCC	R3	Power/Other	
VCC	R5	Power/Other	
VCC	R7	Power/Other	
VCC	R9	Power/Other	
VCC	R23	Power/Other	
VCC	R25	Power/Other	
VCC	R27	Power/Other	

Table 30. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
VCC	R29	Power/Other	
VCC	T2	Power/Other	
VCC	T4	Power/Other	
VCC	T6	Power/Other	
VCC	T8	Power/Other	
VCC	T24	Power/Other	
VCC	T26	Power/Other	
VCC	T28	Power/Other	
VCC	U3	Power/Other	
VCC	U5	Power/Other	
VCC	U7	Power/Other	
VCC	U9	Power/Other	
VCC	U23	Power/Other	
VCC	U25	Power/Other	
VCC	U27	Power/Other	
VCC	U29	Power/Other	
VCC	V2	Power/Other	
VCC	V4	Power/Other	
VCC	V6	Power/Other	
VCC	V8	Power/Other	
VCC	V24	Power/Other	
VCC	V26	Power/Other	
VCC	V28	Power/Other	
VCC	W25	Power/Other	
VCC	W27	Power/Other	
VCC	W29	Power/Other	
VCC	Y10	Power/Other	
VCC	Y16	Power/Other	
VCC	Y2	Power/Other	
VCC	Y22	Power/Other	
VCC	AA4	Power/Other	
VCC	AA6	Power/Other	
VCC	AA12	Power/Other	
VCC	AA20	Power/Other	
VCC	AA26	Power/Other	
VCC	AB2	Power/Other	
VCC	AB8	Power/Other	

Table 30. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
VCC	AB14	Power/Other	
VCC	AB18	Power/Other	
VCC	AB24	Power/Other	
VCC	AC3	Power/Other	
VCC	AC4	Power/Other	
VCC	AC10	Power/Other	
VCC	AC16	Power/Other	
VCC	AC22	Power/Other	
VCC	AD2	Power/Other	
VCC	AD6	Power/Other	
VCC	AD12	Power/Other	
VCC	AD20	Power/Other	
VCC	AD26	Power/Other	
VCC	AE3	Power/Other	
VCC	AE8	Power/Other	
VCC	AE14	Power/Other	
VCC	AE18	Power/Other	
VCC	AE24	Power/Other	
VCCA	AB4	Power/Other	Input
VCCIOPLL	AD4	Power/Other	Input
VCCSENSE	B27	Power/Other	Output
VID0	F3	Power/Other	Output
VID1	E3	Power/Other	Output
VID2	D3	Power/Other	Output
VID3	C3	Power/Other	Output
VID4	B3	Power/Other	Output
VSS	A5	Power/Other	
VSS	A11	Power/Other	
VSS	A21	Power/Other	
VSS	A27	Power/Other	
VSS	A29	Power/Other	
VSS	B2	Power/Other	
VSS	B9	Power/Other	
VSS	B15	Power/Other	
VSS	B17	Power/Other	
VSS	B23	Power/Other	
VSS	B28	Power/Other	

Table 30. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
VSS	C7	Power/Other	
VSS	C13	Power/Other	
VSS	C19	Power/Other	
VSS	C25	Power/Other	
VSS	C29	Power/Other	
VSS	D2	Power/Other	
VSS	D5	Power/Other	
VSS	D11	Power/Other	
VSS	D21	Power/Other	
VSS	D27	Power/Other	
VSS	D28	Power/Other	
VSS	E9	Power/Other	
VSS	E15	Power/Other	
VSS	E17	Power/Other	
VSS	E23	Power/Other	
VSS	E29	Power/Other	
VSS	F2	Power/Other	
VSS	F7	Power/Other	
VSS	F13	Power/Other	
VSS	F19	Power/Other	
VSS	F25	Power/Other	
VSS	F28	Power/Other	
VSS	G3	Power/Other	
VSS	G5	Power/Other	
VSS	G7	Power/Other	
VSS	G9	Power/Other	
VSS	G25	Power/Other	
VSS	G27	Power/Other	
VSS	G29	Power/Other	
VSS	H2	Power/Other	
VSS	H4	Power/Other	
VSS	H6	Power/Other	
VSS	H8	Power/Other	
VSS	H24	Power/Other	
VSS	H26	Power/Other	
VSS	H28	Power/Other	
VSS	J3	Power/Other	

Table 30. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
VSS	J5	Power/Other	
VSS	J7	Power/Other	
VSS	J9	Power/Other	
VSS	J23	Power/Other	
VSS	J25	Power/Other	
VSS	J27	Power/Other	
VSS	J29	Power/Other	
VSS	K2	Power/Other	
VSS	K4	Power/Other	
VSS	K6	Power/Other	
VSS	K8	Power/Other	
VSS	K24	Power/Other	
VSS	K26	Power/Other	
VSS	K28	Power/Other	
VSS	L3	Power/Other	
VSS	L5	Power/Other	
VSS	L7	Power/Other	
VSS	L9	Power/Other	
VSS	L23	Power/Other	
VSS	L25	Power/Other	
VSS	L27	Power/Other	
VSS	L29	Power/Other	
VSS	M2	Power/Other	
VSS	M4	Power/Other	
VSS	M6	Power/Other	
VSS	M8	Power/Other	
VSS	M24	Power/Other	
VSS	M26	Power/Other	
VSS	M28	Power/Other	
VSS	N2	Power/Other	
VSS	N4	Power/Other	
VSS	N6	Power/Other	
VSS	N8	Power/Other	
VSS	N24	Power/Other	
VSS	N26	Power/Other	
VSS	N28	Power/Other	
VSS	P3	Power/Other	

Table 30. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
VSS	P5	Power/Other	
VSS	P7	Power/Other	
VSS	P9	Power/Other	
VSS	P23	Power/Other	
VSS	P25	Power/Other	
VSS	P27	Power/Other	
VSS	P29	Power/Other	
VSS	R2	Power/Other	
VSS	R4	Power/Other	
VSS	R6	Power/Other	
VSS	R8	Power/Other	
VSS	R24	Power/Other	
VSS	R26	Power/Other	
VSS	R28	Power/Other	
VSS	T3	Power/Other	
VSS	T5	Power/Other	
VSS	T7	Power/Other	
VSS	T9	Power/Other	
VSS	T23	Power/Other	
VSS	T25	Power/Other	
VSS	T27	Power/Other	
VSS	T29	Power/Other	
VSS	U2	Power/Other	
VSS	U4	Power/Other	
VSS	U6	Power/Other	
VSS	U8	Power/Other	
VSS	U24	Power/Other	
VSS	U26	Power/Other	
VSS	U28	Power/Other	
VSS	V3	Power/Other	
VSS	V5	Power/Other	
VSS	V7	Power/Other	
VSS	V9	Power/Other	
VSS	V23	Power/Other	
VSS	V25	Power/Other	
VSS	V27	Power/Other	
VSS	V29	Power/Other	

Table 30. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
VSS	W2	Power/Other	
VSS	W4	Power/Other	
VSS	W24	Power/Other	
VSS	W26	Power/Other	
VSS	W28	Power/Other	
VSS	Y5	Power/Other	
VSS	Y7	Power/Other	
VSS	Y13	Power/Other	
VSS	Y19	Power/Other	
VSS	Y25	Power/Other	
VSS	AA2	Power/Other	
VSS	AA9	Power/Other	
VSS	AA15	Power/Other	
VSS	AA17	Power/Other	
VSS	AA23	Power/Other	
VSS	AB5	Power/Other	
VSS	AB11	Power/Other	
VSS	AB21	Power/Other	
VSS	AB27	Power/Other	
VSS	AC2	Power/Other	
VSS	AC7	Power/Other	

Table 30. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
VSS	AC13	Power/Other	
VSS	AC19	Power/Other	
VSS	AC25	Power/Other	
VSS	AD3	Power/Other	
VSS	AD9	Power/Other	
VSS	AD15	Power/Other	
VSS	AD17	Power/Other	
VSS	AD23	Power/Other	
VSS	AE2	Power/Other	
VSS	AE11	Power/Other	
VSS	AE21	Power/Other	
VSS	AE27	Power/Other	
VSSA	AA5	Power/Other	Input
VSSSENSE	D26	Power/Other	Output

NOTES:
1. These pins are Reserved. However, the platform must terminate these signals to the processor V_{CC}. Refer to the appropriate Platform Design Guidelines for specific implementation details.
2. These pins may be connected to V_{CC} to enable the platform to be forward compatible with future processors.
3. These pins may be connected to V_{SS} to enable the platform to be forward compatible with future processors.

5.1.2 Pin Listing by Pin Number

Table 31 contains a listing of the Intel® Xeon™ processor pins in order by pin number.

Table 31. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
A1	Reserved	Reserved	Reserved
A2	VCC	Power/Other	
A3	SKTOCC#	Power/Other	Output
A4	Reserved	Reserved	Reserved
A5	VtSS	Power/Other	
A6	A32#	Source Sync	Input/Output
A7	A33#	Source Sync	Input/Output
A8	VCC	Power/Other	
A9	A26#	Source Sync	Input/Output
A10	A20#	Source Sync	Input/Output
A11	VSS	Power/Other	
A12	A14#	Source Sync	Input/Output
A13	A10#	Source Sync	Input/Output
A14	VCC	Power/Other	
A15	Reserved	Reserved	Reserved
A16	Reserved	Reserved	Reserved
A17	LOCK#	Common Clk	Input/Output
A18	VCC	Power/Other	
A19	A7#	Source Sync	Input/Output
A20	A4#	Source Sync	Input/Output
A21	VSS	Power/Other	
A22	A3#	Source Sync	Input/Output
A23	HITM#	Common Clk	Input/Output
A24	VCC	Power/Other	
A25	TMS	TAP	Input
A26	Reserved	Reserved	Reserved
A27	VSS	Power/Other	
A28	VCC	Power/Other	
A29	VSS	Power/Other	
A30[2]	N/C	N/C	N/C
A31[3]	N/C	N/C	N/C
B1	Reserved	Reserved	Reserved
B2	VSS	Power/Other	
B3	VID4	Power/Other	Output

Table 31. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
B4[2]	N/C	N/C	N/C
B5	OTDEN	Power/Other	Input
B6	VCC	Power/Other	
B7	A31#	Source Sync	Input/Output
B8	A27#	Source Sync	Input/Output
B9	VSS	Power/Other	
B10	A21#	Source Sync	Input/Output
B11	A22#	Source Sync	Input/Output
B12	VCC	Power/Other	
B13	A13#	Source Sync	Input/Output
B14	A12#	Source Sync	Input/Output
B15	VSS	Power/Other	
B16	A11#	Source Sync	Input/Output
B17	VSS	Power/Other	
B18	A5#	Source Sync	Input/Output
B19	REQ0#	Common Clk	Input/Output
B20	VCC	Power/Other	
B21	REQ1#	Common Clk	Input/Output
B22	REQ4#	Common Clk	Input/Output
B23	VSS	Power/Other	
B24	LINT0	Async GTL+	Input
B25	PROCHOT#	Power/Other	Output
B26	VCC	Power/Other	
B27	VCCSENSE	Power/Other	Output
B28	VSS	Power/Other	
B29	VCC	Power/Other	
B30[3]	N/C	N/C	N/C
B31[2]	N/C	N/C	N/C
C1[3]	N/C	N/C	N/C
C2	VCC	Power/Other	
C3	VID3	Power/Other	Output
C4	VCC	Power/Other	
C5	Reserved	Reserved	Reserved
C6	RSP#	Common Clk	Input

Table 31. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
C7	VSS	Power/Other	
C8	A35#	Source Sync	Input/Output
C9	A34#	Source Sync	Input/Output
C10	VCC	Power/Other	
C11	A30#	Source Sync	Input/Output
C12	A23#	Source Sync	Input/Output
C13	VSS	Power/Other	
C14	A16#	Source Sync	Input/Output
C15	A15#	Source Sync	Input/Output
C16	VCC	Power/Other	
C17	A8#	Source Sync	Input/Output
C18	A6#	Source Sync	Input/Output
C19	VSS	Power/Other	
C20	REQ3#	Common Clk	Input/Output
C21	REQ2#	Common Clk	Input/Output
C22	VCC	Power/Other	
C23	DEFER#	Common Clk	Input
C24	TDI	TAP	Input
C25	VSS	Power/Other	Input
C26	IGNNE#	Async GTL+	Input
C27	SMI#	Async GTL+	Input
C28	VCC	Power/Other	
C29	VSS	Power/Other	
C30[2]	N/C	N/C	N/C
C31[3]	N/C	N/C	N/C
D1[2]	N/C	N/C	N/C
D2	VSS	Power/Other	
D3	VID2	Power/Other	Output
D4	STPCLK#	Async GTL+	Input
D5	VSS	Power/Other	
D6	INIT#	Async GTL+	Input
D7	MCERR#	Common Clk	Input/Output
D8	VCC	Power/Other	
D9	AP1#	Common Clk	Input/Output
D10	BR3# [1]	Common Clk	Reserved
D11	VSS	Power/Other	
D12	A29#	Source Sync	Input/Output

Table 31. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
D13	A25#	Source Sync	Input/Output
D14	VCC	Power/Other	
D15	A18#	Source Sync	Input/Output
D16	A17#	Source Sync	Input/Output
D17	A9#	Source Sync	Input/Output
D18	VCC	Power/Other	
D19	ADS#	Common Clk	Input/Output
D20	BR0#	Common Clk	Input/Output
D21	VSS	Power/Other	
D22	RS1#	Common Clk	Input
D23	BPRI#	Common Clk	Input
D24	VCC	Power/Other	
D25	Reserved	Reserved	Reserved
D26	VSSSENSE	Power/Other	Output
D27	VSS	Power/Other	
D28	VSS	Power/Other	
D29	VCC	Power/Other	
D30[3]	N/C	N/C	N/C
D31[2]	N/C	N/C	N/C
E1[3]	N/C	N/C	N/C
E2	VCC	Power/Other	
E3	VID1	Power/Other	Output
E4	BPM5#	Common Clk	Input/Output
E5	IERR#	Common Clk	Output
E6	VCC	Power/Other	
E7	BPM2#	Common Clk	Input/Output
E8	BPM4#	Common Clk	Input/Output
E9	VSS	Power/Other	
E10	AP0#	Common Clk	Input/Output
E11	BR2# [1]	Common Clk	Reserved
E12	VCC	Power/Other	
E13	A28#	Source Sync	Input/Output
E14	A24#	Source Sync	Input/Output
E15	VSS	Power/Other	
E16	COMP1	Power/Other	Input
E17	VSS	Power/Other	
E18	DRDY#	Common Clk	Input/Output

Table 31. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
E19	TRDY#	Common Clk	Input
E20	VCC	Power/Other	
E21	RS0#	Common Clk	Input
E22	HIT#	Common Clk	Input/Output
E23	VSS	Power/Other	
E24	TCK	TAP	Input
E25	TDO	TAP	Output
E26	VCC	Power/Other	
E27	FERR#	Async GTL+	Output
E28	VCC	Power/Other	
E29	VSS	Power/Other	
E30[2]	N/C	N/C	N/C
E31[3]	N/C	N/C	N/C
F1[2]	N/C	N/C	N/C
F2	VSS	Power/Other	
F3	VID0	Power/Other	Output
F4	VCC	Power/Other	
F5	BPM3#	Common Clk	Input/Output
F6	BPM0#	Common Clk	Input/Output
F7	VSS	Power/Other	
F8	BPM1#	Common Clk	Input/Output
F9	GTLREF	Power/Other	Input
F10	VCC	Power/Other	
F11	BINIT#	Common Clk	Input/Output
F12	BR1#	Common Clk	Input
F13	VSS	Power/Other	
F14	ADSTB1#	Source Sync	Input/Output
F15	A19#	Source Sync	Input/Output
F16	VCC	Power/Other	
F17	ADSTB0#	Source Sync	Input/Output
F18	DBSY#	Common Clk	Input/Output
F19	VSS	Power/Other	
F20	BNR#	Common Clk	Input/Output
F21	RS2#	Common Clk	Input
F22	VCC	Power/Other	
F23	GTLREF	Power/Other	Input
F24	TRST#	TAP	Input

Table 31. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
F25	VSS	Power/Other	
F26	THERMTRIP#	Async GTL+	Output
F27	A20M#	Async GTL+	Input
F28	VSS	Power/Other	
F29	VCC	Power/Other	
F30[3]	N/C	N/C	N/C
F31[2]	N/C	N/C	N/C
G1[3]	N/C	N/C	N/C
G2	VCC	Power/Other	
G3	VSS	Power/Other	
G4	VCC	Power/Other	
G5	VSS	Power/Other	
G6	VCC	Power/Other	
G7	VSS	Power/Other	
G8	VCC	Power/Other	
G9	VSS	Power/Other	
G23	LINT1	Async GTL+	Input
G24	VCC	Power/Other	
G25	VSS	Power/Other	
G26	VCC	Power/Other	
G27	VSS	Power/Other	
G28	VCC	Power/Other	
G29	VSS	Power/Other	
G30[2]	N/C	N/C	N/C
G31[3]	N/C	N/C	N/C
H1[2]	N/C	N/C	N/C
H2	VSS	Power/Other	
H3	VCC	Power/Other	
H4	VSS	Power/Other	
H5	VCC	Power/Other	
H6	VSS	Power/Other	
H7	VCC	Power/Other	
H8	VSS	Power/Other	
H9	VCC	Power/Other	
H23	VCC	Power/Other	
H24	VSS	Power/Other	
H25	VCC	Power/Other	

Table 31. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
H26	VSS	Power/Other	
H27	VCC	Power/Other	
H28	VSS	Power/Other	
H29	VCC	Power/Other	
H30[3]	N/C	N/C	N/C
H31[2]	N/C	N/C	N/C
J1[3]	N/C	N/C	N/C
J2	VCC	Power/Other	
J3	VSS	Power/Other	
J4	VCC	Power/Other	
J5	VSS	Power/Other	
J6	VCC	Power/Other	
J7	VSS	Power/Other	
J8	VCC	Power/Other	
J9	VSS	Power/Other	
J23	VSS	Power/Other	
J24	VCC	Power/Other	
J25	VSS	Power/Other	
J26	VCC	Power/Other	
J27	VSS	Power/Other	
J28	VCC	Power/Other	
J29	VSS	Power/Other	
J30[2]	N/C	N/C	N/C
J31[3]	N/C	N/C	N/C
K1[2]	N/C	N/C	N/C
K2	VSS	Power/Other	
K3	VCC	Power/Other	
K4	VSS	Power/Other	
K5	VCC	Power/Other	
K6	VSS	Power/Other	
K7	VCC	Power/Other	
K8	VSS	Power/Other	
K9	VCC	Power/Other	
K23	VCC	Power/Other	
K24	VSS	Power/Other	
K25	VCC	Power/Other	
K26	VSS	Power/Other	

Table 31. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
K27	VCC	Power/Other	
K28	VSS	Power/Other	
K29	VCC	Power/Other	
K30[3]	N/C	N/C	N/C
K31[2]	N/C	N/C	N/C
L1[3]	N/C	N/C	N/C
L2	VCC	Power/Other	
L3	VSS	Power/Other	
L4	VCC	Power/Other	
L5	VSS	Power/Other	
L6	VCC	Power/Other	
L7	VSS	Power/Other	
L8	VCC	Power/Other	
L9	VSS	Power/Other	
L23	VSS	Power/Other	
L24	VCC	Power/Other	
L25	VSS	Power/Other	
L26	VCC	Power/Other	
L27	VSS	Power/Other	
L28	VCC	Power/Other	
L29	VSS	Power/Other	
L30[2]	N/C	N/C	N/C
L31[3]	N/C	N/C	N/C
M1[2]	N/C	N/C	N/C
M2	VSS	Power/Other	
M3	VCC	Power/Other	
M4	VSS	Power/Other	
M5	VCC	Power/Other	
M6	VSS	Power/Other	
M7	VCC	Power/Other	
M8	VSS	Power/Other	
M9	VCC	Power/Other	
M23	VCC	Power/Other	
M24	VSS	Power/Other	
M25	VCC	Power/Other	
M26	VSS	Power/Other	
M27	VCC	Power/Other	

Table 31. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
M28	VSS	Power/Other	
M29	VCC	Power/Other	
M30[3]	N/C	N/C	N/C
M31[2]	N/C	N/C	N/C
N1[2]	N/C	N/C	N/C
N2	VSS	Power/Other	
N3	VCC	Power/Other	
N4	VSS	Power/Other	
N5	VCC	Power/Other	
N6	VSS	Power/Other	
N7	VCC	Power/Other	
N8	VSS	Power/Other	
N9	VCC	Power/Other	
N23	VCC	Power/Other	
N24	VSS	Power/Other	
N25	VCC	Power/Other	
N26	VSS	Power/Other	
N27	VCC	Power/Other	
N28	VSS	Power/Other	
N29	VCC	Power/Other	
N30[3]	N/C	N/C	N/C
N31[2]	N/C	N/C	N/C
P1[3]	N/C	N/C	N/C
P2	VCC	Power/Other	
P3	VSS	Power/Other	
P4	VCC	Power/Other	
P5	VSS	Power/Other	
P6	VCC	Power/Other	
P7	VSS	Power/Other	
P8	VCC	Power/Other	
P9	VSS	Power/Other	
P23	VSS	Power/Other	
P24	VCC	Power/Other	
P25	VSS	Power/Other	
P26	VCC	Power/Other	
P27	VSS	Power/Other	
P28	VCC	Power/Other	

Table 31. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
P29	VSS	Power/Other	
P30[2]	N/C	N/C	N/C
P31[3]	N/C	N/C	N/C
R1[2]	N/C	N/C	N/C
R2	VSS	Power/Other	
R3	VCC	Power/Other	
R4	VSS	Power/Other	
R5	VCC	Power/Other	
R6	VSS	Power/Other	
R7	VCC	Power/Other	
R8	VSS	Power/Other	
R9	VCC	Power/Other	
R23	VCC	Power/Other	
R24	VSS	Power/Other	
R25	VCC	Power/Other	
R26	VSS	Power/Other	
R27	VCC	Power/Other	
R28	VSS	Power/Other	
R29	VCC	Power/Other	
R30[3]	N/C	N/C	N/C
R31[2]	N/C	N/C	N/C
T1[3]	N/C	N/C	N/C
T2	VCC	Power/Other	
T3	VSS	Power/Other	
T4	VCC	Power/Other	
T5	VSS	Power/Other	
T6	VCC	Power/Other	
T7	VSS	Power/Other	
T8	VCC	Power/Other	
T9	VSS	Power/Other	
T23	VSS	Power/Other	
T24	VCC	Power/Other	
T25	VSS	Power/Other	
T26	VCC	Power/Other	
T27	VSS	Power/Other	
T28	VCC	Power/Other	
T29	VSS	Power/Other	

Table 31. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
T30[2]	N/C	N/C	N/C
T31[3]	N/C	N/C	N/C
U1[2]	N/C	N/C	N/C
U2	VSS	Power/Other	
U3	VCC	Power/Other	
U4	VSS	Power/Other	
U5	VCC	Power/Other	
U6	VSS	Power/Other	
U7	VCC	Power/Other	
U8	VSS	Power/Other	
U9	VCC	Power/Other	
U23	VCC	Power/Other	
U24	VSS	Power/Other	
U25	VCC	Power/Other	
U26	VSS	Power/Other	
U27	VCC	Power/Other	
U28	VSS	Power/Other	
U29	VCC	Power/Other	
U30[3]	N/C	N/C	N/C
U31[2]	N/C	N/C	N/C
V1[3]	N/C	N/C	N/C
V2	VCC	Power/Other	
V3	VSS	Power/Other	
V4	VCC	Power/Other	
V5	VSS	Power/Other	
V6	VCC	Power/Other	
V7	VSS	Power/Other	
V8	VCC	Power/Other	
V9	VSS	Power/Other	
V23	VSS	Power/Other	
V24	VCC	Power/Other	
V25	VSS	Power/Other	
V26	VCC	Power/Other	
V27	VSS	Power/Other	
V28	VCC	Power/Other	
V29	VSS	Power/Other	
V30[2]	N/C	N/C	N/C

Table 31. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
V31[3]	N/C	N/C	N/C
W1[2]	N/C	N/C	N/C
W2	VSS	Power/Other	
W3	Reserved	Reserved	Reserved
W4	VSS	Power/Other	
W5	BCLK1	Sys Bus Clk	Input
W6	TESTHI0	Power/Other	Input
W7	TESTHI1	Power/Other	Input
W8	TESTHI2	Power/Other	Input
W9	GTLREF	Power/Other	Input
W23	GTLREF	Power/Other	Input
W24	VSS	Power/Other	
W25	VCC	Power/Other	
W26	VSS	Power/Other	
W27	VCC	Power/Other	
W28	VSS	Power/Other	
W29	VCC	Power/Other	
W30[3]	N/C	N/C	N/C
W31[2]	N/C	N/C	N/C
Y1[3]	N/C	N/C	N/C
Y2	VCC	Power/Other	
Y3	Reserved	Reserved	Reserved
Y4	BCLK0	Sys Bus Clk	Input
Y5	VSS	Power/Other	
Y6	TESTHI3	Power/Other	Input
Y7	VSS	Power/Other	
Y8	RESET#	Common Clk	Input
Y9	D62#	Source Sync	Input/Output
Y10	VCC	Power/Other	
Y11	DSTBP3#	Source Sync	Input/Output
Y12	DSTBN3#	Source Sync	Input/Output
Y13	VSS	Power/Other	
Y14	DSTBP2#	Source Sync	Input/Output
Y15	DSTBN2#	Source Sync	Input/Output
Y16	VCC	Power/Other	
Y17	DSTBP1#	Source Sync	Input/Output
Y18	DSTBN1#	Source Sync	Input/Output

Table 31. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
Y19	VSS	Power/Other	
Y20	DSTBP0#	Source Sync	Input/Output
Y21	DSTBN0#	Source Sync	Input/Output
Y22	VCC	Power/Other	
Y23	D5#	Source Sync	Input/Output
Y24	D2#	Source Sync	Input/Output
Y25	VSS	Power/Other	
Y26	D0#	Source Sync	Input/Output
Y27	Reserved	Reserved	Reserved
Y28	Reserved	Reserved	Reserved
Y29	SM_TS_A1	SMBus	Input
Y30[2]	N/C	N/C	N/C
Y31[3]	N/C	N/C	N/C
AA1[2]	N/C	N/C	N/C
AA2	VSS	Power/Other	
AA3	Reserved	Reserved	Reserved
AA4	VCC	Power/Other	
AA5	VSSA	Power/Other	Input
AA6	VCC	Power/Other	
AA7	TESTHI4	Power/Other	Input
AA8	D61#	Source Sync	Input/Output
AA9	VSS	Power/Other	
AA10	D54#	Source Sync	Input/Output
AA11	D53#	Source Sync	Input/Output
AA12	VCC	Power/Other	
AA13	D48#	Source Sync	Input/Output
AA14	D49#	Source Sync	Input/Output
AA15	VSS	Power/Other	
AA16	D33#	Source Sync	Input/Output
AA17	VSS	Power/Other	
AA18	D24#	Source Sync	Input/Output
AA19	D15#	Source Sync	Input/Output
AA20	VCC	Power/Other	
AA21	D11#	Source Sync	Input/Output
AA22	D10#	Source Sync	Input/Output
AA23	VSS	Power/Other	
AA24	D6#	Source Sync	Input/Output

Table 31. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
AA25	D3#	Source Sync	Input/Output
AA26	VCC	Power/Other	
AA27	D1#	Source Sync	Input/Output
AA28	SM_TS_A0	SMBus	Input
AA29	SM_EP_A0	SMBus	Input
AA30[3]	N/C	N/C	N/C
AA31[2]	N/C	N/C	N/C
AB1[3]	N/C	N/C	N/C
AB2	VCC	Power/Other	
AB3	Reserved	Reserved	Reserved
AB4	VCCA	Power/Other	Input
AB5	VSS	Power/Other	
AB6	D63#	Source Sync	
AB7	PWRGOOD	Async GTL+	Input
AB8	VCC	Power/Other	
AB9	DBI3#	Source Sync	Input/Output
AB10	D55#	Source Sync	Input/Output
AB11	VSS	Power/Other	
AB12	D51#	Source Sync	Input/Output
AB13	D52#	Source Sync	Input/Output
AB14	VCC	Power/Other	
AB15	D37#	Source Sync	Input/Output
AB16	D32#	Source Sync	Input/Output
AB17	D31#	Source Sync	Input/Output
AB18	VCC	Power/Other	
AB19	D14#	Source Sync	Input/Output
AB20	D12#	Source Sync	Input/Output
AB21	VSS	Power/Other	
AB22	D13#	Source Sync	Input/Output
AB23	D9#	Source Sync	Input/Output
AB24	VCC	Power/Other	
AB25	D8#	Source Sync	Input/Output
AB26	D7#	Source Sync	Input/Output
AB27	VSS	Power/Other	
AB28	SM_EP_A2	SMBus	Input
AB29	SM_EP_A1	SMBus	Input
AB30[2]	N/C	N/C	N/C

Table 31. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
AB31[3]	N/C	N/C	N/C
AC1	Reserved	Reserved	Reserved
AC2	VSS	Power/Other	
AC3	VCC	Power/Other	
AC4	VCC	Power/Other	
AC5	D60#	Source Sync	Input/Output
AC6	D59#	Source Sync	Input/Output
AC7	VSS	Power/Other	
AC8	D56#	Source Sync	Input/Output
AC9	D47#	Source Sync	Input/Output
AC10	VCC	Power/Other	
AC11	D43#	Source Sync	Input/Output
AC12	D41#	Source Sync	Input/Output
AC13	VSS	Power/Other	
AC14	D50#	Source Sync	Input/Output
AC15	DP2#	Common Clk	Input/Output
AC16	VCC	Power/Other	
AC17	D34#	Source Sync	Input/Output
AC18	DP0#	Common Clk	Input/Output
AC19	VSS	Power/Other	
AC20	D25#	Source Sync	Input/Output
AC21	D26#	Source Sync	Input/Output
AC22	VCC	Power/Other	
AC23	D23#	Source Sync	Input/Output
AC24	D20#	Source Sync	Input/Output
AC25	VSS	Power/Other	
AC26	D17#	Source Sync	Input/Output
AC27	DBI0#	Source Sync	Input/Output
AC28	SM_CLK	SMBus	Input
AC29	SM_DAT	SMBus	Output
AC30[3]	N/C	N/C	N/C
AC31[2]	N/C	N/C	N/C
AD1	Reserved	Reserved	Reserved
AD2	VCC	Power/Other	
AD3	VSS	Power/Other	
AD4	VCCIOPLL	Power/Other	Input
AD5	TESTHI5	Power/Other	Input

Table 31. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
AD6	VCC	Power/Other	
AD7	D57#	Source Sync	Input/Output
AD8	D46#	Source Sync	Input/Output
AD9	VSS	Power/Other	
AD10	D45#	Source Sync	Input/Output
AD11	D40#	Source Sync	Input/Output
AD12	VCC	Power/Other	
AD13	D38#	Source Sync	Input/Output
AD14	D39#	Source Sync	Input/Output
AD15	VSS	Power/Other	
AD16	COMP0	Power/Other	Input
AD17	VSS	Power/Other	
AD18	D36#	Source Sync	Input/Output
AD19	D30#	Source Sync	Input/Output
AD20	VCC	Power/Other	
AD21	D29#	Source Sync	Input/Output
AD22	DBI1#	Source Sync	Input/Output
AD23	VSS	Power/Other	
AD24	D21#	Source Sync	Input/Output
AD25	D18#	Source Sync	Input/Output
AD26	VCC	Power/Other	
AD27	D4#	Source Sync	Input/Output
AD28	SM_ALERT#	SMBus	Output
AD29	SM_WP	SMBus	Input
AD30[2]	N/C	N/C	N/C
AD31[3]	N/C	N/C	N/C
AE2	VSS	Power/Other	
AE3	VCC	Power/Other	
AE4	Reserved	Reserved	Reserved
AE5	TESTHI6	Power/Other	Input
AE6	SLP#	Async GTL+	Input
AE7	D58#	Source Sync	Input/Output
AE8	VCC	Power/Other	
AE9	D44#	Source Sync	Input/Output
AE10	D42#	Source Sync	Input/Output
AE11	VSS	Power/Other	
AE12	DBI2#	Source Sync	Input/Output

Table 31. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
AE13	D35#	Source Sync	Input/Output
AE14	VCC	Power/Other	
AE15	Reserved	Reserved	Reserved
AE16	Reserved	Reserved	Reserved
AE17	DP3#	Common Clk	Input/Output
AE18	VCC	Power/Other	
AE19	DP1#	Common Clk	Input/Output
AE20	D28#	Source Sync	Input/Output
AE21	VSS	Power/Other	
AE22	D27#	Source Sync	Input/Output
AE23	D22#	Source Sync	Input/Output
AE24	VCC	Power/Other	

Table 31. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
AE25	D19#	Source Sync	Input/Output
AE26	D16#	Source Sync	Input/Output
AE27	VSS	Power/Other	
AE28	SM_VCC	Power/Other	
AE29	SM_VCC	Power/Other	

NOTES:
1. These pins are Reserved. However, the platform must terminate these signals to the processor V_{CC}. Refer to the appropriate Platform Design Guidelines for specific implementation details.
2. These pins may be connected to V_{CC} to enable the platform to be forward compatible with future processors.
3. These pins may be connected to V_{SS} to enable the platform to be forward compatible with future processors.

5.2 Signal Definitions

Table 30. Signal Definitions (Page 1 of 9)

Name	Type	Description
A[35:3]#	I/O	A[35:3]# (Address) define a 2^{36}-byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the processor system bus. A[35:3]# are protected by parity signals AP[1:0]#. A[35:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. On the active-to-inactive transition of RESET#, the processors sample a subset of the A[35:3]# pins to determine their power-on configuration. See Section 7.1.
A20M#	I	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O write bus transaction This signal is also sampled on the deassertion of RESET# to set the core-to-system bus frequency ratio. See Section 2.4 and Chapter 10.0 for more details.
ADS#	I/O	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction. This signal must connect the appropriate pins on all processor system bus agents.
ADSTB[1:0]#	I/O	Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edge.
AP[1:0]#	I/O	AP[1:0]# (Address Parity) are driven by the request initiator along with ADS#, A[35:3]#, and the transaction type on the REQ[4:0]# pins. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should connect the appropriate pins of all processor system bus agents. The following table defines the coverage model of these signals.

Request Signals	Subphase 1	Subphase 2
A[35:24]#	AP0#	AP1#
A[23:3]#	AP1#	AP0#
REQ[4:0]#	AP1#	AP0#

BCLK[1:0]	I	The differential pair BCLK (Bus Clock) determines the bus frequency. All processor system bus agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of BCLK0 crossing the falling edge of BCLK1.

Table 30. Signal Definitions (Page 2 of 9)

Name	Type	Description
BINIT#	I/O	BINIT# (Bus Initialization) may be observed and driven by all processor system bus agents and if used, must connect the appropriate pins of all such agents. If the BINIT# driver is enabled during power on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future information. If BINIT# observation is enabled during power-on configuration (see Section 7.1) and BINIT# is sampled asserted, symmetric agents reset their bus LOCK# activity and bus request arbitration state machines. The bus agents **do not** reset their IOQ and transaction tracking state machines upon observation of BINIT# assertion. Once the BINIT# assertion has been observed, the bus agents will re-arbitrate for the system bus and attempt completion of their bus queue and IOQ entries. If BINIT# observation is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the error handling architecture of the system.
BNR#	I/O	BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions. Since multiple agents might need to request a bus stall at the same time, BNR# is a wire-OR signal which must connect the appropriate pins of all processor system bus agents. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.
BPM[5:0]#	I/O	BPM[5:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[5:0]# should connect the appropriate pins of all processor system bus agents. BPM4# provides PRDY# (Probe Ready) functionality for the TAP port. PRDY# is a processor output used by debug tools to determine processor debug readiness. BPM5# provides PREQ# (Probe Request) functionality for the TAP port. PREQ# is used by debug tools to request debug operation of the processors. BPM[5:4]# must be bussed to all bus agents. Please refer to the appropriate platform design guidelines for more detailed information. **These signals do not have on-die termination and must be terminated at the end agent.**
BPRI#	I	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor system bus. It must connect the appropriate pins of all processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.

Table 30. Signal Definitions (Page 3 of 9)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>BR0#
BR[1:3]#[1]</td><td>I/O
I</td><td>BR[3:0]# (Bus Request) drive the BREQ[3:0]# signals in the system. The BREQ[1:0]# signals are interconnected in a rotating manner to individual processor pins. BR2# and BR3# must not be utilized in dual processor platform designs. The tables below give the rotating interconnect between the processor and bus signals for dual processor systems.

BR[1:0]# Signal Rotating Interconnect, dual processor system
<table><tr><th>Bus Signal</th><th>Agent 0 Pins</th><th>Agent 1 Pins</th></tr><tr><td>BREQ0#</td><td>BR0#</td><td>BR1#</td></tr><tr><td>BREQ1#</td><td>BR1#</td><td>BR0#</td></tr></table>During power-up configuration, the central agent must assert the BR0# bus signal. All symmetric agents sample their BR[1:0]# pins on active-to-inactive transition of RESET#. The pin on which the agent samples an active level determines its agent ID. All agents then configure their pins to match the appropriate bus signal protocol, as shown below:

BR[1:0]# Signal Agent IDs
<table><tr><th>BR[1:0]# Signals Rotating Interconnect, 2-way system (Intel® Xeon™ processors only)</th><th>Agent ID</th></tr><tr><td>BR0#</td><td>0</td></tr><tr><td>BR1#</td><td>1</td></tr></table>During power-on configuration, the central agent must assert the BREQ0# bus signal. All symmetric agents sample their BR[1:0]# pins on the active-to-inactive transition of RESET#. The pin which the agent samples asserted determines it’s agent ID.
These signals do not have on-die termination and must be terminated at the end agent.</td></tr>
<tr><td>COMP[1:0]</td><td>I</td><td>COMP[1:0] must be terminated to V_{SS} on the system board using precision resistors. These inputs configure the AGTL+ drivers of the processor. Refer to the appropriate platform design guidelines and Table 11 for implementation details.</td></tr>
<tr><td>D[63:0]#</td><td>I/O</td><td>D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor system bus agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer.
D[63:0]# are quad-pumped signals, and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to strobes and DBI#.

<table><tr><th>Data Group</th><th>DSTBN/ DSTBP</th><th>DBI#</th></tr><tr><td>D[15:0]#</td><td>0</td><td>0</td></tr><tr><td>D[31:16]#</td><td>1</td><td>1</td></tr><tr><td>D[47:32]#</td><td>2</td><td>2</td></tr><tr><td>D[63:48]#</td><td>3</td><td>3</td></tr></table>Furthermore, the DBI# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DBI# signal. When the DBI# signal is active, the corresponding data group is inverted and therefore sampled active high.</td></tr>
</table>

Table 30. Signal Definitions (Page 4 of 9)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>DBI[3:0]#</td><td>I/O</td><td>DBI[3:0]# are source synchronous and indicate the polarity of the D[63:0]# signals. The DBI[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within a 16-bit group, change logic level in the next cycle.

DBI[3:0] Assignment To Data Bus
<table><tr><th>Bus Signal</th><th>Data Bus Signals</th></tr><tr><td>DBI0#</td><td>D[15:0]#</td></tr><tr><td>DBI1#</td><td>D[31:16]#</td></tr><tr><td>DBI2#</td><td>D[47:32]#</td></tr><tr><td>DBI3#</td><td>D[63:48]#</td></tr></table></td></tr>
<tr><td>DBSY#</td><td>I/O</td><td>DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on all processor system bus agents.</td></tr>
<tr><td>DEFER#</td><td>I</td><td>DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or I/O agent. This signal must connect the appropriate pins of all processor system bus agents.</td></tr>
<tr><td>DP[3:0]#</td><td>I/O</td><td>DP[3:0]# (Data Parity) provide parity protection for the D[63:0]# signals. They are driven by the agent responsible for driving D[63:0]#, and must connect the appropriate pins of all processor system bus agents.</td></tr>
<tr><td>DRDY#</td><td>I/O</td><td>DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of all processor system bus agents.</td></tr>
<tr><td>DSTBN[3:0]#</td><td>I/O</td><td>Data strobe used to latch in D[63:0]#. Must connect to the appropriate pins of all processor bus agents.</td></tr>
<tr><td>DSTBP[3:0]#</td><td>I/O</td><td>Data strobe used to latch in D[63:0]#. Must connect to the appropriate pins of all processor bus agents.</td></tr>
<tr><td>FERR#</td><td>O</td><td>FERR# (Floating-point Error) is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting.</td></tr>
<tr><td>GTLREF</td><td>I</td><td>GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3Vcc. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or a logical 1.</td></tr>
<tr><td>HIT#
HITM#</td><td>I/O
I/O</td><td>HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Any system bus agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
Since multiple agents may deliver snoop results at the same time, HIT# and HITM# are wire-OR signals which must connect the appropriate pins of all processor system bus agents. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, HIT# and HITM# are activated on specific clock edges and sampled on specific clock edges.</td></tr>
</table>

Table 30. Signal Definitions (Page 5 of 9)

Name	Type	Description
IERR#	O	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#. **This signal does not have on-die termination and must be terminated at the end agent.**
IGNNE#	I	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O write bus transaction. This signal is also sampled on the deassertion of RESET# to set the core-to-system bus frequency ratio. See Section 2.4 and Chapter 10.0 for more details.
INIT#	I	INIT# (Initialization), when asserted, resets integer registers inside all processors without affecting their internal caches or floating-point registers. Each processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all processor system bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).
LINT[1:0]	I	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all system bus agents. When the APIC functionality is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration. These signals are also sampled on the deassertion of RESET# to set the core-to-system bus frequency ratio. See Section 2.4 and Chapter 10.0 for more details.
LOCK#	I/O	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.

Table 30. Signal Definitions (Page 6 of 9)

Name	Type	Description
MCERR#	I/O	MCERR# (Machine Check Error) is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all processor system bus agents. MCERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options: • Enabled or disabled. • Asserted, if configured, for internal errors along with IERR#. • Asserted, if configured, by the request initiator of a bus transaction after it observes an error. • Asserted by any bus agent when it observes an error in a bus transaction. For more details regarding machine check architecture, refer to the *IA-32 Software Developer's Manual, Volume 3: System Programming Guide*. Since multiple agents may drive this signal at the same time, MCERR# is a wire-OR signal which must connect the appropriate pins of all processor system bus agents. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, MCERR# is activated on specific clock edges and sampled on specific clock edges.
ODTEN	I	ODTEN (On-die termination enable) should be connected to V_{CC} to enable on-die termination for end bus agents. For middle bus agents, pull this signal down via a resistor to ground to disable on-die termination. Whenever ODTEN is high, on-die termination will be active, regardless of other states of the bus.
PROCHOT#	O	PROCHOT# (processor hot) indicates that the processor Thermal Control Circuit (TCC) has been activated. Under most conditions, PROCHOT# will go active when the processor's thermal sensor detects that the processor has reached its maximum safe operating temperature. See Section 7.3 for more details.
PWRGOOD	I	PWRGOOD (Power Good) is an input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. "Clean" implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. Figure 10 illustrates the relationship of PWRGOOD to the RESET# signal. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. It must also meet the minimum pulse width specification in Table 14, and be followed by a 1 ms RESET# pulse. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
REQ[4:0]#	I/O	REQ[4:0]# (Request Command) must connect the appropriate pins of all processor system bus agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[1:0]#. Refer to the AP[1:0]# signal description for details on parity checking of these signals.
RESET#	I	Asserting the RESET# signal resets all processors to known states and invalidates their internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least one millisecond after VCC and BCLK have reached their proper specifications. On observing active RESET#, all system bus agents will deassert their outputs within two clocks. RESET# must not be kept asserted for more than 10ms. A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the Section 7.1. **This signal does not have on-die termination and must be terminated at the end agent.**

Table 30. Signal Definitions (Page 7 of 9)

Name	Type	Description
RS[2:0]#	I	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor system bus agents.
RSP#	I	RSP# (Response Parity) is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect to the appropriate pins of all processor system bus agents. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. While RS[2:0]# = 000, RSP# is also high, since this indicates it is not being driven by any agent guaranteeing correct parity.
SKTOCC#	O	SKTOCC# (Socket occupied) will be pulled to ground by the processor to indicate that the processor is present.
SLP#	I	SLP# (Sleep), when asserted in Stop-Grant state, causes processors to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal or deassertion of SLP#. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units.
SM_ALERT#	O	SM_ALERT# is an asynchronous interrupt line associated with the SMBus Thermal Sensor device. It is an open-drain output and the processor includes a 10kΩ pull-up resistor to SM_V_{CC} for this signal. For more information on the usage of the SM_ALERT# pin, see Section 7.4.5.
SM_CLK	I/O	The SM_CLK (SMBus Clock) signal is an input clock to the system management logic which is required for operation of the system management features of the processor. This clock is driven by the SMBus controller and is asynchronous to other clocks in the processor.The processor includes a 10kΩ pull-up resistor to SM_V_{CC} for this signal.
SM_DAT	I/O	The SM_DAT (SMBus Data) signal is the data signal for the SMBus. This signal provides the single-bit mechanism for transferring data between SMBus devices.The processor includes a 10kΩ pull-up resistor to SM_V_{CC} for this signal.
SM_EP_A[2:0]	I	The SM_EP_A (EEPROM Select Address) pins are decoded on the SMBus in conjunction with the upper address bits in order to maintain unique addresses on the SMBus in a system with multiple processors. To set an SM_EP_A line high, a pull-up resistor should be used that is no larger than 1 kΩ. The processor includes a 10kΩ pull-down resistor to V_{SS} for each of these signals. For more information on the usage of these pins, see Section 7.4.8.
SM_TS_A[1:0]	I	The SM_TS_A (Thermal Sensor Select Address) pins are decoded on the SMBus in conjunction with the upper address bits in order to maintain unique addresses on the SMBus in a system with multiple processors. The device's addressing, as implemented, includes a Hi-Z state for both address pins. The use of the Hi-Z state is achieved by leaving the input floating (unconnected). For more information on the usage of these pins, see Section 7.4.8.
SM_VCC	I	Provides power to the SMBus components on the processor. In addition, this supply must be present for future processors utilizing the 603-pin socket.
SM_WP	I	WP (Write Protect) can be used to write protect the Scratch EEPROM. The Scratch EEPROM is write-protected when this input is pulled high to SM_V_{CC}.The processor includes a 10kΩ pull-down resistor to V_{SS} for this signal.

Table 30. Signal Definitions (Page 8 of 9)

Name	Type	Description
SMI#	I	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, processors save the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tri-state its outputs.
STPCLK#	I	STPCLK# (Stop Clock), when asserted, causes processors to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the system bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	I	TCK (Test Clock) provides the clock input for the processor Test Access Port).
TDI	I	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	O	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TESTHI[6:0]	I	For each processor, all TESTHI inputs must be connected to V_{CC} through a 1k - 10kΩ resistor for proper processor operation. TESTHI[3:0] and TESTHI[6:5] may all be tied together at each processor and pulled up to V_{CC} with a single 1 kΩ – 4.7 kΩ resistor if desired. However, boundary scan test will not function if these pins are tied together. TESTHI4 must always be pulled up independently from the other TESTHI pins. The TESTHI pins must not be connected between system bus agents.
THERMTRIP#	O	Activation of THERMTRIP# (Thermal Trip) indicates the processor junction temperature has reached a level beyond which permanent silicon damage may occur. Measurement of the temperature is accomplished through an internal thermals sensor which is configured to trip at approximately 135°C. To properly protect the processor, power must be removed upon THERMTRIP# becoming active. See Figure 13 and Table 15 for the appropriate power down sequence and timing requirement. In parallel, the processor will attempt to reduce its temperature by shutting off internal clocks and stopping all program execution. Once activated, THERMTRIP# remains latched and the processor will be stopped until RESET# is asserted. A RESET# pulse will reset the processor and execution will begin at the boot vector. If the temperature has not dropped below the trip level, the processor will assert THERMTRIP# and return to the shutdown state. The processor releases THERMTRIP# when RESET# is activated even if the processor is still too hot.
TMS	I	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	I	TRDY# (Target Ready) is asserted by the target, indicating it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all bus agents.
TRST#	I	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.
V_{CCA}	I	VCCA provides isolated power for the analog portion of the internal PLL's. Use a discrete RLC filter to provide clean power. Use the filter defined in Section 2.4.1 to provide clean power to the PLL. The tolerance and total ESR for the filter is important. Refer to the appropriate platform design guidelines for complete implementation details.
$V_{CCIOPLL}$	I	$V_{CCIOPLL}$ provides isolated power for digital portion of the internal PLL's. Follow the guidelines for V_{CCA} (Section 2.4.1), and refer to the appropriate platform design guidelines for complete implementation details.

Table 30. Signal Definitions (Page 9 of 9)

Name	Type	Description
$V_{CCSENSE}$ $V_{SSSENSE}$	O	The $V_{CCSENSE}$ and $V_{SSSENSE}$ pins are the points for which processor minimum and maximum voltage requirements are specified. Uni processor designs may utilize these pins for voltage sensing for the processor's voltage regulator. However, multiprocessor designs must not connect these pins to sense logic, rather utilize them for power delivery validation.
VID[4:0]	O	VID[4:0] (Voltage ID) pins can be used to support automatic selection of power supply voltages (V_{CC}). These pins are not signals, but are either an open circuit or a short circuit to V_{SS} on the processor. The combination of opens and shorts defines the voltage required by the processor. The VID pins are needed to cleanly support processor voltage specification variations. See Table 2 for definitions of these pins. The power supply must supply the voltage that is requested by these pins, or disable itself.
V_{SSA}	I	V_{SSA} provides an isolated, **internal** ground for internal PLL's. Do not connect directly to ground. This pin is to be connected to V_{CCA} and $V_{CCIOPLL}$ through a discrete filter circuit.

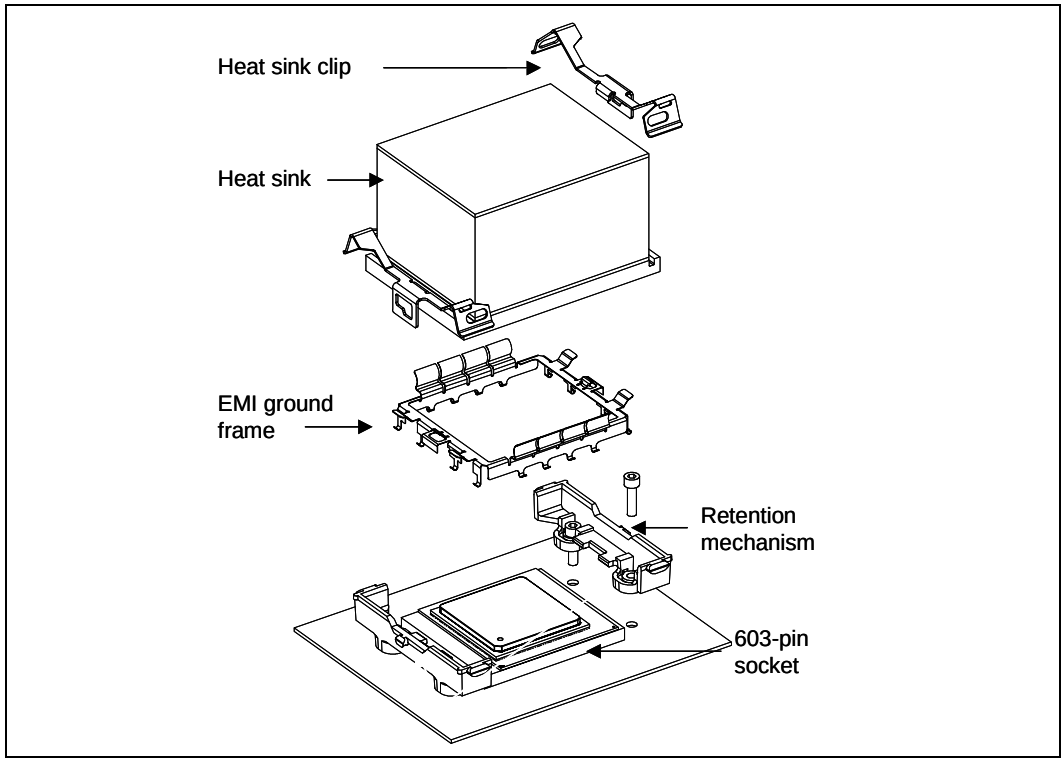
NOTES:
1. Intel™ Xeon® processors only support BR0# and BR1# signals. BR2# and BR3# must be terminated to processor V_{CC}.

6.0 Thermal Specifications

This chapter provides the data used for designing a thermal solution for Intel® Xeon™ processors. However, for the correct thermal measuring processes, refer to the *Intel® Xeon™ Processor Family Thermal Design Guidelines* . The Intel Xeon processor utilizes a integrated heat spreader (IHS) for heatsink attachment which is intended to provide for multiple types of thermal solutions, thus thermal specifications are with reference to T_{CASE} (the IHS). See Figure 30 for an exploded view of the processor package and thermal solution assembly.

Note: The processor is either shipped alone or with a heatsink (boxed processor only). All other components shown in Figure 30 must be purchased separately.

Figure 30. Processor with Thermal and Mechanical Components - Exploded View



Note: This is a graphical representation. For specifications, see each component's respective documentation listed in Section 1.3.

6.1 Thermal Specifications

Table 31 specifies the thermal design power dissipation envelope for the processor. The processor power listed in Table 31 is described in terms of thermal design power. Analysis indicates that real applications are unlikely to cause the processor to consume the maximum possible power consumption. Intel recommends that system thermal designs utilize the Thermal Design Power indicated in Table 31. Thermal Design Power recommendations have been chosen through characterization of server and workstation applications on the processor.

The Thermal Monitor feature is intended to protect the processor from over heating on any high power code that exceeds the recommendations in this table. For more details on the Thermal Monitor feature, refer to Section 7.3. In all cases, the Thermal Monitor feature must be enabled for the processor to be operating within specification. Table 31 also lists the maximum and minimum processor temperature specifications for T_{CASE}. A thermal solution should be designed to ensure the temperature of the processor never exceeds these specifications.

Table 31. Processor Thermal Design Power

Core Frequency[1]	Thermal Design Power[2] (W)	Minimum TCASE (°C)	Maximum TCASE (°C)
1.40 GHz	56.0	5	69
1.50 GHz	59.2	5	70
1.70 GHz	65.8	5	73
2 GHz	77.5	5	78

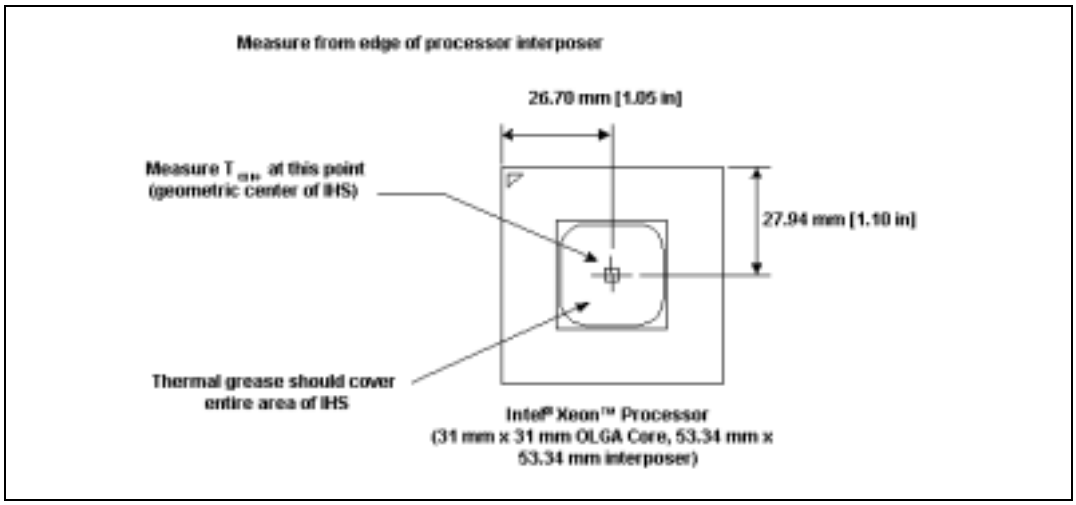
NOTES:
1. These values are specified at $V_{CC\_MID} = (V_{CC\_MAX} + V_{CC\_MIN})/2$ for all processor frequencies and cache sizes. Systems must be designed to ensure that the processor not be subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds $V_{CC\_MID} + 0.200 * (1\text{-}I_{CC}/I_{CC\_MAX})$[V]. Moreover, V_{CC} should never exceed V_{CC_MAX} (VID). Failure to adhere to this specification can shorten the processor lifetime.
2. Intel recommends that thermal solutions be designed utilizing the Thermal Design Power values. Refer to the *Intel® Xeon™ Processor Family Thermal Design Guidelines* for more details.

6.2 Thermal Analysis

6.2.1 Processor Case Temperature Measurement

The maximum and minimum case temperature (T_{CASE}) for processors are specified above. These temperature specifications are meant to ensure correct and reliable operation of the processor. Figure 31 illustrates the thermal measurement point for T_{CASE}. This point is at the center of the integrated heat spreader (IHS).

Figure 31. Thermocouple Placement for Case Temperature (T_{CASE}) Measurement



NOTE: This drawing is not to scale, it is for reference only. For specific processor mechanical specifications, refer to Chapter 4.0.

7.0 Features

7.1 Power-On Configuration Options

The Intel® Xeon™ processor processor includes several configuration options which are determined by hardware.

Intel Xeon processors sample their hardware configuration at reset, on the active-to-inactive transition of RESET#. The sampled information configures the processor for subsequent operation. These configuration options cannot be changed except by another reset. All resets reconfigure the processor(s); they do not distinguish between a “software” reset and a “power-on” reset.

Table 32. Power-On Configuration Option Pins

Configuration Option	Pin [1]	Notes
Output tri-state	SMI#	
Execute BIST (Built-In Self Test)	INIT#	
In Order Queue de-pipelining (set IOQ depth to 1)	A7#	
Disable MCERR# observation	A9#	
Disable BINIT# observation	A10#	
Disable bus parking	A15#	
Bus frequency-to-core ratio	LINT[1:0], IGNNE#, A20M#	2
Symmetric agent arbitration ID	BR[1:0]#	3

NOTES:
1. Asserting this signal during RESET# will select the corresponding option.
2. These signals are used for bus frequency-to-core-ratio determination. See Table 1 for the supported settings. The processor ignores requests for ratios higher than the maximum ratio it supports. For example, a 1.40 GHz processor will recognize ratios of 1/14 and lower. For more details, see Chapter 10.0.
3. Intel® Xeon™ processors only utilize the BR0# and BR1# signals.

7.2 Clock Control and Low Power States

The processor allows the use of AutoHALT, Stop-Grant, and Sleep states to reduce power consumption by stopping the clock to internal sections of the processor, depending on each particular state. See Figure 32 for a visual representation of the processor low power states.

Due to the inability of processors to recognize bus transactions during the Sleep state, multiprocessor systems are not allowed to simultaneously have one processor in the Sleep state and the other processor in Normal or Stop-Grant state.

7.2.1 Normal State—State 1

This is the normal operating state for the processor.

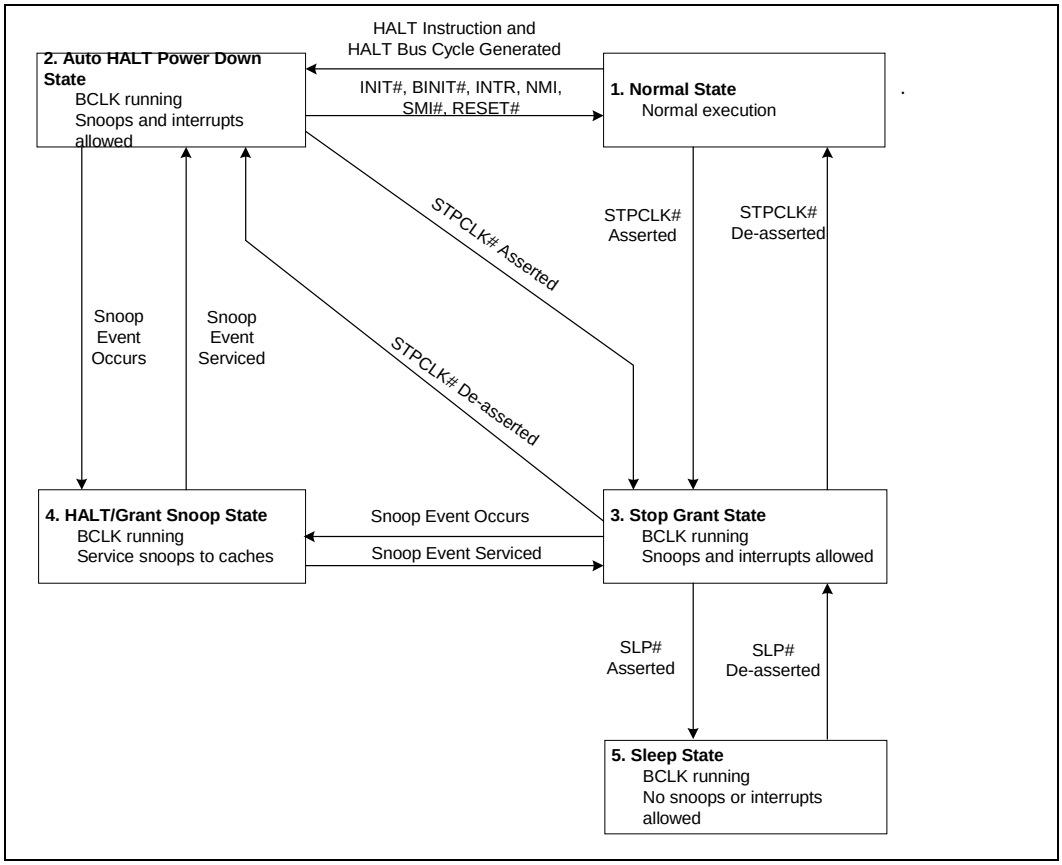
7.2.2 AutoHALT Powerdown State—State 2

AutoHALT is a low power state entered when the processor executes the HALT instruction. The processor will transition to the Normal state upon the occurrence of SMI#, BINIT#, INIT#, LINT[1:0] (NMI, INTR), or an interrupt delivered over the system bus. RESET# will cause the processor to immediately initialize itself.

The return from a System Management Interrupt (SMI) handler can be to either Normal Mode or the AutoHALT Power Down state. See the *Intel Architecture Software Developer's Manual, Volume III: System Programmer's Guide* for more information.

The system can generate a STPCLK# while the processor is in the AutoHALT Power Down state. When the system deasserts the STPCLK# interrupt, the processor will return execution to the HALT state.

Figure 32. Stop Clock State Machine



7.2.3 Stop-Grant State—State 3

When the STPCLK# pin is asserted, the Stop-Grant state of the processor is entered 20 bus clocks after the response phase of the processor-issued Stop Grant Acknowledge special bus cycle. Once the STPCLK# pin has been asserted, it may only be deasserted once the processor is in the Stop Grant state.

Since the AGTL+ signal pins receive power from the system bus, these pins should not be driven (allowing the level to return to V_{CC}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the system bus should be driven to the inactive state.

BINIT# will be recognized while the processor is in Stop-Grant state. If STPCLK# is still asserted at the completion of the BINIT# bus initialization, the processor will remain in Stop-Grant mode. If the STPCLK# is not asserted at the completion of the BINIT# bus initialization, the processor will return to Normal state.

RESET# will cause the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. A transition back to the Normal state will occur with the deassertion of the STPCLK# signal. When re-entering the Stop-Grant state from the sleep state, STPCLK# should only be deasserted one or more bus clocks after the deassertion of SLP#.

A transition to the HALT/Grant Snoop state will occur when the processor detects a snoop on the system bus (see Section 7.2.4). A transition to the Sleep state (see Section 7.2.5) will occur with the assertion of the SLP# signal.

While in the Stop-Grant state, SMI#, INIT#, BINIT# and LINT[1:0] will be latched by the processor, and only serviced when the processor returns to the Normal state. Only one occurrence of each event will be recognized upon return to the Normal state.

7.2.4 HALT/Grant Snoop State—State 4

The processor will respond to snoop transactions on the system bus while in Stop-Grant state or in AutoHALT Power Down state. During a snoop transaction, the processor enters the HALT/Grant Snoop state. The processor will stay in this state until the snoop on the system bus has been serviced (whether by the processor or another agent on the system bus). After the snoop is serviced, the processor will return to the Stop-Grant state or AutoHALT Power Down state, as appropriate.

7.2.5 Sleep State—State 5

The Sleep state is a very low power state in which each processor maintains its context, maintains the phase-locked loop (PLL), and has stopped most of internal clocks. The Sleep state can only be entered from Stop-Grant state. Once in the Stop-Grant state, the SLP# pin can be asserted, causing the processor to enter the Sleep state. The SLP# pin is not recognized in the Normal or AutoHALT states.

Snoop events that occur while in Sleep state or during a transition into or out of Sleep state will cause unpredictable behavior.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP# or RESET#) are allowed on the system bus while the processor is in Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, then the processor will reset itself, ignoring the transition through Stop-Grant state. If RESET# is driven active while the processor is in the Sleep state, the SLP# and STPCLK# signals should be deasserted immediately after RESET# is asserted to ensure the processor correctly executes the reset sequence.

Once in the Sleep state, the SLP# pin can be deasserted if another asynchronous system bus event occurs. The SLP# pin should only be asserted when the processor is in the Stop-Grant state. SLP# assertions while the processors are not in the Stop-Grant state is out of specification and may result in illegal operation.

7.2.6 Bus Response During Low Power States

While in AutoHALT Power Down and Stop-Grant states, the processor will process a system bus snoop.

When the processor is in the Sleep state, it will not respond to interrupts or snoop transactions.

7.3 Thermal Monitor

Thermal Monitor is a feature found in the Intel Xeon processor which allows system designers to develop lower cost thermal solutions, without compromising system integrity or reliability. By using a factory-tuned, precision on-die temperature sensor, and a fast acting thermal control circuit (TCC), the processor, without the aid of any additional software or hardware, can control the processors die temperature within factory specifications under typical real-world operating conditions. Thermal Monitor thus allows the processor and system thermal solutions to be designed much closer to the power envelopes of real applications, instead of being designed to the much higher maximum processor power envelopes.

Thermal Monitor controls the processor temperature by modulating (starting and stopping) the internal processor core clocks. The processor clocks are modulated when the thermal control circuit (TCC) is activated. Thermal Monitor uses two modes to activate the TCC. Automatic mode and On-Demand mode. **Automatic mode is required for the processor to operate within specifications and must first be enabled via BIOS**. Once automatic mode is enabled, the TCC will activate only when the internal die temperature is very near the temperature limits of the processor. When the TCC is enabled, and a high temperature situation exists (i.e. TCC is active), the clocks will be modulated by alternately turning the clocks off and on at a 50% duty cycle. Clocks will not be off or on more than 3.0 µs when the TCC is active. Cycle times are processor speed dependent and will decrease as processor core frequencies increase. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near the trip point. Once the temperature has returned to a non-critical level, and the hysteresis timer has expired, modulation ceases and the TCC goes inactive. Processor performance will be decrease by ~50% when the TCC is active (assuming a 50% duty cycle), however, with a properly designed and characterized thermal solution the TCC most likely will only be activated briefly during the most power intensive applications while at maximum chassis ambient temperature within the chassis.

For automatic mode, the 50% duty cycle is factory configured and cannot be modified. Also, automatic mode does not require any additional hardware, software drivers or interrupt handling routines.

The TCC may also be activated via On-Demand mode. If bit 4 of the ACPI Thermal Monitor Control Register is written to a “1” the TCC will be activated immediately, independent of the processor temperature. When using On-Demand mode to activate the TCC, the duty cycle of the clock modulation is programmable via bits 3:1 of the same ACPI Thermal Monitor Control Register. In automatic mode, the duty cycle is fixed at 50% on, 50% off, however in On-Demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off, to 87.5% on/12.5% off in 12.5% increments. On-Demand mode may be used at the same time Automatic mode is enabled,

however, if the TCC is enabled via On-Demand mode at the same time automatic mode is enabled AND a high temperature condition exists, the 50% duty cycle of the automatic mode will override the duty cycle selected by the On-Demand mode

An external signal, PROCHOT# (processor hot) is asserted at any time the TCC is active (either in Automatic or On-Demand mode). Bus snooping and interrupt latching are also active while the TCC is active. The temperature at which the thermal control circuit activates is not user configurable and is not software visible.

Besides the thermal sensor and thermal control circuit, the Thermal Monitor feature also includes one ACPI register, one performance counter register, three model specific registers (MSR), and one I/O pin (PROCHOT#). All are available to monitor and control the state of the Thermal Monitor feature. Thermal Monitor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT# (i.e. upon the activation/deactivation of TCC). Refer to Volume 3 of the *IA32 Intel Architecture Software Developer's Manual* for specific register and programming details.

If automatic mode is disabled the processor will be operating out of specification and cannot be guaranteed to provide reliable results. Regardless of enabling of the automatic or On-Demand modes, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a temperature of approximately 135 °C. At this point the system bus signal THERMTRIP# will go active and stay active until the processor has cooled down and RESET# has been initiated. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. If THERMTRIP# is asserted, processor core power (VCC) must be removed within the timeframe defined in Table 14.

7.3.1 Thermal Diode

The processor incorporates an on-die thermal diode. A thermal sensor located on the processor may be used to monitor the die temperature of the processor for thermal management/long term die temperature change purposes. This thermal diode is separate from the Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Thermal Monitor. See Section 7.4.4 for details.

7.4 System Management Bus (SMBus) Interface

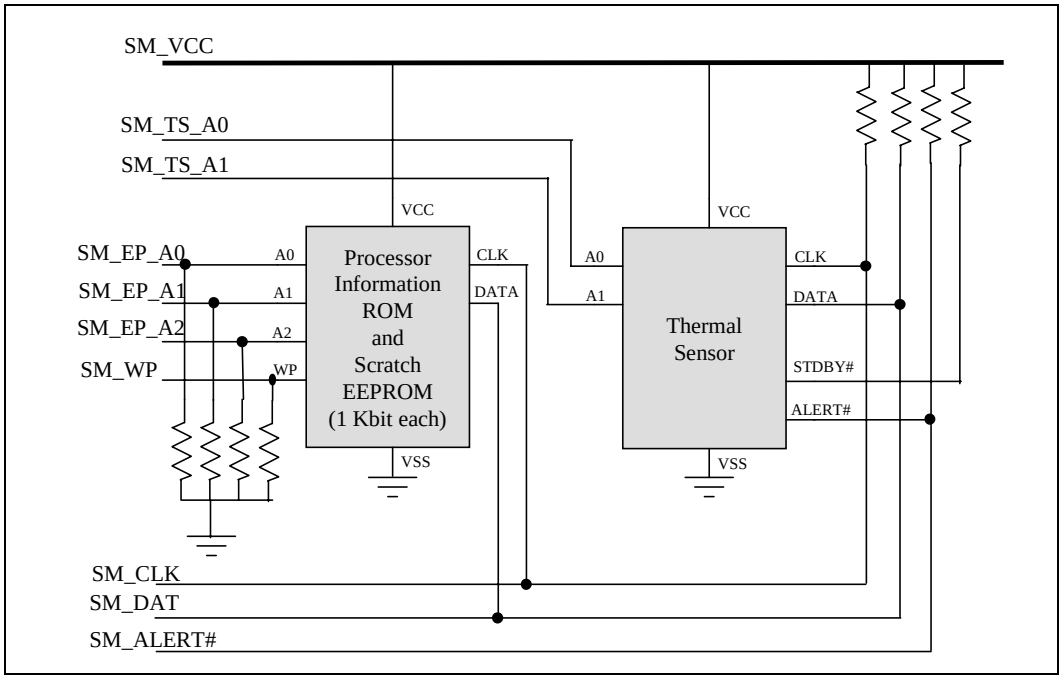
The processor includes an SMBus interface which allows access to a memory component with two sections (referred to as the Processor Information ROM and the Scratch EEPROM) and a thermal sensor on the substrate. The SMBus thermal sensor may be used to read the thermal diode mentioned in Section 7.3.1. These devices and their features are described below. See Chapter 4.0 for the physical location of these devices.

Note: The SMBus thermal sensor and its associated thermal diode are not related to the precision on-die temperature sensor and thermal control circuit (TCC) of the Thermal Monitor feature discussed in Section 7.3.

The processor SMBus implementation uses the clock and data signals of the V1.1 *System Management Bus Specification*. It does not implement the SMBSUS# signal. Layout and routing guidelines are available in the appropriate platform design guidelines document.

For platforms which do not implement any of the SMBus features found on the processor, all of the SMBus connections to the 603-pin socket may be left unconnected (SM_ALERT#, SM_CLK, SM_DAT, SM_EP_A[2:0], SM_TS_A[1:0], SM_WP). SM_VCC must be supplied when support for future processors utilizing the 603-pin socket is desired.

Figure 33. Logical Schematic of SMBus Circuitry



NOTE: Actual implementation may vary. For use in general understanding of the architecture. All SMBus pull-up and pull-down resistors are 10 KΩ and located on the processor.

7.4.1 Processor Information ROM (PIROM)

The lower one kilobit portion of the processor SMBus memory component is an electrically programmed read-only memory with information about the processor. This information is permanently write-protected. Table 33 shows the data fields and formats provided in the Processor Information ROM (PIROM).

Table 33. Processor Information ROM Format (Page 1 of 2)

Offset/Section	# of Bits	Function	Notes
Header:			
00h	8	Data Format Revision	Two 4-bit hex digits
01 - 02h	16	EEPROM Size	Size in bytes (MSB first)
03h	8	Processor Data Address	Byte pointer, 00h if not present
04h	8	Processor Core Data Address	Byte pointer, 00h if not present
05h	8	L3 Cache Data Address	Byte pointer, 00h if not present
06h	8	Package Data Address	Byte pointer, 00h if not present
07h	8	Part Number Data Address	Byte pointer, 00h if not present
08h	8	Thermal Reference Data Address	Byte pointer, 00h if not present
09h	8	Feature Data Address	Byte pointer, 00h if not present
0Ah	8	Other Data Address	Byte pointer, 00h if not present
0B - 0Ch	16	Reserved	Reserved for future use
0Dh	8	Checksum	1 byte checksum
Processor Data:			
0E - 13h	48	QDF Number	Six 8-bit ASCII characters
14h	6 2	Reserved Sample/Production	Reserved for future use 00b = Sample only, 01-11b = Production
15h	8	Checksum	1 byte checksum
Processor Core Data:			
16 - 17h	2	Processor Core Type	From CPUID
	4	Processor Core Family	From CPUID
	4	Processor Core Model	From CPUID
	4	Processor Core Stepping	From CPUID
	2	Reserved	Reserved for future use
18 - 19h	16	Reserved	Reserved for future use
1A - 1Bh	16	System Bus Frequency	16-bit binary number (in MHz)
1Ch	2 6	Multiprocessor Support Reserved	00b = UP,01b = DP,10b = RSVD,11b = MP Reserved for future use
1D - 1Eh	16	Maximum Core Frequency	16-bit binary number (in MHz)
1F - 20h	16	Processor VID (Voltage Identification)	Voltage requested by the VID outputs in mV
21 - 22h	16	Core Voltage, Minimum	Minimum processor DC Vcc spec in mV
23h	8	T_{CASE} Maximum	Maximum case temperature spec in °C
24h	8	Checksum	1 byte checksum
Cache Data:			
25 - 26h	16	Reserved	Reserved for future use
27 - 28h	16	L2 Cache Size	16-bit binary number (in Kbytes)

Table 33. Processor Information ROM Format (Page 2 of 2)

Offset/Section	# of Bits	Function	Notes
29 - 2Ah	16	L3 Cache Size	16-bit binary number (in Kbytes)
2B - 30h	48	Reserved	Reserved for future use.
31h	8	Checksum	1 byte checksum
Package Data:			
32 - 35h	32	Package Revision	Four 8-bit ASCII characters
36h	8	Reserved	Reserved for future use
37h	8	Checksum	1 byte checksum
Part Number Data:			
38 - 3Eh	56	Processor Part Number	Seven 8-bit ASCII characters
3F - 4Ch	112	Processor BOM ID	Fourteen 8-bit ASCII characters (Reserved)
4D - 54h	64	Processor Electronic Signature	64-bit identification number
55 - 6Eh	208	Reserved	Reserved for future use
6Fh	8	Checksum	1 byte checksum
Thermal Ref. Data:			
70h	8	Thermal Reference Byte	See Section 7.4.4 for details
71 - 72h	16	Reserved	Reserved for future use
73h	8	Checksum	1 byte checksum
Feature Data:			
74 - 77h	32	Processor Core Feature Flags	From CPUID function 1, EDX contents
78h	8	Processor Feature Flags	[7] = Reserved [6] = Serial Signature [5] = Electronic Signature Present [4] = Thermal Sense Device Present [3] = Thermal Reference Byte Present [2] = OEM EEPROM Present [1] = Core VID Present [0] = L3 Cache Present
79-7Bh	24	Additional Processor Feature Flags	Reserved
7Ch	8	Reserved	Reserved for future use
7Dh	8	Checksum	1 byte checksum
Other Data:			
7E - 7Fh	16	Reserved	Reserved for future use

7.4.2 Scratch EEPROM

Also available in the memory component on the processor SMBus is an EEPROM which may be used for other data at the system or processor vendor's discretion. The data in this EEPROM, once programmed, can be write-protected by asserting the active-high SM_WP signal. This signal has a weak pull-down (10 kΩ) to allow the EEPROM to be programmed in systems with no implementation of this signal. The Scratch EEPROM resides in the upper half of the memory component (addresses 80 - FFh). The lower half comprises the Processor Information ROM (address 00 - 7Fh), which is permanently write protected by Intel.

7.4.3 PIROM and Scratch EEPROM Supported SMBus Transactions

The Processor Information ROM (PIROM) responds to two SMBus packet types: Read Byte and Write Byte. However, since the PIROM is write-protected, it will acknowledge a Write Byte command but ignore the data. The Scratch EEPROM responds to Read Byte and Write Byte commands. Table 34 diagrams the Read Byte command. Table 35 diagrams the Write Byte command. Following a write cycle to the scratch ROM, software must allow a minimum of 10ms before accessing either ROM of the processor.

In the tables, 'S' represents the SMBus start bit, 'P' represents a stop bit, 'R' represents a read bit, 'W' represents a write bit, 'A' represents an acknowledge (ACK), and '///' represents a negative acknowledge (NACK). The shaded bits are transmitted by the Processor Information ROM or Scratch EEPROM, and the bits that aren't shaded are transmitted by the SMBus host controller. In the tables the data addresses indicate 8 bits. The SMBus host controller should transmit 8 bits with the most significant bit indicating which section of the EEPROM is to be addressed: the Processor Information ROM (MSB = 0) or the Scratch EEPROM (MSB = 1).

Table 34. Read Byte SMBus Packet

S	Slave Address	Write	A	Command Code	A	S	Slave Address	Read	A	Data	///	P
1	7-bits	1	1	8-bits	1	1	7-bits	1	1	8-bits	1	1

Table 35. Write Byte SMBus Packet

S	Slave Address	Write	A	Command Code	A	Data	A	P
1	7-bits	1	1	8-bits	1	8-bits	1	1

7.4.4 SMBus Thermal Sensor

The processor's SMBus thermal sensor provides a means of acquiring thermal data from the processor. The thermal sensor is composed of control logic, SMBus interface logic, a precision analog-to-digital converter, and a precision current source. The sensor drives a small current through the p-n junction of a thermal diode located on the processor core. The forward bias voltage generated across the thermal diode is sensed and the precision A/D converter derives a single byte of thermal reference data, or a "thermal byte reading." The nominal precision of the least significant bit of a thermal byte is 1°C.

The processor incorporates the SMBus thermal sensor and thermal reference byte onto the processor package as was done with the previous Intel® Pentium® III Xeon™ processor family. Upper and lower thermal reference thresholds can be individually programmed for the SMBus thermal sensor. Comparator circuits sample the register where the single byte of thermal data

(thermal byte reading) is stored. These circuits compare the single byte result against programmable threshold bytes. If enabled, the alert signal on the processor SMBus (SM_ALERT#) will be asserted when the sensor detects that either threshold is reached or crossed. Analysis of SMBus thermal sensor data may be useful in detecting changes in the system environment that may require attention.

During manufacturing, the thermal reference byte programmed it into the Processor Information ROM. The thermal reference byte represent the approximate maximum temperate of the processor and is determined through device characterization.

The processor's SMBus thermal sensor and thermal reference byte may be used to monitor long term temperature trends, but cannot be used to manage the short term temperature of the processor or predict the activation of the thermal control circuit. As mentioned earlier, the processors high thermal ramp rates make this infeasible. Refer to the *Intel® Xeon™ Processor Family Thermal Design Guidelines* for more details.

The SMBus thermal sensor feature in the processor cannot be used to measure T_{CASE}. The T_{CASE} specification in Chapter 6.0 must be met regardless of the reading of the processor's thermal sensor in order to ensure adequate cooling for the entire processor. The SMBus thermal sensor feature is only available while V_{CC} and SM_VCC are at valid levels and the processor is not in a low-power state.

7.4.5 Thermal Sensor Supported SMBus Transactions

The thermal sensor responds to five of the SMBus packet types: Write Byte, Read Byte, Send Byte, Receive Byte, and Alert Response Address (ARA). The Send Byte packet is used for sending one-shot commands only. The Receive Byte packet accesses the register commanded by the last Read Byte packet and can be used to continuously read from a register. If a Receive Byte packet was preceded by a Write Byte or send Byte packet more recently than a Read Byte packet, then the behavior is undefined. Table 36 through Table 40 diagram the five packet types. In these figures, 'S' represents the SMBus start bit, 'P' represents a stop bit, 'Ack' represents an acknowledge, and '///' represents a negative acknowledge (NACK). The shaded bits are transmitted by the thermal sensor, and the bits that aren't shaded are transmitted by the SMBus host controller. Table 41 shows the encoding of the command byte.

Table 36. Write Byte SMBus Packet

S	Slave Address	Write	Ack	Command Code	Ack	Data	Ack	P
1	7-bits	1	1	8-bits	1	8-bits	1	1

Table 37. Read Byte SMBus Packet

S	Slave Address	Write	Ack	Command Code	Ack	S	Slave Address	Read	Ack	Data	///	P
1	7-bits	1	1	8-bits	1	1	7-bits	1	1	8-bits	1	1

Table 38. Send Byte SMBus Packet

S	Slave Address	Read	Ack	Command Code	Ack	P
1	7-bits	1	1	8-bits	1	1

Table 39. Receive Byte SMBus Packet

S	Slave Address	Read	Ack	Data	///	P
1	7-bits	1	1	8-bits	1	1

Table 40. ARA SMBus Packet

S	ARA	Read	Ack	Address	///	P
1	0001 100	1	1	Device Address[1]	1	1

NOTE:
1. This is an 8-bit field. The device which sent the alert will respond to the ARA Packet with its address in the seven most significant bits. The least significant bit is undefined and may return as a '1' or '0'. See Section 7.4.8 for details on the Thermal Sensor Device addressing.

Table 41. SMBus Thermal Sensor Command Byte Bit Assignments

Register	Command	Reset State	Function
RESERVED	00h	RESERVED	Reserved for future use
TRR	01h	0000 0000	Read processor core thermal diode
RS	02h	N/A	Read status byte (flags, busy signal)
RC	03h	00XX XXXX	Read configuration byte
RCR	04h	0000 0010	Read conversion rate byte
RESERVED	05h	RESERVED	Reserved for future use
RESERVED	06h	RESERVED	Reserved for future use
RRHL	07h	0111 1111	Read processor core thermal diode T_{HIGH} limit
RRLL	08h	1100 1001	Read processor core thermal diode T_{LOW} limit
WC	09h	N/A	Write configuration byte
WCR	0Ah	N/A	Write conversion rate byte
RESERVED	0Bh	RESERVED	Reserved for future use
RESERVED	0Ch	RESERVED	Reserved for future use
WRHL	0Dh	N/A	Write processor core thermal diode T_{HIGH} limit
WRLL	0Eh	N/A	Write processor core thermal diode T_{LOW} limit
OSHT	0Fh	N/A	One shot command (use send byte packet)
RESERVED	10h – FFh	N/A	Reserved for future use

All of the commands in Table 41 are for reading or writing registers in the SMBus thermal sensor, except the one-shot command (OSHT) register. The one-shot command forces the immediate start of a new conversion cycle. If a conversion is in progress when the one-shot command is received,

then the command is ignored. If the thermal sensor is in stand-by mode when the one-shot command is received, a conversion is performed and the sensor returns to stand-by mode. The one-shot command is not supported when the thermal sensor is in auto-convert mode.

Note: Writing to a read-command register or reading from a write-command register will produce invalid results.

The default command after reset is to a reserved value (00h). After reset, “Receive Byte” SMBus packets will return invalid data until another command is sent to the thermal sensor.

7.4.6 SMBus Thermal Sensor Registers

7.4.6.1 Thermal Reference Registers

Once the SMBus thermal sensor reads the processor thermal diode, it performs an analog to digital conversion and stores the results in the Thermal Reference Register (TRR). The supported range is +127 to 0 decimal and is expressed as an eight-bit number representing temperature in degrees Celsius. This eight-bit value consists of seven bits of data and a sign bit (MSB) where the sign is always positive (sign = 0) and is shown in Table 42. The values shown are also used to program the Thermal Limit Registers.

The value of these registers should be treated as saturating values. Values above 127 are represented as 127 decimal and values of zero and below may be represented as 0 to -127 decimal. If the device returns a value where the sign bit is set (1) and the data is 0000_0000 through 111_1110, the temperature should be interpreted as 0° Celsius.

Table 42. Thermal Reference Register Values

Temperature (°C)	Register Value (binary)
+127	0 111 1111
+126	0 111 1110
+100	0 110 0100
+50	0 011 0010
+25	0 001 1001
+1	0 000 0001
0	0 000 0000

7.4.6.2 Thermal Limit Registers

The SMBus thermal sensor has four Thermal Limit Registers; RRHL is used to read the high limit, RRLL is read for the low limit, WRHL is used to write the high limit, and the WRLL to write the low limit. These registers allow the user to define high and low limits for the processor core thermal diode reading. The encoding for these registers is the same as for the Thermal Reference Register shown in Table 42. If the processor thermal diode reading equals or exceeds one of these limits, then the alarm bit (RHIGH or RLOW) in the Thermal Sensor Status Register is triggered.

7.4.6.3 Status Register

The Status Register shown in Table 43 indicates which (if any) thermal value thresholds for the processor core thermal diode have been exceeded. It also indicates if a conversion is in progress or if an open circuit has been detected in the processor core thermal diode connection. Once set, alarm bits stay set until they are cleared by a Status Register read. A successful read to the Status Register will clear any alarm bits that may have been set, unless the alarm condition persists. If the SM_ALERT# signal is enabled via the Thermal Sensor Configuration Register and a thermal diode threshold is exceeded, an alert will be sent to the platform via the SM_ALERT# signal.

This register is read by accessing the RS Command Register.

Table 43. SMBus Thermal Sensor Status Register

Bit	Name	Reset State	Function
7 (MSB)	BUSY	N/A	If set, indicates that the device's analog to digital converter is busy.
6	RESERVED	RESERVED	Reserved for future use
5	RESERVED	RESERVED	Reserved for future use
4	RHIGH	0	If set, indicates the processor core thermal diode high temperature alarm has activated.
3	RLOW	0	If set, indicates the processor core thermal diode low temperature alarm has activated.
2	OPEN	0	If set, indicates an open fault in the connection to the processor core diode.
1	RESERVED	RESERVED	Reserved for future use.
0 (LSB)	RESERVED	RESERVED	Reserved for future use.

7.4.6.4 Configuration Register

The Configuration Register controls the operating mode (stand-by vs. auto-convert) of the SMBus thermal sensor. Table 44 shows the format of the Configuration Register. If the RUN/STOP bit is set (high) then the thermal sensor immediately stops converting and enters stand-by mode. The thermal sensor will still perform analog to digital conversions in stand-by mode when it receives a one-shot command. If the RUN/STOP bit is clear (low) then the thermal sensor enters auto-conversion mode.

This register is accessed by using the thermal sensor Command Register: The RC command register is used for read commands and the WC command register is used for write commands. See Table 41.

Table 44. SMBus Thermal Sensor Configuration Register

Bit	Name	Reset State	Function
7 (MSB)	MASK	0	Mask SM_ALERT# bit. Clear bit to allow interrupts via SM_ALERT# and allow the thermal sensor to respond to the ARA command when an alarm is active. Set the bit to disable interrupt mode. The bit is not used to clear the state of the SM_ALERT# output. An ARA command may not be recognized if the mask is enabled.
6	RUN/STOP	0	Stand-by mode control bit. If set, the device immediately stops converting, and enters stand-by mode. If cleared, the device converts in either one-shot mode or automatically updates on a timed basis.
5:0	RESERVED	RESERVED	Reserved for future use.

7.4.6.5 Conversion Rate Registers

The contents of the Conversion Rate Registers determine the nominal rate at which analog to digital conversions happen when the SMBus thermal sensor is in auto-convert mode. There are two Conversion Rate Registers, RCR for reading the conversion rate value and WCR for writing the value. Table 45 shows the mapping between Conversion Rate Register values and the conversion rate. As indicated in Table 41, the Conversion Rate Register is set to its default state of 02h (0.25 Hz nominally) when the thermal sensor is powered up. There is a ±30% error tolerance between the conversion rate indicated in the conversion rate register and the actual conversion rate.

Table 45. SMBus Thermal Sensor Conversion Rate Registers

Register Value	Conversion Rate (Hz)
00h	0.0625
01h	0.125
02h	0.25
03h	0.5
04h	1.0
05h	2.0
06h	4.0
07h	8.0
08h to FFh	Reserved for future use

7.4.7 SMBus Thermal Sensor Alert Interrupt

The SMBus thermal sensor located on the processor includes the ability to interrupt the SMBus when a fault condition exists. The fault conditions consist of: 1) a processor thermal diode value measurement that exceeds a user-defined high or low threshold programmed into the Command Register or 2) disconnection of the processor thermal diode from the thermal sensor. The interrupt can be enabled and disabled via the thermal sensor Configuration Register and is delivered to the system board via the SM_ALERT# open drain output. Once latched, the SM_ALERT# should only be cleared by reading the Alert Response byte from the Alert Response Address of the thermal sensor. The Alert Response Address is a special slave address shown in Table 40. The

SM_ALERT# will be cleared once the SMBus master device reads the slave ARA unless the fault condition persists. Reading the Status Register or setting the mask bit within the Configuration Register does not clear the interrupt.

7.4.8 SMBus Device Addressing

Of the addresses broadcast across the SMBus, the memory component claims those of the form "1010XXXZb". The "XXX" bits are defined by pullups and pulldowns on the system baseboard. These address pins are pulled down weakly (10 kΩ) on the processor substrate to ensure that the memory components are in a known state in systems which do not support the SMBus, or only support a partial implementation. The "Z" bit is the read/write bit for the serial bus transaction.

The thermal sensor internally decodes one of three upper address patterns from the bus of the form "0011XXXZb", "1001XXXZb", or "0101XXXZb". The device's addressing, as implemented, uses the SM_TS_A[1:0] pins in either the HI, LO, or Hi-Z state. Therefore, the thermal sensor supports nine unique addresses. To set either pin for the Hi-Z state, the pin must be left floating. As before, the "Z" bit is the read/write bit for the serial transaction.

Note that addresses of the form "0000XXXXb" are Reserved and should not be generated by an SMBus master. The thermal sensor samples and latches the SM_TS_A[1:0] signals at power-up and at the starting point of every conversion. System designers should ensure that these signals are at valid input levels before the thermal sensor powers up. This should be done by pulling the pins to SM_VCC or V_{SS} via a 1 kΩ or smaller resistor, or leaving the pins floating to achieve the Hi-Z state. If the designer desires to drive the SM_TS_A[1:0] pins with logic, the designer must ensure that the pins are at input levels of 3.3V or 0V before SM_VCC begins to ramp. The system designer must also ensure that their particular implementation does not add excessive capacitance to the address inputs. Excess capacitance at the address inputs may cause address recognition problems. Refer to the appropriate platform design guidelines document and the *System Management Bus Specification*.

Figure 33 on page 94 shows a logical diagram of the pin connections. Table 46 and Table 47 describe the address pin connections and how they affect the addressing of the devices.

Table 46. Thermal Sensor SMBus Addressing

Address (Hex)	Upper Address[1]	Device Select		8-bit Address Word on Serial Bus
		SM_TS_A1	SM_TS_A0	b[7:0]
3Xh	0011	0	0	0011000Xb
		Z[2]	0	0011001Xb
		1	0	0011010Xb
5Xh	0101	0	Z[2]	0101001Xb
		Z[2]	Z[2]	0101010Xb
		1	Z[2]	0101011Xb
9Xh	1001	0	1	1001100Xb
		Z[2]	1	1001101Xb
		1	1	1001110Xb

NOTES:
1. Upper address bits are decoded in conjunction with the select pins.

2. A tri-state or “Z” state on this pin is achieved by leaving this pin unconnected.

Note: System management software must be aware of the processor dependent addresses for the thermal sensor.

Table 47. Memory Device SMBus Addressing

Address (Hex)	Upper Address[1]	Device Select			R/W
	bits 7-4	SM_EP_A2 bit 3	SM_EP_A1 bit 2	SM_EP_A0 bit 1	bit 0
A0h/A1h	1010	0	0	0	X
A2h/A3h	1010	0	0	1	X
A4h/A5h	1010	0	1	0	X
A6h/A7h	1010	0	1	1	X
A8h/A9h	1010	1	0	0	X
AAh/ABh	1010	1	0	1	X
ACh/ADh	1010	1	1	0	X
AEh/AFh	1010	1	1	1	X

NOTES:
1. This addressing scheme will support up to 8 processors on a single SMBus.

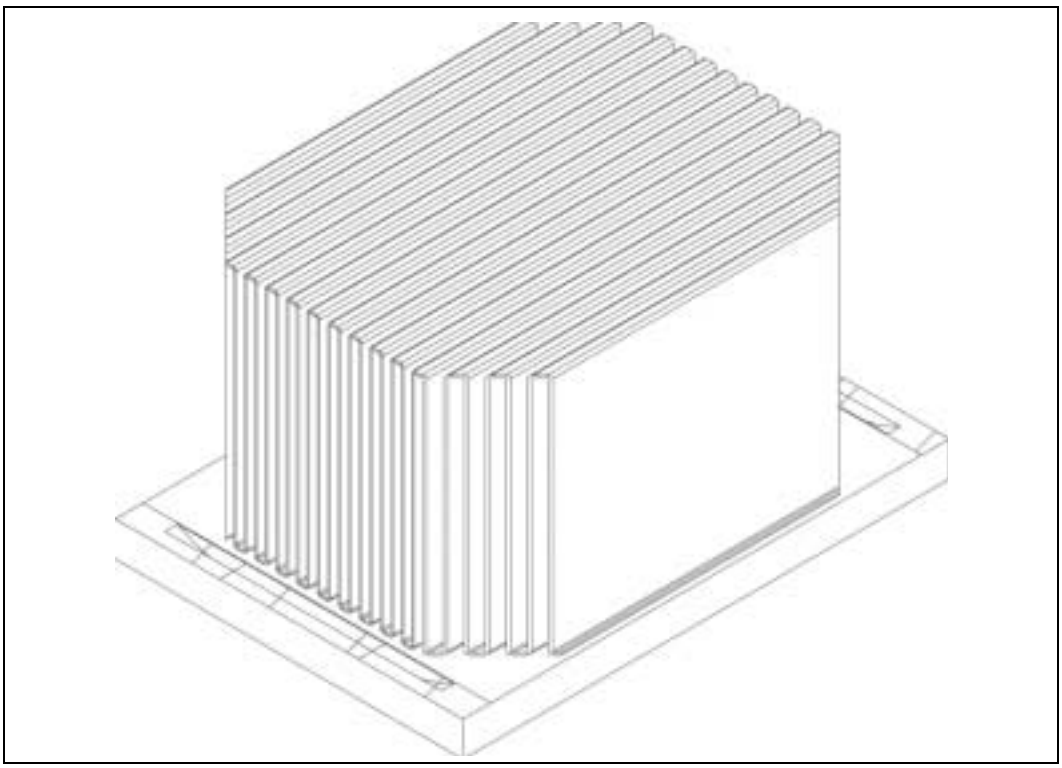
8.0 Boxed Processor Specifications

8.1 Introduction

The Intel® Xeon™ processor is also offered as an Intel boxed processor. Intel boxed processors are intended for system integrators who build systems from components available through distribution channels. The boxed Intel Xeon processor will be supplied with an unattached passive heatsink. It also contains an optional active duct solution, called Processor Wind Tunnel (PWT), to provide adequate airflow across the heatsink. If the chassis or motherboard used contains an alternate cooling solution that has been thermally validated, the PWT may be discarded. This chapter documents system board and platform requirements for the cooling solution that is supplied with the boxed processor. This chapter is particularly important for OEM's that manufacture system boards and chassis for integrators. Unless otherwise noted, all figures in this chapter are dimensioned in millimetres and in inches [in brackets]. Figure 34 shows a mechanical representation of a boxed processor heatsink.

Note: Drawings in this section reflect only the specifications on the Intel boxed processor product. These dimensions should not be used as a generic keep-out zone for all cooling solutions. It is the system designer's responsibility to consider their proprietary cooling solution when designing to the required keep-out zone on their system platform and chassis.

Figure 34. Mechanical Representation of the Boxed Processor Passive Heatsink



8.2 Mechanical Specifications

This section documents the mechanical specifications of the boxed processor passive heatsink and the PWT.

Proper clearance is required around the heatsink to ensure proper installation of the processor and unimpeded airflow for proper cooling.

8.2.1 Boxed Processor Heatsink Dimensions

The boxed processor will be shipped with an unattached passive heatsink. Clearance is required around the heatsink to ensure unimpeded airflow for proper cooling. The physical space requirements and dimensions for the boxed processor with assembled heatsink are shown in Figure 36 (Multiple Views). The airflow requirements for the boxed processor heatsink must also be taken into consideration when designing new system boards and chassis. The airflow requirements are detailed in the Thermal Specifications, Section 8.4.

8.2.2 Boxed Processor Heatsink Weight

The boxed processor heatsink will not weigh more than 450 grams. See Chapter 4.0 and Chapter 6.0 of this document along with the *Intel® Xeon™ Processor Family Thermal Design Guidelines* for details on the processor weight and heatsink requirements.

8.2.3 Boxed Processor Retention Mechanism and Heatsink Supports

The boxed processor requires processor retention mechanisms to secure the processor in the baseboard. The retention solution contains two retention mechanisms and two retention clips per processor. It has not yet been determined if these will ship with the boxed processor or with the basboards. Installation instructions should ship with the retention solution.

The retention mechanism that ships with the boxed processor is different than the reference solution from Intel. It adds tabs that allow the PWT to be attached directly to it. Please reference Figure 35 below, which contains the dimensions for the tabs that are different. For dimensions of the reference solution, please see the appropriate platform design guidelines.

Figure 35. Boxed Processor Retention Mechanism and Clip

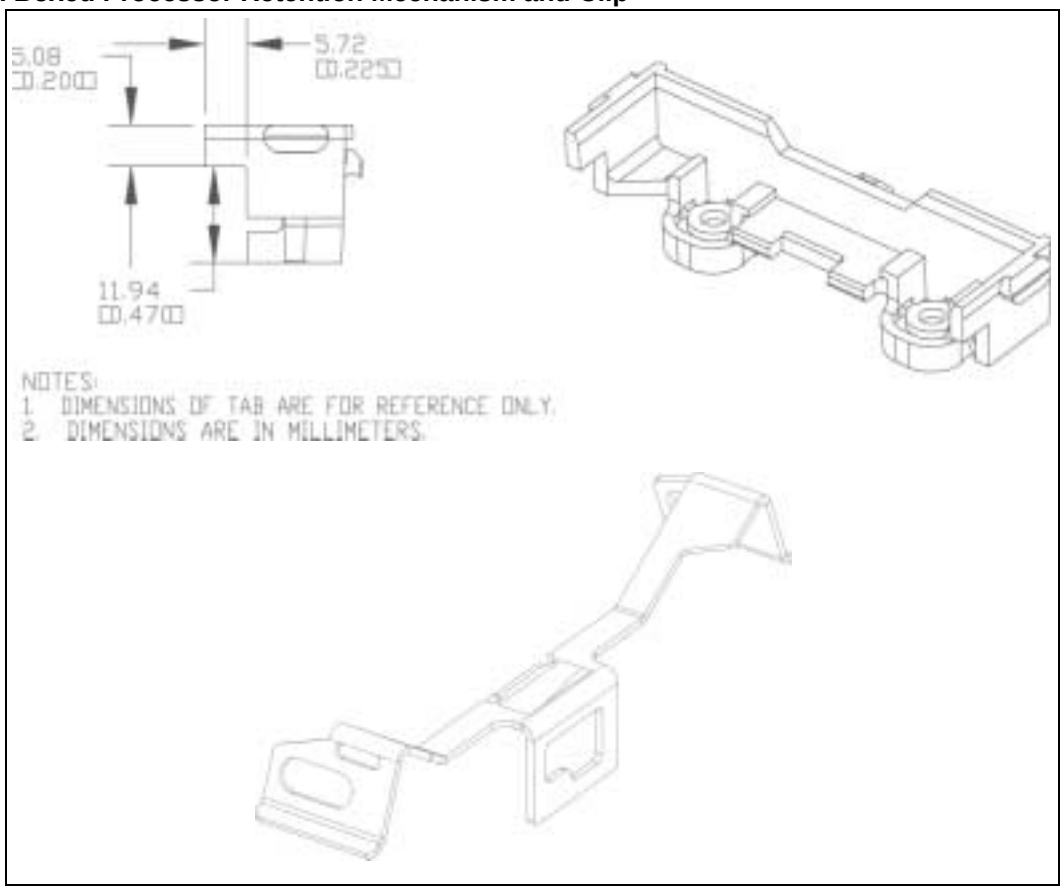
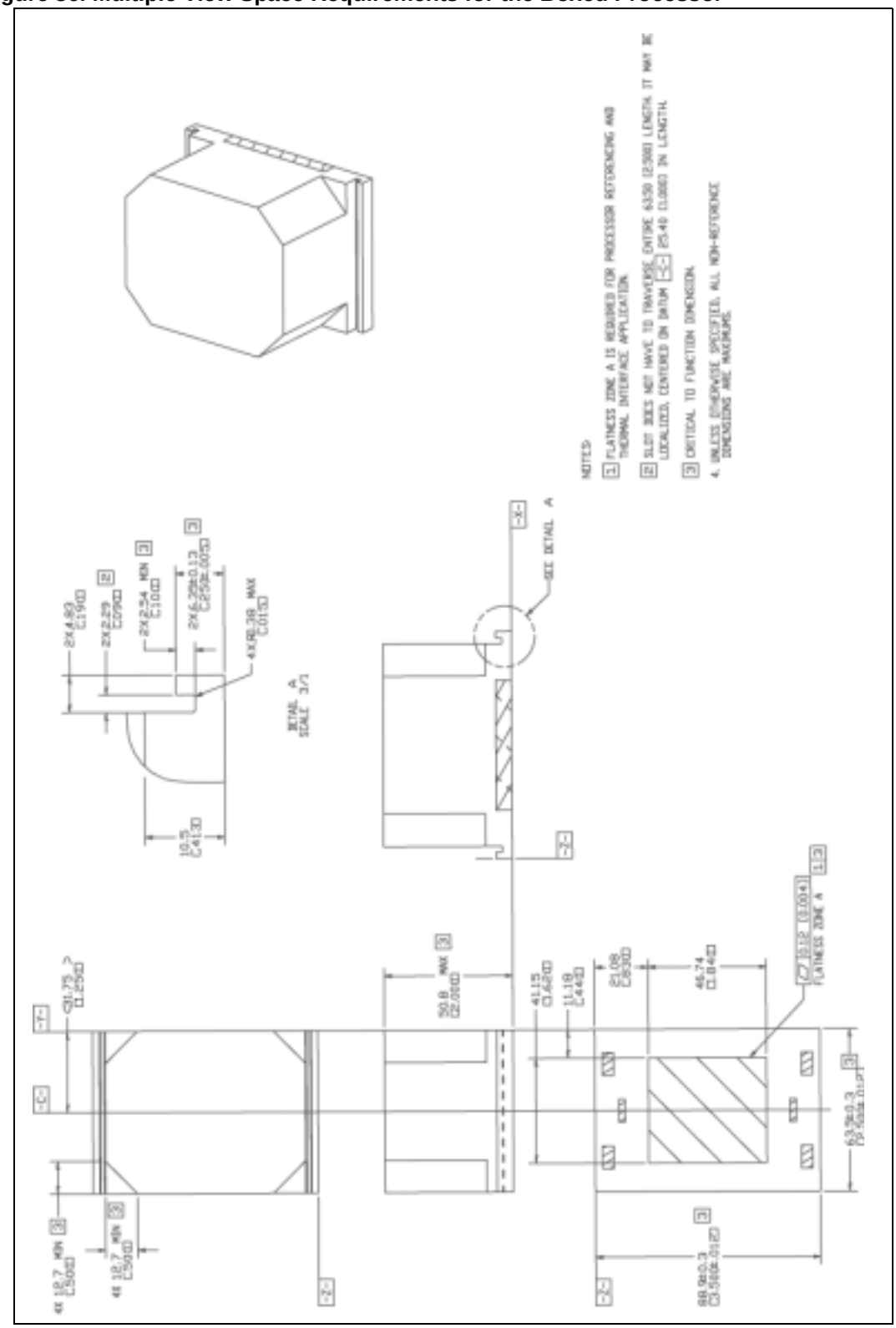


Figure 36. Multiple View Space Requirements for the Boxed Processor



8.3 Boxed Processor Requirements

8.3.1 Processor Wind Tunnel

The boxed processor ships with an active duct cooling solution called the Processor Wind Tunnel, or PWT. This is an optional cooling solution that is designed to meet the thermal requirements of a diverse combination of boards and chassis. It ships with the processor in order to reduce the burden on the chassis manufacture to provide adequate airflow across the processor heatsink. Manufacturers may elect to use their own cooling solution.

Note: Although Intel will be testing a select number of board and chassis combinations for thermal compliance, this is in no way a comprehensive test. It is ultimately the system integrator's responsibility to test that their solution meets all of the requirements specified in this document. The PWT is meant to assist in processor cooling, but additional cooling techniques may be required in order to ensure that the entire system meets the thermal requirements.

See Figure 38 for the Processor Wind Tunnel dimensions.

8.3.2 Fan Power Supply

The Processor Wind Tunnel includes a fan, which requires a +12V power supply. A fan power cable is shipped with the boxed processor to draw power from a power header on the system board. The power cable connector and pinouts are shown in Table 37. Platforms must provide a matched power header to support the boxed processor. Table 48 contains specifications for the input and output signals at the fan heatsink connector. The fan heatsink outputs a SENSE signal, an open-collector output, that pulses at a rate of two pulses per fan revolution. A system board pull-up resistor provides V_{OH} to match the system board-mounted fan speed monitor requirements, if applicable. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 of the connector should be tied to GND.

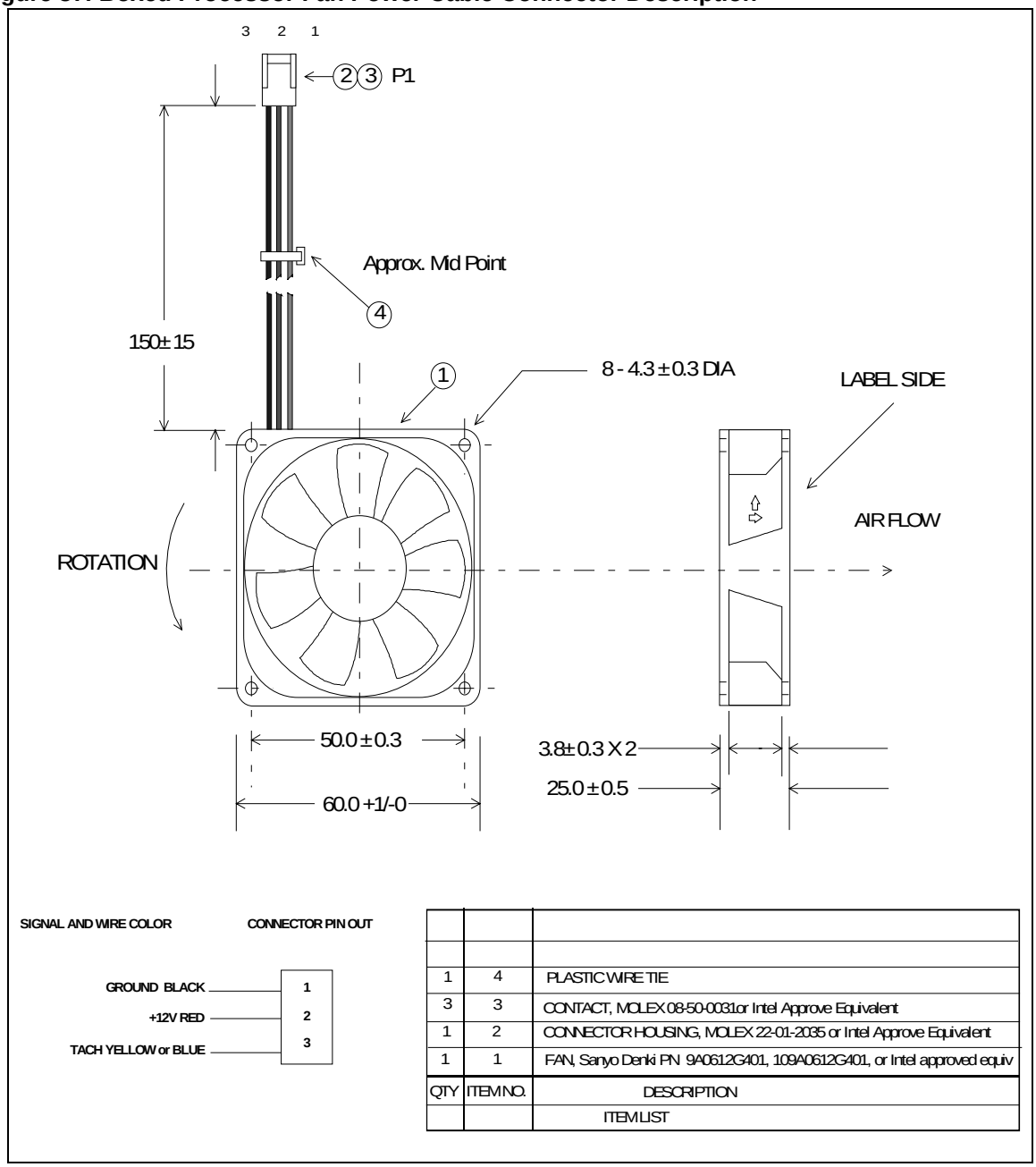
The power header on the baseboard must be positioned to allow the fan heatsink power cable to reach it. The power header identification and location should be documented in the platform documentation, or on the system board itself. The system board power header should be positioned within 7 inches from the center of the processor socket.

Table 48. Fan Power and Signal Specifications

Description	Min	Typ	Max	Unit	Notes
+12V: 12 Vot Fan Power Supply	6.0	12.0	13.2	V	
IC: Fan Current Draw			400	mA	
SENSE Frequency		2		Pulses per fan revolution	1

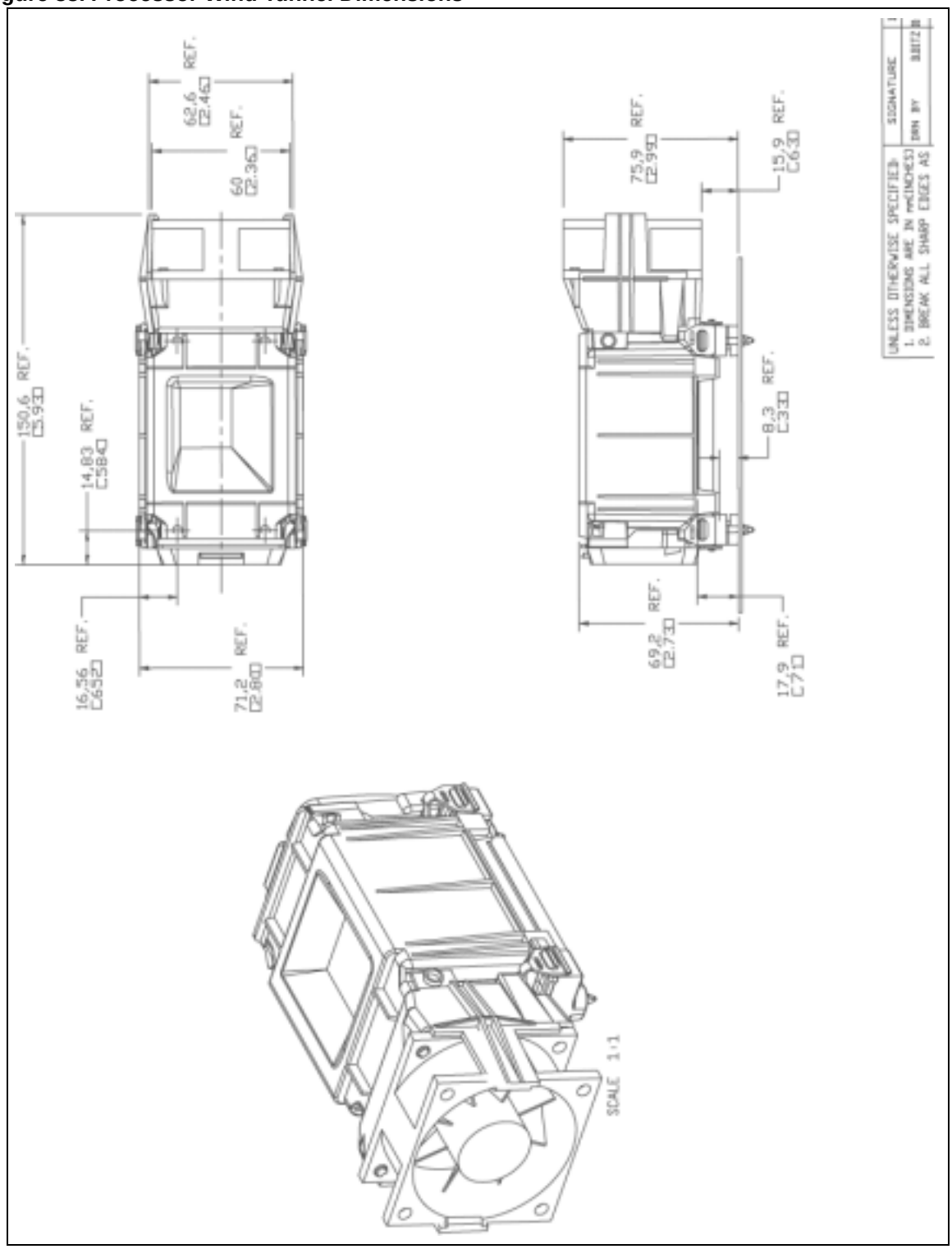
NOTE:
1. System board should pull this pin up to Vcc with a resistor.

Figure 37. Boxed Processor Fan Power Cable Connector Description



QTY	ITEM NO.	DESCRIPTION
		ITEM LIST
1	4	PLASTIC WIRE TIE
3	3	CONTACT, MOLEX 08-50-0031or Intel Approve Equivalent
1	2	CONNECTOR HOUSING, MOLEX 22-01-2035 or Intel Approve Equivalent
1	1	FAN, Sanyo Denki P/N 9A0612G401, 109A0612G401, or Intel approved equiv

Figure 38. Processor Wind Tunnel Dimensions



8.4 Thermal Specifications

This section describes the cooling requirements of the heatsink solution utilized by the boxed processor.

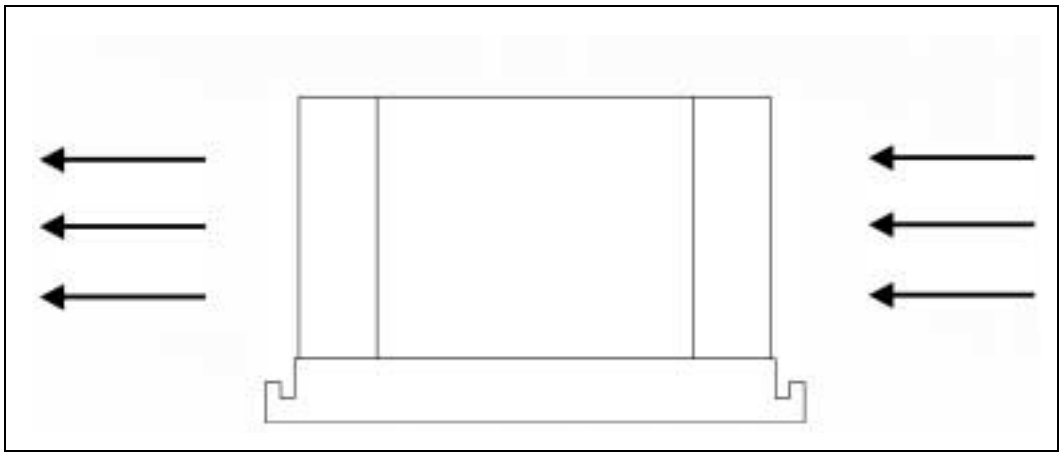
8.4.1 Boxed Processor Cooling Requirements

The boxed processor will be directly cooled with a passive heatsink. For the passive heatsink to effectively cool the boxed processor, it is critical that sufficient, unimpeded, cool air flow over the heatsink of every processor in the system. Meeting the processor's temperature specification is a function of the thermal design of the entire system, and ultimately the responsibility of the system integrator. The processor temperature specification is found in Chapter 6.0. It is important that system integrators perform thermal tests to verify that the boxed processor is kept below its maximum temperature specification in a specific baseboard and chassis.

At an absolute minimum, the boxed processor heatsink will require 500 Linear Feet per Minute (LFM) of cool air flowing over the heatsink. The airflow should be directed from the outside of the chassis directly over the processor heatsinks in a direction passing from one retention mechanism to the other. See Figure 39 for the proper airflow direction. Directing air over the passive heatsink of the boxed Intel® Xeon™ processor processor can be done with auxiliary chassis fans, fan ducts, or other techniques.

It is also recommended that the ambient air temperature of the chassis be kept at or below 45°C. The air passing directly over the processor heatsink should not be preheated by other system components (such as another processor), and should be kept at or below 45°C. Again, meeting the processor's temperature specification is the responsibility of the system integrator. The processor temperature specification is found in Chapter 6.0.

Figure 39. Boxed Processor Heatsink Airflow Direction



9.0 Debug Tools Specifications

Design support information for the in-target probe and Debug Port is contained in the *ITP700 Debug Port Design Guide*. This document includes all information necessary to include a Debug Port in a platform, including electrical specifications, mechanical requirements, and other design considerations. Refer to the references listed in Section 1.3.

9.1 Debug Port System Requirements

The Intel® Xeon™ processor debug port is the command and control interface for the In-Target Probe (ITP) debugger. The ITP enables run-time control of the processors for system debug. The debug port, which is connected to the system bus, is a combination of the system, JTAG and execution signals. There are several mechanical, electrical and functional constraints on the debug port which must be followed. The mechanical constraint requires the debug port connector to be installed in the system with adequate physical clearance. Electrical constraints exist due to the mixed high and low speed signals of the debug port for the processor. While the JTAG signals operate at a maximum of 16MHz, the execution signals operate at the common clock system bus frequency (100MHz). The functional constraint requires the debug port to use the JTAG system via a handshake and multiplexing scheme.

In general, the information in this chapter may be used as a basis for including all run-control tools in Intel® Xeon™ processor processor-based system designs, including tools from vendors other than Intel.

Note: The debug port and JTAG signal chain must be designed into the processor board to utilize the ITP for debug purposes.

9.2 Target System Implementation

9.2.1 System Implementation

Specific connectivity and layout guidelines for the Debug Port are provided in the *ITP700 Debug Port Design Guide*. Refer to Section 1.3.

9.3 Logic Analyzer Interface (LAI)

Two vendors provide logic analyzer interfaces (LAIs) for use in debugging Intel® Xeon™ processor processor-based systems. Tektronix* and Agilent* should be contacted to get specific information about their logic analyzer interfaces. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of Intel® Xeon™ processor processor-based multiprocessor systems, the LAI is critical in providing the ability to probe and capture system bus signals using a logic analyzer. There are two sets of considerations to keep in mind when designing a Intel® Xeon™ processor processor-based system that can make use of an LAI: mechanical and electrical.

9.3.1 Mechanical Considerations

The LAI is installed between the processor socket and the processor. The LAI pins plug into the socket, while the processor pins plug into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the processor and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system. Note that it is possible that the keepout volume reserved for the LAI may include space normally occupied by the heatsink. If this is the case, the logic analyzer vendor will provide a cooling solution as part of the LAI.

9.3.2 Electrical Considerations

The LAI will also affect the electrical performance of the system bus, therefore it is critical to obtain electrical load models from each of the logic analyser vendors to be able to run system level simulations to prove that their tool will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide

10.0 Processor Core Frequency Determination

To allow system debug and multiprocessor configuration flexibility, the core frequency of the Intel® Xeon™ processor is configured during the active-to-inactive edge of RESET# by using the A20M#, IGNNE#, LINT[1]/NMI, and LINT[0]/INTR pins. The value on these pins during the release of RESET# (see Section 2.12 for setup and hold time requirements) determines the multiplier that the PLL will use for the internal core clock (see Table 1). See Section 5.2 for details regarding the operation of these pins after Reset.

See Figure 40 for the timing relationship between the system bus multiplier signals, RESET#, CRESET#, and normal processor operation. CRESET# (Configuration Reset) is a delayed copy of system bus Reset signal. This signal is used to control the multiplexer for the processor frequency configuration pins listed above. CRESET# is delayed from the system bus reset by two host clocks. Using CRESET# and the timing shown in Figure 40, the circuit in Figure 41 can be used to share these configuration signals. The component used as the multiplexer must not have outputs that drive higher than V_{CC} in order to meet processor asynchronous GTL+ buffer specifications listed in Table 8. The multiplexer output current should be limited to 200 mA maximum, in case the V_{CC} supply to the processor ever fails.

As shown in Figure 41, the pull-up resistors between the multiplexer and the processor force a “safe” ratio into the processor in the event that the processor powers up before the multiplexer and/or core logic. This prevents the processor from ever seeing a ratio higher than the final ratio.

The compatibility inputs to the multiplexer must meet the input specifications of the multiplexer. This may require a level translation before the multiplexer inputs unless the inputs and the signals driving them are already compatible.

The system bus frequency multipliers supported are shown in Table 1; other combinations will not be validated nor are they authorized for implementation.

Clock multiplying within the processor is provided by the internal Phase Lock Loop (PLL), which requires a constant frequency BCLK inputs. For Spread Spectrum Clocking, please refer to the *CK00 Clock Synthesizer/Driver Design Guidelines*. The system bus frequency ratio cannot be changed dynamically during normal operation, nor can it be changed during any low power modes. The system bus frequency ratio can be changed when RESET# is active, assuming that all Reset specifications are met.

Figure 40. Timing Diagram of the Clock Ratio Signals

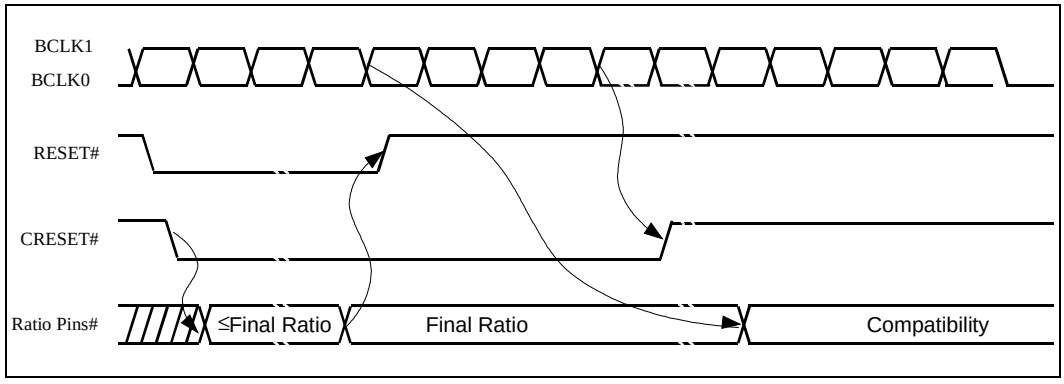
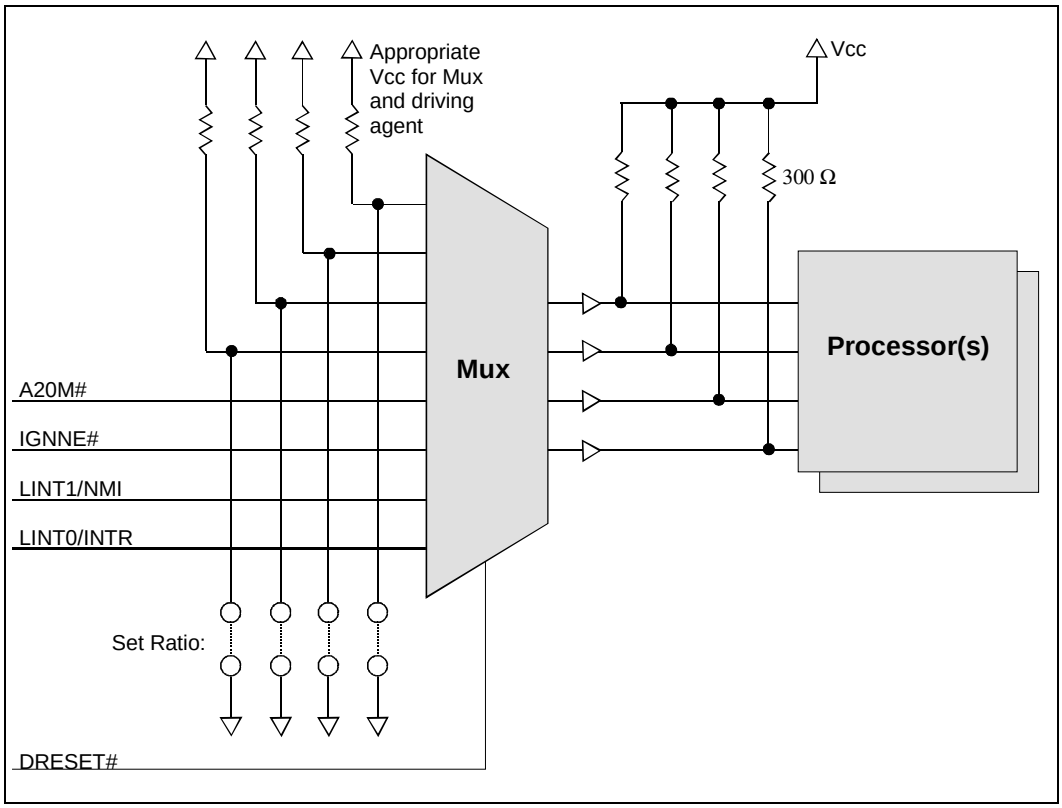


Figure 41. Example Schematic for Clock Ratio Pin Sharing



Note: Check your chipset documentation to determine if it includes this multiplexing logic for clock ratio pin sharing.