Dual Intel® Xeon™ Processor Voltage Regulator Down (VRD) Design Guidelines

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Contents

Guideline Definitions

This document defines DC-to-DC converters to meet the power requirements of computer systems using Intel® microprocessors. VRD requirements will vary according to the needs of different computer systems and processors that a specific VRD is expected to support. The "VRD" designation refers to an embedded voltage regulator on a system board. Please refer to the VRM 9.1 document for Voltage Regulator Module design guidelines.

The Dual Intel® Xeon™ Processor VRD Design Guidelines definition is specifically intended to meet the needs of systems based on two Intel Xeon processors or Low Voltage Intel Xeon processors (604-pin package only) in the 603-or 604-pin package.

Each guideline is placed into one of three categories. The category immediately follows the section heading and is one of the following:

REQUIRED:	An essential part of the design—necessary to meet processor voltage and current specifications and follow processor layout guidelines.
EXPECTED:	Part of Intel's processor power definitions; necessary for consistency among the designs of many systems and power devices. May be specified or expanded by system OEMs.
PROPOSED:	Normally met by this type of DC-to-DC converter and, therefore, included as a design target. May be specified or expanded by system OEMs.

1 Scope

This document details the guidelines for developing a single embedded voltage regulator circuit (VRD) to supply the required current and voltage to the common power plane for two Intel® Xeon™ processors or Low Voltage Intel Xeon Processors on a dual-processor-capable system board. The parameters specified in this document are provided as guidelines only. For the most current processor specifications please refer to the appropriate component datasheet.

Intel Xeon processors have unique requirements for voltages supplied to them. Their bus implementation, called AGTL+, the processor core, and the cache are being powered from the same voltage supply. Figure 1 shows two possible power distribution scheme options for the system board designer:

- Two plug-in voltage regulator modules (as defined in the VRM 9.0 or VRM 9.1 design guidelines) operating in tandem with current-shared outputs and with one VRM per occupied processor socket: that is, a 1:1 VRM-to-processor ratio
- A single VRD, as detailed in this document.

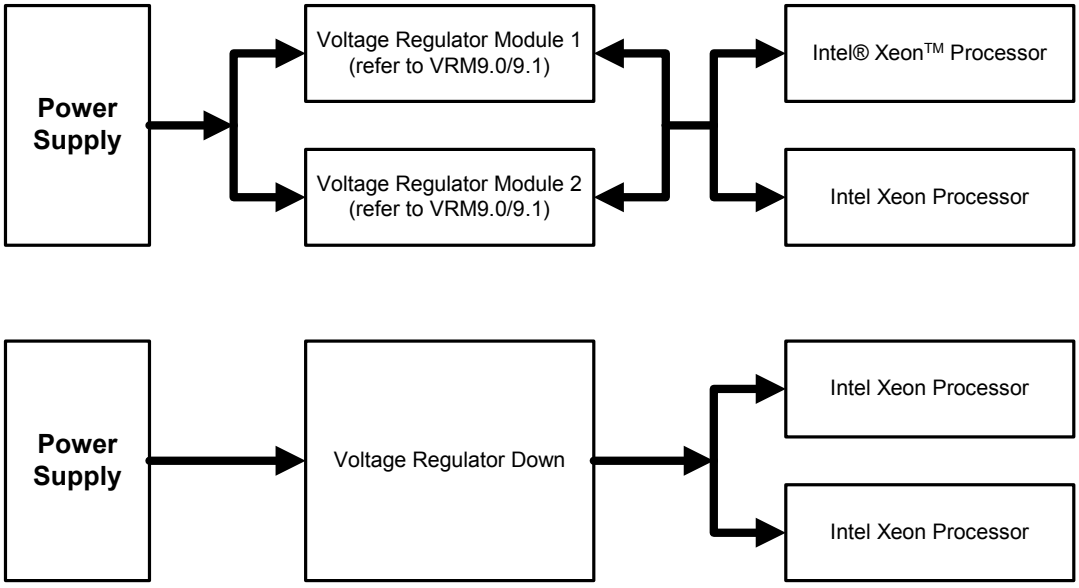

Figure 1 – Power Distribution Options

This document does not address system boards supporting in excess of two processors (i.e., Multiple Processor or MP systems). Intel expects MP systems to use voltage regulator modules (VRM 9.1), with a 1:1 VRM-to-processor ratio. The Dual Intel Xeon Processor VRD and VRM 9.1 are electrically equivalent: a processor requires either implementation and its related power delivery design to deliver the same voltage and current to the processor's socket.

Figure 2 illustrates a basic electrical model for a single VRD, dual-processor power delivery approach, based on an Intel Xeon processor – Intel 860 chipset platform core design.

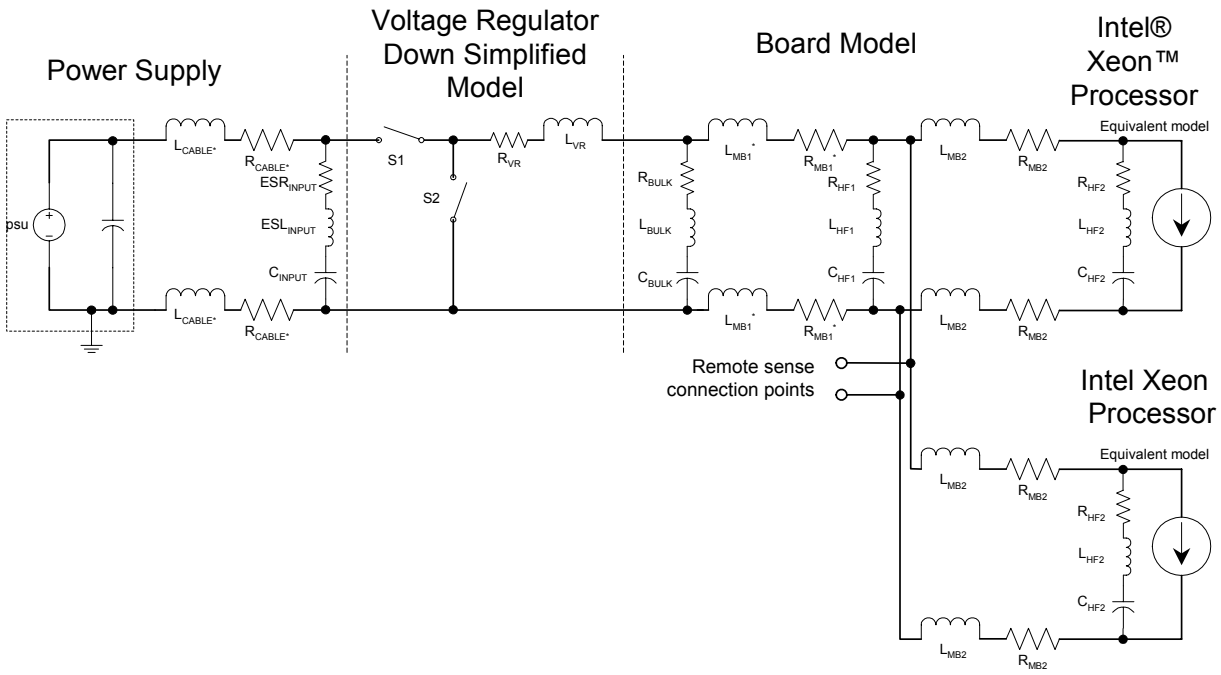

Figure 2 – Base VRD Electrical Delivery Model

Table 1 lists model parameters for the motherboard. These values are guidelines, which will vary according to board layout and component selection. The ultimate VRD and power distribution requirement is to meet the die-level Vcc specifications in the processor data sheet or EMTS.

Table 1– Intel® Xeon™ Processor Power Delivery Models

Supply	Motherboard Capacitance			Capacitor Inductance			Capacitor Resistance			Motherboard Inductance		Motherboard Resistance	
	C_{BULK} (µF)	C_{HF1} (µF)	C_{HF2} (µF)	L_{BULK} (pH)	L_{HF1} (pH)	L_{HF2} (pH)	R_{BULK} (mΩ)	R_{HF1} (mΩ)	R_{HF2} (mΩ)	L_{MB1} (pH)	L_{MB2} (pH)	R_{MB1} (mΩ)	R_{MB2} (mΩ)
V_{CC}	10008	352	264	172	68	90	0.667	1.25	0.833	12.7	60	0.03	0.29

Figure 3 is a simplified block diagram of a four-phase, interleaved VRD example.

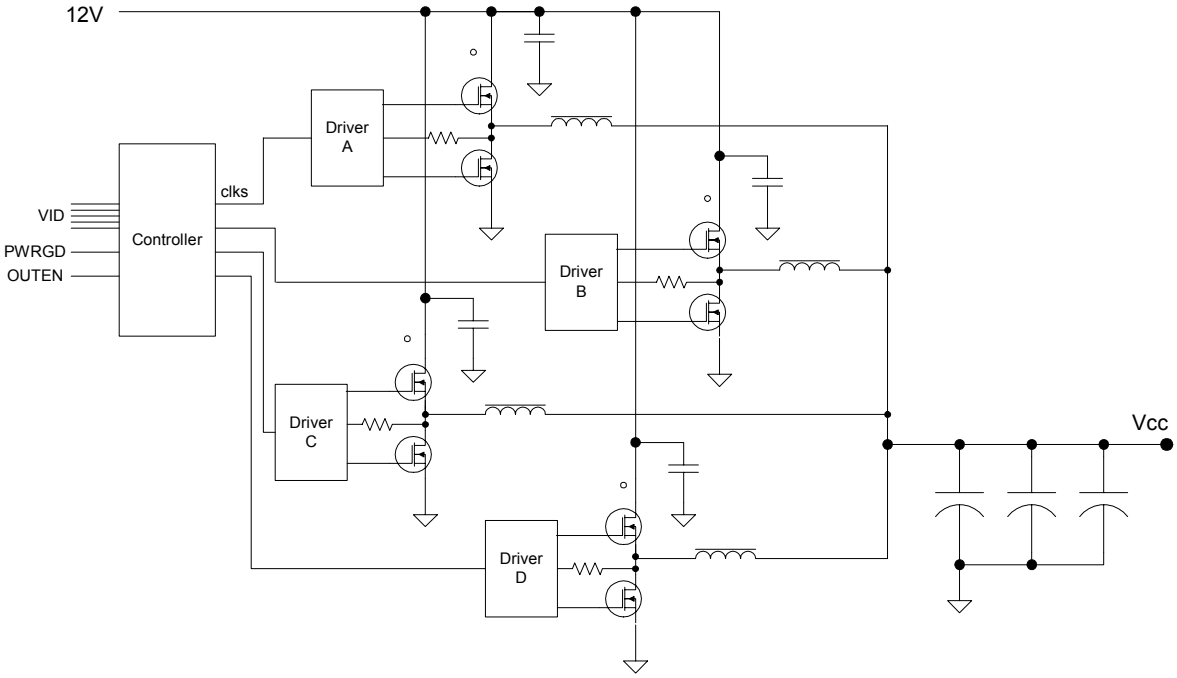

Figure 3 – Simplified VRD Circuit Example

2 Electrical Specifications

2.1 Output Requirements REQUIRED

2.1.1 Voltage and Current

The voltages and currents supplied by the VRD are shown in the following tables. Load-line specifications are specified at the processor socket pins. A five-bit voltage identification (VID) code described in Section 2.3.2 determines a reference VRD output voltage. The term "reference voltage" indicates that the VID provides a reference point for the voltage tolerance values provided in the Table 4. Due to voltage regulator tolerances and current draw variations, the average voltage seen at the processor may be slightly higher or lower than the reference value. However, VRD designers must meet the entire range of processor load and processor tolerance limits.

2.1.2 Voltage Tolerance

Failure to meet voltage tolerance specifications at the low end results in transistors' slowing down and the processor's not meeting timing specifications. Not meeting the specifications at the high end can cause damage or reduce the life of the processor.

Unlike many previous processors, the Intel Xeon processor and Low Voltage Intel Xeon processor specifications for V_{CC} and I_{CC} are interdependent. The VID definition is the absolute maximum Vcc allowed. Icc_{max} is measured at Vcc_{mid} which is defined as $[Vcc_{max} + Vcc_{min}]/2$. The VRD regulates the Vcc voltage to:

- Minimum voltage for two processors: $Vcc_{min} = 0.980 * VID – Icc * 0.475m\Omega$
- Maximum voltage for two processors: $Vcc_{max} = VID – Icc * 0.475m\Omega$

Note: These equations yield guideline voltages at the sense point. The voltage at the processor die must meet the values specified in the respective data sheet . The voltage measured at the sense point must be within the range shown in Figure 4 through Figure 9 and Table 2 and Table 3, except during input voltage turn-on and turn-off.

Voltage tolerance includes:

- Initial DC output voltage set-point error
- Component aging effects
- Output ripple and noise
- Full ambient temperature range and warm up
- Static operation
- Transient operation: dynamic output load changes from minimum-to-maximum or maximum-to-minimum loads, as measured over a 100 MHz bandwidth.

2.1.3 Output Voltage Measurements

The VRD output voltage is measured at the remote sense pins on the board: i.e., the "remote sense connection points" in Figure 2.

Transients should be measured across the remote sense pins on the board. Use an oscilloscope with 100MHz bandwidth, 1.5 pF maximum probe capacitance, and 1MΩ minimum impedance. The probe's maximum ground wire length should be less than 5mm. Ensure that external noise from the system is not coupled into the scope probe.

2.1.4 Single or Dual Processor Operation

Many OEMs require that a dual-processor VRD supplying a Intel Xeon processor's or Low Voltage Intel Xeon processor's common voltage plane operate with either one or two processors installed on the board: i.e., the design must meet the static and transient voltage characteristics of both the dual- and single-processor load lines. A solution is to adjust the load line for the number of installed processors. OEMs who want jumper-free systems can do this with logic that detects the presence of processors in each of the sockets and selects resistor combinations to produce the right slopes. For example: no processors (00) = disable VRD; one processor (01 or 10) = single-processor load line; both processors (11) = dual-processor load line.

2.1.5 No-Load Operation

The VRD should operate in a no-load condition: i.e., with no processor installed. The VRD does not need to meet the output regulation specifications described in section 2.1, but its output must not exceed 110% of the value of the maximum VID output voltage, and it must not trigger over-voltage fault detection circuitry.

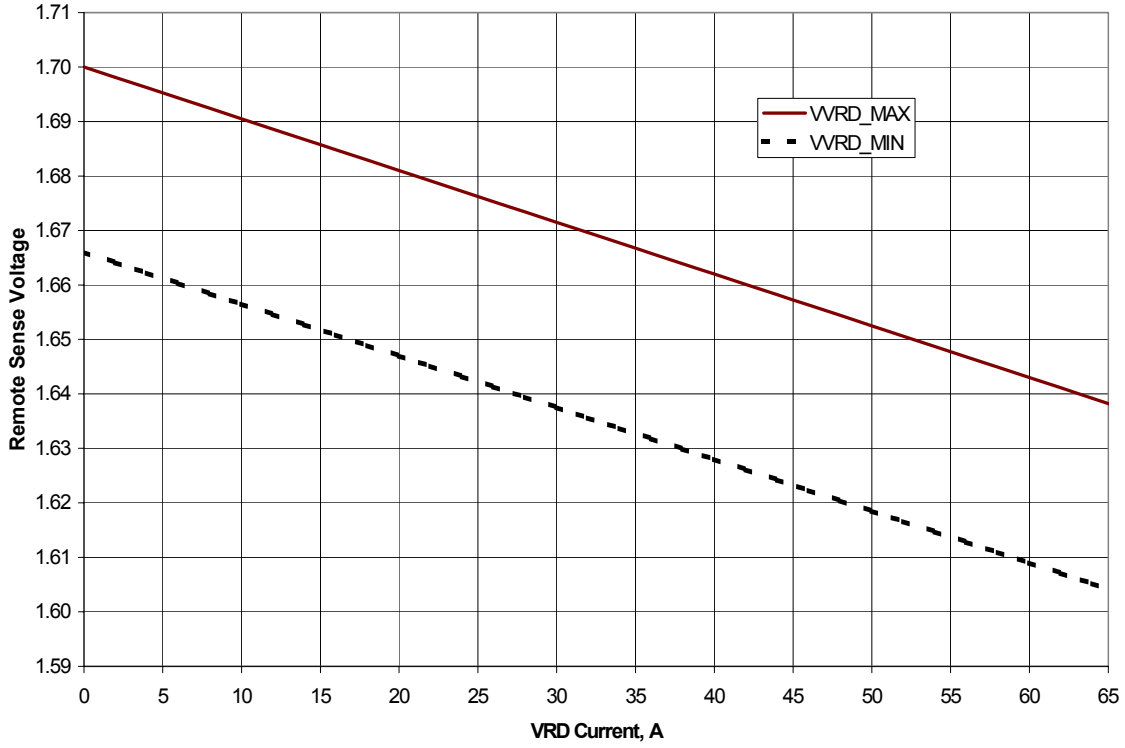

Figure 4 – Single (UP) Intel® Xeon™ Processor Voltage Regulation Limits

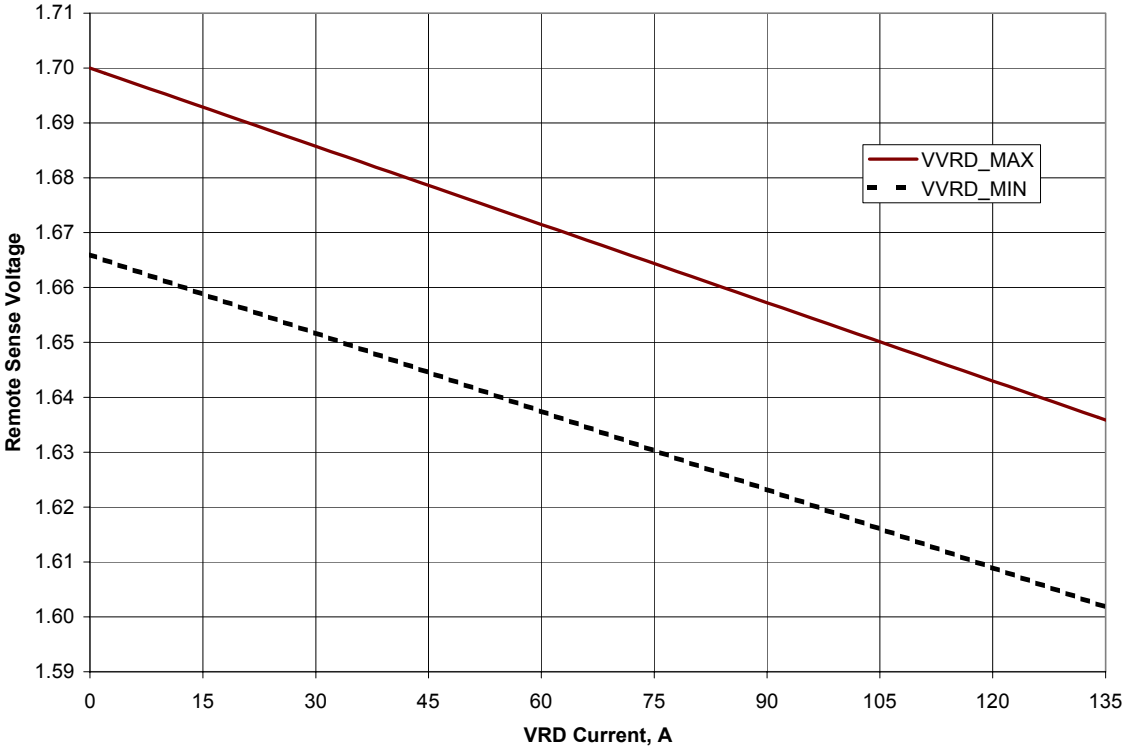

Figure 5 – Dual (DP) Intel® Xeon ™ Processor Voltage Regulation Limits

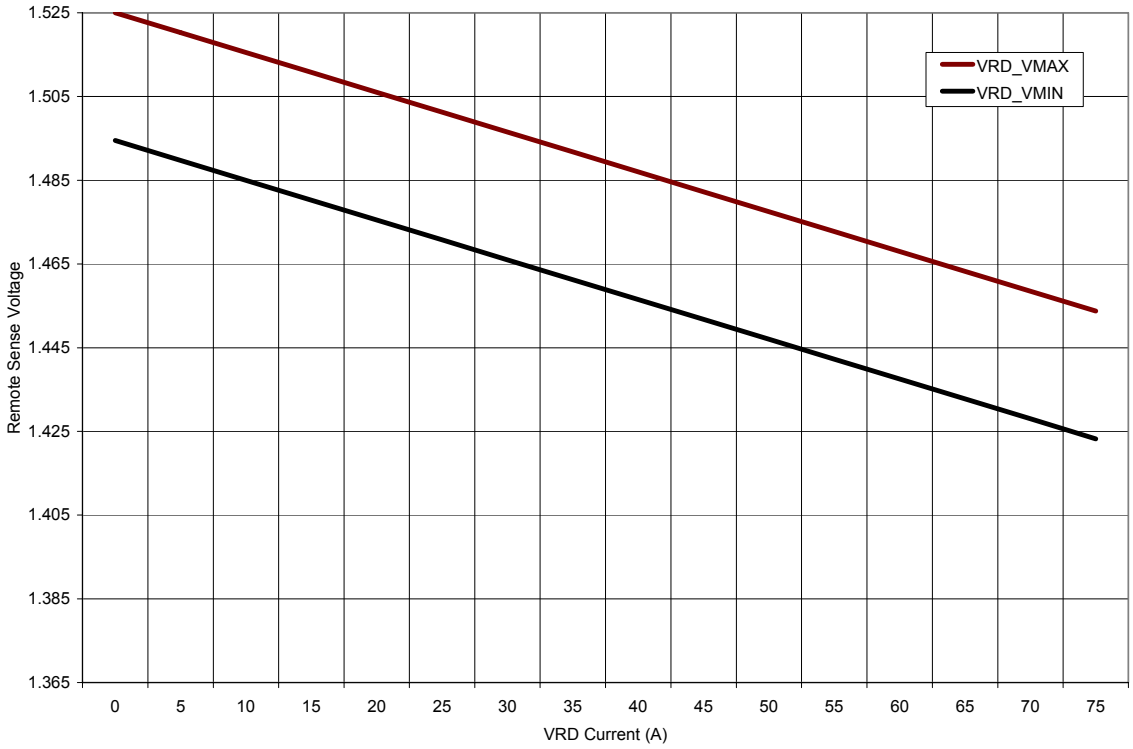

Figure 6- Single(UP) Intel® Xeon™ Processor with 512-KB L2 Cache Voltage Regulation Limits

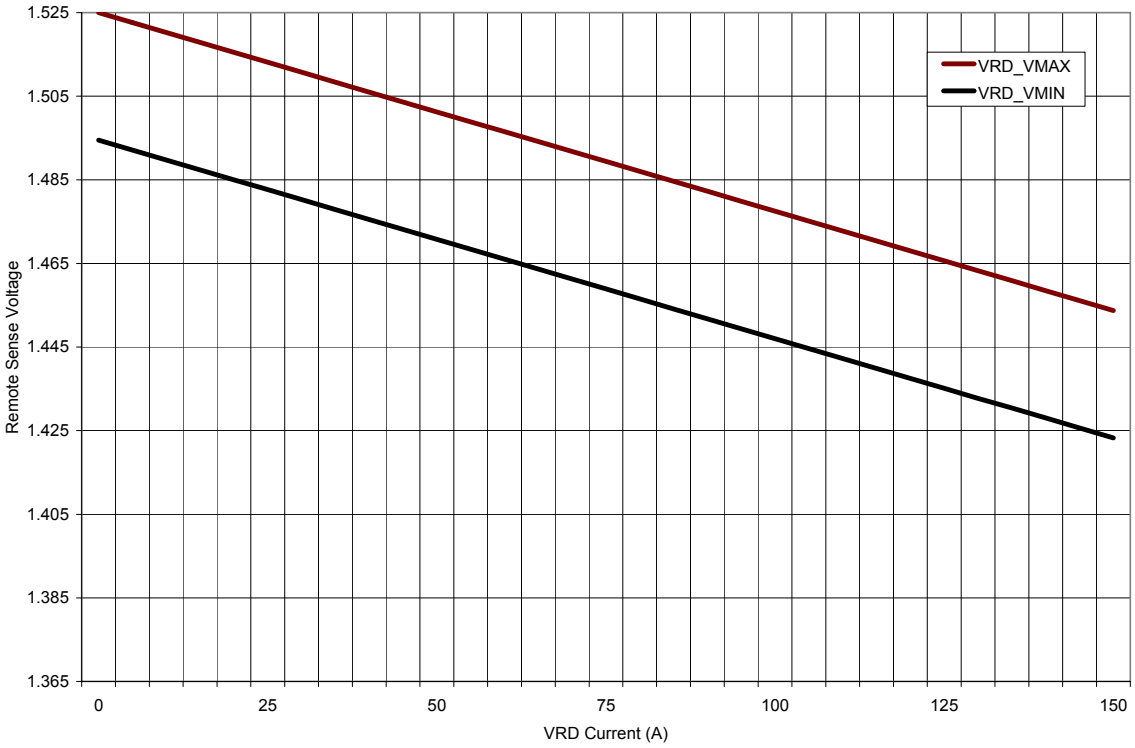

Figure 7 - Dual (DP) Intel® Xeon™ Processor with 512-KB L2 Cache Voltage Regulation Limits

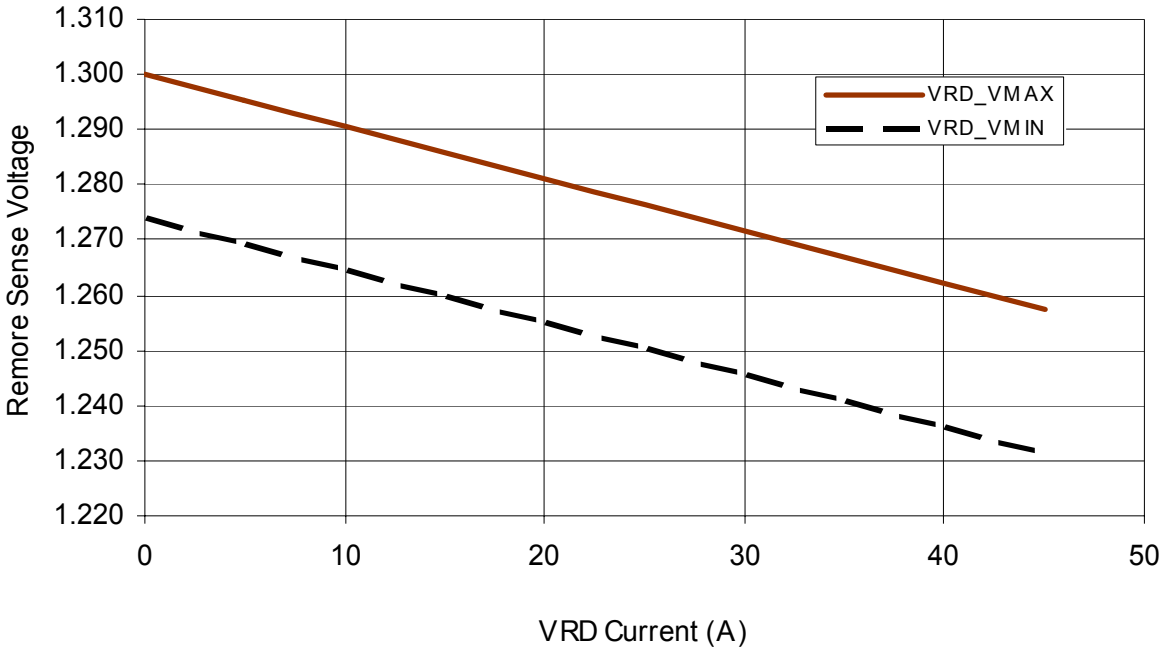

Figure 8 – Single (UP) Low Voltage Intel® Xeon™ Processor Voltage Regulation Limits

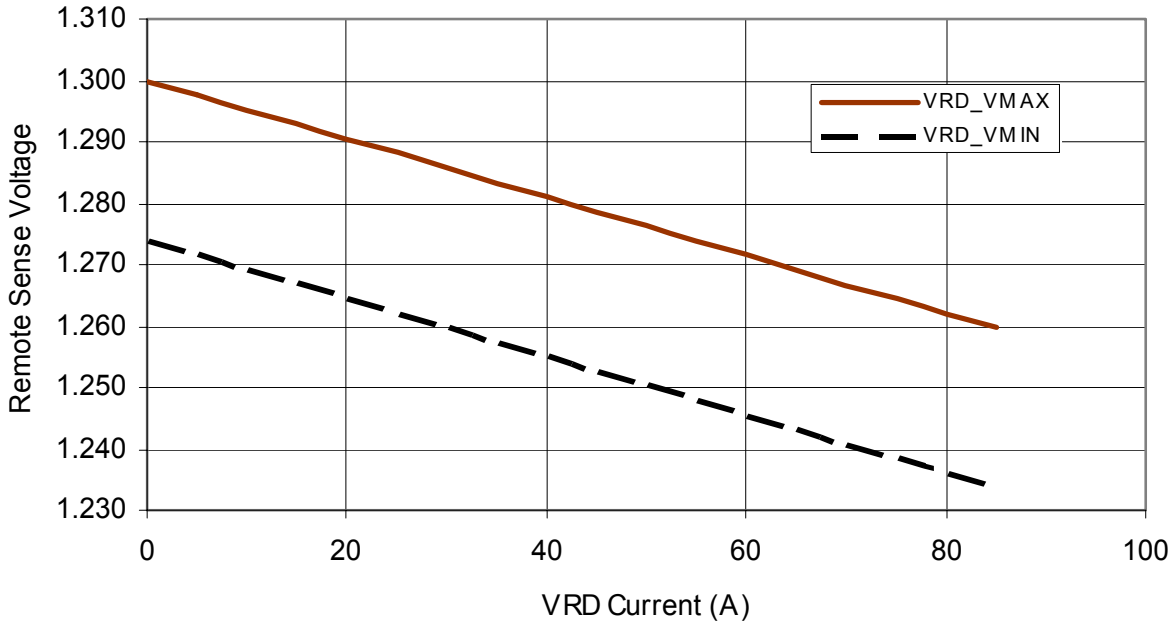

Figure 9 - Dual (DP) Low Voltage Intel® Xeon™ Processor Voltage Regulation Limits

Table 2 and Table 3 show the minimum and maximum allowable deviation against VID voltages specified in 4 for all load changes except turn-on and turn-off.

Table 2 – Intel® Xeon ™ Processor Voltage Deviations from VID

VRD Icc	UP Intel Xeon Processor Vcc		DP Intel Xeon Processor Vcc		UP Intel Xeon Processor with 512-KB L2 Cache Vcc		DP Intel Xeon Processor with 512-KB L2 Cache Vcc		UP Intel Xeon Processor with 512-KB L2 Cache Vcc		DP Intel Xeon Processor with 512- KB L2 Cache Vcc	
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min
0	1.700	1.666	1.700	1.666	1.500	1.470	1.500	1.470	1.525	1.495	1.525	1.495
5	1.695	1.661	1.698	1.664	1.495	1.465	1.498	1.468	1.520	1.490	1.523	1.492
10	1.691	1.657	1.695	1.661	1.491	1.461	1.495	1.465	1.516	1.485	1.520	1.490
15	1.686	1.652	1.693	1.659	1.486	1.456	1.493	1.463	1.511	1.480	1.518	1.487
20	1.681	1.647	1.691	1.657	1.481	1.451	1.491	1.461	1.506	1.476	1.516	1.485
25	1.676	1.642	1.688	1.654	1.476	1.446	1.488	1.458	1.501	1.471	1.513	1.483
30	1.672	1.638	1.686	1.652	1.472	1.442	1.486	1.456	1.497	1.466	1.511	1.480
35	1.667	1.633	1.683	1.649	1.467	1.437	1.483	1.453	1.492	1.461	1.508	1.478
40	1.662	1.628	1.681	1.647	1.462	1.432	1.481	1.451	1.487	1.457	1.506	1.476
45	1.657	1.623	1.679	1.645	1.457	1.427	1.479	1.449	1.482	1.452	1.504	1.473
50	1.653	1.619	1.676	1.642	1.453	1.423	1.476	1.446	1.478	1.447	1.501	1.471
55	1.648	1.614	1.674	1.640	1.448	1.418	1.474	1.444	1.473	1.442	1.499	1.468
60	1.643	1.609	1.672	1.638	1.443	1.413	1.472	1.442	1.468	1.438	1.497	1.466
65	1.638	1.604	1.669	1.635	1.438	1.408	1.469	1.439	1.463	1.433	1.494	1.464
70			1.667	1.633	1.434	1.404	1.467	1.437	1.459	1.428	1.492	1.461
75			1.664	1.630	1.429	1.399	1.464	1.434	1.454	1.423	1.489	1.459
80			1.662	1.628			1.462	1.432			1.487	1.457
85			1.660	1.626			1.460	1.430			1.485	1.454
90			1.657	1.623			1.457	1.427			1.482	1.452
95			1.655	1.621			1.455	1.425			1.480	1.449
100			1.653	1.619			1.453	1.423			1.478	1.447
105			1.650	1.616			1.450	1.420			1.475	1.445
110			1.648	1.614			1.448	1.418			1.473	1.442
115			1.645	1.611			1.445	1.415			1.470	1.440
120			1.643	1.609			1.443	1.413			1.468	1.438
125			1.641	1.607			1.441	1.411			1.466	1.435
130			1.638	1.604			1.438	1.408			1.463	1.433
135			1.636	1.602			1.436	1.406			1.461	1.430
140							1.434	1.404			1.459	1.428
145							1.431	1.401			1.456	1.426
150							1.429	1.399			1.454	1.423

Table 3 – Low Voltage Intel® Xeon ™ Processor Voltage Deviations from VID

VRD Icc	UP Low Voltage Intel Xeon Processor Vcc		DP Low Voltage Intel Xeon Processor Vcc	
	Max	Min	Max	Min
0	1.300	1.274	1.300	1.274
5	1.295	1.269	1.298	1.272
10	1.291	1.265	1.295	1.269
15	1.286	1.260	1.293	1.267
20	1.281	1.255	1.291	1.265
25	1.276	1.250	1.288	1.262
30	1.272	1.246	1.286	1.260
35	1.267	1.241	1.283	1.257
40	1.262	1.236	1.281	1.255
45	1.257	1.231	1.279	1.253
50			1.276	1.250
55			1.274	1.248
60			1.272	1.246
65			1.269	1.243
70			1.267	1.241
75			1.264	1.238
80			1.262	1.236
85			1.260	1.234

2.1.6 Turn-on Response Time

The output voltage should reach its specified range within 50 msec of the input power's reaching its minimum voltage.

2.1.7 Overshoot at Turn-On or Turn-Off

Overshoot upon the application or removal of the input voltage must be less than 2% above the nominal output voltage set by the Voltage Identification (VID) code. No negative voltage below –0.1V may be present at the output at any time.

2.1.8 Converter Stability

The VRD should be unconditionally stable under all output voltage ranges and current transients when developed against and incorporating the elements of the load model defined in Figure 2.

Stability requirements include a Thermal Monitor operating condition in which the processor core clocks may periodically stop to reduce its average power dissipation in response to a high-temperature condition. Figure 8 shows worst-case Thermal Monitor operation (maximum current in the ON state).

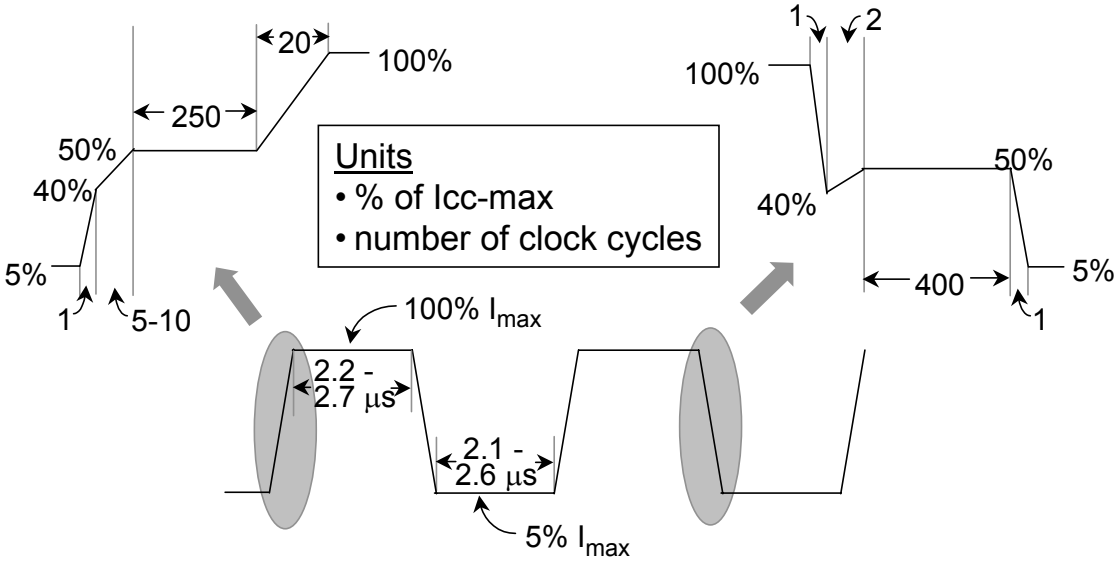

Figure 10 – Processor Current during Thermal Monitor Operation

Notes:
1. Duration of on-off periods depends on processor speed: higher frequency processors have shorter durations.
2. Other operating system-controlled events could have on-times as short as 700 cycles.
3. A possible worst-case routine could cause processor Icc to go through a 100% → 40% → 100% set of transitions within 30-50 core clock cycles.

2.2 Input Voltage and Current

2.2.1 Input Voltages

In order to minimize power distribution losses, the recommended main power source for the VRD is 12V +5%, -8%. This voltage is supplied by a conventional workstation or server power supply such as the SSI EPS-12V. The system designer should ensure that the input circuit of the VRD incorporates the necessary local bulk bypassing on the 12V rail.

2.2.2 Load Transient Effects on Input Current **EXPECTED**

When the VRD is providing an output current step to the load from $Iout_{MIN}$ to $Iout_{MAX}$ or $Iout_{MAX}$ to $Iout_{MIN}$ at the slew rate of 450A/µsec at the processor socket, the slew rate of the input current to the VR should not exceed 0.5A/µsec. The system board needs sufficient bulk decoupling to

ensure that the supply voltage on the system board does not go outside of regulation requirements during times of transient load on the VRD.

2.3 Control Inputs REQUIRED

2.3.1 Output Enable—(OUTEN)

The VR should accept an open-collector, open-drain, open-switch-to-ground, low-voltage TTL or low-voltage CMOS signal to enable the output. The input should have a pull-up resistor between 1 kΩ and 10 kΩ to 3.3V. The maximum low-input voltage is 0.8V; the minimum high-input voltage is 1.7V. When disabled, the VR should not sink or source current. When Output Enable is pulled low during the shutdown process, the VR should not exceed its previous voltage level regardless of the VID setting.

2.3.2 Voltage Identification—(VID[4:0])

The VR must accept five input lines to set the nominal voltage as defined by the table below. Five processor pins (VID[4:0]) will have either an open-ground combination (Intel Xeon Processor) or open-drain driver outputs (Intel Xeon Processor with 512 KByte L2 cache and Low Voltage Intel Xeon processor). When all five VID inputs are high (11111), such as when no processor is installed, the VR should disable its output.

The maximum low-input voltage is 0.8V; the minimum high-input voltage is 1.7V. Each VID input should have a 1 kΩ ± 10% pull-up resistor to 3.3V ± 5%. Board designers using other values should check them against data sheets for the VR components and the processor.

Table 4 – Voltage Identification (VID)

Processor Pins (0 = low, 1 = high)					Vcc	Processor Pins (0 = low, 1 = high)					Vcc
VID4	VID3	VID2	VID1	VID0	(VDC)	VID4	VID3	VID2	VID1	VID0	(VDC)
1	1	1	1	1	Off	0	1	1	1	1	1.475
1	1	1	1	0	1.1	0	1	1	1	0	1.5
1	1	1	0	1	1.125	0	1	1	0	1	1.525
1	1	1	0	0	1.15	0	1	1	0	0	1.55
1	1	0	1	1	1.175	0	1	0	1	1	1.575
1	1	0	1	0	1.2	0	1	0	1	0	1.6
1	1	0	0	1	1.225	0	1	0	0	1	1.625
1	1	0	0	0	1.250	0	1	0	0	0	1.65
1	0	1	1	1	1.275	0	0	1	1	1	1.675
1	0	1	1	0	1.3	0	0	1	1	0	1.7
1	0	1	0	1	1.325	0	0	1	0	1	1.725
1	0	1	0	0	1.35	0	0	1	0	0	1.75
1	0	0	1	1	1.375	0	0	0	1	1	1.775
1	0	0	1	0	1.4	0	0	0	1	0	1.8
1	0	0	0	1	1.425	0	0	0	0	1	1.825
1	0	0	0	0	1.45	0	0	0	0	0	1.85

2.4 Power Good Output (PWRGD) REQUIRED

The VRD should provide an open collector or equivalent Power Good signal consistent with TTL DC levels. This signal should transition to the open (>100kΩ) state within 10ms of the output voltage stabilizing within the range specified in Section 2.1.1. The signal should be in the

low-impedance (to ground) state whenever Vcc is outside of the required range below and be in the open state whenever Vcc is within its specified range, Section 2.1. On power up, the PWRGD signal must remain in the low-impedance state until the output voltage has stabilized within the required tolerance.

2.4.1 Power Good Threshold Voltages

The minimum voltage at which PWRGD is asserted should be the minimum Vcc specified in Section 2.1.2**,** minus margin to prevent false de-assertion, but at least 95% of (VID minus 125mV).

The maximum voltage at which PWRGD is asserted should be the VID set-point voltage, plus margin to prevent false de-assertion, but must be no greater than (VID plus 250 mV).

2.4.2 Power Good Operation

This PWRGD should be capable of sinking up to 4mA, while maintaining a voltage of 0.4V or lower. When the output is in the open state it should be capable of withstanding up to 5.5V. Latch-up or damage cannot occur if the pull-up voltage on the system board is present with no +12V input present.

VRD Power Good should remain low if the VRD is disabled by the Output Enable pin.

2.5 Intel Xeon Processor with 512-KB L2 Cache Power Sequencing

The Intel Xeon processor with 512-KB L2 cache's and Low Voltage Intel Xeon processor's VID outputs use an active driver (Section 2.3.2). A 3.3-volt source connected to the processor's SM_VCC pins supplies the VID output devices. As shown in Figure 11, the VID outputs will be valid within 10 milliseconds after the 3.3-volt supply reaches 95% of its nominal value. The system power supply should generate PWR_OK no less than 100 milliseconds after all of its outputs reach their respective 95% values. PWR_OK may be used to enable the VRD output. For example, a supply adhering to ATX12V design guidelines meets this requirement. The VRD's PWRGD output may be used to generate the PWRGOOD input to the processor. PWR_OK should be de-asserted when any output of the supply falls below 95% of its nominal value (also consistent with ATX12V). It is important to maintain SM_VCC anytime the output of the VRM is enabled. Driving The VRD's OUTEN control input with the PWR_OK signal will ensure correct sequencing at both power up and power down.

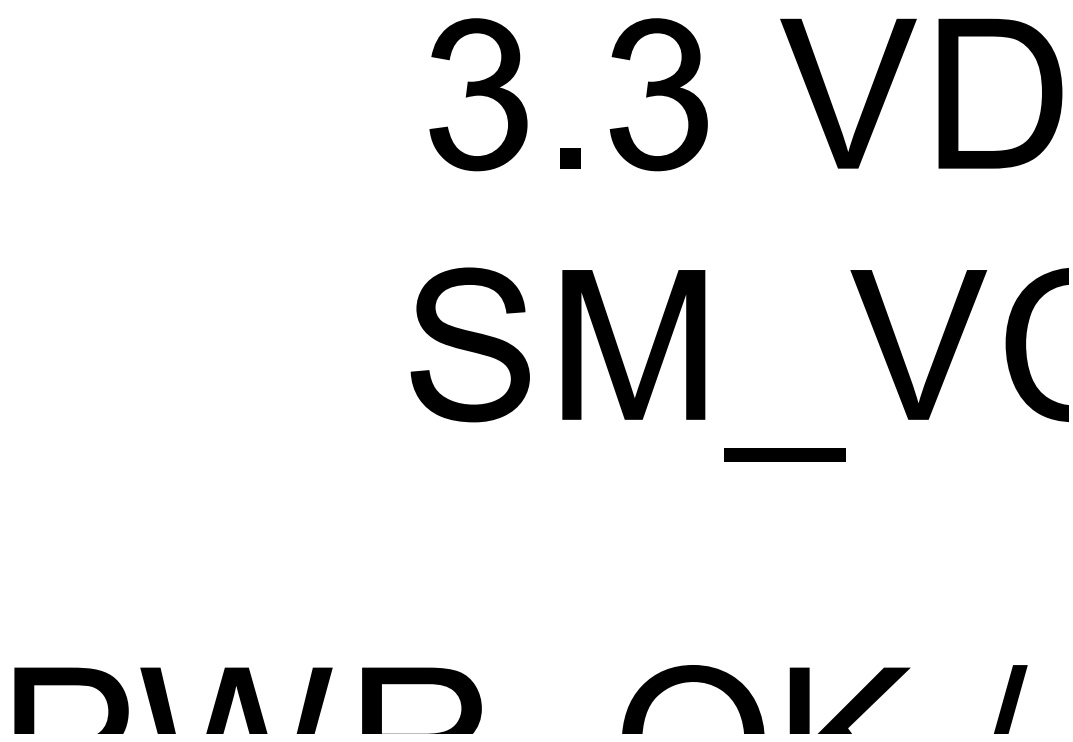

Figure 11 – Power-Up and Power-Down Timing

2.6 Efficiency PROPOSED

The efficiency of the VRD should be greater than 80% at maximum output current and across input voltage range. It should not dissipate more power under any load condition than it does at maximum output current and maximum input voltage.

2.7 Fault Protection PROPOSED

These are features built into the VRD to prevent damage to itself or the circuits it powers.

2.7.1 Over Voltage Protection

The VRD should provide over-voltage protection (OVP) by including a circuit, separate from the voltage sense path, capable of shutting off the output drive when the output voltage rises beyond Vtrip. If practical, the protection circuit should also enable a low-resistance path to ground such that if the output transistor shorts to input power the output voltage will not rise above Vtrip. A non-resetable or resetable fuse may be included in the input of the VR for this function. The response time should be such that the output voltage will not exceed (VID plus 250 mV).

Minimum Vtrip should be the Maximum Vcc specified in Section 2.1 to compensate for remote sense plus margin to prevent false trips. No combination of input voltage sequences should falsely trigger an OVP event.

2.7.2 Fuse Protection for Power Input

The power input (12V) should be protected with a fuse rated not greater than 30A, which sustains all operating and inrush conditions and which “blows” only on catastrophic failure of the converter.

2.7.3 Overload Protection

The VRD should be capable of withstanding a continuous, abnormally low resistance on the output without damage or over-stress to the unit. Output current under this condition will be limited to no more than 150% of the maximum rated output of the VRD. Latching off or hiccup mode is acceptable during over-current conditions. The VRD should be capable of starting into a constant current load of 50% of maximum rated load current with maximum load capacitance, as defined in Section 2.1, without tripping the OCP circuitry.

2.7.4 Reset After Shutdown

If the VRD goes into a shutdown state due to a fault condition on its output (not an internal failure) it should return to normal operation after the fault has been removed, or after the fault has been removed and power has been cycled off and on.

3 Design Considerations

Several voltage-regulation component manufacturers have developed reference dual Intel Xeon processor and Low Voltage Intel Xeon processor VRD designs. System designers are

encouraged to contact these companies and discuss applications of those circuit designs in their specific system board requirements.

3.1 Controller Tolerance

To maximize VRD voltage tolerance over load and temperature conditions, Intel recommends the use of controllers with Vref tolerances of ≤ 0.5% over temperature.

3.2 Power Plane

A single set of Vcc and Vss planes must deliver power to all processor sharing a system bus. Intel recommends 2-oz copper power planes for V_{CC} and V_{SS}. Each can be implemented on two 1-oz copper layers or four ½-oz copper layers.

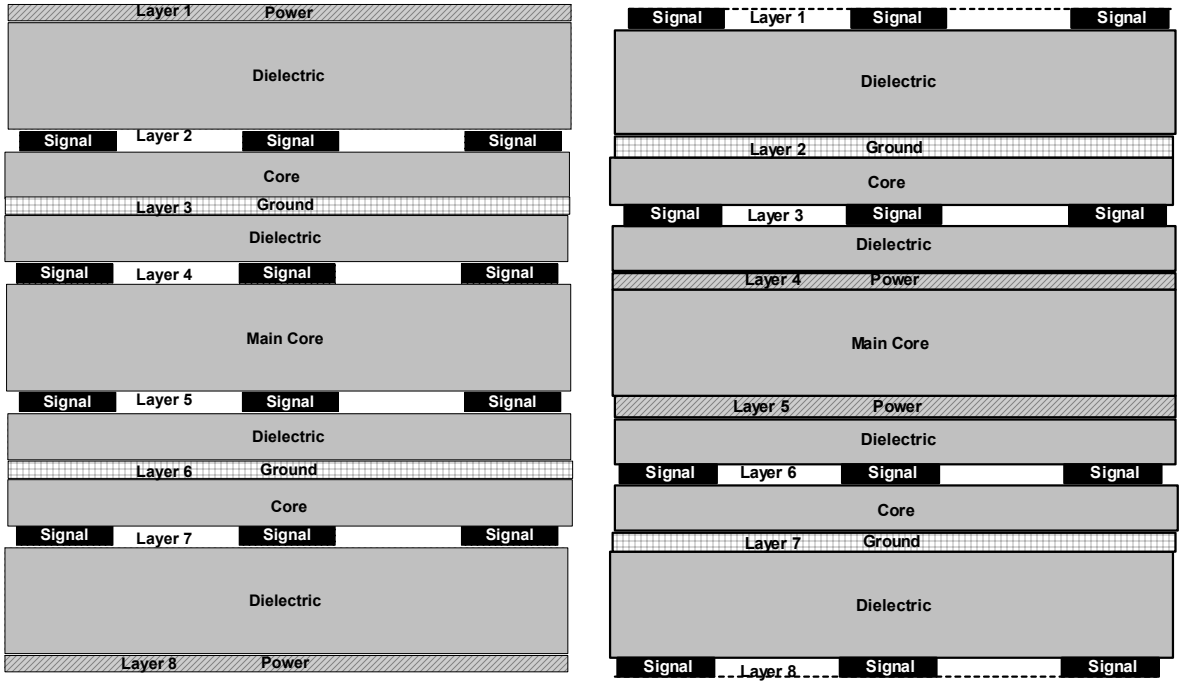

Figure 12 – Suggested Stack-ups for Dual Intel® Xeon™ Processor-Based Systems

3.3 Basic Layout

The Intel Xeon processor socket has 603 pins with 50 mil pitch. The routing of signals, power, and ground will require numerous vias through the power and ground planes beneath the processor, increasing the inductance of these planes. The layout of the VRD becomes important for keeping the PCB parasitics from affecting the performance of the design. These rules also apply to Intel Xeon processors and Low Voltage Intel Xeon processors in the 604-pin package

- All high-frequency capacitors should be located as close as possible to the socket. All components associated with the controller should be mounted as close as possible to the controller with minimal trace lengths. Figure 13 shows examples of two configurations of a VR and the two processors it supplies.
- The MOSFET drivers, MOSFETs, inductors, and input supply filter capacitors for each phase should be mounted as close as possible. These will be referred to as “phase drivers.”

- Each of the phase drivers should be somewhat equally spaced from the socket.
- The bulk capacitors should be mounted between the phase drivers and the socket, as close as possible to the socket. If the phase drivers are separated substantially from each other, the bulk capacitors should be divided up among them. Figure 14 details one example of phase driver and bulk capacitor placement.
- All Vcc and return trace lengths associated with the power supply delivery to the socket should be as short as possible, as wide as possible, and multi-layered with interleaved layers, to minimize the trace resistance and inductance.
- Each processor's 603 vias (and associated antipads) create a "Swiss cheese" effect in the V_{CC} power plane underneath the processor. To maximize the copper going to each processor (thus improving power distribution), the minimum manufacturable antipad should be used for the processor's 603 vias.

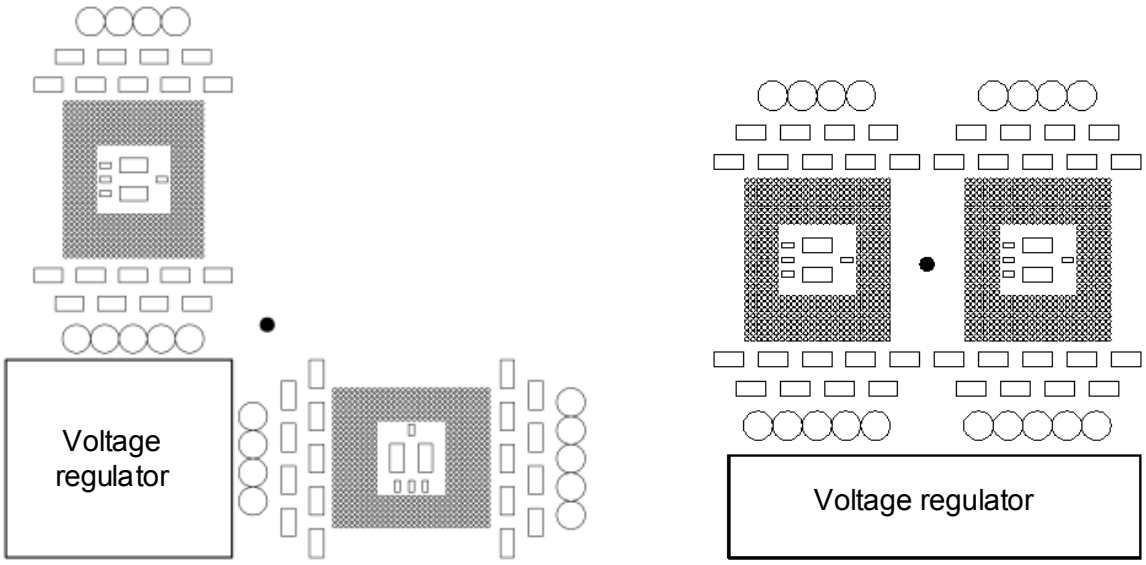

Figure 13 – Dual-Processor VRD Layout Examples

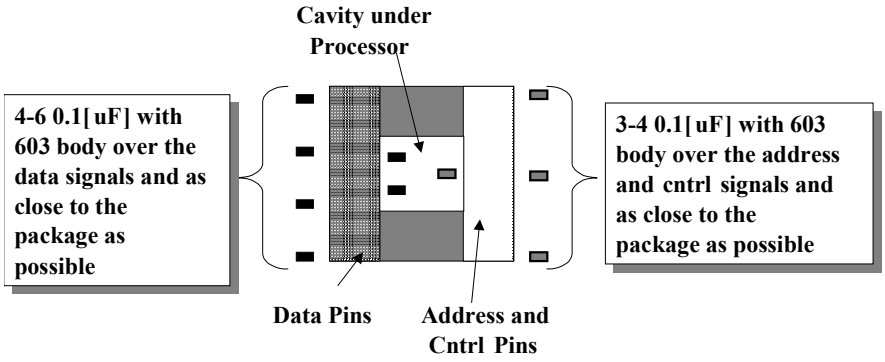

Figure 14 – Capacitor Placement

3.4 Thermal Management

The power output capability of the VRD demands careful thermal management. The controller and gate drivers, although they will have thermal losses, will generally not require any special

considerations. The main components requiring attention during the design process are the high- and low-side MOSFETs and output inductor. A thermal analysis on a per phase basis will show the main contributors to the losses.