# Intel® Xeon™ Processor with 512 KB L2 Cache System Compatibility Guidelines

Order Number: 298645-001

January 2002

Information in this document is provided in connection with Intel products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Intel's Terms and Conditions of Sale for such products, Intel assumes no liability whatsoever, and Intel disclaims any express or implied warranty, relating to sale and/or use of Intel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. Intel products are not intended for use in medical, life saving, or life sustaining applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

This document contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local sales office that you have the latest datasheet before finalizing a design.

The Intel® Xeon™ processor may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an order number and are referenced in this document, or other Intel literature, may be obtained by calling 1-800-548-4725, or by visiting Intel's website at http://www.intel.com.

Intel, Intel logo, Pentium, Intel NetBurst, and Intel Xeon are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

* Other names and brands may be claimed as the property of others.

Copyright © Intel Corporation 2002.

# Table of Contents

# 1.0 Revision History

| Revision | Date | Changes |
|---|---|---|
| -001 | January 2002 | Initial Release |

# 2.0 Introduction

This document describes the required changes to Intel® Xeon™ processor-based platforms in order to provide Intel® Xeon™ processor with 512 KB L2 cache compatibility. The information in this document should be used in conjunction with specifications presented in the latest version of the *Intel® Xeon™ Processor with 512 KB L2 Cache at 1.80 GHz, 2 GHz, and 2.20 GHz* Datasheet and *Intel® Xeon™ Processor at 1.40 GHz, 1.50 GHz, 1.70 GHz and 2 GHz* Datasheet, as well as information provided in other processor related design guides listed in the References section below. Design decisions should always be based on information contained in the latest applicable processor datasheet. For proper and reliable processor operation, the designer must ensure that the requirements in this guideline are fully satisfied.

## 2.1 Audience

This document is targeted at the following audience:

- Intel Xeon processor-based system developers who want to ensure system compatibility with the Intel Xeon processor with 512 KB L2 cache.

## 2.2 References

Material and concepts available in the following documents may be beneficial when reading this document:

- *Intel® Xeon™ Processor with 512 KB L2 Cache at 1.80 GHz, 2 GHz, and 2.20 GHz* Datasheet
- *Intel® Xeon™ Processor at 1.40 GHz, 1.50 GHz, 1.70 GHz and 2 GHz* Datasheet
- *Intel® Xeon™ Processor and Intel® 860 Chipset Platform Design Guidelines*
- *VRM 9.0 DC-DC Converter Design Guidelines*
- *VRM 9.1 DC-DC Converter Design Guidelines*
- *Dual Intel® Xeon™ Processor Voltage Regulator Down (VRD) Design Guidelines*
- *Intel® Xeon™ Processor Thermal Design Guidelines*
- *ATX/ATX12V Power Supply Design Guide* (available at http://www.formfactors.org)
- *MPS Power Supply: A Server System Infrastructure (SSI) Specification For Midrange Chassis Power Supplies* (available at http://www.ssiforum.org)

# 3.0 Compatibility

Implementing the changes outlined in this document will help assure that an Intel® Xeon™ processor-based system design will be compatible with the Intel Xeon processor with 512 KB L2 cache. Compatibility is likely to be ultimately limited by the ability of the system to supply the required current and to adequately cool the processor.

# 4.0 SM_VCC

SM_VCC must be connected to the system 3.3 volt power supply since the Intel® Xeon™ processor with 512 KB L2 cache drives the voltage identification (VID) outputs using core circuitry powered by the SM_VCC supply.

Refer to Section 6.0 for further considerations involving the power sequencing requirements of SM_VCC

# 5.0 603-Pin Socket Pin Definition Changes

The Intel® Xeon™ processor with 512 KB L2 cache is mechanically and electrically compatible with the same 603-pin socket used for the Intel Xeon processor. However, in order to support the increased frequencies offered by the Intel Xeon processor with 512 KB L2 cache, "Reserved" and "N.C." pins from the original Intel Xeon processor pin definition have been designated as either $V_{CC}$ or $V_{SS}$. Intel Xeon processor-based platforms need to redefine the 603-pin socket pin map as listed in the “New Name” column of Table 1 to allow compatibility with the Intel Xeon processor with 512 KB L2 cache.

**Table 1. 603-Pin Socket Pin-Map Change**

| Pin | Old Name | New Name | Comment |
|---|---|---|---|
| A30 | RSVD | $V_{CC}$ | Processor Power |
| A31 | RSVD | $V_{SS}$ | Processor Ground |
| B4 | RSVD | $V_{CC}$ | Processor Power |
| B30 | RSVD | $V_{SS}$ | Processor Ground |
| B31 | RSVD | $V_{CC}$ | Processor Power |
| C1 | RSVD | $V_{SS}$ | Processor Ground |
| C30 | RSVD | $V_{CC}$ | Processor Power |
| C31 | RSVD | $V_{SS}$ | Processor Ground |
| D1 | RSVD | $V_{CC}$ | Processor Power |
| D30 | RSVD | $V_{SS}$ | Processor Ground |

**Table 1. 603-Pin Socket Pin-Map Change**

| Pin | Old Name | New Name | Comment |
|---|---|---|---|
| D31 | RSVD | $V_{CC}$ | Processor Power |
| E1 | RSVD | $V_{SS}$ | Processor Ground |
| E30 | RSVD | $V_{CC}$ | Processor Power |
| E31 | RSVD | $V_{SS}$ | Processor Ground |
| F1 | RSVD | $V_{CC}$ | Processor Power |
| F30 | RSVD | $V_{SS}$ | Processor Ground |
| F31 | RSVD | $V_{CC}$ | Processor Power |
| G1 | RSVD | $V_{SS}$ | Processor Ground |
| G30 | RSVD | $V_{CC}$ | Processor Power |
| G31 | RSVD | $V_{SS}$ | Processor Ground |
| H1 | RSVD | $V_{CC}$ | Processor Power |
| H30 | RSVD | $V_{SS}$ | Processor Ground |
| H31 | RSVD | $V_{CC}$ | Processor Power |
| J1 | RSVD | $V_{SS}$ | Processor Ground |
| J30 | RSVD | $V_{CC}$ | Processor Power |
| J31 | RSVD | $V_{SS}$ | Processor Ground |
| K1 | RSVD | $V_{CC}$ | Processor Power |
| K30 | RSVD | $V_{SS}$ | Processor Ground |
| K31 | RSVD | $V_{CC}$ | Processor Power |
| L1 | RSVD | $V_{SS}$ | Processor Ground |
| L30 | RSVD | $V_{CC}$ | Processor Power |
| L31 | RSVD | $V_{SS}$ | Processor Ground |
| M1 | RSVD | $V_{CC}$ | Processor Power |
| M30 | RSVD | $V_{SS}$ | Processor Ground |
| M31 | RSVD | $V_{CC}$ | Processor Power |
| N1 | RSVD | $V_{CC}$ | Processor Power |
| N30 | RSVD | $V_{SS}$ | Processor Ground |
| N31 | RSVD | $V_{CC}$ | Processor Power |
| P1 | RSVD | $V_{SS}$ | Processor Ground |
| P30 | RSVD | $V_{CC}$ | Processor Power |
| P31 | RSVD | $V_{SS}$ | Processor Ground |
| R1 | RSVD | $V_{CC}$ | Processor Power |
| R30 | RSVD | $V_{SS}$ | Processor Ground |
| R31 | RSVD | $V_{CC}$ | Processor Power |
| T1 | RSVD | $V_{SS}$ | Processor Ground |
| T30 | RSVD | $V_{CC}$ | Processor Power |
| T31 | RSVD | $V_{SS}$ | Processor Ground |
| U1 | RSVD | $V_{CC}$ | Processor Power |

**Table 1. 603-Pin Socket Pin-Map Change**

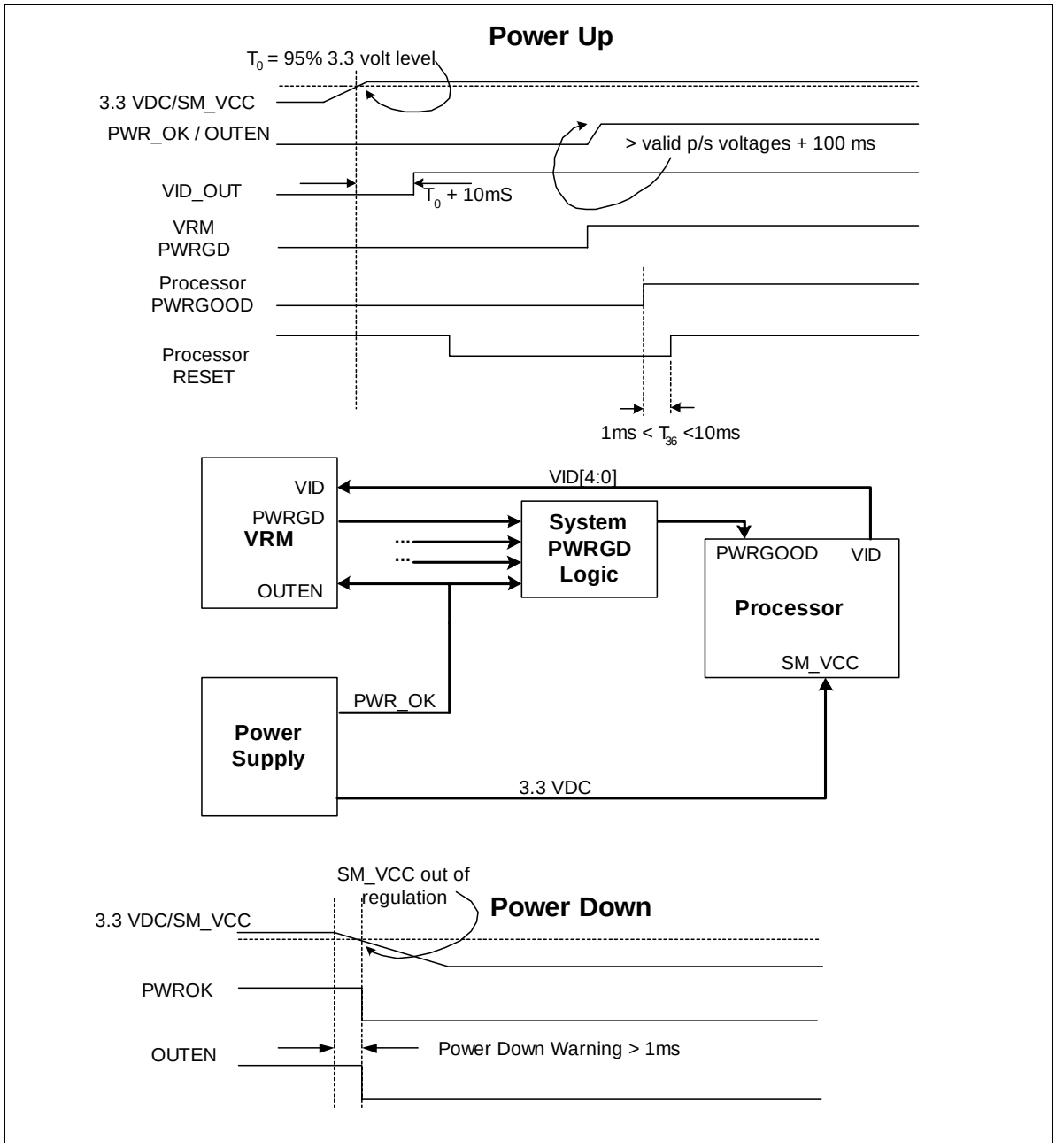
| Pin | Old Name | New Name | Comment |
|---|---|---|---|
| U30 | RSVD | $V_{SS}$ | Processor Ground |
| U31 | RSVD | $V_{CC}$ | Processor Power |
| V1 | RSVD | $V_{SS}$ | Processor Ground |
| V30 | RSVD | $V_{CC}$ | Processor Power |
| V31 | RSVD | $V_{SS}$ | Processor Ground |
| W1 | RSVD | $V_{CC}$ | Processor Power |
| W30 | RSVD | $V_{SS}$ | Processor Ground |
| W31 | RSVD | $V_{CC}$ | Processor Power |
| Y1 | RSVD | $V_{SS}$ | Processor Ground |
| Y30 | RSVD | $V_{CC}$ | Processor Power |
| Y31 | RSVD | $V_{SS}$ | Processor Ground |
| AA1 | RSVD | $V_{CC}$ | Processor Power |
| AA30 | RSVD | $V_{SS}$ | Processor Ground |
| AA31 | RSVD | $V_{CC}$ | Processor Power |
| AB1 | RSVD | $V_{SS}$ | Processor Ground |
| AB30 | RSVD | $V_{CC}$ | Processor Power |
| AB31 | RSVD | $V_{SS}$ | Processor Ground |
| AC30 | RSVD | $V_{SS}$ | Processor Ground |
| AC31 | RSVD | $V_{CC}$ | Processor Power |
| AD30 | RSVD | $V_{CC}$ | Processor Power |
| AD31 | RSVD | $V_{SS}$ | Processor Ground |

# 6.0 $V_{CC}$ Power Sequencing

As outlined in Section 4.0, a 3.3 volt power supply must be connected to the Intel® Xeon™ processor with 512 KB L2 cache SM_VCC pins (AE28 & AE29). SM_VCC is the supply voltage used for the SMBus functions and for the VID output signal circuits. The VID signals are programmed by Intel during the manufacturing process so that the VRM output voltage will be set correctly. As indicated in Figure 1, the VID outputs will be valid within 10 milliseconds after the time at which the 3.3 volt supply reaches 95% of its nominal value. For a power supply that adheres to the ATX12V power supply design guidelines, PWR_OK will be generated no less than 100 milliseconds after all of its outputs reach their respective 95% values (please refer to the document *ATX/ATX12V Power Supply Design Guide*). Similarly, for a power supply that adheres to the Server System Infrastructure (SSI) power supply specification, PWR_OK will be generated no less than 100 milliseconds after all of its outputs are within their respective regulation limits (please refer to the document *MPS Power Supply: A Server System Infrastructure (SSI) Specification For Midrange Chassis Power Supplies*). PWR_OK may be used to enable the output of the VRM ($V_{CC}$) using the OUTEN signal. The VRM PWRGD output, in conjunction with the rest of the system's powergood logic, may be used to generate the

PWRGOOD input to the processor. PWR_OK will be deasserted when any output of an ATX12V-compliant or SSI-compliant power supply falls below regulation limits. It is important to maintain SM_VCC at any time the output of the VRM is enabled. Driving the VRM's OUTEN with the PWR_OK signal will ensure correct sequencing at both power up and power down.

**Figure 1. Voltage Sequence Timing Requirements**



# 7.0 Power and Signal Levels

The VID for the Intel® Xeon™ processor with 512 KB L2 cache is 1.500 volts compared to a VID level of 1.700 volts for the Intel Xeon processor. The Intel Xeon processor with 512 KB L2 cache still uses a single core voltage supply ($V_{CC}$) to supply the termination voltage ($V_{TT}$). Table 2 outlines changes to the way AGTL+ signal level specifications are defined for the Intel Xeon processor with 512 KB L2 cache. The Intel Xeon processor with 512 KB L2 cache defines the $V_{IH}$ and $V_{IL}$ specifications based on a percentage of the GTLREF level instead of a fixed voltage offset level. In Table 2, use a value of GTLREF = 2/3*$V_{CC}$ for both processors. It is important to simulate the system bus to ensure that these levels are met. Other bus electrical characteristics are expected to be compatible with the Intel® Xeon™ processor specifications. Refer to the processor datasheets given in Section 2.2 for complete details regarding all processor specifications referenced in this section.

**Table 2. AGTL+ Signal Changes**

| Symbol | Intel® Xeon™ Processor | Intel® Xeon™ Processor with 512 KB L2 Cache |
|---|---|---|
| $V_{IL}$ Max | GTLREF - 0.100 | 0.90*GTLREF |
| $V_{IH}$ Min | GTLREF + 0.100 | 1.10*GTLREF |

**NOTE:** These values are for reference only. The latest processor datasheet contains the actual specifications for the processor. If the specifications in this table conflict with the specifications found in the datasheet, the datasheet supersedes.

# 8.0 VRM 9.0 and VRM 9.1

Voltage regulator designs for Intel® Xeon™ processor-based platforms were initially based on Intel's *VRM 9.0 DC-DC Converter Design Guidelines*. However, to provide additional VRM high current capability for new platforms, Intel created an updated voltage regulator design guide entitled *VRM 9.1 DC-DC Converter Design Guidelines*. Intel Xeon processor platforms intending to support the Intel Xeon processor with 512 KB L2 cache are not required to upgrade to VRM 9.1 and may continue to use VRM 9.0 voltage regulator solutions. However, new platforms should consider implementing VRM 9.1 since it provides the most recent voltage regulator design guidelines for the Intel Xeon processor with 512 KB L2 cache.

# 9.0 Core Frequency to System Bus Ratio Determination

The core frequency to system bus ratio for the Intel® Xeon™ processor is configured by driving the ratio select signals (LINT[1]/NMI, A20M#, IGNNE#, and LINT[0]/INTR) with appropriate ratio encoding values during processor power-on reset. The Intel Xeon processor with 512 KB L2 cache implements a new method for setting the core frequency to system bus ratio and will ignore the ratio select signals at power-on reset. The Intel

Xeon processor with 512 KB L2 cache operates at its tested frequency at initial power-on. If the processor needs to run at a lower core frequency, as must be done when a higher speed processor is added to a system that contains a lower frequency processor, the system BIOS is able to effect the change in the core to system bus ratio.