Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 10.2

Design Guidelines

March 2005

Document Number: 306760-001

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Revision History

Document Number	Revision Number	Description	Date
306760	001	• InitIal release of this document	March 2005

NOTE: Not all revisions may be published.

Guideline Categories	
REQUIRED:	An essential part of the design – necessary to meet processor voltage and current specifications and follow processor layout guidelines.
EXPECTED:	Part of Intel's processor power definitions; necessary for consistency among the designs of many systems and power devices. May be specified or expanded by system OEMs.
PROPOSED:	Normally met by this type of DC-to-DC converter and, therefore, included as a design target. May be specified or expanded by system OEMs.

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1 Applications

1.1 Introduction and Terminology

This document defines DC-to-DC converters to meet the power requirements of computer systems using 64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache, 64-bit Intel® Xeon™ processor MP with 1MB L2 cache processors. Requirements will vary according to the needs of different computer systems and processors that a specific voltage regulator is expected to support.

The intent of this document is to define electrical, thermal and mechanical specifications for VRM10.2.

VRM – The voltage regulator module (VRM) designation in this document refers to a voltage regulator that is plugged into a baseboard, where the baseboard is designed to support more than one processor. VRM output requirements in this document are intended to match the needs of a set of microprocessors.

EVRD – The Enterprise Voltage Regulator-Down (EVRD) designation in this document refers to a voltage regulator that is embedded on a baseboard. The EVRD output requirements in this document are intended to match the needs of a set of microprocessors. Each implementation of a specific board must meet the specifications of all processors supported by the board.

'1' – In this document refers to a high voltage level (V_{OH} and V_{IH}).

'0' – In this document refers to a low voltage level (V_{OL} and V_{IL})

'#' – Symbol after a signal name in this document refers to an active low signal, indicating that a signal is in the asserted state when driven to a low level.

The specifications in the respective processor's datasheet always take precedence over the data provided in this document.

VRM/EVRD 10.2 incorporates functional changes from prior EVRD and VRM guidelines:

- Continuous load core current (Icc_{TDC}) (thermal design current) has been increased to 130A (Section 2.1).
- Maximum core current (Icc_{MAX}) has been increased to 150A peak.
- Maximum current slew rate has been increased to 1200 A/µs.

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2 Output Voltage Requirements

2.1 Voltage and Current - REQUIRED

There will be independent selectable voltage identification (VID) codes for the core voltage regulator. The regulator's 6-bit code (VID) will be provided by the processor to the VRM/EVRDs, which will determine a reference output voltage, as described in Section 3.2. Section 2.2 and Section 2.3 specify deviations from the VID reference voltage.

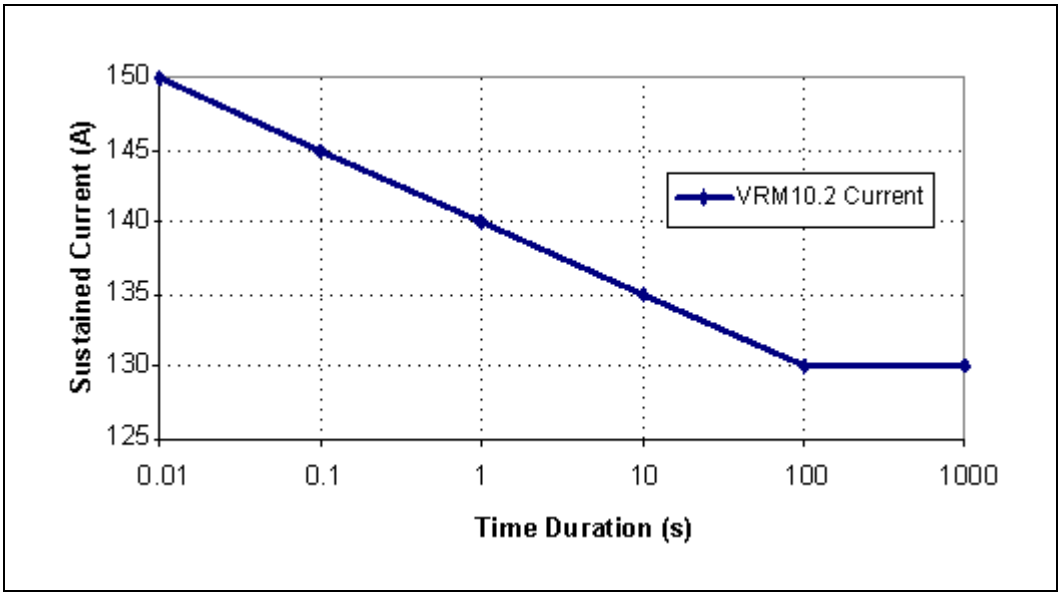
The load line tolerance in Section 2.2 shows the relationship between Vcc and Icc for the processor.

The VRM/EVRD is required to support the following:

- A maximum continuous load current (Icc_{TDC}) of 130A.
- A maximum load current (Icc_{MAX}) of 150A peak.
- A maximum load current step (Icc_{STEP}), within a 1 µs period, of 100A.
- A maximum current slew rate (dIcc/dt) of 1200 A/µs at the pins of the processor (refer to Table 2-2 for more information).

Figure 2-1displays the load current over time.

Figure 2-1. VRM/EVRD 10.2 Load Current vs. Time



NOTE: Voltage regulator thermal protection circuitry should not trip for load currents greater than Icc_{TDC}

The continuous load current can also be referred to as the Thermal Design Current (TDC). TDC is the sustained (DC equivalent) current that the processor is capable of drawing indefinitely and defines the current to use for the voltage regulator temperature assessment. At TDC, switching FETs reach maximum allowed temperature and may heat the baseboard layers and neighboring components. The envelope of the system operating conditions establishes actual component and

baseboard temperatures. This includes voltage regulator layout, processor fan selection, ambient temperature, chassis configuration, etc. To avoid heat related failures, baseboards should be validated for thermal compliance under the envelope of system operating conditions. It is proposed that the voltage regulator thermal protection be implemented for all designs (Section 6.2).

The maximum load current represents the maximum peak current that the processor is capable of drawing. It is the maximum current the VRM/EVRD must be electrically designed to support without tripping any protection circuitry.

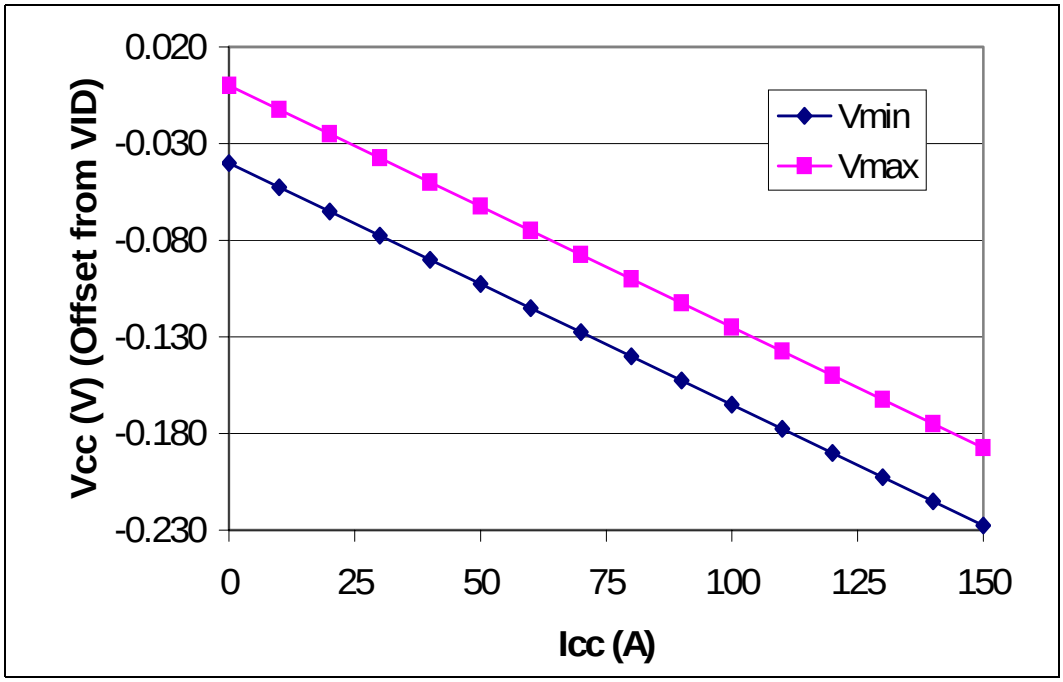
2.2 Load Line Definitions - REQUIRED

The following load line contains static and transient voltage regulation data as well as maximum and minimum voltage levels. It is recommended that the regulator's differential remote sense point for the processor's voltage regulator be located at the center of the processor's socket cavity.

The upper and lower load lines represent the allowable range of voltages that must be presented to the processor. The voltage must never exceed these boundaries for proper operation of the processor.

Figure 2-2 shows the load line voltage offsets and current levels based on the VID specifications for the core regulator.

Figure 2-2. VRM/EVRD 10.2 Socket Load Line



The encoding in Table 2-1 for the load lines is valid for the range of load current from 0 A to 150 A. The Load Line 0 (LL0) and Load Line 1 (LL1) control signals from Section 3.4, form a 2-bit load line selection and will be used to configure the Vcc VRM/EVRD to supply the proper load lines for the processors. For implementation of LL0 and LL1 on the baseboard refer to the appropriate platform design guidelines.

Table 2-1. LL0, LL1 Codes

LL0	LL1	Processor			
0	0	Reserved			
0	1	64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache, 64-bit Intel® Xeon™ processor MP with 1MB L2 cache and mPGA604 Die Load Line			
1	0	Reserved			
1	1	Reserved			
LL0	**LL1**	**Vcc Tolerance / Load Line**		**Units**	**Notes**
0	0	Vcc_{MAX} =	Reserved	V	
		Vcc_{MIN} =	Reserved		
0	1	Vcc_{MAX} =	VID (V) – 1.25 m • Icc (A)	V	64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache and 64-bit Intel® Xeon™ processor MP with 1MB L2 cache
		Vcc_{MIN} =	VID (V) – 1.25 m • Icc (A) – 40 mV		
1	0	Vcc_{MAX} =	Reserved	V	
		Vcc_{MIN} =	Reserved		
1	1	Vcc_{MAX} =	Reserved	V	
		Vcc_{MIN} =	Reserved		

2.3 Voltage Tolerance - REQUIRED

The voltage ranges shown in Section 2.2 include the following tolerances:

- Initial DC output voltage set-point error.
- Output ripple and noise.
- No-load offset centering error.
- Current sensing and droop errors.
- Component aging effects.
- Full ambient temperature range and warm up.
- Dynamic output changes from minimum-to-maximum and maximum-to-minimum load should be measured at the point of regulation (recommended to be at the center of the processor socket) using an oscilloscope set to a 20-MHz bandwidth. When measuring the response of the die voltage to dynamic loads, use the VCCSENSE and VSSSENSE pins on the processor socket with an oscilloscope set to 100 MHz bandwidth and with probes that are 1.5 pF maximum and 1M Ω minimum impedance.
- Variations of the input voltage.

2.4 Stability - REQUIRED

The VRM/EVRD needs to be unconditionally stable under all specified output voltage ranges, current transients of any duty cycle, and up to repetition rates of 1 MHz. The VRM/EVRD should be stable under a no load condition.

2.5 Processor Power Sequencing - REQUIRED

The VRM/EVRD must support platforms with defined power-up sequences. Figure 2-3 shows a block diagram of a system power-on sequencing implementation, and Figure 2-4 shows a timing diagram of the power-on sequencing requirements.

Figure 2-3. Power-On Sequence Block Diagram

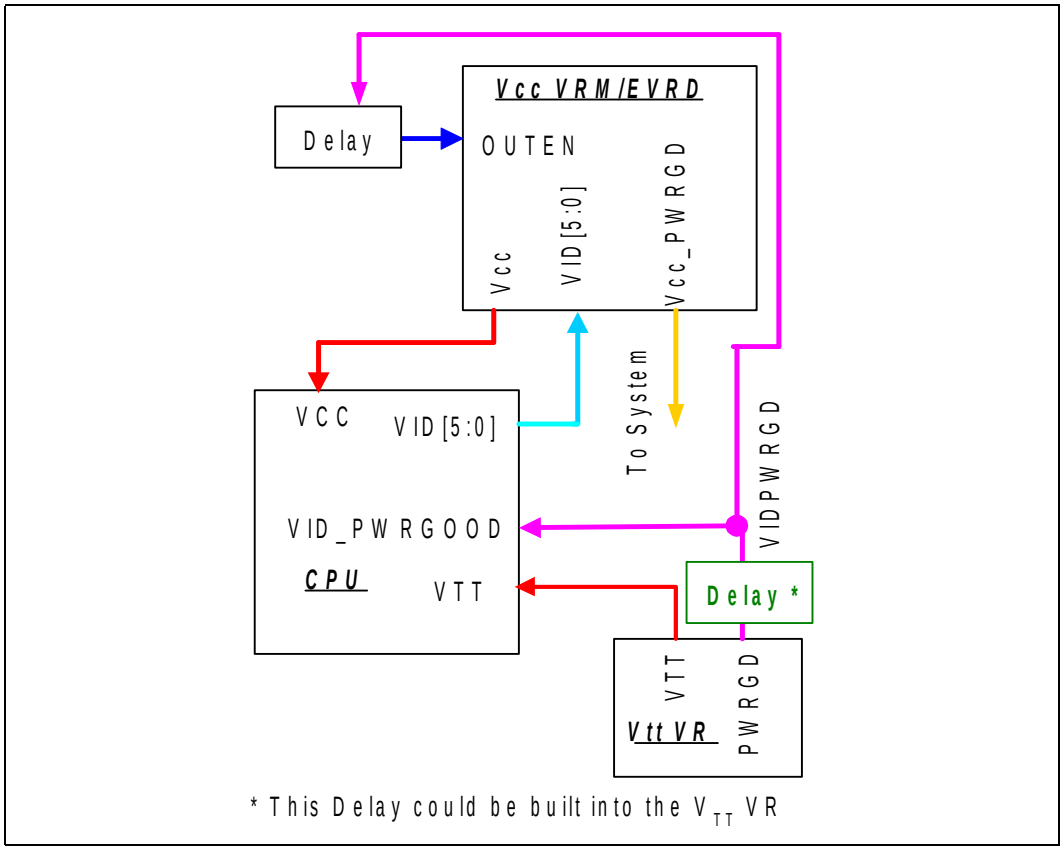
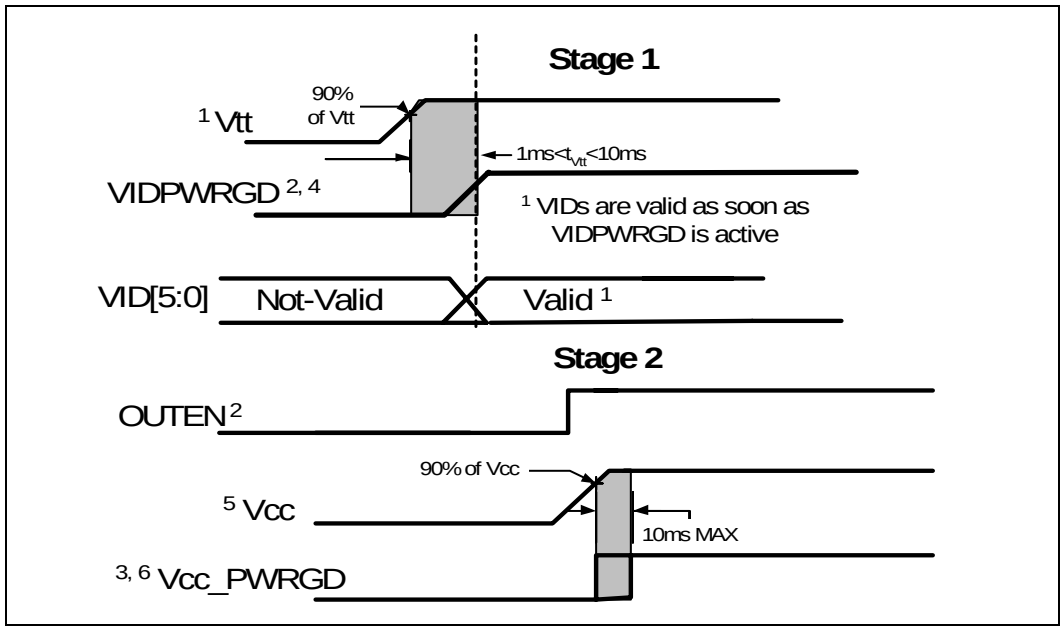


Figure 2-4. Power-On Sequence Timing Diagram



NOTES:
1. V_{TT} comes up at the application of system power to the Vtt VR. Vtt is used to supply VID [5:0] power to the processor.
2. V_{TT} VR generates VIDPWRGD after the VTT supply reaches 90% of the final value and must be a minimum of 1 ms. It is used by the Vcc VR to latch the processor's core VIDs outputs and should be a qualifier for enabling the output of the Vcc VR.
3. Vcc_PWRGD is generated by the Vcc VR and may be used elsewhere in the system.
4. VIDPWRGD must deactivate and Vcc must be disabled immediately when Vtt becomes invalid.
5. Vcc should not be enabled until at least 1ms after the VIDPWRGD is asserted.
6. Vcc_PWRGD should assert between 0 and 10 ms after Vcc reaches 90% of the final value.
7. See the processor datasheet for the latest timing requirements.

2.6 Dynamic Voltage Identification (D-VID) - REQUIRED

VRM/EVRD 10.2 supports dynamic VID across the entire VID table. The VRM/EVRD must be capable of accepting voltage level changes of 12.5 mV steps every 5 µs, up to 36 steps (450 mV) in 180 µs. The low voltage state will be maintained for at least 50 µs. The worst case settling time, including line-to-line skew, for the six VID lines is 400 ns. The VID inputs should contain circuitry to prevent false tripping or latching of VID codes during the settling time.

During a transition, the output voltage must be between the maximum voltage of the high range ("A" in Figure 2-5) and the minimum voltage of the low range ("B"). The VRM/EVRD must respond to a transition from VID-low to VID-high by regulating its Vcc output to the range defined by the new, final VID code within 50 µs of the final step. The time to move the output voltage from VID-high to VID-low will depend on the PWM controller design, the amount of system decoupling capacitance, and the processor load.

Figure 2-5 shows operating states as a representative processor changes levels. The diagram assumes steady state, maximum current during the transition for ease of illustration; actual processor behavior allows for any dIcc/dt event during the transitions, depending on the code it is executing at that time. In the example, the processor begins in a high-load condition. In transitions 12 and 23, the processor prepares to switch to the low-voltage range with a transition to a low-load

condition, followed by an increased activity level. Transition 34 is a simplification of the multiple steps from the high-voltage load line to the low-voltage load line. Transition 45 is an example of a response to a load change during normal operation in the lower range.

Figure 2-5. Processor Transition States

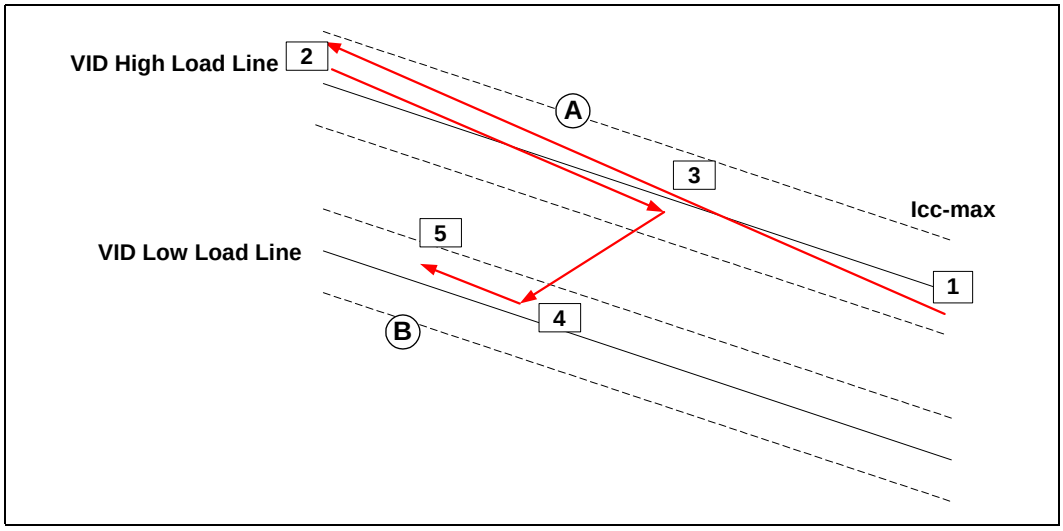
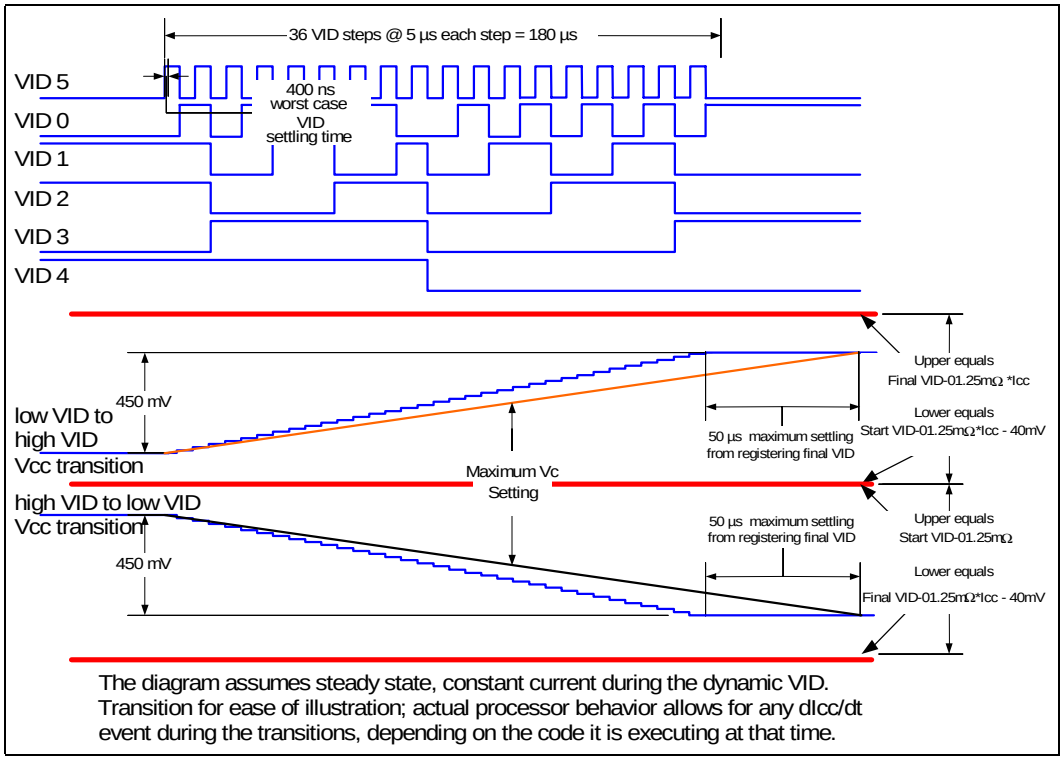


Figure 2-6 is an example of dynamic VID. The diagram in Figure 2-6 assumes steady state, constant current during the dynamic VID transition for ease of illustration; actual processor behavior allows for any dIcc/dt during the transitions, depending on the code it is executing at that time. Note that during dynamic VID, the processor will not output VID codes that would disable the voltage regulator output voltage.

Figure 2-6. Dynamic VID Transition States Illustration



The processor load may not be sufficient to absorb all of the energy from the output capacitors on the baseboard, when VID changes to a lower output voltage. The VRM/EVRD design should ensure that any energy transfer from the capacitors does not impair the operation of the VRM/EVRD, the AC-DC supply, or any other parts of the system.

2.7 Overshoot at Turn-On or Turn-Off - REQUIRED

The core VRM/EVRD output voltage should remain within the load-line regulation band for the VID setting, while the VRM/EVRD is turning on or turning off, with no over or undershoot out of regulation. No negative voltage below –100 mV may be present at the VRM/EVRD output during turn-on or turn-off.

2.8 Output Filter Capacitance - REQUIRED

The output filter capacitance for the VRM/EVRD based designs will be located on the baseboard. The system design must ensure that the output voltage of the VRM/EVRD conforms to the load line of Figure 2-2 and with the baseboard and processor loads. Table 2-2 shows the number of decoupling caps recommended and other related specifications based on updated processor power requirements supported by VRM/EVRD 10.2.

Table 2-2. Recommended Decoupling and Other Specifications for Supported Processors

Processor	560 µF Alum-Polymer	10 µF MLCC	Slew Rate (di/dt) A/µs	Thermal Design Current (A)	Max Icc (A)
64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache	12	44	770	86	91
64-bit Intel® Xeon™ processor MP with 1MB L2 cache	14	45	575	105	120

Figure 2-7 and Figure 2-8 are the recommended examples of a baseboard decoupling solution and a processor load. The number of capacitors needed could change based on updated processor power requirements. The values shown are for a four-phase 200 kHz to 800 kHz switching voltage regulator design. The parasitic board values are extracted from a design using four layers of the board with 2 ounces total of copper for Vcc and 2 ounces total of copper for ground. The type and number of bulk decoupling required is dependent on the voltage regulator design and it is highly recommended that the OEM work with the VRM supplier for an optimal decoupling solution for their system and in accordance to the processor's design requirements.

Figure 2-7. 64-bit Intel® Xeon™ Processor MP with up to 8MB L3 Cache Load Model

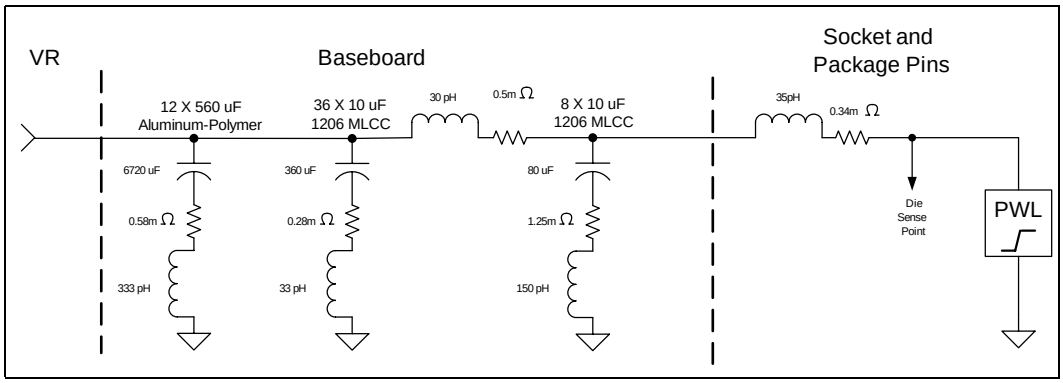
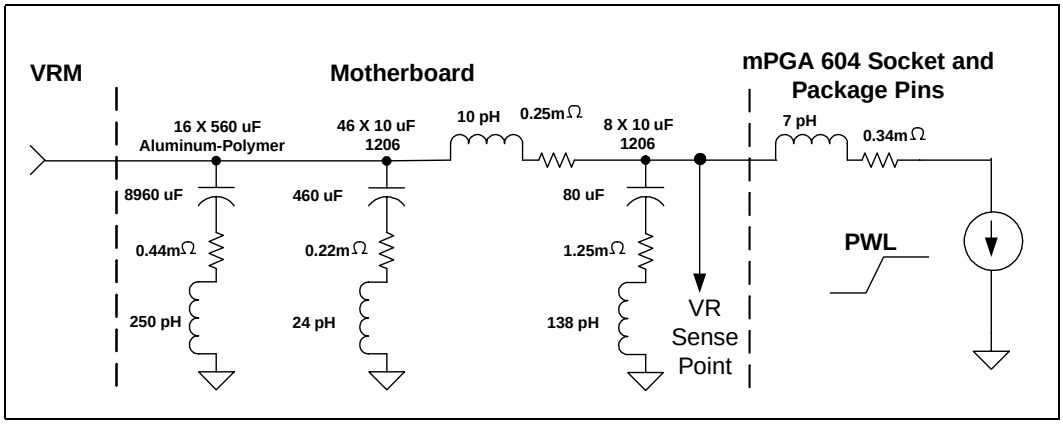


Figure 2-8. 64-bit Intel® Xeon™ Processor MP with up to 1MB L2 Cache Load Model



This VRM/EVRD10.2 design incorporates sixteen 560 µF Aluminum-polymer bulk capacitors and fifty-four 10 µF ceramic high-frequency capacitors per processor (Table 2-3). Eight of the fifty-four 10 µF capacitors should be placed in the cavity of the processor socket. The remaining forty-six capacitors should be split evenly such that half are on one side of the processor socket and half are on the other side as close to the processor socket as the keep-out zones allow. If backside passive components were allowed in the design, it would be beneficial to place the forty-six capacitors under the processor socket on the backside of the baseboard. Eight of the sixteen 560 µF capacitors should be placed on one side of the processor socket and the other eight on the opposite side as close to the processor socket as the keep-out zones allow.

Note: The amount of bulk decoupling needed is dependent on the voltage regulator design. Some multiphase buck regulators may have a higher switching frequency that would require a different output decoupling solution to meet the processor load line requirements than described in this document.

Table 2-3. VRM 10.2 Decoupling Capacitor Recommendations

Quantity	Value	Tolerance	Temperature Coefficient	ESR (mΩ)	ESL (nH)	Notes
16	560 µF Al-Polymer	±20%	N/A	7	4	
46	10 µF Ceramic	±20%	X5R or X6S	10	1.1	
8	10 µF Ceramic	±20%	X6S	10	1.1	1

NOTE:
1. Only the decoupling caps inside the socket cavity need to have the temperature coefficient of “X6S”.

In Figure 2-7 and Figure 2-8 the impedance values labeled “mPGA604 Socket and Package Pins” are supplied by Intel Corporation and are beyond the control of the system designer.

It is recommended that the system designer work with the VRM supplier to ensure proper implementation of the VRM converter.

2.9 Shut-Down Response - REQUIRED

Once the VRM/EVRD is operating after power-up, if either the Output Enable signal is deasserted or VID [5:0] = X11111, the VRM/EVRD should turn off its output (the output should go to high impedance) within 500 ms.

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3 Control Signals

3.1 Output Enable (OUTEN) - REQUIRED

The VRM/EVRD should accept an input signal to enable its output voltage. When disabled, the regulator's output should go to a high impedance state and should not sink or source current. When OUTEN is pulled low during the shutdown process, the VRM/EVRD should not exceed the previous voltage level regardless of the VID setting during the shutdown process. Once operating after power-up, it should respond to a deasserted OUTEN within 500 ms. The circuitry driving OUTEN is an open-collector/drain signal. It is **EXPECTED** that the pull-up resistor will be located on the baseboard and will not be integrated into the PWM controller chip or VRM.

Table 3-1. OUTEN Specifications

Symbol	Parameter	Min	Max	Units
VIH	Input Voltage High	0.8	3.465	V
VIL	Input Voltage Low	0	0.4	V

3.2 Voltage Identification (VID [5:0]) - REQUIRED

VID [4:0] are compatible with Intel® Pentium® 4 and Intel® Xeon™ processors using 5-bit VID codes. VID [5] will be used on the next generation of processors with 6-bit VID codes.

The VRM/EVRD must accept six lines to set the nominal voltage as defined by Table 3-2. When the VID [4:0] inputs are all high (in this case VID5 is a don't care), such as when no processor is installed, the regulator should disable its output voltage. If this disable code appears during previously normal operation, the regulator should turn off its output within 500 ms. The circuitry driving VID [5:0] is an open-collector/drain signal. It is **EXPECTED** that the pull-up resistors will be located on the baseboard and will not be integrated into the PWM controller chip or VRM. Other platform components may use VID inputs and may require tighter limits than specified in Table 3-2.

A normal no-processor VID [5:0] code for a Vcc regulator will be X11111, where X is defined as logic 1 or 0, disabling the VRM/EVRD.

Table 3-2. VID [5:0] Specifications

Symbol	Parameter	Min	Max	Units	Notes
V_{IH}	Input High Voltage	0.8	3.465	V	1
V_{IL}	Input Low Voltage	0	0.4	V	1

NOTE:
1. Other platform components may use VID inputs and may require tighter limits.

Table 3-3. Voltage Identification (VID)

Processor Pins (0 = low, 1 = high)						Vout (V)	Processor Pins (0 = low, 1 = high)						Vout (V)
VID4	VID3	VID2	VID1	VID0	VID5		VID4	VID3	VID2	VID1	VID0	VID5	
0	1	0	1	0	0	0.8375	1	1	0	1	0	0	1.2125
0	1	0	0	1	1	0.8500	1	1	0	0	1	1	1.2250
0	1	0	0	1	0	0.8625	1	1	0	0	1	0	1.2375
0	1	0	0	0	1	0.8750	1	1	0	0	0	1	1.2500
0	1	0	0	0	0	0.8875	1	1	0	0	0	0	1.2625
0	0	1	1	1	1	0.9000	1	0	1	1	1	1	1.2750
0	0	1	1	1	0	0.9125	1	0	1	1	1	0	1.2875
0	0	1	1	0	1	0.9250	1	0	1	1	0	1	1.3000
0	0	1	1	0	0	0.9375	1	0	1	1	0	0	1.3125
0	0	1	0	1	1	0.9500	1	0	1	0	1	1	1.3250
0	0	1	0	1	0	0.9625	1	0	1	0	1	0	1.3375
0	0	1	0	0	1	0.9750	1	0	1	0	0	1	1.3500
0	0	1	0	0	0	0.9875	1	0	1	0	0	0	1.3625
0	0	0	1	1	1	1.0000	1	0	0	1	1	1	1.3750
0	0	0	1	1	0	1.0125	1	0	0	1	1	0	1.3875
0	0	0	1	0	1	1.0250	1	0	0	1	0	1	1.4000
0	0	0	1	0	0	1.0375	1	0	0	1	0	0	1.4125
0	0	0	0	1	1	1.0500	1	0	0	0	1	1	1.4250
0	0	0	0	1	0	1.0625	1	0	0	0	1	0	1.4375
0	0	0	0	0	1	1.0750	1	0	0	0	0	1	1.4500
0	0	0	0	0	0	1.0875	1	0	0	0	0	0	1.4625
1	1	1	1	1	1	OFF[1]	0	1	1	1	1	1	1.4750
1	1	1	1	1	0	OFF[1]	0	1	1	1	1	0	1.4875
1	1	1	1	0	1	1.1000	0	1	1	1	0	1	1.5000
1	1	1	1	0	0	1.1125	0	1	1	1	0	0	1.5125
1	1	1	0	1	1	1.1250	0	1	1	0	1	1	1.5250
1	1	1	0	1	0	1.1375	0	1	1	0	1	0	1.5375
1	1	1	0	0	1	1.1500	0	1	1	0	0	1	1.5500
1	1	1	0	0	0	1.1625	0	1	1	0	0	0	1.5625
1	1	0	1	1	1	1.1750	0	1	0	1	1	1	1.5750
1	1	0	1	1	0	1.1875	0	1	0	1	1	0	1.5875
1	1	0	1	0	1	1.2000	0	1	0	1	0	1	1.6000

NOTE:
1. Output disabled – the same as deasserting the output enable input (Section 3.1).

3.3 Differential Remote Sense (VO_SEN+/-) - REQUIRED

The PWM controller should include differential sense inputs to compensate for an output voltage offset of <300 mV in the power distribution path. This common mode voltage is expected to occur due to transient currents and parasitic inductances and is not expected to be caused by parasitic resistances. The remote sense lines should draw no more than 10 mA, to minimize offset errors.

Note: VCCSENSE and VSSSENSE of the processor pins are not to be used as the VR sense input. It is recommended that the regulator's differential remote sense point for the processor's voltage regulator be at the center of the processor's socket cavity.

3.4 Load Line Select (LL0, LL1) - REQUIRED

Control signals LL0 and LL1 form a 2-bit load line selection and are used to configure the VRM/EVRD to supply the proper load line for the processors. These load lines, LL0 and LL1, are generated from a board management chip to set the load lines for the processor. LL0 and LL1 are open-collector/drain or equivalent signal. Table 3-4 shows the LL0 and LL1 pins specification and Table 2-1 shows equations in how to obtain V_{MAX} and V_{MIN} based on LL0 and LL1 bit code. It is **EXPECTED** that the pull-up resistor will be located on the baseboard and will not be integrated into the VRM.

Table 3-4. LL0, LL1 Specifications

Symbol	Parameter	Min	Max	Units
I_{OL}	Output Low Current	0	4	mA
V_{IH}	Input Voltage High	0.8	3.465	V
V_{IL}	Input Voltage Low	0	0.4	V

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4 Input Voltage and Current

4.1 Input Voltages - EXPECTED

The power source for the VRM/EVRD is 12V +5% / –8%. This voltage is supplied by a separate power supply. For input voltages outside the normal operating range, the VRM/EVRD should either operate properly or shut down.

4.2 Load Transient Effects on Input Current - EXPECTED

The design of the VRM/EVRD, including the input power delivery filter, must ensure that the maximum slew rate of the input current does not exceed 0.5 A/µs, or as specified by the separate power supply.

Note: In the case of a VRM design, the input power delivery filter may be located either on the VRM or on the baseboard. The decision for the placement of the filter will need to be coordinated between the baseboard and VRM designers.

It is recommended that the bulk input decoupling be placed on the baseboard by the VRM input connector and high frequency decoupling on the VRM module. Expected baseboard decoupling should be between 1000 µF to 2240 µF depending on VRM design and system power supply.

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5 Processor Voltage Output Protection

These are features built into the VRM/EVRD to prevent damage to itself, the processor, or other system components.

5.1 Over-Voltage Protection (OVP) - PROPOSED

The OVP circuit monitors the processor core voltage (Vcc) for an over-voltage condition. If the output is more than 200 mV above the VID level, the VRM/EVRD shuts off the output.

5.2 Over-Current Protection (OCP) - PROPOSED

The core VRM/EVRD should be capable of withstanding a continuous, abnormally low resistance on the output without damage or over-stress to the unit. Output current under this condition will be limited to no more than 120% of the maximum peak rated output of the voltage regulator.

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6 Output Indicators

6.1 Power Good (Vcc_PWRGD - PROPOSED

The VRM/EVRD may provide a power-good output signal, which remains in the low state until a maximum of 10 ms after the output voltage reaches the range specified in Section 2.2. The signal should then remain asserted as long as the VRM/EVRD output is operating within specification. It will be an open-collector/drain or equivalent signal. The pull-up resistor and voltage source will be located on the baseboard. If this signal is not implemented on the VRM, it should be left unconnected. Table 6-1shows the Vcc_PWRGD pin specification.

Table 6-1. Vcc_PWRGD Specifications

Symbol	Parameter	Min	Max	Units
I_{OL}	Output Low Current	0	4	mA
V_{OH}	Output High Voltage	0.8	5.5	V
V_{OL}	Output Low Voltage	0	0.4	V

6.2 Voltage Regulator Hot (VR_hot#) - PROPOSED

The VRM/EVRD VR_hot# signal is an output signal that is asserted low when a thermal event is detected in the converter. Assertion of this signal will be used by the system to minimize damage to the converter due to the thermal conditions. Table 6-2 shows the VR_hot# pin specification. This signal will be an open-collector/drain or equivalent signal and needs to be pulled up to an appropriate voltage through a pull-up resistor on the baseboard. A typical implementation would be a 50 ohm resistor pulled up to 1.2 V.

Table 6-2. VR_hot# Specifications

Symbol	Parameter	Min	Max	Units
I_{OL}	Output Low Current	19.9	30	mA
V_{OH}	Output High Voltage	0.8	3.465	V
V_{OL}	Output Low Voltage	0	0.4	V

Each customer is responsible for identifying maximum temperature specifications for all components in the VRM/EVRD design and ensuring that these specifications are not violated, while continuously drawing specified Icc (TDC) levels. In the occurrence of a thermal event, a thermal sense circuit may assert the processors signal FORCEPR# immediately prior to exceeding maximum VRM, baseboard, and/or component thermal ratings to prevent heat damage. The assertion may be made through direct connection to the FORCEPR# pin or through system management logic. Assertion of this signal will lower processor power consumption and reduce current draw through the voltage regulator, resulting in lower component temperatures. Sustained assertion of the FORCEPR# pin will cause noticeable platform performance degradation and should not occur when drawing less than specified thermal design current for a properly designed system.

It is recommended that hysteresis be designed into the thermal sense circuit to prevent a scenario in which the VR_hot# signal is rapidly being asserted and de-asserted.

6.3 Load Indicator Output (Load Current) - PROPOSED

The VRM/EVRD may have an output with a voltage (Load Current) level that varies linearly with the VRM/EVRD output current. The PWM controller supplier may specify a voltage-current relationship consistent with the controller's current sensing method. Baseboard designers may route this output to a test point for system validation.

6.4 VRM Present (VRM_pres#) - EXPECTED

The VRM should have the VRM_pres# signal. This signal is an output signal used to indicate to the system that a VRM is plugged into the socket. VRM_pres# is an open-collector/drain or equivalent signal. Table 6-3 shows the VRM_pres# pin specification. It is **EXPECTED** that the pull-up resistor will be located on the baseboard and will not be integrated into the VRM.

Table 6-3. VRM_pres Specifications

Symbol	Parameter	Min	Max	Units
I_{OL}	Output Low Current	0	4	mA
V_{OH}	Output High Voltage	0.8	5.5	V
V_{OL}	Output Low Voltage	0	0.4	V

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7 VRM – Mechanical Guidelines

7.1 VRM Connector - EXPECTED

The part number and vendor name for the connector can be found in Table 7-1. The VRM interface with the system board is a 27-pin pair edge connector. The connector uses latches to hold the VRM in place. The connector will be rated to handle a continuous load current of 130 A.

Table 7-1. VRM 10.2 Connector Part Number and Vendor Name

Connector	Vendor Part Number	Note
Tyco / Elcon	283-0172-01303B (Molded)	1
	283-0172-00900B (Machined)	
	284-0202-03003 (Surface mount)	

NOTE:
1. These vendors are listed by Intel as a convenience to Intel's general customer base, but Intel does not make any representations or warranties whatsoever regarding quality, reliability, functionality, or compatibility of these devices. This list and/or these devices may be subject to change without notice.

7.2 VRM Connector Keying

7.2.1 Connector Keying

- Single notch between pins 3 and 4 (51 and 52 opposite side).
- Single notch between pins 12 and 13 (42 and 43 opposite side).
- Single notch between pins 21 and 22 (33 and 34 opposite side).

7.2.2 Connector Pin 1 Orientation

Referencing Figure 7-1, Outline Drawing, Far Side (FS) pins sequence 1 through 27, left to right. Near Side (NS) pins sequence 54 through 28. Pin 1 and 54 are opposite one another.

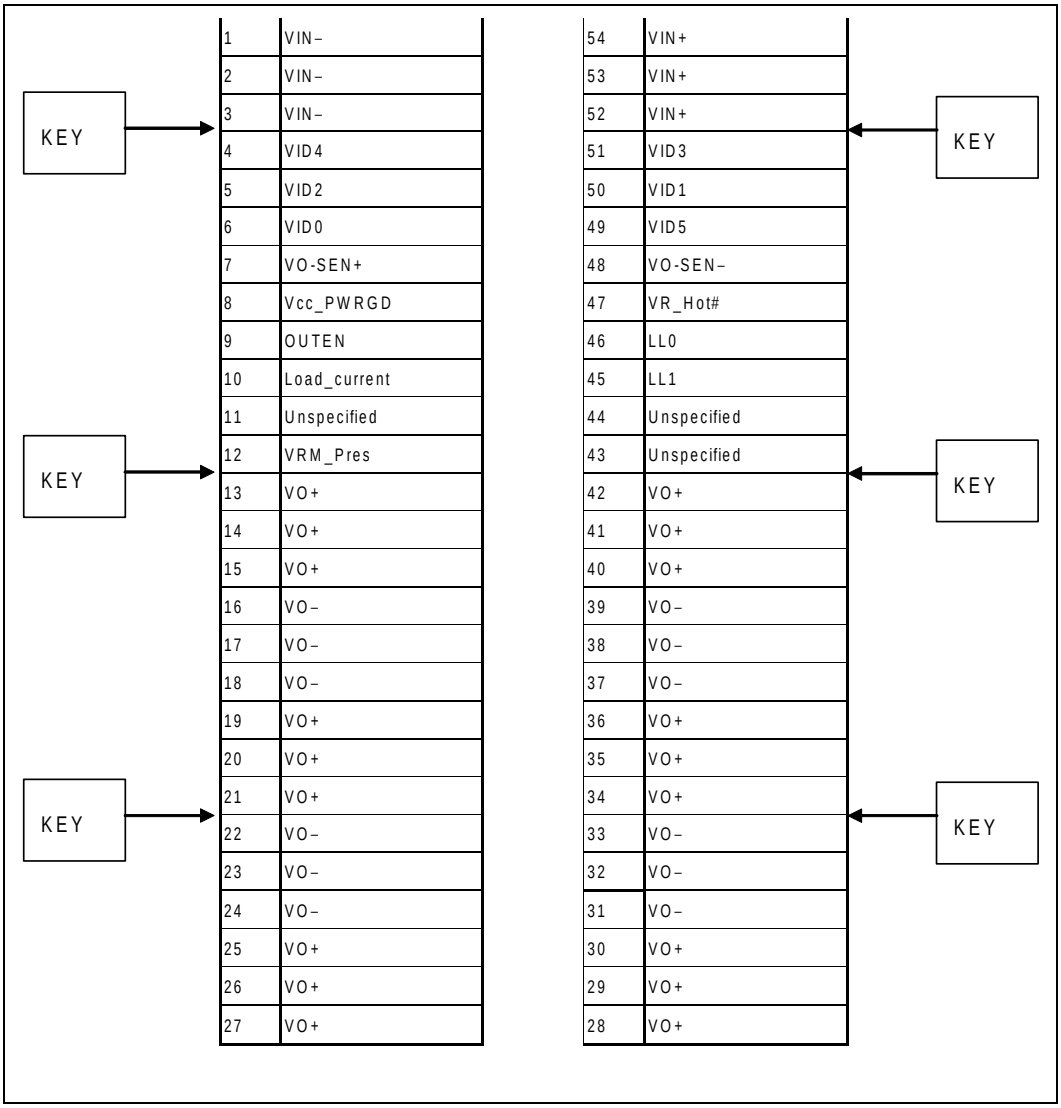
7.3 Pin Descriptions and Assignments

Table 7-2 shows the VRM 10.2 connector pin description. Pin assignments are shown in Table 7-3.

Table 7-2. VRM 10.2 Connector Pin Descriptions

Name	Type	Description
Load current	Output	Analog signal representing the output load current
OUTEN	Input	Output enable
Vcc_PWRGD	Output	Output signal indicating that the output voltage of the VRM is in the specified range
VID [5:0]	Input	Voltage ID pins used to specify the VRM output voltage
VIN+	Power	VRM Input Voltage
VIN–	Ground	VRM Input Ground
VO+	Power	VRM Output Voltage
VO–	Ground	VRM Output Ground
VO_SEN+ VO_SEN–	Input	Output voltage sense pins
VR_hot#	Output	Indicates to the system that a thermal event has been detected in the VR
VRM_pres#	Output	Indicates to the system that a VRM is plugged into the socket
LL0, LL1	Input	Used to configure VR load line value

Table 7-3. VRM 10.2 Pin Assignments



1	VIN–	54	VIN+
2	VIN–	53	VIN+
3	VIN–	52	VIN+
4	VID4	51	VID3
5	VID2	50	VID1
6	VID0	49	VID5
7	VO-SEN+	48	VO-SEN–
8	Vcc_PWRGD	47	VR_Hot#
9	OUTEN	46	LL0
10	Load_current	45	LL1
11	Unspecified	44	Unspecified
12	VRM_Pres	43	Unspecified
13	VO+	42	VO+
14	VO+	41	VO+
15	VO+	40	VO+
16	VO–	39	VO–
17	VO–	38	VO–
18	VO–	37	VO–
19	VO+	36	VO+
20	VO+	35	VO+
21	VO+	34	VO+
22	VO–	33	VO–
23	VO–	32	VO–
24	VO–	31	VO–
25	VO+	30	VO+
26	VO+	29	VO+
27	VO+	28	VO+

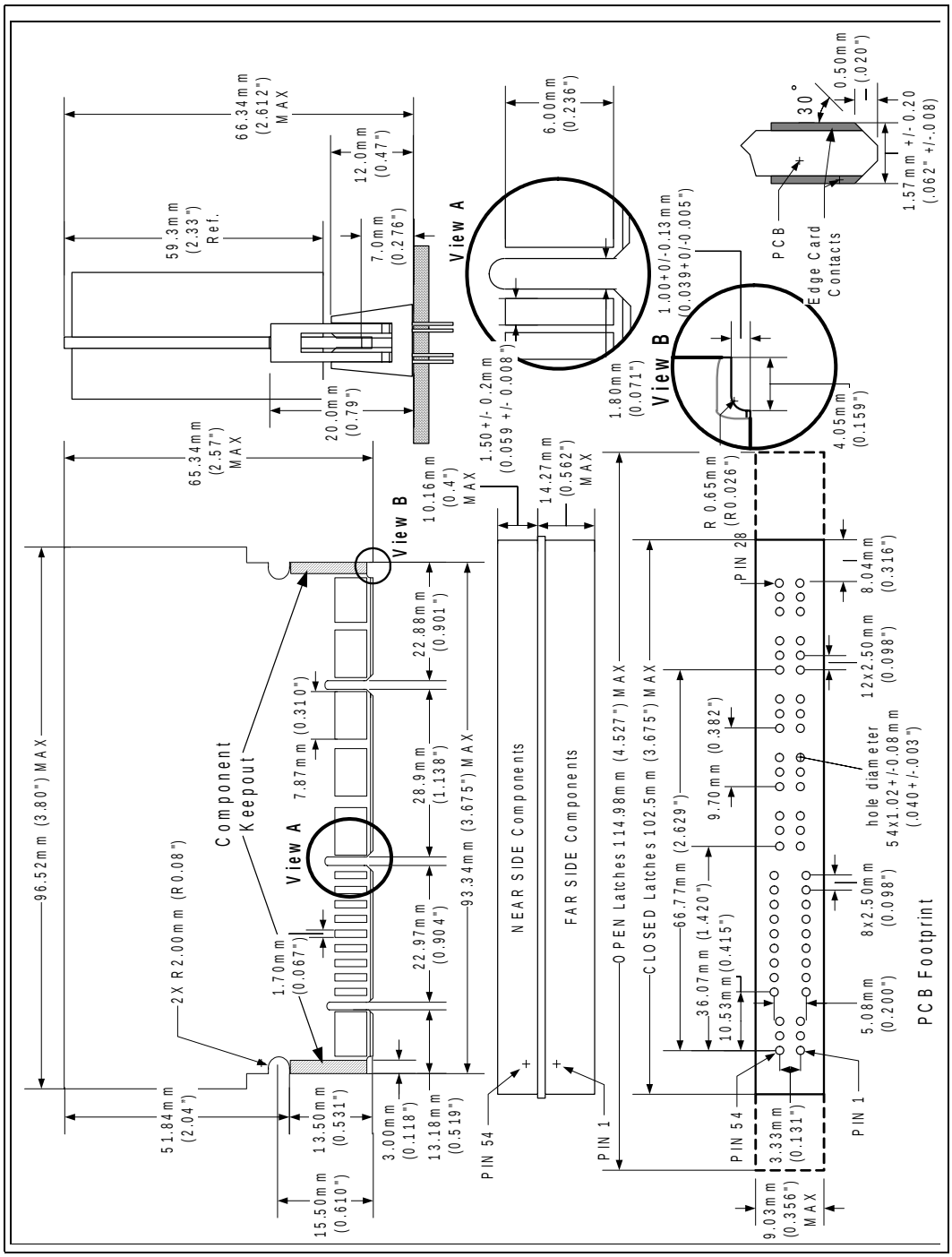
7.4 Mechanical Dimensions - PROPOSED

The mechanical dimensions for the VRM 10.2 module and connector are shown in Figure 7-1.

7.4.1 Gold Finger Specification

The VRM board must contain gold lands (fingers) for interfacing with the VRM connector that is 1.50 mm ±0.2 mm [0.059” ±0.008”] wide by 6.00 mm [0.236”] minimum long and spaced 2.50 mm [0.098”] apart. Traces from the lands to the power plane should be a minimum of 0.89 mm [0.035”] wide and of a minimal length.

Figure 7-1. VRM 10.2 Module and Connector



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8 VRM – Environmental Conditions

The VRM design, including materials, should be consistent with the manufacture of units that meet the environmental requirements specified below;

8.1 Operating Temperature - PROPOSED

The VRM shall meet all electrical requirements when operated at Thermal Design Current (Icc (TDC)) over an ambient temperature range of 0º C to +45º C with a minimum airflow of 400 LFM. The volumetric airflow (Q) can be measured through a wind tunnel. The VRM should be mounted on a PCB, which is then mounted in a duct. The recommended duct cross section, assuming the PCG is horizontal and flush with the bottom of the duct is as follows:

- Y direction duct width (perpendicular to flow, horizontal) = 0.3 m
- Z direction duct height (perpendicular to flow, vertical) = 0.15 m
- Minimum X direction duct length in front of VRM = 6 hydraulic diameters = 1.2 m
- Minimum X direction duct length behind VRM = 2 hydraulic diameters = 0.4 m

Velocity (v) is calculated from the volumetric flow and cross-sectional area at the inlet as:

- $v = Q/(0.3 \times 0.15)m^2$

Operating conditions shall be considered to include 10 cycles between min and max temperature as a rate of 10º C / hour and a dwell time of 30 minutes at extremes. Temperature and airflow measurements should be made in close proximity to the VRM.

8.2 Non-Operating Temperature - PROPOSED

The VRM shall not be damaged when exposed to temperatures between –40º C and +70º C. These shall be considered to include 50 cycles of minimum to maximum temperatures at 20ºC / hour with a dwell time of 20 minutes at the extremes.

8.3 Humidity - PROPOSED

85% relative – operating

95% relative – non-operating

8.4 Altitude - PROPOSED

3.05 km [10k feet] – operating

15.24 km [50k feet] – non-operating

8.5 Electrostatic Discharge - PROPOSED

Testing shall be in accordance with IEC 61000-4-2.

Operating – 15 kV initialization level. The direct ESD event shall cause no out-of-regulation conditions – including overshoot, undershoot and nuisance trips of over-voltage protection, over-current protection or remote shutdown circuitry.

Non-operating –25 kV initialization level. The direct ESD event shall not cause damage to the VRM circuitry.

8.6 Shock and Vibration - PROPOSED

The shock and vibration tests should be applied at the baseboard level. The VRM should not be damaged and the interconnect integrity not compromised during:

- A shock of 30g with a 11 ms half sine wave, non-operating, to be applied in each of the orthogonal axes.
- Vibration of $0.01g^2$ per Hz at 5 Hz, sloping to $0.02g^2$ per Hz at 20 Hz and maintaining $0.02g^2$ per Hz from 20 Hz to 500 Hz, non-operating, applied in each of the orthogonal axes.

8.7 Electromagnetic Compatibility - PROPOSED

Design, including materials, should be consistent with the manufacture of units that comply with the limits of FCC Class B and CISPR22 Class B for radiated emissions.

8.8 Reliability - PROPOSED

Design, including materials, should be consistent with the manufacture of units with a Mean Time Between Failure (MTBF) of 500,000 hours of continuous operation at 55ºC, maximum-outputs load, and worst-case line, while meeting specified requirements. MTBF should be calculated in accordance with MIL-STD-217F or Bellcore.

8.9 Safety - PROPOSED

The voltage regulator is to be UL Recognized to standard UL1950 3rd Ed., including requirements of IEC950 and EN 60950. Plastic parts and printed wiring board are to be UL-Recognized with 94V-0-flame class.

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9 Lead Free (Pb Free)

The use of lead in electronic products is an increasingly visible environmental and political concern. The drivers for the reduction or elimination of lead in electronic products include:

- Customer desire for environmentally friendly (‘green’) products.
- Manufacturer desire to be environmentally friendly, and be perceived as such.
- Government initiatives regarding recycling of electronic products.
- Planned and potential legislation.

The most notable legislation is the European Union (EU) Restriction on Hazardous Materials directive, also known as RoHS. The commission directive may be found at the following URL:

http://europa.eu.int/eur-lex/pri/en/oj/dat/2003/l_037/l_03720030213en00190023.pdf

European Union “Member States shall ensure that, from 1 July 2006, new electrical and electronic equipment put on the market does not contain lead…” Each EU country will implement this law and establish penalties and fines for non-compliance. The RoHS directive includes certain exemptions:

- Lead in high melting temperature type solders (i.e. tin-lead solder alloys containing more than 85% lead).
- Lead in solders for servers, storage and storage array systems (exemption granted until 2010).
- Lead in solders for network infrastructure equipment for switching, signaling, transmission as well as network management for telecommunication.
- Lead in electronic ceramic parts (e.g. piezoelectronic devices).

For the latest information on RoHS please refer to the following URL:

http://europa.eu.int/eur-lex/en

The VRM10.2 lifetime is expected to extend beyond July 1, 2006.

Intel recommends that you consider Pb Free manufacturing processes and components for the module and module connector.

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