VRM 9.1 DC-DC Converter

Design Guidelines

March 2005

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Revision History

Document Number	Revision Number	Description	Date
306826	001	• Initial release of this document	March 2005

NOTE: Not all revisions may be published.

Applications and Terminology

This document defines one or more DC-to-DC converters to meet the power requirements of computer systems using Intel microprocessors. It does not attempt to define a specific voltage regulator module (VRM) implementation. VRM requirements will vary according to the needs of different computer systems, including the range of processors a specific VRM is expected to support in a system. The “VRM” designation refers to a voltage regulator module that is plugged into a system board.

The VRM 9.1 definition is specifically intended to meet the needs of Intel® Xeon™ processors using the 603-pin socket, and the cache regulator requirement for 64-bit Intel Xeon processor MP using the 604-pin socket, in multiprocessor platforms.

Each guideline is placed into one of three categories. The category immediately follows the section heading and is one of the following:

REQUIRED	An essential part of the design -- necessary to meet processor voltage and current specifications and follow processor layout guidelines.
EXPECTED	Part of Intel’s processor power definitions; necessary for consistency among the designs of many systems and power devices. May be specified or expanded by system OEMs.
PROPOSED	Normally met by this type of DC-to-DC converter and, therefore, included as a design target. May be specified or expanded by system OEMs.

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1 Electrical Specifications

1.1 Output Requirements

1.1.1 Voltage and Current - REQUIRED

The VRM 9.1 Voltage Regulator Module is a DC-DC converter that supplies the correct voltage and current to a single processor, or when paralleled with other like converters, supplies the required voltage and current to multiple processors, whose Vcc and Vss or V_{CACHE} and Vss are also connected in parallel.

One VRM per processor is assumed for Intel® Xeon™ processor with 512 KByte L2 cache and one VRM per two processor cache for 64-bit Intel® Xeon™ processor MP. Current requirements are shown in Table 1-1. The maximum output voltage is determined by the five-bit VID code provided to the VRM, as described in Section 1.3.2. The system baseboard must supply additional decoupling capacitance and sufficient power and ground plane area to properly carry the DC currents. The required V-I relationship for the Intel® Xeon™ processor is given in Figure 1-1, the one for the Intel Xeon processor with 512 KByte L2 cache is in Figure 1-2 and the ones for the 64-bit Intel Xeon processor MP in Figure 1-3 and Figure 1-4.

Processor data is shown for reference. The corresponding processor data sheet takes precedence for processor specifications.

1.1.2 Maximum Ratings - EXPECTED

To supply the anticipated requirements of the planned processor versions, VRM 9.1 should be able to provide a sustained output current of 81 A. Refer to Table 1-1 for maximum design parameters.

Table 1-1. VRM 9.1 Current Requirements

Symbol	Parameter	Unit	Value
Icc_{MIN}	Minimum current drawn by a single processor	A	0.5[1]
Icc_{ACTIVE}	Maximum step current change by a single processor	A	54
Icc_{MAX}	Maximum total current drawn by a single processor	A	75
$Ivrm_{MAX}$	Maximum current required [2]	A	81
$Ivrm_{SLEW}$	VRM output current slew rate [3]	A/µs	50

NOTES:
1. Estimate of lowest current state for VRM regulation, not to be construed as a processor specification. Refer to data sheet for actual design information.
2. Includes tolerance for needs of current sharing
3. Typical value for slew rate. Actual requirement will depend on decoupling of actual VRM and baseboard. Slew rate of processor load at the socket is 450 A/µs.

1.1.3 Output Voltage Tolerance - REQUIRED

The remote sense lines of each VRM should be routed on the system board to a remote sense point at the geometric center of the processors, where they are connected to each other and to the Vcc and Vss planes for Intel Xeon processors using the 603 socket. For 64-bit Intel Xeon processor MP cache remote sense traces, the processor $V_{CCSENSE}$ and $V_{SSSENSE}$ pins should be connected to test points on the baseboard in order to probe the die voltage. Unstuffed resistor pads on the baseboard can be used for this purpose.

The VRM regulates this point as follows:

- VvrmMIN = 0.980 * VID_Setpoint_Voltage - VRM_Output_Current * 0.95 mΩ
- VvrmMAX = VID_Setpoint_Voltage - VRM_Output_Current * 0.95 mΩ
- $Vvrm_{MIN}$ and $Vvrm_{MAX}$ are VRM voltage regulation requirements measured at the power plane reference point (VRM remote-sense star connection at the geometric center of the processor loads on the system board).
- $Vvrm_{MIN}$ is the minimum voltage allowed for a given VRM output current.
- $Vvrm_{MAX}$ is the maximum voltage allowed for a given VRM output current.

See example load lines in Figure 1-1, Figure 1-2, Figure 1-3, and Figure 1-4 and their corresponding numerical values in Table 1-2 and Table 1-3. The VRM shall regulate as defined above for all VID set-points (except during input voltage turn-on and turn-off - see Section 1.1.6 for turn-on and turn-off tolerances).

Voltage tolerance includes:

- Initial DC output voltage set-point error
- Component aging effects
- Output ripple and noise from DC to 100 MHz
- Full ambient temperature range and warm up
- Static operation
- Dynamic output load changes
- Input voltage variations

Figure 1-1. VRM 9.1 Regulation Requirement for Intel® Xeon™ Processor (VID = 1.7 V)

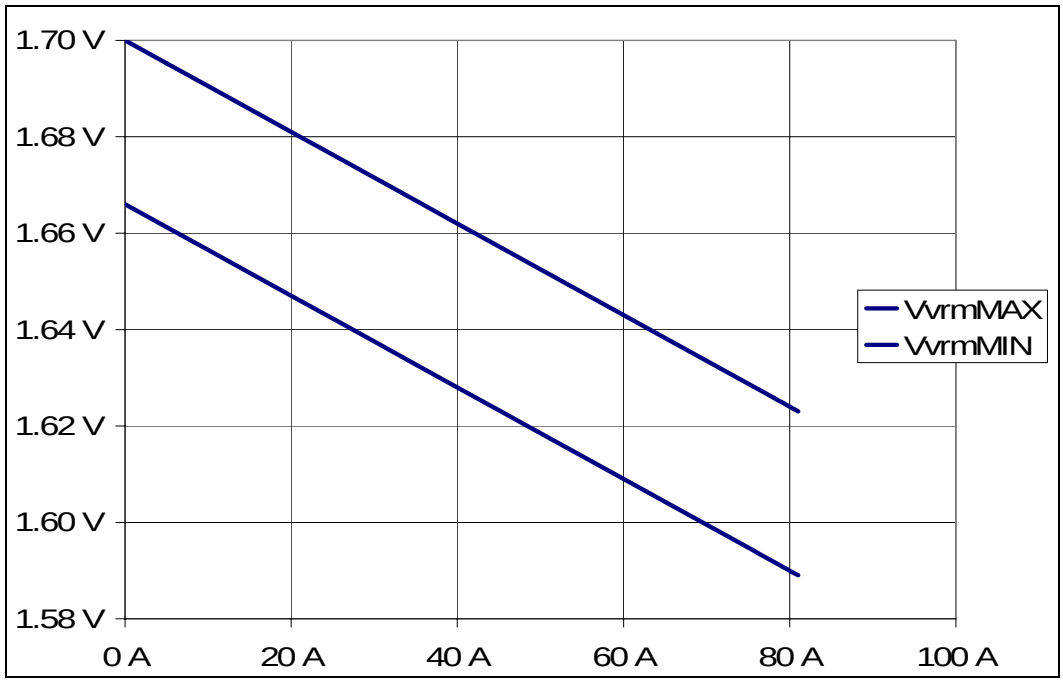

Figure 1-2. VRM 9.1 Regulation Requirement for Intel® Xeon™ Processor with 512 KByte L2 Cache (VID = 1.5 V)

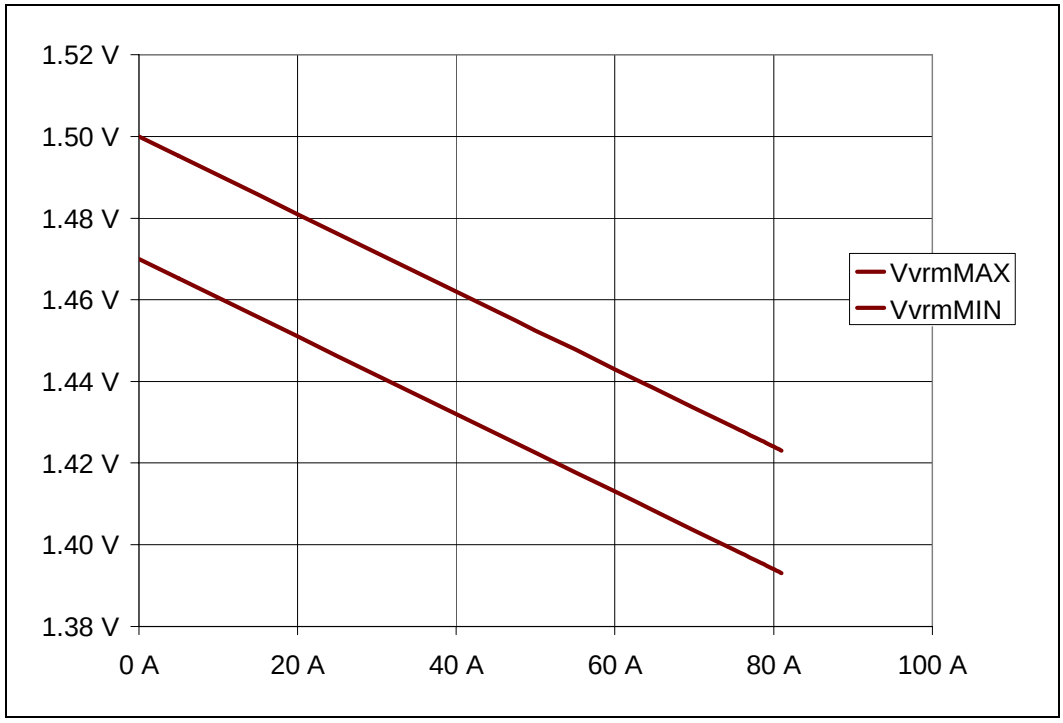

Figure 1-3. VRM 9.1 Regulation Requirement for 64-bit Intel® Xeon™ Processor MP Cache (VID = 1.125 V)

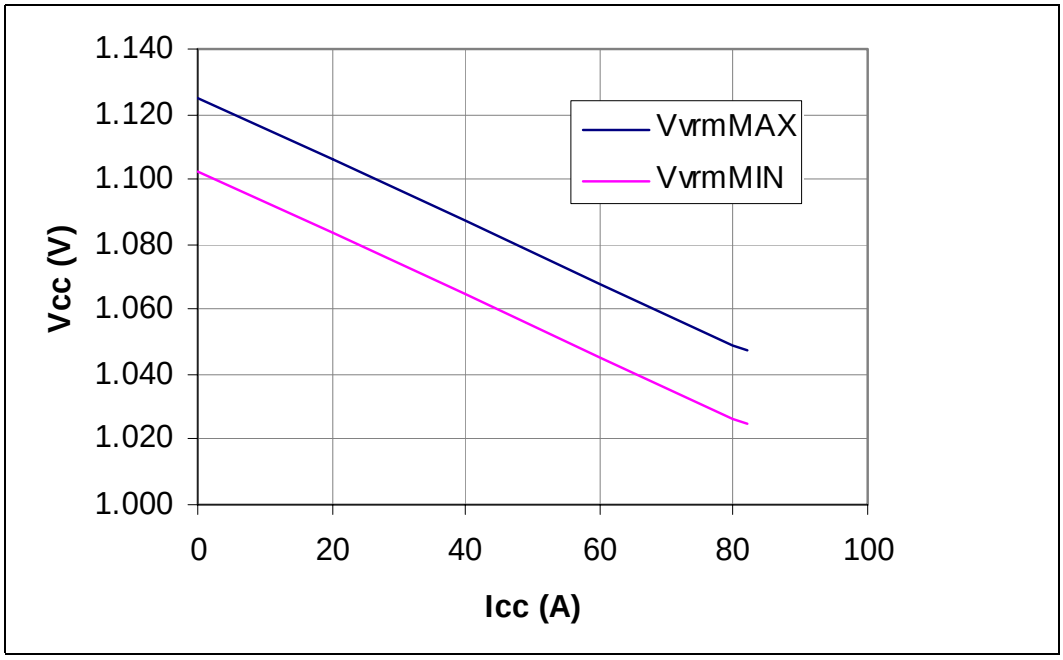

Figure 1-4. VRM 9.1 Regulation Requirement for 64-bit Intel® Xeon™ Processor MP Cache (VID = 1.1275 V)

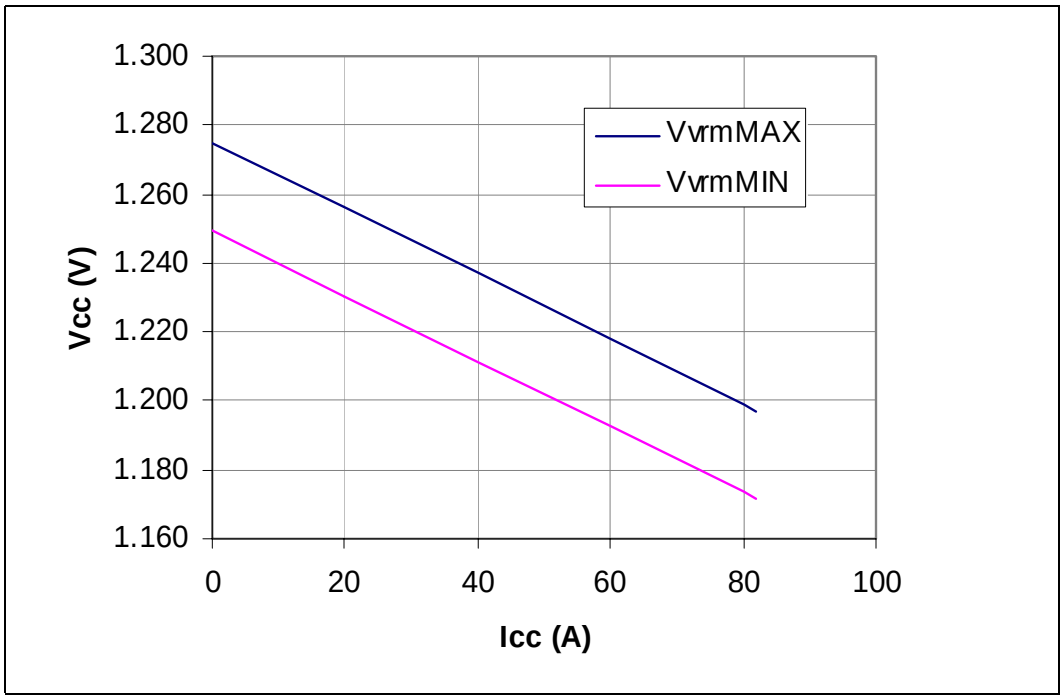

Table 1-2. Intel® Xeon™ Processor VRM Regulation Requirements

VRM Output Current, Amperes	Intel® Xeon™ Processor with 512 KByte L2 Cache (VID = 1.5V) Remote Sense Voltage		Intel® Xeon™ Processor (VID = 1.7V) Remote Sense Voltage		VRM Output Current, Amperes	Intel® Xeon™ Processor with 512 KByte L2 Cache (VID = 1.5V) Remote Sense Voltage		Intel® Xeon™ Processor (VID = 1.7V) Remote Sense Voltage	
	$Vvrm_{MAX}$	$Vvrm_{Min}$	$Vvrm_{MAX}$	$Vvrm_{Min}$		$Vvrm_{MAX}$	$Vvrm_{Min}$	$Vvrm_{MAX}$	$Vvrm_{Min}$
0	1.500	1.470	1.700	1.666	42	1.460	1.430	1.660	1.626
2	1.498	1.468	1.698	1.664	44	1.458	1.428	1.658	1.624
4	1.496	1.466	1.696	1.662	46	1.456	1.426	1.656	1.622
6	1.494	1.464	1.694	1.660	48	1.454	1.424	1.654	1.620
8	1.492	1.462	1.692	1.658	50	1.453	1.423	1.653	1.619
10	1.491	1.461	1.691	1.657	52	1.451	1.421	1.651	1.617
12	1.489	1.459	1.689	1.655	54	1.449	1.419	1.649	1.615
14	1.487	1.457	1.687	1.653	56	1.447	1.417	1.647	1.613
16	1.485	1.455	1.685	1.651	58	1.445	1.415	1.645	1.611
18	1.483	1.453	1.683	1.649	60	1.443	1.413	1.643	1.609
20	1.481	1.451	1.681	1.647	62	1.441	1.411	1.641	1.607
22	1.479	1.449	1.679	1.645	64	1.439	1.409	1.639	1.605
24	1.477	1.447	1.677	1.643	66	1.437	1.407	1.637	1.603
26	1.475	1.445	1.675	1.641	68	1.435	1.405	1.635	1.601
28	1.473	1.443	1.673	1.639	70	1.434	1.404	1.634	1.600
30	1.472	1.442	1.672	1.638	72	1.432	1.402	1.632	1.598
32	1.470	1.440	1.670	1.636	74	1.430	1.400	1.630	1.596
34	1.468	1.438	1.668	1.634	76	1.428	1.398	1.628	1.594
36	1.466	1.436	1.666	1.632	78	1.426	1.396	1.626	1.592
38	1.464	1.434	1.664	1.630	80	1.424	1.394	1.624	1.590
40	1.462	1.432	1.662	1.628	82	1.422	1.392	1.622	1.588

Table 1-3. 64-bit Intel® Xeon™ Processor MP, VRM Regulation Requirements

VRM Output Current, Amperes	64-bit Intel® Xeon™ Processor Cache (VID = 1.125V) Remote Sense Voltage		64-bit Intel® Xeon™ Processor Cache (VID = 1.275V) Remote Sense Voltage		VRM Output Current, Amperes	64-bit Intel® Xeon™ Processor Cache (VID = 1.125V) Remote Sense Voltage		64-bit Intel® Xeon™ Processor Cache (VID = 1.275V) Remote Sense Voltage	
	$Vvrm_{MAX}$	$Vvrm_{Min}$	$Vvrm_{MAX}$	$Vvrm_{Min}$		$Vvrm_{MAX}$	$Vvrm_{Min}$	$Vvrm_{MAX}$	$Vvrm_{Min}$
0	1.125	1.103	1.275	1.250	42	1.085	1.063	1.235	1.210
2	1.123	1.101	1.273	1.248	44	1.083	1.061	1.233	1.208
4	1.121	1.099	1.271	1.246	46	1.081	1.059	1.231	1.206
6	1.119	1.097	1.269	1.244	48	1.079	1.057	1.229	1.204
8	1.117	1.095	1.267	1.242	50	1.078	1.055	1.228	1.202
10	1.116	1.093	1.266	1.240	52	1.076	1.053	1.226	1.200
12	1.114	1.091	1.264	1.238	54	1.074	1.051	1.224	1.198
14	1.112	1.089	1.262	1.236	56	1.072	1.049	1.222	1.196
16	1.110	1.087	1.260	1.234	58	1.070	1.047	1.220	1.194
18	1.108	1.085	1.258	1.232	60	1.068	1.046	1.218	1.193
20	1.106	1.084	1.256	1.231	62	1.066	1.044	1.216	1.191
22	1.104	1.082	1.254	1.229	64	1.064	1.042	1.214	1.189
24	1.102	1.080	1.252	1.227	66	1.062	1.040	1.212	1.187
26	1.100	1.078	1.250	1.225	68	1.060	1.038	1.210	1.185
28	1.098	1.076	1.248	1.223	70	1.059	1.036	1.209	1.183
30	1.097	1.074	1.247	1.221	72	1.057	1.034	1.207	1.181
32	1.095	1.072	1.245	1.219	74	1.055	1.032	1.205	1.179
34	1.093	1.070	1.243	1.217	76	1.053	1.030	1.203	1.177
36	1.091	1.068	1.241	1.215	78	1.051	1.028	1.201	1.175
38	1.089	1.066	1.239	1.213	80	1.049	1.027	1.199	1.174
40	1.087	1.065	1.237	1.212	82	1.047	1.025	1.197	1.172

1.1.4 No-Load Operation - REQUIRED

The VRM shall operate at all load conditions from maximum current down to zero load. In practice the VID code generated when no processors are installed (true zero-load condition) will turn off the VRM output. During ‘no load’ conditions the VRM does not need to meet the output regulation specifications described in Section 1.1.3, but its output must not exceed 110% of the value of the maximum DC output voltage (VID set-point voltage), and it must not trigger over-voltage fault detection circuitry.

When the VRM is loaded with the Icc_{MIN} listed in Table 1-1, it must regulate and source current without triggering failures or causing control signal malfunction.

1.1.5 Turn-on Response Time - EXPECTED

The output voltage should reach its specified range within 15 ms after the input power reaches its minimum voltage and the OUTEN signal is asserted.

1.1.6 Overshoot and Undershoot at Turn-On or Turn-Off - REQUIRED

Overshoot must be less than 2% above the Voltage Identification (VID) code. No negative voltage below –0.1 V may be present at the output at any time.

1.1.7 Converter Stability - REQUIRED

The VRM, operating independently or paralleled with other VRMs, needs to be unconditionally stable under all output voltage ranges and current transients with system board capacitance ranging from 5,000 µF to 20,000 µF and with less than 2.0 mΩ ESR.

1.1.8 Current Sharing - REQUIRED

Multi-processor applications require that current-sharing capability be available to avoid power-plane splits.

One pin of the VRM is reserved for control of star-point or single-wire current sharing. This pin will be connected to other VRMs within the system. VRMs designed for current sharing by means of accurate output control need not use this pin. If a VRM does not use the current share pin, the pin should not be connected on the module.

There is no time limit for response to power-up or transients: VRMs must meet all other electrical specifications during transitions, and output current levels must not damage the VRMs.

1.1.8.1 Current Sharing Tolerance - REQUIRED

The output current of any VRM should match the output current of all paralleled VRMs within 10% of the rated output current over the full output current range, except during initial power-up. For instance, if a particular VRM model is designed to supply a 50 A processor as a maximum, the difference between the output currents of two or more VRMs in parallel may be as much as 5 A at any value of current actually produced, even to the point where one VRM is producing 5 A, and one in parallel with it is producing no current in supplying a 5 A load.

The VRM must supply current equal to the total load multiplied by the ratio of (1 + tol) and (n + tol) where “tol” is the current sharing accuracy and “n” is the number of VRMs sharing the load. Current sharing accuracy better than 10% would allows the VRM to be designed for a lower output current. It may more cost effective to design to a looser current sharing accuracy and a higher output current. For example, assuming a 300 A load supplied by four parallel VRMs, each would need to be designed for 77.8 A and 80.5 A for respective current share accuracies of 5% and 10%.

1.1.8.2 Interoperability Between Manufacturers - EXPECTED

Current sharing among different VRM models, including VRMs from different manufacturers, is an expected feature. However, cost optimization and difficulties involved with fully testing interoperability may preclude use of this feature.

1.1.8.3 Negative Current Limit - EXPECTED

Because the output of the VRM will be connected in parallel with other voltage sources (other VRMs) the VRM should incorporate negative current limiting or equivalent functionality to protect the VRM from current from external voltage sources.

1.1.8.4 Current Sharing Methodology - PROPOSED

The method used to accomplish current sharing will depend upon the VRM design. The simplest method is to share unloaded set-point voltage references and rely on the drooping of the load line to force current sharing. If the shared error amplifier voltage method is used the VRMs must be of identical design. If auto-master/slave or current-average methods are used, then the Ishare bus output should operate between 0 to 2 V, representing 0 to 81 A. Current sharing during transients is accomplished by adhering to the load line as defined in Figure 1-1 and Figure 1-2 and Table 1-2 to a tolerance of ± 3 mV.

Hot-swapping capability is not a requirement.

1.2 Input Voltage and Current

1.2.1 Input Voltages - EXPECTED

The main power source for the VRM is 12 V +5%, -8%. This voltage is supplied by a conventional computer power supply through a cable to the system board. The system board will supply local bulk bypassing on the 12V rail. For input voltages outside the normal operating range, the VRM should either operate properly or shut down.

1.2.2 Load Transient Effects on Input Current - EXPECTED

When the VRM is providing an output current step to the load from $Iout_{MIN}$ to $Iout_{MAX}$ or $Iout_{MAX}$ to $Iout_{MIN}$ at the slew rate listed in Section 1.1.3, the slew rate of the input current to the VRM should not exceed 1.0 A/µs.

The system board needs sufficient bulk decoupling to ensure that the supply voltage on the system board does not go outside of regulation requirements during times of transient load on the VRM(s).

1.3 Control Inputs - REQUIRED

Control inputs should accept an open-collector, open-drain, open-switch-to-ground, low-voltage TTL or low-voltage CMOS signal.

1.3.1 Output Enable—(OUTEN) - REQUIRED

The VRM must accept an input signal to enable the output. An open-circuit or active high enables the VRM and a ground or active low disables the VRM. The input should have an internal pull-up resistor between 1 kΩ and 10 kΩ to 3.3 or 5.0 volts. The maximum low-input voltage is 0.8 V; the minimum high-input voltage is 1.7 V. These inputs should be capable of withstanding up to 5.5 V.

When disabled, the VRM should sink less than 100 mA from the 12 V Input and less than 1 A from shared VRMs that remain on.

1.3.2 Voltage Identification—(VID[4:0]) - REQUIRED

The VRM must accept five lines to set the nominal (maximum) voltage as defined by the table below. Five processor package pins will have a high-low pattern corresponding to the voltage required by the individual processor. When all five VID inputs are high (11111), the VRM should disable its output.

The maximum low-input voltage is 0.8V; the minimum high-input voltage is 1.7 V. Each VID input should have a 1 kΩ ± 10% pull-up resistor to 3.3V ± 5%.

Table 1-4. Voltage Identification (VID)

Processor Pins (0 = low, 1 = high)					Vcc (V)	Processor Pins (0 = low, 1 = high)					Vcc (V)
VID4[1]	VID3	VID2	VID1	VID0		VID4[1]	VID3	VID2	VID1	VID0	
1	1	1	1	1	Off	0	1	1	1	1	1.475
1	1	1	1	0	1.1	0	1	1	1	0	1.5
1	1	1	0	1	1.125	0	1	1	0	1	1.525
1	1	1	0	0	1.15	0	1	1	0	0	1.55
1	1	0	1	1	1.175	0	1	0	1	1	1.575
1	1	0	1	0	1.2	0	1	0	1	0	1.6
1	1	0	0	1	1.225	0	1	0	0	1	1.625
1	1	0	0	0	1.250	0	1	0	0	0	1.65
1	0	1	1	1	1.275	0	0	1	1	1	1.675
1	0	1	1	0	1.3	0	0	1	1	0	1.7
1	0	1	0	1	1.325	0	0	1	0	1	1.725
1	0	1	0	0	1.35	0	0	1	0	0	1.75
1	0	0	1	1	1.375	0	0	0	1	1	1.775
1	0	0	1	0	1.4	0	0	0	1	0	1.8
1	0	0	0	1	1.425	0	0	0	0	1	1.825
1	0	0	0	0	1.45	0	0	0	0	0	1.85

NOTE: When using the VRM as a cache regulator, only VID [3:0] will be utilized. VID4 should be pull up high as described in section Voltage Identification—(VID[4:0]) - REQUIRED.

1.4 Remote Sense (VO-sen+, VO-sen–) - EXPECTED

A star remote sense connection should be provided at the geometric center of the processors to allow the VRM to sense voltage and compensate for an output voltage offset of 55 mV in the power distribution path. VO-sen+ is the + sense line, and VO–sen– is the sense return. Differential sense inputs are required. In the event of an open sense line the VRM should maintain regulation through a local sense resistor on the VRM board. Systems that do not use remote sense will not connect these lines on the system board. The remote sense lines should draw no more than 10 mA, to minimize offset errors.

1.5 Power Good Output (PWRGD) - REQUIRED

The VRM must provide an open collector or equivalent Power Good signal consistent with TTL DC levels. This signal should transition to the open (>100 kΩ) state within 10 ms of the output voltage stabilizing within the range specified in Section 1.1.1. The signal should be in the low-impedance (to ground) state whenever $Vout_{VRM}$ is outside of the required range below and be in the open state whenever $Vout_{VRM}$ is within the range specified in Section 1.1.3. On power up, the PWRGD signal must remain in the low-impedance state until the output voltage has stabilized within the required tolerance.

1.5.1 Power Good Threshold Voltages - EXPECTED

The minimum voltage at which PWRGD is asserted should be the $Vvrm_{MIN}$ specified in Section 1.1.3, minus margin to prevent false de-assertion, but at least 95% of (VID minus 125 mV).

The maximum voltage at which PWRGD is asserted should be the VID (set-point) voltage, plus margin to prevent false de-assertion, but should be no greater than VID plus 250mV.

1.5.2 Power Good Operation - EXPECTED

This PWRGD output should be capable of sinking up to 4 mA, while maintaining a voltage of 0.4 V or lower. When the output is in the open state it should be capable of withstanding up to 5.5 V. Latch-up or damage cannot occur if the pull-up voltage on the system board is present with no +12 V input present.

VRM Power Good should remain low if the VRM is disabled by the Output Enable pin. System designers need to provide appropriate logic on the system board to decode VRM Power Good, VRM Enable, and system Power Good to prevent a false not-good condition (Power Good = low) when the VRM is disabled.

The VRM should be able to detect an internal failure and de-assert PWRGD even if the output is within the defined PWRGD range. It is sufficient for this purpose to detect whether all phases are switching at their output inductors. The intention of this provision is to detect failures independently when VRMs are sharing current to a common power plane in a multiple-processor system.

1.6 VRM Present (VRM-pres) - EXPECTED

This line is ground when the VRM is installed. The system board can use this signal to detect the presence of each VRM installed in the system.

1.7 Efficiency - PROPOSED

The efficiency of the VRM should be greater than 80% at maximum output current. It should not dissipate more power under any load condition than it does at maximum output current and maximum input voltage.

1.8 Isolation - PROPOSED

Isolation from input to output is optional. A transformer-based topology may have advantages over a non-isolated buck converter: Over-voltage due to a shorted FET is eliminated, and duty cycles can be optimized to simplify control or improve efficiency. A common ground between input and output is required with an isolated topology.

1.9 Fault Protection

These features are built into the VRM to prevent damage to the VRM or the circuits it powers.

1.9.1 Over Voltage Protection - EXPECTED

The VRM should provide over-voltage protection (OVP) by including a circuit, separate from the voltage sense path, capable of shutting off the output drive when the output voltage rises beyond Vtrip. If practical, the protection circuit should also enable a low-resistance path to ground, so that no single component failure results in the output voltage rising above Vtrip. A non-resettable or resettable fuse may be included in the input of the VRM for this function. The response time should be such that the output voltage will not exceed VID plus 250 mV.

Minimum Vtrip should be:

- The VID set-point voltage
- plus 55 mV to compensate for remote sense
- plus margin to prevent false trips.

Maximum Vtrip should be VID plus 250 mV.

No combination of input voltage or output load sequences should falsely trigger an OVP event.

1.9.2 Fuse Protection for Power Input - EXPECTED

The power input (12 V) should be protected with a fuse rated not greater than 30 A, which sustains all operating and inrush conditions and which “trips” only on catastrophic failure of the converter.

1.9.3 Overload Protection - EXPECTED

The VRM should be capable of withstanding a continuous, abnormally low resistance on the output without damage or over-stress to the unit. Output current under this condition will be limited to no more than 150% of the maximum rated output of the VRM. Latching off or hiccup mode is acceptable during over-current conditions. The VRM should be capable of starting into a constant current load of 50% of maximum rated load current with maximum load capacitance, as defined in Section 1.1.7, without tripping the OCP circuitry. Errors in current sharing (see Section 1.1.8) during startup should not cause OCP circuits to shut down the converter.

1.9.4 Reset After Shutdown - PROPOSED

If the VRM goes into a shutdown state due to a fault condition on its output (not an internal failure) it should return to normal operation after the fault has been removed, or after the fault has been removed and power has been cycled off and on.

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2 Module Layout Guidelines

2.1 VRM Connector - EXPECTED

The VRM interface with the system board is a 100 mil-pitch, 62-pin edge connector, with an overall 3.95” length. The connector uses a retention clip or side latches to hold the VRM in place. The connector has a maximum rated temperature of 90°C, based on 2-oz. minimum copper lands on the VRM PCB and 19 contact pairs carrying 4.26 A each.

Table 2-1. Connector Part Numbers and Descriptions

Attributes		VRM 9.0 12V Input	VRM 9.1 12V Input	VRM 9.1 48V Input
Key Located between slots		11, 12	12, 13	4, 5
Omit Pin for Keying		6	6	6
Max Current per Contact Pair		3.6 amps	4.26 amps	4.26 amps
Max Current Output – VRM		68 amps	81 amps	81 amps
Mounting	Connector Style	Part Numbers (Tyco)		
Solder Tail	Connector	1364125-1	1489162-1	1489162-2
	Clip	1364124-1	1364124-1	1364124-1
	Connector with Latch	145432-3	N/A	N/A
	Connector with Latch Supports	1364666-1	1489165-1	1489165-2
Press Fit	Connector, clip, latch	†		

NOTE: † Please contact vendor(s) for mounting and latching options.

See Table 2-2 for the VRM pinout definitions.

Table 2-2. VRM Pins

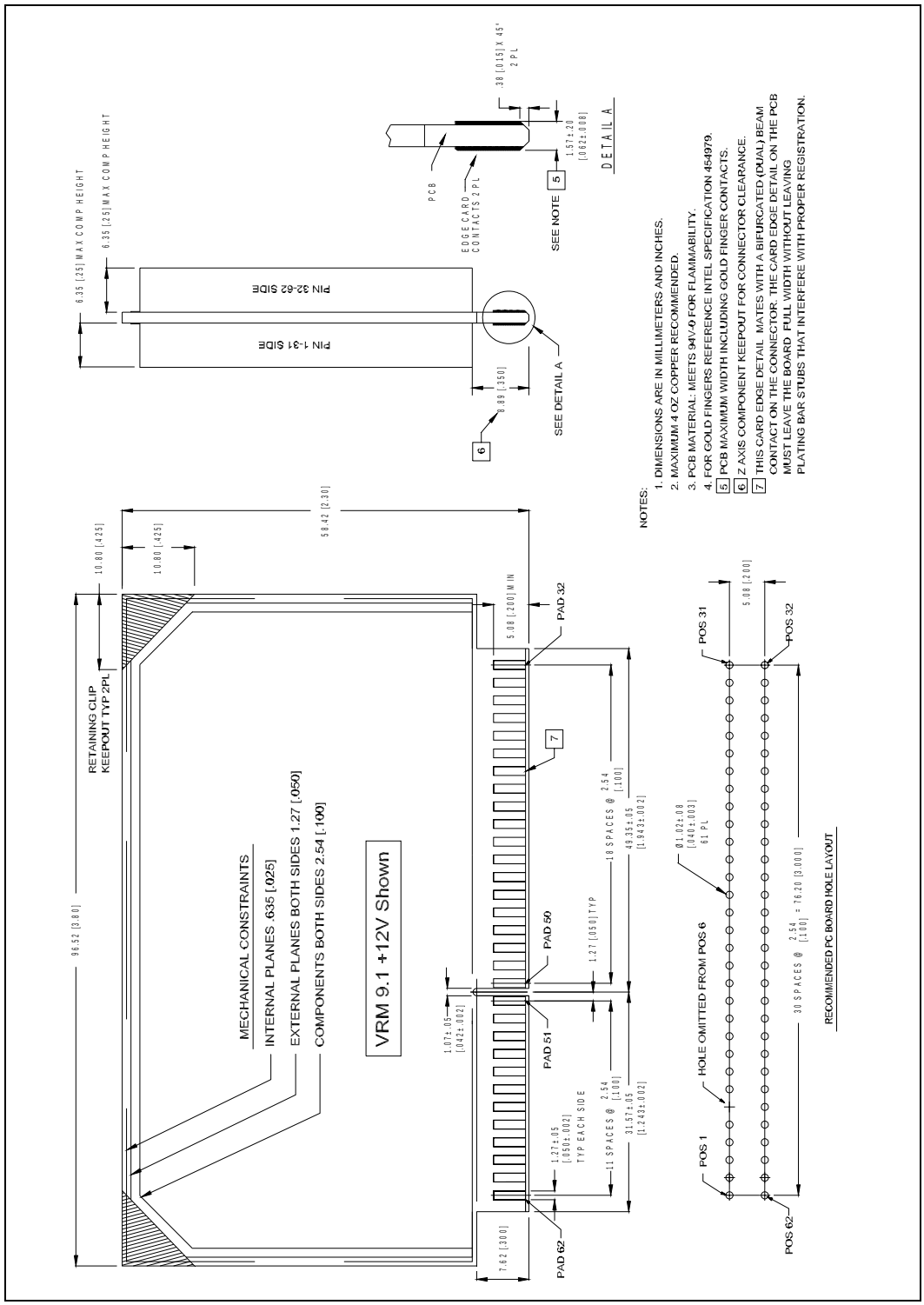
Pin	Function		Pin	Function		Pin	Function		Pin	Function
1	VIN+		62	VIN-		16	VO+		47	VO+
2	VIN+		61	VIN-		17	VO-		46	VO-
3	VIN+		60	VIN-		18	VO+		45	VO+
4[1]	VIN+		59[1]	VIN-		19	VO-		44	VO-
5[1]	Reserved[3]		58[1]	VRM-pres		20	VO+		43	VO+
6	key		57	VID4		21	VO-		42	VO-
7	VID3		56	VID2		22	VO+		41	VO+
8	VID1		55	VID0		23	VO-		40	VO-
9	Reserved[3]		54	Ishare		24	VO+		39	VO+
10	PWRGD		53	OUTEN		25	VO-		38	VO-
11	VO-sen-		52	VO-sen+		26	VO+		37	VO+
12[2]	Reserved[3]		51[2]	Reserved[3]		27	VO-		36	VO-
13[2]	VO-		50[2]	VO+		28	VO+		35	VO+
14	VO+		49	VO+		29	VO-		34	VO-
15	VO-		48	VO-		30	VO+		33	VO+
						31	VO-		32	VO-

NOTES:
1. A single notch between pins 4&5 and between pins 58&59 is reserved for +48 V input VRMs
2. A single notch between pins 12&13 and between pins 50&51 identifies a +12 V input VRM
3. Reserved pins can be used for an I^2C interface:
   - 5 12C_CLK
   - 9 12C_DATA
   - 12 12C_A0
   - 51 12C_A1

2.2 Mechanical Dimensions - PROPOSED

The maximum outline dimensions of the VRM should be as shown in Figure 2-1.

Figure 2-1. VRM Footprint and Space Requirements



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3 Environmental Conditions

The VRM design, including materials, should be consistent with the manufacture of units that meet the environmental requirements specified below.

3.1 Operating Temperature - PROPOSED

The VRM should meet all electrical requirements when operated over an ambient temperature of 0^{o}C to +60^{o}C at full load with a minimum airflow of 400 LFM.

Operating conditions should be considered to include 10 cycles between min and max temperature at a rate of 10^{o}C/hour and a dwell time of 30 minutes at extremes.

3.2 VRM Board Temperature - REQUIRED

To maintain the connector within its operating temperature range, the board temperature at the connector interface, cannot exceed a temperature of 90^{o} C.

At no time during operation is the board permitted to exceed 90^{o} C within a distance of 2.54 mm [.100 in] from the top of the connector (0.4” from board edge). In order not to exceed 90^{o} C, it is recommended that the board be constructed from 2 ounce copper cladding.

The VRM board must contain gold lands (fingers) for interfacing with the VRM connector that are 1.27 ± 0.05 mm [.050 ± .002 in] wide by 5.08 mm [.200 in] minimum long and spaced 2.54 ± 0.05 mm [.100 ± .002 in] apart. Traces from the lands to the power plane should be a minimum of 0.89 mm [.035 in] wide and of a minimal length.

3.3 Non-Operating Temperature - PROPOSED

The VRM should not be damaged when exposed to temperatures between –40^{o} C and +70^{o} C. These should be considered to include 50 cycles of min to max temperatures at 20^{o} / hour with a dwell time of 20 minutes at extremes

3.4 Humidity - PROPOSED

85% relative – operating

95% relative – non-operating

3.5 Altitude - PROPOSED

- 10 k feet – operating
- 50 k feet – non-operating

3.6 Electrostatic Discharge - PROPOSED

Testing should be in accordance with IEC 61000-4-2.

Operating – 15 kV initialization level. The direct ESD event should cause no out-of-regulation conditions – including overshoot, undershoot and nuisance trips of over-voltage protection, over-current protection or remote shutdown circuitry.

Non-operating - 25 kV initialization level. The direct ESD event should not cause damage to VRM circuitry.

3.7 Shock and Vibration - PROPOSED

The VRM should not be damaged and the interconnect integrity not compromised during:

A shock of 50 G with an 11 millisecond half sine wave, non-operating, the shock to be applied in each of the orthogonal axes.

Vibration of 0.01 G^2 per Hz at 5 Hz, sloping to 0.02 G^2 per Hz at 20 Hz and maintaining 0.02 G^2 per Hz from 20 Hz to 500 Hz, non-operating, applied in each of the orthogonal axes.

3.8 Electromagnetic Compatibility - PROPOSED

Design, including materials, should be consistent with the manufacture of units that comply with the limits of FCC Class B and CISPR22 Class B for radiated emissions.

3.9 Reliability - PROPOSED

Design, including materials, should be consistent with the manufacture of units with an MTBF of 500,000 hours of continuous operation at 55° C maximum, outputs loaded and worst-case line, while meeting specified requirements. MTBF should be calculated in accordance with MIL-STD-217F or Bellcore.

3.10 Safety - PROPOSED

The VRM should be UL Recognized to standard UL1950 3rd Ed., including requirements of IEC950 and EN 60950. Plastic parts and printed wiring board are to be UL Recognized with 94V-0 flame class.

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