# Dual-Core Intel® Xeon® Processor 2.80 GHz

## Thermal/Mechanical Design Guidelines

*October 2005*

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# Contents

# Figures

# Tables

# Revision History

| Reference Number | Revision Number | Description | Date |
|---|---|---|---|
| 309160 | -001 | • Initial release of the document. | October 2005 |

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# 1 Introduction

## 1.1 Objective

The purpose of this guide is to describe the reference thermal solution and design parameters required for the Dual-Core Intel® Xeon® processor 2.80 GHz. It is also the intent of this document to comprehend and demonstrate the processor cooling solution features and requirements. Furthermore, this document provides an understanding of the processor thermal characteristics, and discusses guidelines for meeting the thermal requirements imposed on the entire life of the processor. The thermal/mechanical solutions described in this document are intended to aid component and system designers in the development and evaluation of processor compatible solutions.

## 1.2 Scope

The thermal/mechanical solutions described in this document pertain to solutions intended for use with the Dual-Core Intel Xeon processor 2.80 GHz in 1U and 2U+ form factor systems. This document contains the mechanical and thermal requirements of the processor cooling solutions. In case of conflict, the data in the *Dual-Core Intel® Xeon® Processor 2.80 GHz Datasheet* supersedes any data in this document. Additional information is provided as a reference in the appendix section(s).

## 1.3 References

Material and concepts available in the following documents may be beneficial when reading this document.

**Table 1-1. References (Sheet 1 of 2)**

| Document | Comment |
|---|---|
| *Dual-Core Intel® Xeon® Processor 2.80 GHz Datasheet* | http://developer.intel.com/ |
| *mPGA604 Socket Design Guidlines* | http://developer.intel.com/ |
| *Dual-Core Intel® Xeon® Processor 2.80 GHz and Intel® Xeon® Processor 7000 Sequence Cooling Solution Mechanical Models* | http://developer.intel.com/ |
| *Dual-Core Intel® Xeon® Processor 2.80 GHz and Intel® Xeon® Processor 7000 Sequence Cooling Solution Thermal Models* | http://developer.intel.com/ |
| *Dual-Core Intel® Xeon® Processor 2.80 GHz and Intel® Xeon® Processor 7000 Sequence Mechanical Models* | http://developer.intel.com/ |
| *Prescott, Nocona, and Potomac Processor BIOS Writer's Guide* | http://developer.intel.com/ |
| *IA-32 Intel® Architecture Software Developer's Manual and Intel NetBurst® Microarchitecture BIOS Writer's Guide* | http://developer.intel.com/ |
| *Intel® Xeon® Processor Family Thermal Test Vehicle User's Guide* | http://developer.intel.com/ |
| *Chassis Stregnth and Stiffness Measurement and Improvement Guidelines for Direct Chassis Attach Solutions* | http://developer.intel.com/ |

**Table 1-1. References (Sheet 2 of 2)**

| Document | Comment |
|---|---|
| Thin Electronics Bay Specification (A Server System Infrastructure (SSI) Specification for Thin Servers | www.ssiforum.com |
| European Blue Angel Recycling Standards | http://www.blauer-engel.de |

**NOTE:** Contact your Intel field sales representative for the latest revision and order number of this document.

## 1.4 Definition of Terms

**Table 1-2. Terms and Definitions (Sheet 1 of 2)**

| Term | Description |
|---|---|
| Bypass | Bypass is the area between a passive heatsink and any object that can act to form a duct. For this example, it can be expressed as a dimension away from the outside dimension of the fins to the nearest surface. |
| FMB | Flexible Motherboard Guideline: an estimate of the maximum value of a processor specification over certain time periods. System designers should meet the FMB values to ensure their systems are compatible with future processor releases. |
| FSC | Fan Speed Control |
| IHS | Integrated Heat Spreader: a component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface. |
| mPGA604 | The surface mount Zero Insertion Force (ZIF) socket designed to accept the Dual-Core Intel® Xeon® processor 2.80 GHz. |
| $P_{MAX}$ | The maximum power dissipated by a semiconductor component. |
| $\Psi_{CA}$ | Case-to-ambient thermal characterization parameter (psi). A measure of thermal solution performance using total package power. Defined as $(T_{CASE} - T_{LA})$ / Total Package Power. Heat source should always be specified for $\Psi$ measurements. |
| $\Psi_{CS}$ | Case-to-sink thermal characterization parameter. A measure of thermal interface material performance using total package power. Defined as $(T_{CASE} - T_S)$ / Total Package Power. |
| $\Psi_{SA}$ | Sink-to-ambient thermal characterization parameter. A measure of heatsink thermal performance using total package power. Defined as $(T_S - T_{LA})$ / Total Package Power. |
| $T_{CASE}$ | The case temperature of the processor, measured at the geometric center of the topside of the IHS. |
| $T_{CASE\_MAX}$ | The maximum case temperature as specified in a component specification. |
| TCC | Thermal Control Circuit: Thermal monitor uses the TCC to reduce the die temperature by using clock modulation when the die temperature is very near its operating limits. |
| $T_{CONTROL}$ | A processor unique value, which defines the lower end of the thermal profile and is targeted to be used in fan speed control mechanisms. |
| Offset | A value programmed into each processor during manufacturing that can be obtained by reading IA_32_TEMPERATURE_TARGET MSR. This is a static and a unique value. Refer to *Prescott, Nocona, and Potomac Processor BIOS Writer's Guide* for further details. |
| TDP | Thermal Design Power: Thermal solution should be designed to dissipate this target power level. TDP is not the maximum power that the processor/chipset can dissipate. |
| Thermal Monitor | A feature on the processor that can keep the processor's die temperature within factory specifications under nearly all conditions. |

### Table 1-2. Terms and Definitions (Sheet 2 of 2)

| Term | Description |
|---|---|
| Thermal Profile | Line that defines case temperature specification of a processor at a given power level. |
| TIM | Thermal Interface Material: The thermally conductive compound between the heatsink and the processor case. This material fills the air gaps and voids, and enhances the transfer of the heat from the processor case to the heatsink. |
| $T_{LA}$ | The measured ambient temperature locally surrounding the processor. The ambient temperature should be measured just upstream of a passive heatsink or at the fan inlet for an active heatsink. |
| $T_{SA}$ | The system ambient air temperature external to a system chassis. This temperature is usually measured at the chassis air inlets. |
| CEK | Common Enabling Kit (includes the enabling solution components) |
| U | A unit of measure used to define server rack spacing height. 1U is equal to 1.75 in, 2U equals 3.50 in, etc. |

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# 2 Thermal/Mechanical Reference Design

## 2.1 Mechanical Requirements

The mechanical performance of the processor cooling solution must satisfy the requirements described in this section.

### 2.1.1 Processor Mechanical Parameters

**Table 2-1. Processor Mechanical Parameters Table**

| Parameter | Minimum | Maximum | Unit | Notes |
|---|---|---|---|---|
| Volumetric Requirements and Keepouts | | | | Refer to drawings in Appendix A |
| Heatsink Mass | | 1000<br>2.2 | g<br>lbs | |
| Static Compressive Load | 44<br>10 | 222<br>50 | N<br>lbf | 1,2,3,4 |
| | 44<br>10 | 288<br>65 | N<br>lbf | 1,2,3,5 |
| Dynamic Compressive Load | N/A<br>NA | 222 N + 0.45 kg * 100 G<br>50 lbf (static) + 1 lbm * 100 G | N<br>lbf | 1,3,4,6,7 |
| | N/A<br>NA | 288 N + 0.45 kg * 100 G<br>65 lbf (static) + 1 lbm * 100 G | N<br>lbf | 1,3,5,6,7 |
| Transient | N/A | 445<br>100 | N<br>lbf | 1,3,8 |

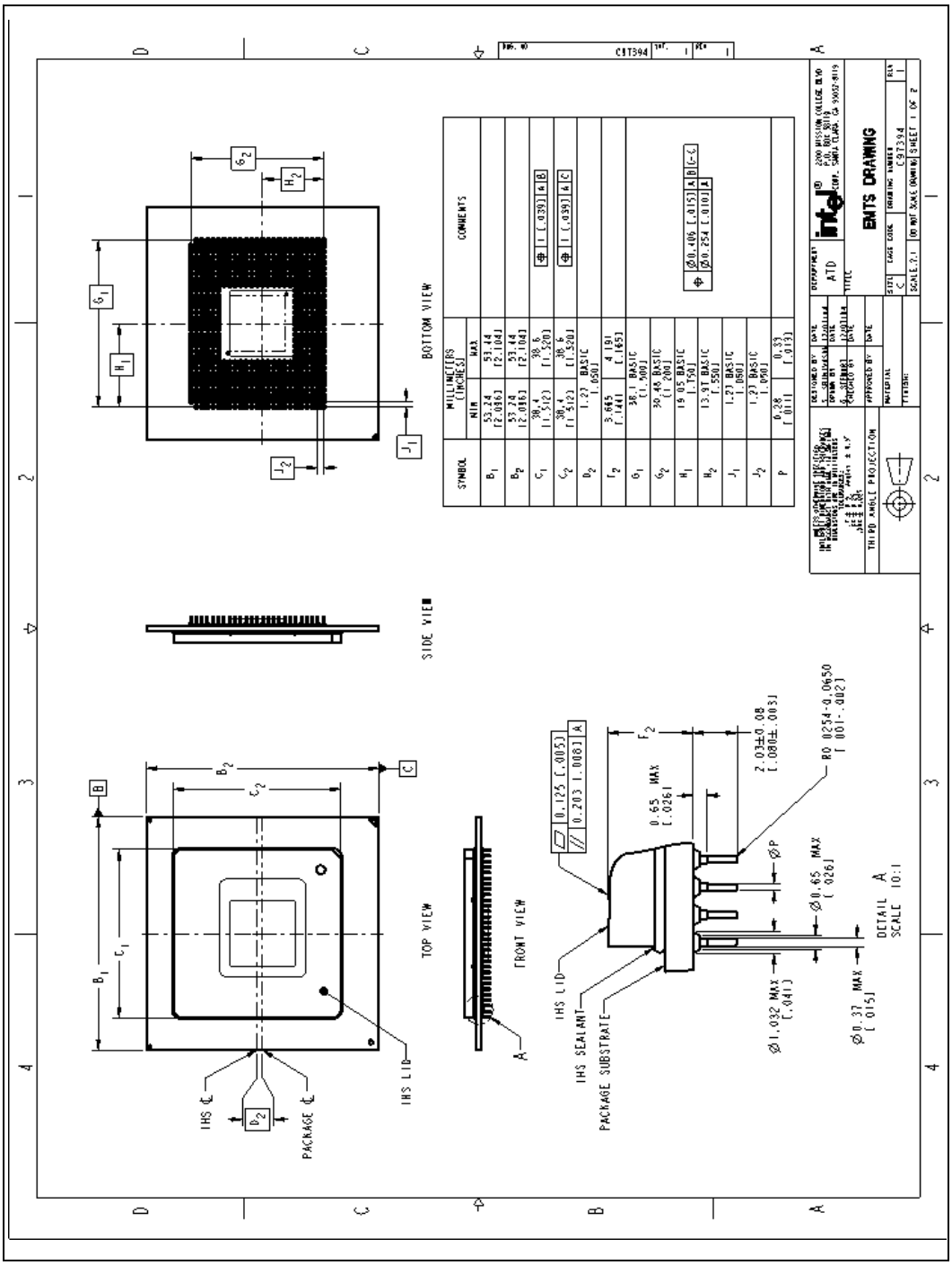
**NOTES:** In the case of a discrepancy, the most recent processor datasheet supersedes targets listed in the above table.

1. These specifications apply to uniform compressive loading in a direction perpendicular to the IHS top surface.
2. This is the minimum and maximum static force that can be applied by the heatsink and retention solution to maintain the heatsink and processor interface.
3. These parameters are based on limited testing for design characterization. Loading limits are for the package only and do not include the limits of the processor socket.
4. This specification applies for thermal retention solutions that allow baseboard deflection.
5. This specification applies for thermal retention solutions that prevent baseboard deflection.
6. Dynamic loading is defined as an 11 ms duration average load superimposed on the static load requirement.
7. Experimentally validated test condition used a heatsink mass of 1 lbm (~0.45 kg) with 100 G acceleration measured at heatsink mass. The dynamic portion of this specification in the product application can have flexibility in specific values, but the ultimate product of mass times acceleration should not exceed this validated dynamic load (1 lbm x 100 G = 100 lb).
8. Transient loading is defined as a 2 second duration peak load superimposed on the static load requirement, representative of loads experienced by the package during heatsink installation.

### 2.1.2 Dual-Core Intel® Xeon® Processor 2.80 GHz Package

The Dual-Core Intel® Xeon® processor 2.80 GHz is packaged using the flip-chip micro pin grid array 4 (FC-mPGA4) package technology. Please refer to the *Dual-Core Intel® Xeon® Processor 2.80 GHz Datasheet* for detailed mechanical specifications. The Dual-Core Intel Xeon processor 2.80 GHz Mechanical drawing, Figure 2-1, provides the mechanical information for Dual-Core Intel Xeon processor 2.80 GHz. The stack up height of the processor in the socket is shown in Appendix A. The drawing is superseded with the drawing in the processor datasheet, should there be any conflicts.

**Figure 2-1. Dual-Core Intel® Xeon® Processor 2.80 GHz Mechanical Drawing**




The package includes an integrated heat spreader (IHS). The IHS transfers the non-uniform heat from the die to the top of the IHS, out of which the heat flux is more uniform and spread over a larger surface area (not the entire IHS area). This allows more efficient heat transfer out of the package to an attached cooling device. The IHS is designed to be the interface for contacting a heatsink. Details can be found in the *Dual-Core Intel® Xeon® Processor 2.80 GHz Datasheet*.

The processor connects to the baseboard through a 604-pin surface mount, zero insertion force (ZIF) socket. A description of the socket can be found in the *mPGA604 Socket Design Guidelines*.

The processor package has mechanical load limits that are specified in the processor datasheet and in Table 2-1. These load limits should not be exceeded during heatsink installation, removal, mechanical stress testing, or standard shipping conditions. For example, when a compressive static load is necessary to ensure thermal performance of the Thermal Interface Material (TIM) between the heatsink base and the IHS, it should not exceed the corresponding specification given in the processor datasheet.

The heatsink mass can also add additional dynamic compressive load to the package during a mechanical shock event. Amplification factors due to the impact force during shock must be taken into account in dynamic load calculations. The total combination of dynamic and static compressive load should not then exceed the processor compressive dynamic load specified in the datasheet and in Table 2-1 during a vertical shock. It is not recommended to use any portion of the processor substrate as a mechanical reference or load- bearing surface in either static or dynamic compressive load conditions.

### 2.1.3 Dual-Core Intel Xeon Processor 2.80 GHz Considerations

An attachment mechanism must be designed to support the heatsink since there are no features on the mPGA604 socket to directly attach a heatsink. In addition to holding the heatsink in place on top of the IHS, this mechanism plays a significant role in the robustness of the system in which it is implemented, in particular:

- Ensuring thermal performance of the TIM applied between the IHS and the heatsink. TIMs, especially ones based on phase change materials, are very sensitive to applied pressure: the higher the pressure, the better the initial performance. TIMs such as thermal greases are not as sensitive to applied pressure. Refer to Section 2.4.2 for information on tradeoffs made with TIM selection. Designs should consider possible decrease in applied pressure over time due to potential structural relaxation in enabled components.
- Ensuring system electrical, thermal, and structural integrity under shock and vibration events. The mechanical requirements of the attach mechanism depend on the weight of the heatsink and the level of shock and vibration that the system must support. The overall structural design of the baseboard and system must be considered when designing the heatsink attach mechanism. Their design should provide a means for protecting mPGA604 socket solder joints as well as preventing package pullout from the socket.

***Note:*** The load applied by the attachment mechanism must comply with the package specifications, along with the dynamic load added by the mechanical shock and vibration requirements, as identified in Section 2.1.1.

A potential mechanical solution for heavy heatsinks is the direct attachment of the heatsink to the chassis pan. In this case, the strength of the chassis pan can be utilized rather than solely relying on the baseboard strength. In addition to the general guidelines given above, contact with the baseboard surfaces should be minimized during installation in order to avoid any damage to the baseboard.

The Intel reference design for Dual-Core Intel Xeon processor 2.80 GHz is using such a heatsink attachment scheme. Refer to Section 2.4 for further information regarding the Intel reference mechanical solution.

## 2.2 Thermal Requirements

The operating thermal limits of the processor are defined by the Thermal Profile. The intent of the Thermal Profile specification is to support acoustic noise reduction through fan speed control and ensure the long-term reliability of the processor. This specification requires that the temperature at the center of the processor IHS, known as ($T_{CASE}$) remains within a certain temperature specification. Compliance with the $T_{CASE}$ specification is required to achieve optimal operation and long-term reliability (See Appendix B for Case Temperature definition and measurement methods).

To ease the burden on thermal solutions, the Thermal Monitor feature and associated logic have been integrated into the silicon of the processor. One feature of the Thermal Monitor is the Thermal Control Circuit (TCC). When active, the TCC lowers the processor temperature by reducing the power consumed by the processor. This is done by changing the duty cycle of the internal processor clocks, resulting in a lower effective frequency. When active, the TCC turns the processor clocks off and then back on with a predetermined duty cycle.

By taking advantage of the Thermal Monitor features, system designers may reduce thermal solution cost by designing to the Thermal Design Power (TDP) instead of maximum power. TDP should be used for processor/chipset thermal solution design targets. TDP is not the maximum power that the processor/chipset can dissipate. TDP is based on measurements of processor power consumption while running various high power applications. This data set is used to determine those applications that are interesting from a power perspective. These applications are then evaluated in a controlled thermal environment to determine their sensitivity to activation of the thermal control circuit. This data set is then used to derive the TDP targets published in the processor datasheet. The Thermal Monitor can protect the processor in rare workload excursions above TDP. Therefore, thermal solutions should be designed to dissipate this target power level.

The relationship between TDP to the thermal profile, and thermal management logic and thermal monitor features, is discussed in the sections to follow. The thermal management logic and thermal monitor features are discussed in *Dual-Core Intel® Xeon® Processor 2.80 GHz Datasheet*.

### 2.2.1 Thermal Profile

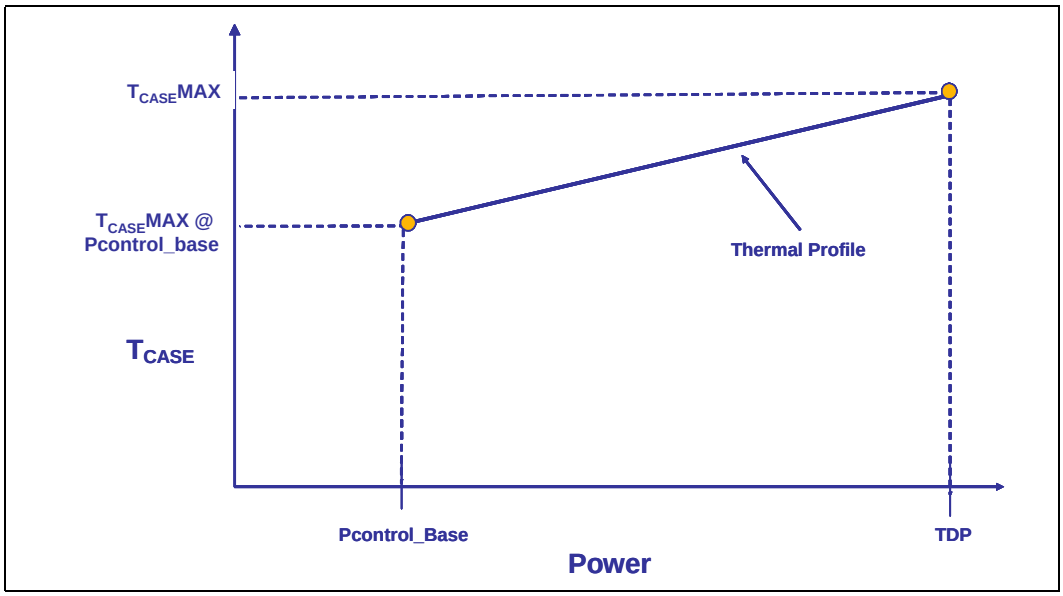
The thermal profile is a linear line that defines the relationship between a processor's case temperature and its power consumption as shown in Figure 2-2. The equation of the thermal profile is defined as:

**Equation 2-1. y = ax + b**

*Where*:

| | | |
|---|---|---|
| y | = | Processor case temperature, $T_{CASE}$ (°C) |
| x | = | Processor power consumption (W) |
| a | = | Case-to-ambient thermal resistance, $\Psi_{CA}$ (°C/W) |
| b | = | Processor local ambient temperature, $T_{LA}$ (°C) |

**Figure 2-2. Thermal Profile Diagram**




The higher end point of the Thermal Profile represents the processor's TDP and the associated maximum case temperature ($T_{CASE}$MAX). The lower end point of the Thermal Profile represents the power value ($P_{CONTROL\_BASE}$) and the associated case temperature ($T_{CASE}$MAX@ $P_{CONTROL\_BASE}$) for the lowest possible theoretical value of $T_{CONTROL}$ (see Section 2.2.2). The slope of the Thermal Profile line represents the case-to-ambient resistance of the thermal solution with the y-intercept being the local processor ambient temperature. The slope of the Thermal Profile is constant between $P_{CONTROL\_BASE}$ and TDP, which indicate that all frequencies of a processor defined by the Thermal Profile, will require the same heatsink case-to-ambient resistance.

In order to satisfy the Thermal Profile specification, a thermal solution must be at or below the Thermal Profile line for the given processor when its diode temperature is greater than $T_{CONTROL}$ (refer to Section 2.2.2). The Thermal Profile allows the customers to make a trade-off between the thermal solution case-to-ambient resistance and the processor local ambient temperature that best suits their platform implementation (refer to Section 2.3.3). There can be multiple combinations of thermal solution case-to-ambient resistance and processor local ambient temperature that can meet a given Thermal Profile. If the case-to-ambient resistance and the local ambient temperature are known for a specific thermal solution, the Thermal Profile of that solution can easily be plotted against the Thermal Profile specification. As explained above, the case-to-ambient resistance represents the slope of the line and the processor local ambient temperature represents the y-axis intercept. Hence the $T_{CASE}$ values of a specific solution can be calculated at the TDP and $P_{CONTROL\_BASE}$ power levels. Once these points are determined, they can be joined by a line, which represents the Thermal Profile of the specific solution. If that line stays at or below the Thermal Profile specification, then that particular solution is deemed as a compliant solution.

## 2.2.2 $T_{CONTROL}$ Definition

$T_{CONTROL}$ is a temperature specification based on a temperature reading from the processor's thermal diode. $T_{CONTROL}$ defines the lower end of the Thermal Profile line for a given processor, and it can be described as a trigger point for fan speed control implementation. The value for $T_{CONTROL}$ is calibrated in manufacturing and configured for each processor individually. For the

Dual-Core Intel Xeon processor 2.80 GHz, the $T_{CONTROL}$ value is obtained by reading a processor model specific register (MSR) and adding this offset value to a base value. The equation for calculating $T_{CONTROL}$ is:

**Equation 2-2. $T_{CONTROL} = T_{CONTROL\_BASE}$ + Offset**

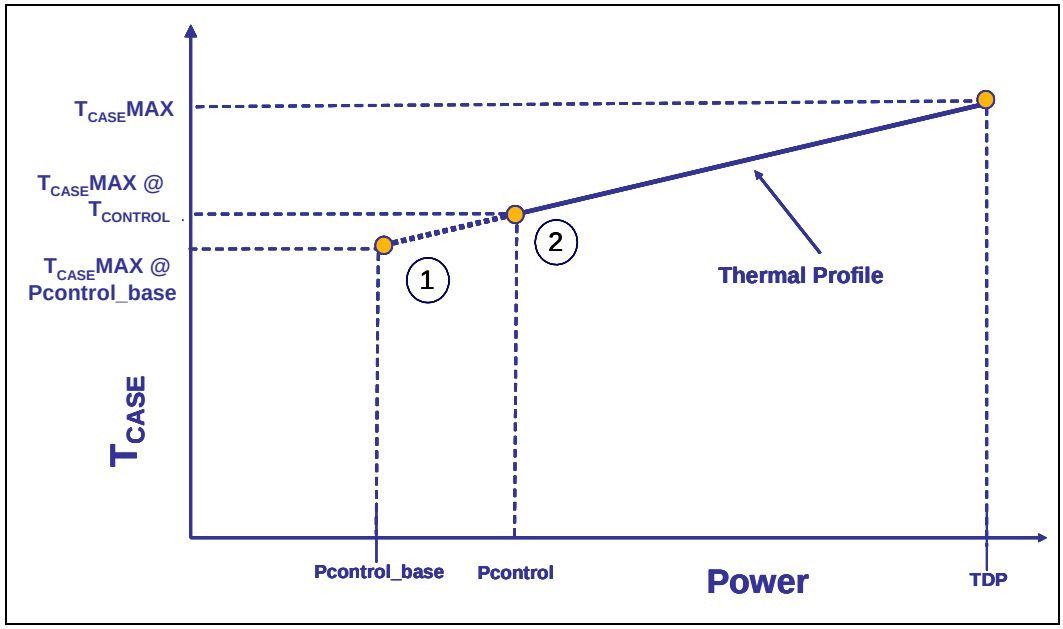
*Where*:

$T_{CONTROL\_BASE}$ = A fixed base value defined for a given processor generation as published in the processor datasheet.

Offset = A value programmed into each processor during manufacturing that can be obtained by reading the IA32_TEMPERATURE_TARGET MSR. This is a static and a unique value. Refer to the *Prescott, Nocona and Potomac Processor BIOS Writer's Guide* for further details.

The $T_{CONTROL\_BASE}$ value for the Dual-Core Intel Xeon processor 2.80 GHz is 50°C. The Offset value, which depends on several factors (i.e. leakage current), can be any number between 0 and ($T_{CASE}$MAX - $T_{CONTROL\_BASE}$). Figure 2-3 depicts the interaction between the Thermal Profile and $T_{CONTROL}$ for an Offset value that is greater than 0 (i.e. $T_{CONTROL}$ greater than $T_{CONTROL\_BASE}$).

**Figure 2-3. $T_{CONTROL}$ and Thermal Profile Interaction**



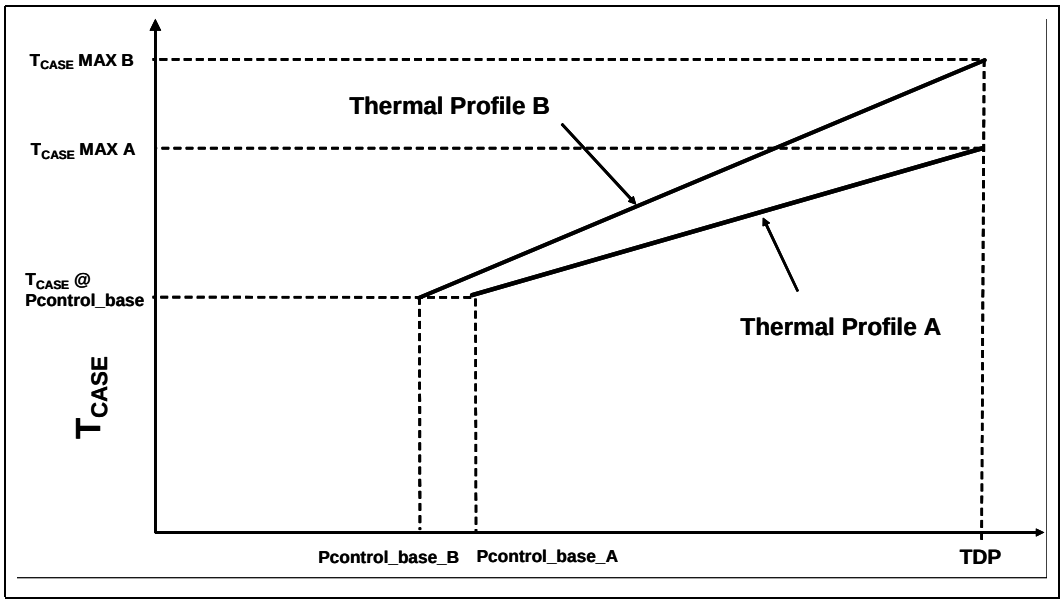

Since $T_{CONTROL}$ is a processor diode temperature value, an equivalent $T_{CASE}$ temperature must be determined to plot the $T_{CASE}$ MAX @ $T_{CONTROL}$ point on the Thermal Profile graph. Location 1 on the Thermal Profile represents a $T_{CASE}$ value corresponding to an Offset of 0 (the theoretical minimum for the given processor family). Any Offset value greater than 0 moves the point where the Thermal Profile must be met upwards, as shown by location 2 on the graph. If the diode temperature is less than $T_{CONTROL}$, then the case temperature is permitted to exceed the Thermal Profile, but the diode temperature must remain at or below $T_{CONTROL}$. In other words, there is no $T_{CASE}$ specification for the processor at power levels less than Pcontrol. The thermal solution for the processor must be able to keep the processor's $T_{CASE}$ at or below the $T_{CASE}$ values defined by the Thermal Profile between the $T_{CASE}$MAX @$T_{CONTROL}$ and $T_{CASE}$MAX points at the corresponding power levels.

Refer to Section 2.3.1 for the implementation of the $T_{CONTROL}$ value in support of fan speed control (FSC) design to achieve better acoustic performance.

## 2.2.3 Dual Thermal Profile Concept for the Dual-Core Intel Xeon Processor 2.80 GHz

The Dual-Core Intel Xeon processor 2.80 GHz is designed to go into various form factors, including the volumetrically constrained 1U and custom blade form factors. Due to certain limitations of such form factors (i.e. airflow, thermal solution height), it is very challenging to meet the thermal requirements of the processor. To mitigate these form factor constraints, Intel has developed a dual Thermal Profile specification, shown in Figure 2-4.

**Figure 2-4. Dual Thermal Profile Diagram**




The Thermal Profile A is based on Intel's 2U+ air cooling solution. Designing to Thermal Profile A ensures that no measurable performance loss due to Thermal Control Circuit (TCC) activation is observed in the processor. It is expected that TCC would only be activated for very brief periods of time when running a worst-case real world application in a worst-case thermal condition. These brief instances of TCC activation are not expected to impact the performance of the processor. A worst case real world application is defined as a commercially available, useful application which dissipates a power equal to, or above, the TDP for a thermally relevant timeframe. One example of a worst-case thermal condition is when a processor local ambient temperature is at or above 43 °C for Dual-Core Intel Xeon processor 2.80 GHz Thermal Profile A.

Thermal Profile B supports volumetrically constrained platforms (i.e. 1U, blades, etc.), and is based on Intel's 1U air cooling solution. Because of the reduced capability represented by such thermal solutions, designing to Thermal Profile B results in an increased probability of TCC activation and an associated measurable performance loss. Refer to *Dual-Core Intel® Xeon® Processor 2.80 GHz Datasheet* for more details on the Thermal Monitor features. Measurable performance loss is defined to be any degradation in the processor's performance greater than 1.5%. The 1.5% number is chosen as the baseline since the run-to-run variation in a given performance benchmark is typically between 1 - 2%.

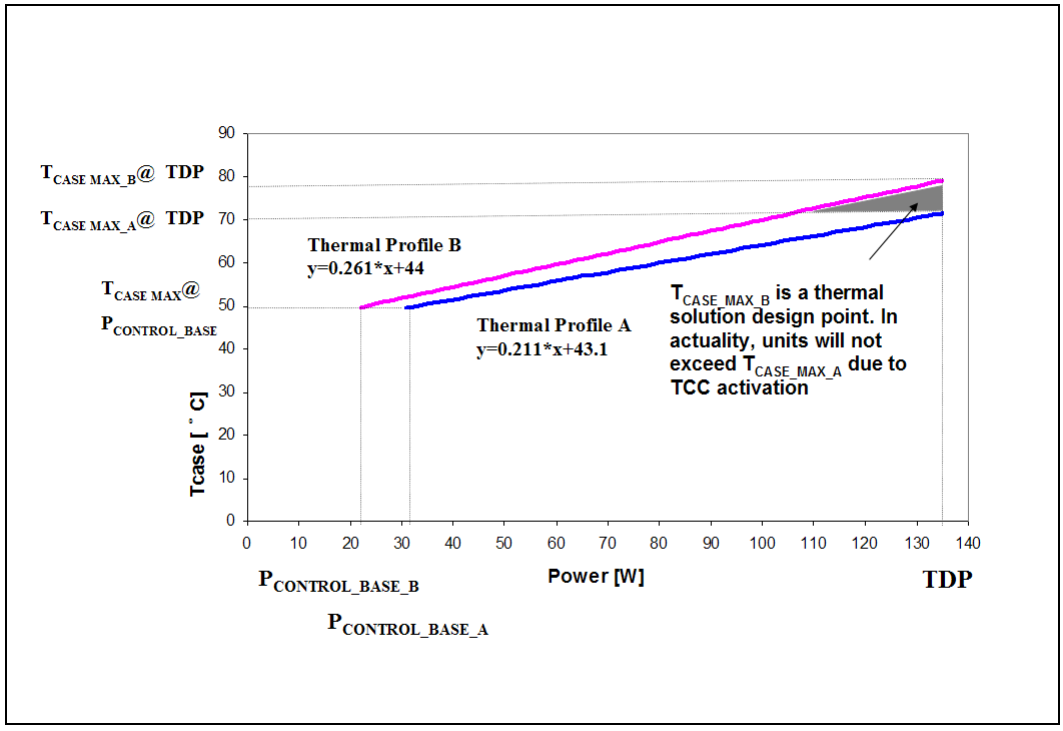
Although designing to Thermal Profile B results in increased $T_{CASE}$ temperatures compared to Thermal Profile A at a given power level, both of these Thermal Profiles ensure that Intel's long-term processor reliability requirements are satisfied. In other words, designing to Thermal Profile B does not impose any additional risk to Intel's long-term reliability requirements. Thermal solutions that exceed Thermal Profile B specification are considered incompliant and will adversely affect the long-term reliability of the processor.

Refer to the *Dual-Core Intel® Xeon® Processor 2.80 GHz Datasheet* or Section 2.2.4 for the Thermal Profile A and Thermal Profile B specifications. Section 2.4 of this document also provides details on the 2U+ and 1U Intel reference thermal solutions that are designed to meet the Dual-Core Intel Xeon processor 2.80 GHz Thermal Profile A and Thermal Profile B respectively.

## 2.2.4 Performance Targets

The Thermal Profile specifications for this processor are published in the *Dual-Core Intel® Xeon® Processor 2.80 GHz Datasheet*. These Thermal Profile specifications are shown as a reference in the subsequent discussions.

**Figure 2-5. Thermal Profiles A and B for the Dual-Core Intel Xeon Processor 2.80 GHz**




***Note:*** The thermal specifications shown in this graph are for reference only. Refer to the *Dual-Core Intel® Xeon® Processor 2.80 GHz Datasheet* for the Thermal Profile specifications. In case of conflict, the data information in the datasheet supersedes any data in this figure.

Table 2-2 describes thermal performance targets for the processor cooling solution enabled by Intel.

**Table 2-2. Intel Reference Heatsink Performance Targets for the Dual-Core Intel Xeon Processor 2.80 GHz**

| Thermal Solution Type | Target Thermal Profile | $T_{LA}$ Assumption (°C) | TDP (W) | Thermal Performance Target, Ψca (Mean + 3σ) (°C/W) |
|---|---|---|---|---|
| 2U+ Form Factor | Thermal Profile A | 40°C | 135 | 0.234 |
| 1U Form Factor | Thermal Profile B | 40°C | 135 | 0.290 |

### 2.2.5 Altitude

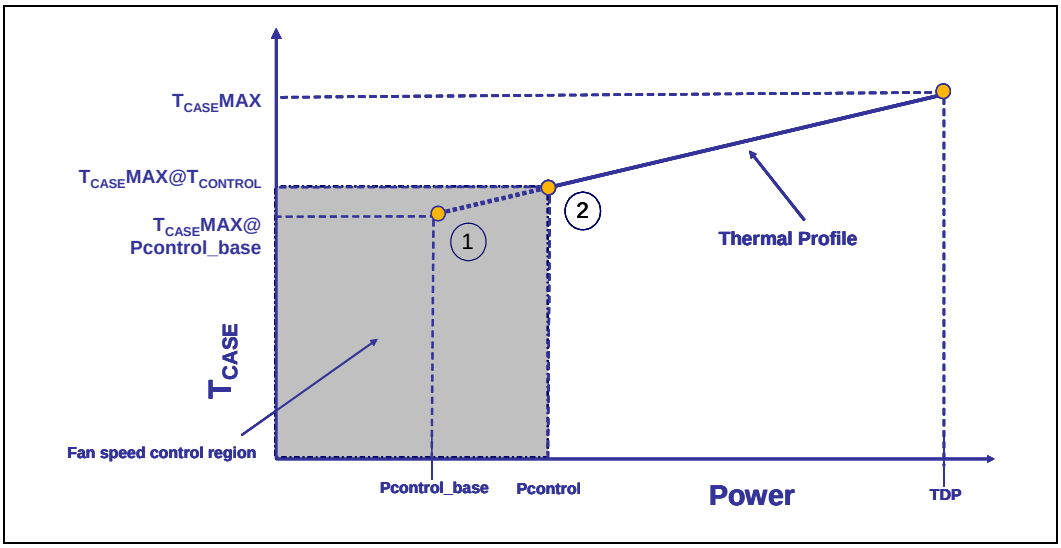
The reference heatsink solutions will be evaluated at sea level (0 meters). The system designers who need to account for altitude effects in the overall system thermal design must make sure that either Thermal Profile A or B specification for the processor is met at the targeted altitude.

## 2.3 Characterizing Cooling Solution Performance Requirements

### 2.3.1 Fan Speed Control

Fan speed control (FSC) techniques to reduce system level acoustic noise are a common practice in server designs. The fan speed is one of the parameters that determine the amount of airflow provided to the thermal solution. Additionally, airflow is proportional to a thermal solution's performance, which consequently determines the $T_{CASE}$ of the processor at a given power level. Since the $T_{CASE}$ of a processor is an important parameter in the long-term reliability of a processor, the FSC implemented in a system directly correlates to the processor's ability to meet the Thermal Profile and hence the long-term reliability requirements. For this purpose, the parameter called $T_{CONTROL}$ as explained in Section 2.2.2, is to be used in FSC designs to ensure that the long-term reliability of the processor is met while keeping the system level acoustic noise down. Figure 2-6 depicts the relationship between $T_{CONTROL}$ and FSC methodology.

**Figure 2-6. $T_{CONTROL}$ and Fan Speed Control**




Once the $T_{CONTROL}$ value is determined as explained earlier, the thermal diode temperature reading from the processor can be compared to this $T_{CONTROL}$ value. A fan speed control scheme can be implemented as described in Table 2-3 without compromising the long-term reliability of the processor.

**Table 2-3. Fan Speed Control, $T_{CONTROL}$ and $T_{DIODE}$ Relationship**

| Condition | FSC Scheme |
|---|---|
| $T_{DIODE} \leq T_{CONTROL}$ | FSC can adjust fan speed to maintain $T_{DIODE} = T_{CONTROL}$ (low acoustic region). |
| $T_{DIODE} > T_{CONTROL}$ | FSC should adjust fan speed to keep $T_{CASE}$ at or below the Thermal Profile specification (increased acoustic region). |

There are many different ways of implementing fan speed control, including FSC based on processor ambient temperature, FSC based on processor thermal diode temperature ($T_{DIODE}$) or a combination of the two. If FSC is based only on the processor ambient temperature, low acoustic targets can be achieved under low ambient temperature conditions. However, the acoustics cannot be optimized based on the behavior of the processor temperature. If FSC is based only on the thermal diode, sustained temperatures above $T_{CONTROL}$, drives fans to maximum RPM. If FSC is based both on ambient and thermal diode, ambient temperature can be used to scale the fan RPM controlled by the thermal diode. This would result in an optimal acoustic performance. Regardless of which scheme is employed, system designers must ensure that the Thermal Profile specification is met when the processor diode temperature exceeds the $T_{CONTOL}$ value for a given processor.

## 2.3.2 Processor Thermal Characterization Parameter Relationships

The idea of a “thermal characterization parameter”, Ψ (psi), is a convenient way to characterize the performance needed for the thermal solution and to compare thermal solutions in identical conditions (heating source, local ambient conditions). A thermal characterization parameter is convenient in that it is calculated using total package power, whereas actual thermal resistance,

θ (theta), is calculated using actual power dissipated between two points. Measuring actual power dissipated into the heatsink is difficult, since some of the power is dissipated via heat transfer into the socket and board. Be aware, however, of the limitations of lumped parameters such as Ψ when it comes to a real design. Heat transfer is a three-dimensional phenomenon that can rarely be accurately and easily modeled by lump values.

The case-to-local ambient thermal characterization parameter value ($\Psi_{CA}$) is used as a measure of the thermal performance of the overall thermal solution that is attached to the processor package. It is defined by the following equation, and measured in units of °C/W:

**Equation 2-3. $\Psi_{CA} = (T_{CASE} - T_{LA}) / TDP$**

*Where:*

$\Psi_{CA}$ = Case-to-local ambient thermal characterization parameter (°C/W).

$T_{CASE}$ = Processor case temperature (°C).

$T_{LA}$ = Local ambient temperature in chassis at processor (°C).

TDP = TDP dissipation (W) (assumes all power dissipates through the integrated heat spreader (IHS)).

The case-to-local ambient thermal characterization parameter of the processor, $\Psi_{CA}$, is comprised of $\Psi_{CS}$, the TIM thermal characterization parameter, and of $\Psi_{SA}$, the sink-to-local ambient thermal characterization parameter:

**Equation 2-4. $\Psi_{CA} = \Psi_{CS} + \Psi_{SA}$**

*Where:*

$\Psi_{CS}$ = Thermal characterization parameter of the TIM (°C/W).

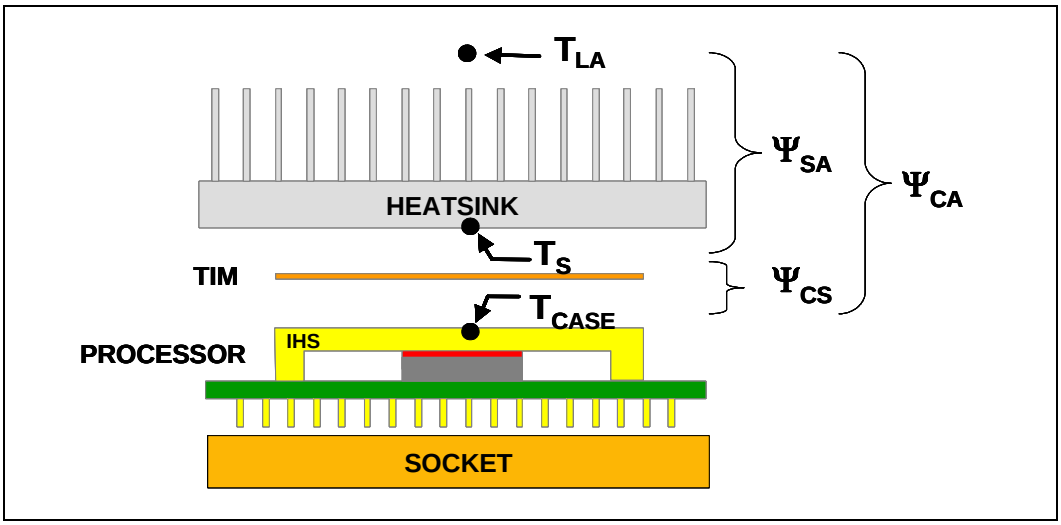
$\Psi_{SA}$ = Thermal characterization parameter from heatsink-to-local ambient (°C/W).

$\Psi_{CS}$ is strongly dependent on the thermal conductivity and thickness of the TIM between the heatsink and IHS.

$\Psi_{SA}$ is a measure of the thermal characterization parameter from the bottom of the heatsink to the local ambient air. $\Psi_{SA}$ is dependent on the heatsink material, thermal conductivity, and geometry. It is also strongly dependent on the air velocity through the fins of the heatsink.

Figure 2-7 illustrates the combination of the different thermal characterization parameters.

**Figure 2-7. Processor Thermal Characterization Parameter Relationships**




### 2.3.2.1 Example

The cooling performance, $\Psi_{CA,}$ is then defined using the principle of thermal characterization parameter described above:

- Define a target case temperature $T_{CASE-MAX}$ and corresponding TDP at a target frequency, F, given in the processor datasheet.
- Define a target local ambient temperature at the processor, $T_{LA}$.

Since the processor thermal specifications ($T_{CASE-MAX}$ and TDP) can vary with the processor frequency, it may be important to identify the worse case (lowest $\Psi_{CA}$) for a targeted chassis (characterized by $T_{LA}$) to establish a design strategy such that a given heatsink can cover a given range of processor frequencies.

The following provides an illustration of how one might determine the appropriate performance targets. The example power and temperature numbers used here are not related to any Intel processor thermal specifications, and are for illustrative purposes only.

Assume the datasheet TDP is 85 W and the case temperature specification is 68 °C for a given frequency. Assume as well that the system airflow has been designed such that the local processor ambient temperature is 45°C. Then the following could be calculated using equation (2-3) from above for the given frequency:

**Equation 2-5. $\Psi_{CA} = (T_{CASE} - T_{LA}) / TDP = (68 - 45) / 85 = 0.27$ °C/W**

To determine the required heatsink performance, a heatsink solution provider would need to determine $\Psi_{CS}$ performance for the selected TIM and mechanical load configuration. If the heatsink solution were designed to work with a TIM material performing at $\Psi_{CS} \leq 0.05$ °C/W, solving for equation (2-4) from above, the performance of the heatsink would be:

**Equation 2-6. $\Psi_{SA} = \Psi_{CA} - \Psi_{CS} = 0.27 - 0.05 = 0.22$ °C/W**

If the local processor ambient temperature is assumed to be 40°C, the same calculation can be carried out to determine the new case-to-ambient thermal resistance:

**Equation 2-7. $\Psi_{CA} = (T_{CASE} - T_{LA}) / TDP = (68 – 40) / 85 = 0.33$ °C/W**

It is evident from the above calculations that, a reduction in the local processor ambient temperature has a significant positive effect on the case-to-ambient thermal resistance requirement.

### 2.3.3 Chassis Thermal Design Considerations

#### 2.3.3.1 Chassis Thermal Design Capabilities and Improvements

One of the critical parameters in thermal design is the local ambient temperature assumption of the processor. Keeping the external chassis temperature fixed, internal chassis temperature rise is the only component that can affect the processor local ambient temperature. Every degree gained at the local ambient temperature directly translates into a degree relief in the processor case temperature.

Given the thermal targets for the processor, it is extremely important to optimize the chassis design to minimize the air temperature rise upstream to the processor ($T_{rise}$), hence minimizing the processor local ambient temperature. Please refer to *$T_{RISE}$ Reduction Guidelines for Rack Servers and Workstations* for more details.

The heat generated by components within the chassis must be removed to provide an adequate operating environment for both the processor and other system components. Moving air through the chassis brings in air from the external ambient environment and transports the heat generated by the processor and other system components out of the system. The number, size and relative position of fans, vents and other heat generating components determine the chassis thermal performance, and the resulting ambient temperature around the processor. The size and type (passive or active) of the thermal solution and the amount of system airflow can be traded off against each other to meet specific system design constraints. Additional constraints are board layout, spacing, component placement, and structural considerations that limit the thermal solution size.

In addition to passive heatsinks, fan heatsinks and system fans, other solutions exist for cooling integrated circuit devices. For example, ducted blowers, heat pipes and liquid cooling are all capable of dissipating additional heat. Due to their varying attributes, each of these solutions may be appropriate for a particular system implementation.

To develop a reliable, cost-effective thermal solution, thermal characterization and simulation should be carried out at the entire system level, accounting for the thermal requirements of each component. In addition, acoustic noise constraints may limit the size, number, placement, and types of fans that can be used in a particular design.

## 2.4 Thermal/Mechanical Reference Design Considerations

### 2.4.1 Heatsink Solutions

#### 2.4.1.1 Heatsink Design Considerations

To remove the heat from the processor, three basic parameters should be considered:

- **The area of the surface on which the heat transfer takes place -** Without any enhancements, this is the surface of the processor package IHS. One method used to improve thermal performance is by attaching a heatsink to the IHS. A heatsink can increase the

effective heat transfer surface area by conducting heat out of the IHS and into the surrounding air through fins attached to the heatsink base.

- **The conduction path from the heat source to the heatsink fins -** Providing a direct conduction path from the heat source to the heatsink fins and selecting materials with higher thermal conductivity typically improves heatsink performance. The length, thickness, and conductivity of the conduction path from the heat source to the fins directly impact the thermal performance of the heatsink. In particular, the quality of the contact between the package IHS and the heatsink base has a higher impact on the overall thermal solution performance as processor cooling requirements become strict. Thermal interface material (TIM) is used to fill in the gap between the IHS and the bottom surface of the heatsink, and thereby improves the overall performance of the thermal stackup (IHS-TIM-Heatsink). With extremely poor heatsink interface flatness or roughness, TIM may not adequately fill the gap. The TIM thermal performance depends on its thermal conductivity as well as the pressure load applied to it. Refer to Section 2.4.2 for further information on the TIM between the IHS and the heatsink base.
- **The heat transfer conditions on the surface on which heat transfer takes place -** Convective heat transfer occurs between the airflow and the surface exposed to the flow. It is characterized by the local ambient temperature of the air, $T_{LA}$, and the local air velocity over the surface. The higher the air velocity over the surface, the resulting cooling is more efficient. The nature of the airflow can also enhance heat transfer via convection. Turbulent flow can provide improvement over laminar flow. In the case of a heatsink, the surface exposed to the flow includes the fin faces and the heatsink base.

**An active heatsink** typically incorporates a fan that helps manage the airflow through the heatsink.

**Passive heatsink** solutions require in-depth knowledge of the airflow in the chassis. Typically, passive heatsinks see slower air speed. Therefore these heatsinks are typically larger (and heavier) than active heatsinks due to the increase in fin surface required to meet a required performance. As the heatsink fin density (the number of fins in a given cross-section) increases, the resistance to the airflow increases: it is more likely that the air will travel around the heatsink instead of through it, unless air bypass is carefully managed. Using air-ducting techniques to manage bypass area is an effective method for maximizing airflow through the heatsink fins.

## 2.4.2 Thermal Interface Material

TIM application between the processor IHS and the heatsink base is generally required to improve thermal conduction from the IHS to the heatsink. Many thermal interface materials can be pre-applied to the heatsink base prior to shipment from the heatsink supplier and allow direct heatsink attach, without the need for a separate TIM dispense or attach process in the final assembly factory.

All thermal interface materials should be sized and positioned on the heatsink base in a way that ensures the entire processor IHS area is covered. It is important to compensate for heatsink-to-processor attach positional alignment when selecting the proper TIM size.

When pre-applied material is used, it is recommended to have a protective application tape over it. This tape must be removed prior to heatsink installation.

The TIM performance is susceptible to degradation (i.e. grease breakdown) during the useful life of the processor due to the temperature cycling phenomena. For this reason, the measured $T_{CASE}$ value of a given processor can decrease over time depending on the type of TIM material.

### 2.4.3 Summary

In summary, considerations in heatsink design include:

- The local ambient temperature $T_{LA}$ at the heatsink, airflow (CFM), the power being dissipated by the processor, and the corresponding maximum $T_{CASE}$. These parameters are usually combined in a single lump cooling performance parameter, $\Psi_{CA}$ (case to air thermal characterization parameter). More information on the definition and the use of $\Psi_{CA}$ is given in Section 2.4 and Section 2.3.2.
- Heatsink interface (to IHS) surface characteristics, including flatness and roughness.
- The performance of the TIM used between the heatsink and the IHS.
- Surface area of the heatsink.
- Heatsink material and technology.
- Development of airflow entering and within the heatsink area.
- Physical volumetric constraints placed by the system.

### 2.4.4 Assembly Overview of the Intel Reference Thermal Mechanical Design

The reference design heatsinks that meet the Dual-Core Intel Xeon processor 2.80 GHz thermal performance targets are called the Common Enabling Kit (CEK) heatsinks, and are available in 1U, 2U& 2U+ sizes. Each CEK consists of the following components:

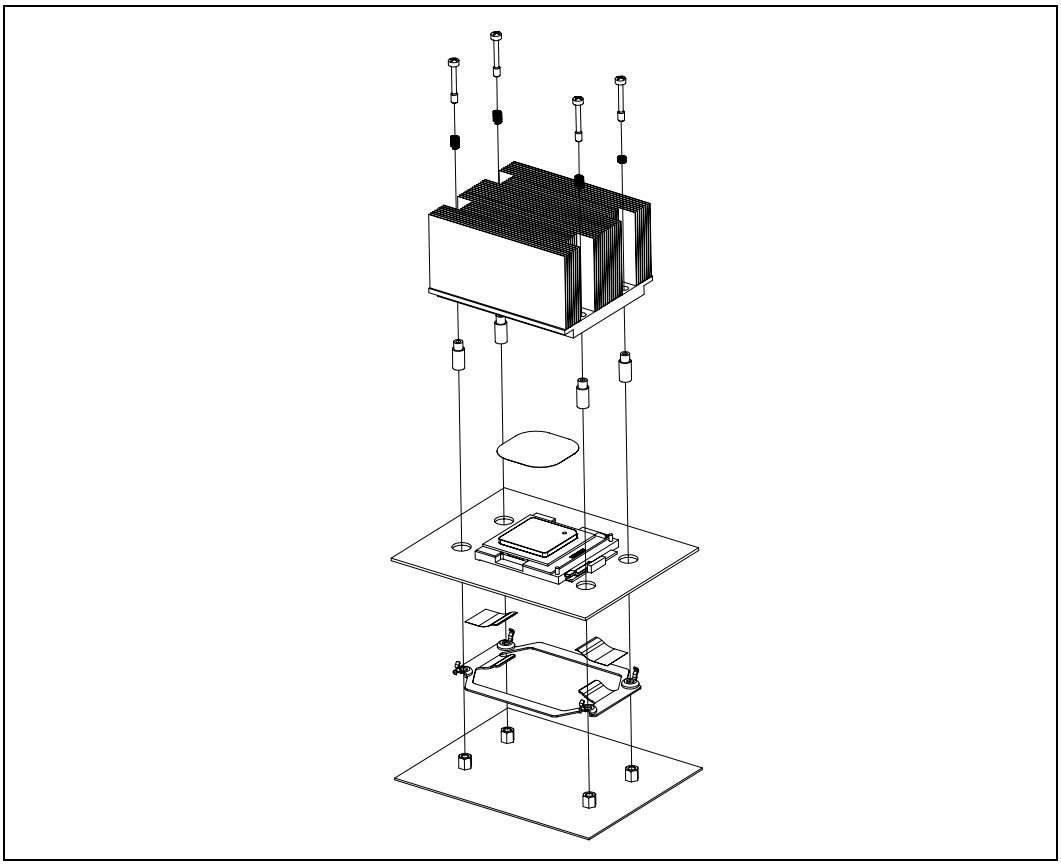
- Heatsink (with captive standoff and screws)
- Thermal Interface Material (TIM-2)
- CEK Spring

#### 2.4.4.1 Geometric Envelope

The baseboard keepout zones on the primary and secondary sides and height restrictions under the enabling component region are shown in detail in Appendix A. The overall volumetric keep in zone encapsulates the processor, socket, and the entire thermal/mechanical enabling solution.

### 2.4.4.2 Assembly Drawing

**Figure 2-8. Exploded View of CEK Thermal Solution Components**



The CEK reference thermal solution is designed to extend air-cooling capability through the use of larger heatsinks with minimal airflow blockage and bypass. CEK retention solution can allow the use of much heavier heatsink masses compared to the legacy limits by using a load path directly attached to the chassis pan. The CEK spring on the secondary side of the baseboard provides the necessary compressive load for the thermal interface material. The baseboard is intended to be isolated such that the dynamic loads from the heatsink are transferred to the chassis pan via the stiff screws and standoffs. This reduces the risk of package pullout and solder-joint failures.

The baseboard mounting holes for the CEK solution are at the same location as the hole locations used for previous Intel® Xeon® processor thermal solution. However, CEK assembly requires 10.16 mm [0.400 in.] large diameter holes to compensate for the CEK spring embosses.

The CEK solution is designed and optimized for a baseboard thickness range of 1.57 – 2.31 mm. [0.062-0.093 in]. While the same CEK spring can be used for this board thickness range, the heatsink standoff height is different for a 1.57 mm [0.062 in] thick board than it is for a 2.31 mm. [0.093 in] thick board. In the heatsink assembly, the standoff protrusion from the base of the heatsink needs to be 0.6 mm. [0.024 in] longer for a 2.31 mm [0.093 in] thick board, compared to a 1.57 mm [0.062 in] thick board. If this solution is intended to be used on baseboards that fall outside of this range, then some aspects of the design, including but not limited to the CEK spring design and the standoff heights, may need to change. Therefore, system designers need to evaluate the thermal performance and mechanical behavior of the CEK design on baseboards with different thicknesses.

Refer to Appendix A for drawings of the heatsinks and CEK spring. The screws and standoffs are standard components that are made captive to the heatsink for ease of handling and assembly.

Contact your Intel field sales representative for an electronic version of mechanical and thermal models of the CEK (Pro Engineer*, IGES and Icepak*, Flotherm* formats). Pro Engineer, Icepak and Flotherm models are available on Intel Business Link (IBL).

***Note:*** Intel reserves the right to make changes and modifications to the design as necessary.

***Note:*** The thermal mechanical reference design for the Dual-Core Intel Xeon processor 2.80 GHz was verified according to the Intel validation criteria given in Appendix C.1. Any thermal mechanical design using some of the reference components in combination with any other thermal mechanical solution needs to be fully validated according to the customer criteria. Also, if customer thermal mechanical validation criteria differ from the Intel criteria, the reference solution should be validated against the customer criteria.

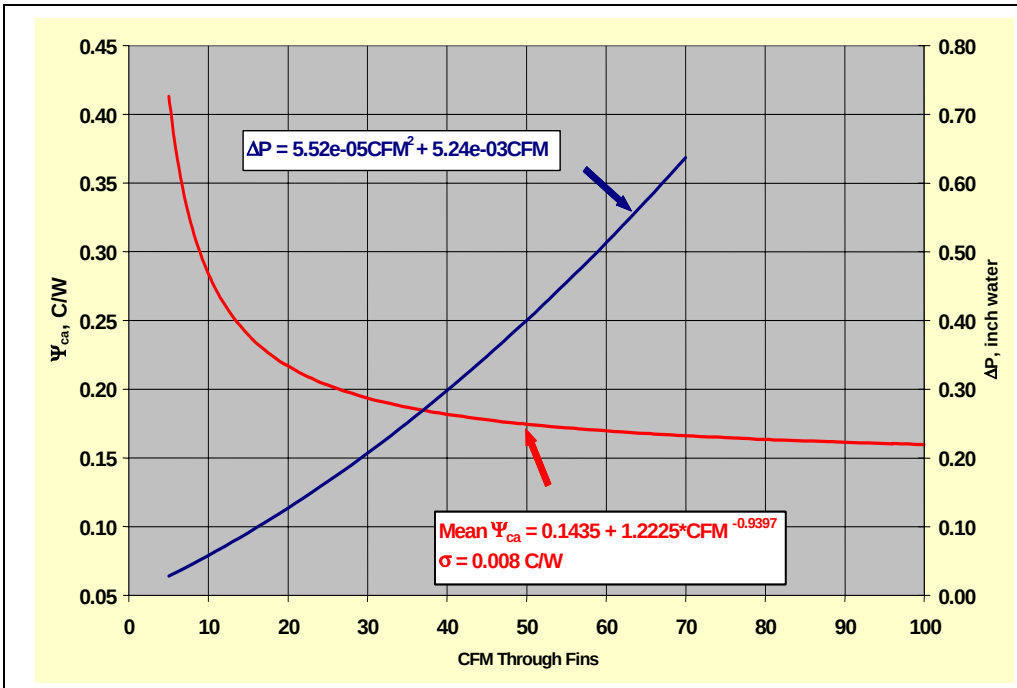
#### 2.4.4.3 Structural Considerations of CEK

As Intel explores methods of keeping thermal solutions within the air-cooling space, the mass of the thermal solutions is increasing significantly. Due to the flexible nature (and associated large deformation) of baseboard-only attachments, Intel reference solutions, such as CEK, are now commonly using direct chassis attach (DCA) as the mechanical retention design. The mass of the new thermal solutions is large enough to require consideration for structural support and stiffening on the chassis. Intel has published a best know method (BKM) document that provides specific structural guidance for designing DCA thermal solutions. The document is titled *Chassis Strength and Stiffness Measurement and Improvement Guidelines for Direct Chassis Attach Solutions*.

### 2.4.5 Thermal Solution Performance Characteristics

The optimization of the CEK heatsinks for thermal performance has been completed. Figure 2-9 and Figure 2-11 show the performance of the 2U+ and 1U passive heatsinks, respectively. These figures show the thermal performance and the pressure drop through fins of the heatsink versus the airflow provided. The best-fit equations for these curves are also provided to make it easier for users to determine the desired value without any error associated with reading the graph.

**Figure 2-9. 2U+ CEK Heatsink Thermal Performance**




If other custom heatsinks are intended for use with the Dual-Core Intel Xeon processor 2.80 GHz, they must support the following interface control requirements to be compatible with the reference mechanical components:

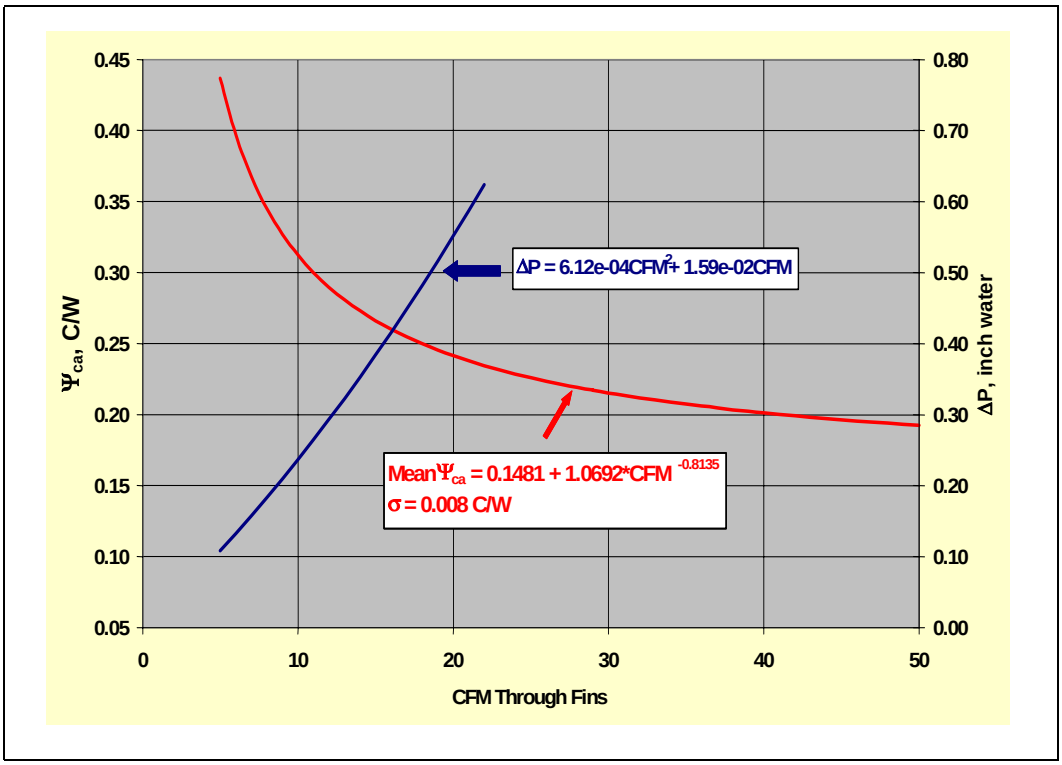
- **Requirement 1:** Heatsink assembly must stay within the volumetric keep-in.
- **Requirement 2:** Maximum mass and center of gravity.

Current maximum heatsink mass is 1000 grams [2.2 lbs] and the maximum center of gravity 38.1 mm [1.5 in.] above the bottom of the heatsink base.

- **Requirement 3:** Maximum and minimum compressive load.

Any custom thermal solution design should meet the loading specification as documented within this document, and should refer to the datasheet for specific details on package loading specifications.

**Figure 2-10. 1U CEK Heatsink Thermal Performance**




## 2.4.6 Thermal Profile Adherence

The 2U+ CEK Intel reference thermal solution is designed to meet the Thermal Profile A for the Dual-Core Intel Xeon processor 2.80 GHz. From Table 2-2, the three-sigma (mean+3sigma) performance of the thermal solution is computed to be 0.234 °C/W and the processor local ambient temperature ($T_{LA}$) for this thermal solution is 40 °C. Hence, the Thermal Profile equation for this thermal solution is calculated as:

**Equation 2-8. y = 0.234x + 40**

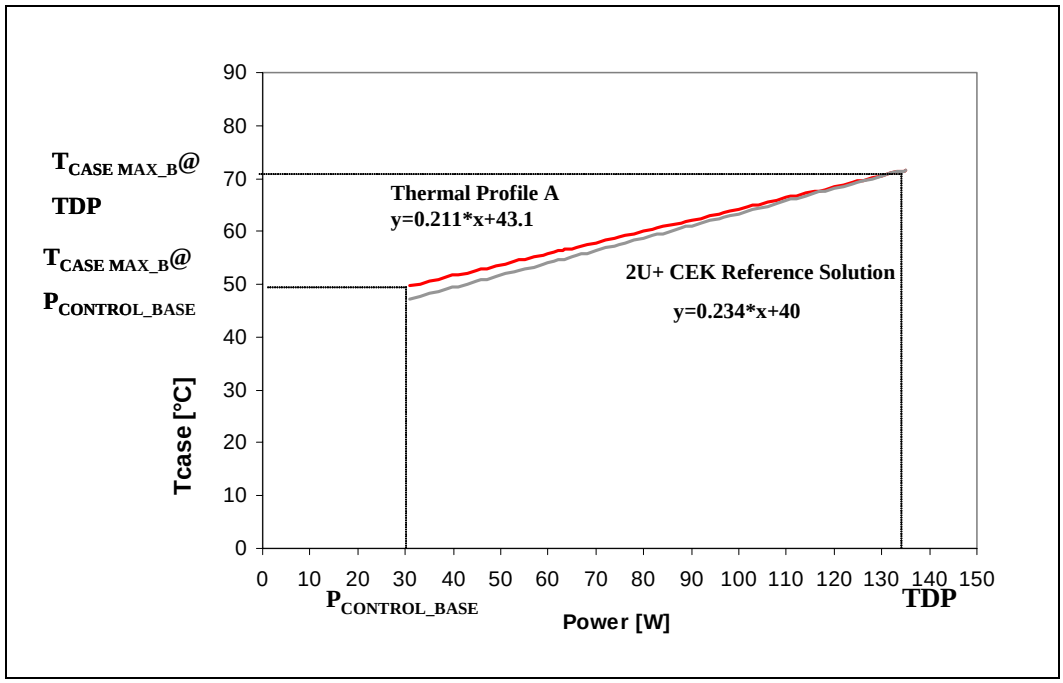
where,

y = Processor $T_{CASE}$ value (°C)

x = Processor power value (W)

Figure 2-11 below shows the comparison of this reference thermal solution's Thermal Profile to the Dual-Core Intel Xeon processor 2.80 GHz Thermal Profile A specification. The 2U+ CEK solution meets the Thermal Profile A with a 0.4 °C margin at the lower end (Pcontrol_base_A) and a 0.4 °C margin at the upper end (TDP). By designing to Thermal Profile A, it is ensured that no measurable performance loss due to TCC activation is observed under the given environmental conditions.

**Figure 2-11. 2U+ CEK Thermal Adherence to Dual-Core Intel Xeon Processor 2.80 GHz Thermal Profile A**




The 1U CEK Intel reference thermal solution is designed to meet the Thermal Profile B for the Dual-Core Intel Xeon processor 2.80 GHz. From Table 2-2 the three-sigma (mean+3sigma) performance of the thermal solution is computed to be 0.290 °C/W and the processor local ambient temperature ($T_{LA}$) for this thermal solution is 40 °C. Hence, the Thermal Profile equation for this thermal solution is calculated as:

**Equation 2-9. y = 0.290x + 40**

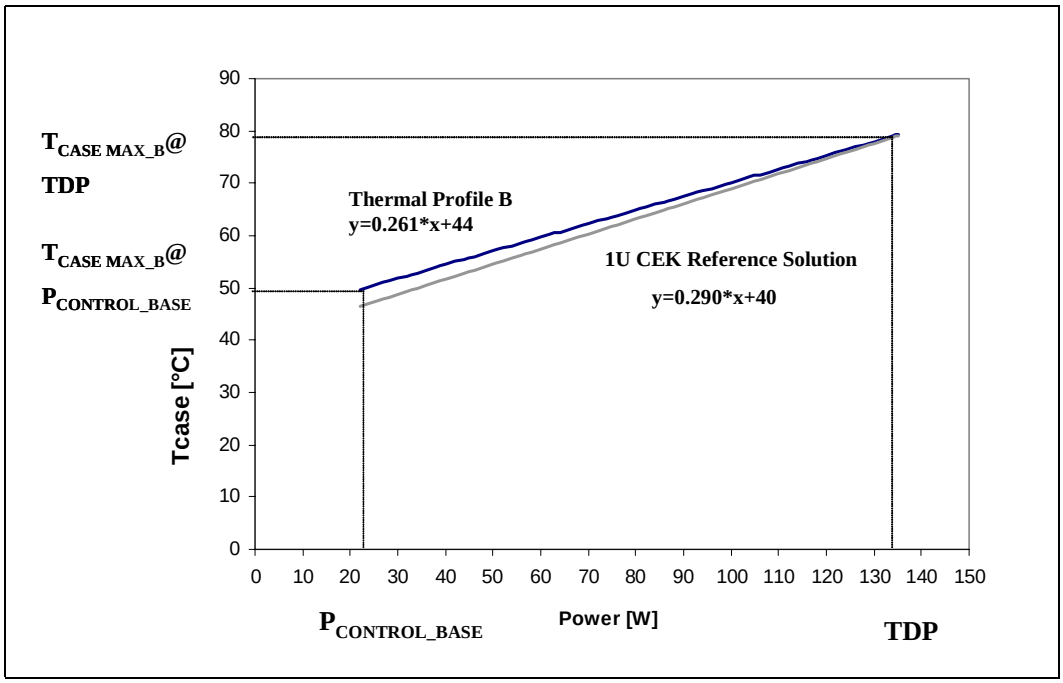
where,

y = Processor $T_{CASE}$ value (°C)

x = Processor power value (W)

Figure 2-12 below shows the comparison of this reference thermal solution's Thermal Profile to the Dual-Core Intel Xeon processor 2.80 GHz Thermal Profile B specification. The 1U CEK solution meets the Thermal Profile B with a 0.3°C margin at the lower end (Pcontrol_base_B) and a 0 °C margin at the upper end (TDP). However, as explained in Section 2.2.3, designing to Thermal Profile B results in increased TCC activation and measurable performance loss for the processor. In this case, it is estimated that up to 5% of all the processors in a population that utilizes the 1U CEK reference solution may see TCC activation that results in a measurable performance loss of >1.5% when running an application that consumes power equivalent to TDP.

**Figure 2-12. 1U CEK Thermal Adherence to Dual-Core Intel Xeon Processor 2.80 GHz Thermal Profile B**

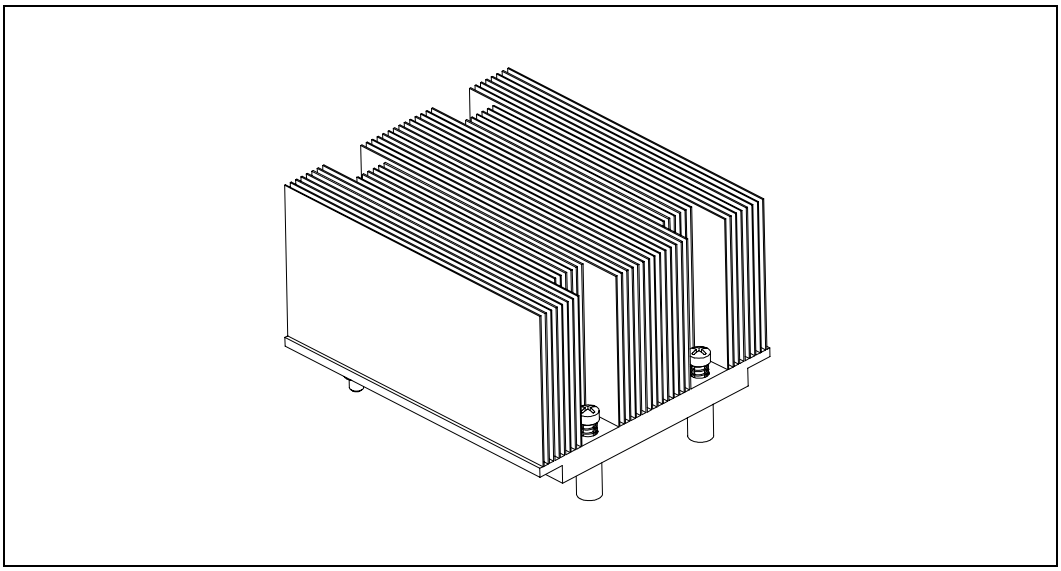



## 2.4.7 Components Overview

### 2.4.7.1 Heatsink with Captive Screws and Standoffs

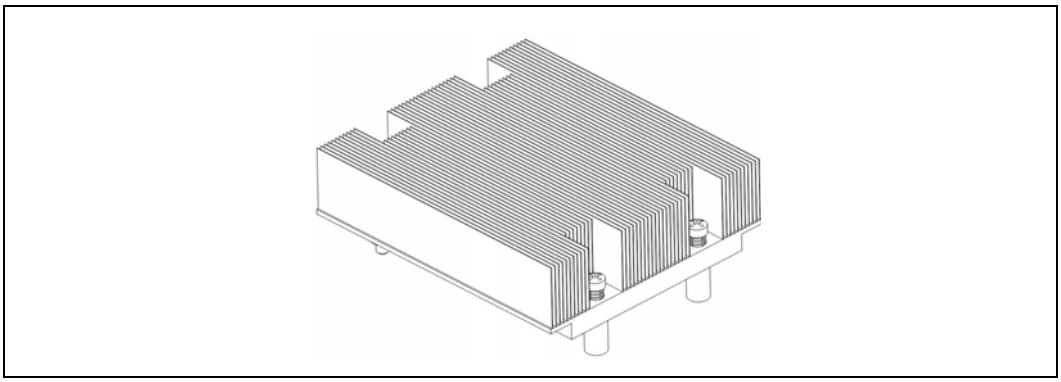
The CEK reference heatsink uses snapped-fin technology for its design. It consists of a copper base and copper fins with Shin-Etsu G751* thermal grease as the TIM. The mounting screws and standoffs are also made captive to the heatsink base for ease of handling and assembly as shown in Figure 2-13 and Figure 2-14 for the 2U+ and 1U heatsinks, respectively.

**Figure 2-13. Isometric View of the 2U+ CEK Heatsink**



***Note:*** Refer to Appendix A for more detailed mechanical drawings of the heatsink.

**Figure 2-14. Isometric View of the 1U CEK Heatsink**



***Note:*** Refer to Appendix A for more detailed mechanical drawings of the heatsink.

The function of the standoffs is to provide a bridge between the chassis and the heatsink for attaching and load carrying. When assembled, the heatsink is rigid against the top of the standoff, and the standoff is rigid to a chassis standoff with the CEK spring firmly sandwiched between the two. In dynamic loading situations the standoff carries much of the heatsink load, especially in lateral conditions, when compared to the amount of load transmitted to the processor package. As such, it is comprised of steel. The distance from the bottom of the heatsink to the bottom of the standoff is 10.26 mm [0.404 in.] for a board thickness of 1.57 mm [0.062 in]. The standoff will need to be modified for use in applications with a different board thickness, as defined in Section 2.4.4.2.

The function of the screw is to provide a rigid attach method to sandwich the entire CEK assembly together, activating the CEK spring under the baseboard, and thus providing the TIM preload. A screw is an inexpensive, low profile solution that does not negatively impact the thermal

performance of the heatsink due to air blockage. Any fastener (i.e. head configuration) can be used as long as it is of steel construction; the head does not interfere with the heatsink fins, and is of the correct length of 20.64 mm [0.8125 in.].

Although the CEK heatsink fits into the legacy volumetric keep-in, it has a larger footprint due to the elimination of retention mechanism and clips used in the older enabled thermal/mechanical components. This allows the heatsink to grow its base and fin dimensions, further improving the thermal performance. A drawback of this enlarged size and use of copper for both the base and fins is the increased weight of the heatsink. The CEK heatsink is estimated to weigh twice as much as previous heatsinks used with Intel Xeon processors. However, the new retention scheme employed by CEK is designed to support heavy heatsinks (approximately up to 1000 grams) in cases of shock, vibration and installation as explained in Appendix C. Some of the thermal and mechanical characteristics of the CEK heatsinks are shown in Section 2-4.

**Table 2-4. CEK Heatsink Thermal Mechanical Characteristics**

| Size | Height mm [in.] | Weight (kg) [lbs] | Target Airflow Through Fins (CFM) | Mean $\Psi_{ca}$ (°C/W) | Standard Deviation $\Psi_{ca}$ (°C/W) | Pressure Drop (in $H_2O$) |
|---|---|---|---|---|---|---|
| 2U+ | 50.8 [2.00] | 1.0 [2.2] | 22 | 0.210 | 0.008 | 0.142 |
| 1U | 26.4 [1.04] | 0.53 [1.2] | 15 | 0.266 | 0.008 | 0.376 |

### 2.4.7.2 Thermal Interface Material (TIM-2)

A TIM must be applied between the package and the heatsink to ensure thermal conduction. The CEK reference design uses Shin-Etsu* G751 thermal grease.

The recommended grease dispenses weight to ensure full coverage of the processor IHS is given below. For an alternate TIM, full coverage of the entire processor IHS is recommended.

**Table 2-5. Recommended Thermal Grease Dispense Weight**

| Processor | Recommended Thermal Grease | Dispense Weight (mg) |
|---|---|---|
| Dual-Core Intel® Xeon® processor 2.80 GHz | Shin-Etsu* G751 | 400 |

It is recommended that you use thermally conductive grease as the TIM requires special handling and dispense guidelines. The following guidelines apply to Shin-Etsu G751 thermal grease. The use of a semi-automatic dispensing system is recommended for high volume assembly to ensure an accurate amount of grease is dispensed on top of the IHS prior to assembly of the heatsink. A typical dispense system consists of an air pressure and timing controller, a hand held output dispenser, and an actuation foot switch. Thermal grease in cartridge form is required for dispense system compatibility. A precision scale with an accuracy of ±5 mg is recommended to measure the correct dispense weight and set the corresponding air pressure and duration. The IHS surface should be free of foreign materials prior to grease dispense

Additional recommendations include recalibrating the dispense controller settings after any two hour pause in grease dispense. The grease should be dispensed just prior to heatsink assembly to prevent any degradation in material performance. Finally, the thermal grease should be verified to be within its recommended shelf life before use.

The CEK reference solution is designed to apply a compressive load of up to 222 N [50 lbf] on the TIM to improve the thermal performance.

### 2.4.7.3 CEK Spring

The CEK spring, which is attached on the secondary side of the baseboard, is made from 0.80 mm [0.0315 in.] thick 301 stainless steel half hard. Any future versions of the spring will be made from a similar material. The CEK spring has four embosses which, when assembled, rest on the top of the chassis standoffs. The CEK spring is located between the chassis standoffs and the heatsink standoffs. The purpose of the CEK spring is to provide compressive preload at the TIM interface when the baseboard is pushed down upon it. This spring does not function as a clip of any kind. The two tabs on the spring are used to provide the necessary compressive preload for the TIM when the whole solution is assembled. The tabs make contact on the secondary side of the baseboard. In order to avoid damage to the contact locations on the baseboard, the tabs will be insulated with a 0.127 mm [0.005 in.] thick Kapton* tape (or equivalent). Figure 2-15 shows an isometric view of the CEK spring design.

**Figure 2-15. CEK Spring Isometric View**

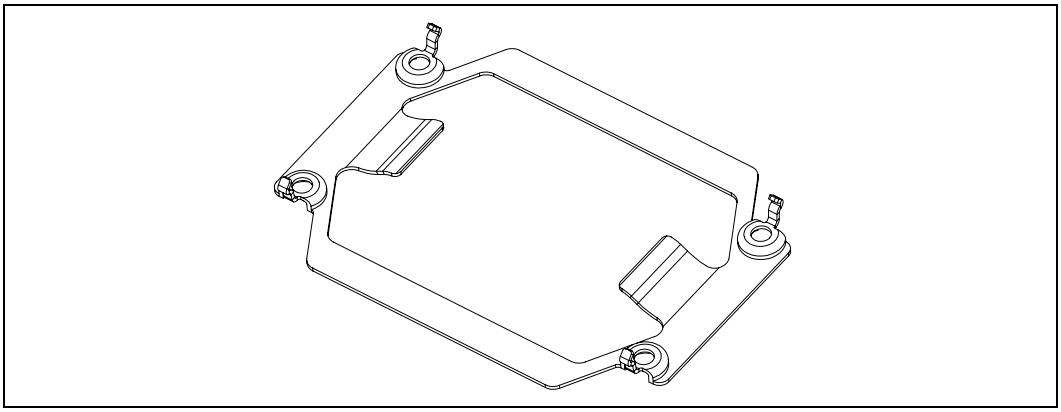
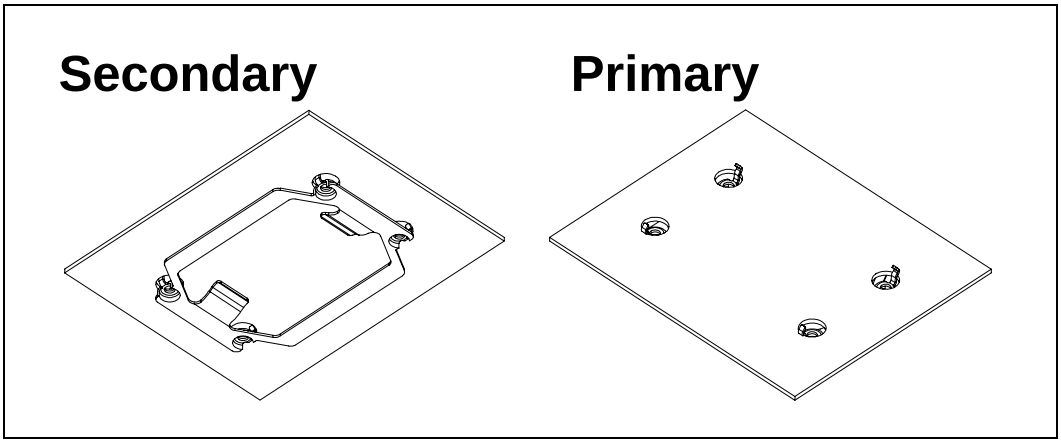


**Figure 2-16. Isometric View of CEK Spring Attachment to the Base Board**




Please refer to Appendix A for more detailed mechanical drawings of the CEK spring. Also, the baseboard keepout requirements shown in Appendix A must be met to use this CEK spring design.

### 2.4.8 Boxed Active Thermal Solution for the Dual-Core Intel Xeon Processor 2.80 GHz

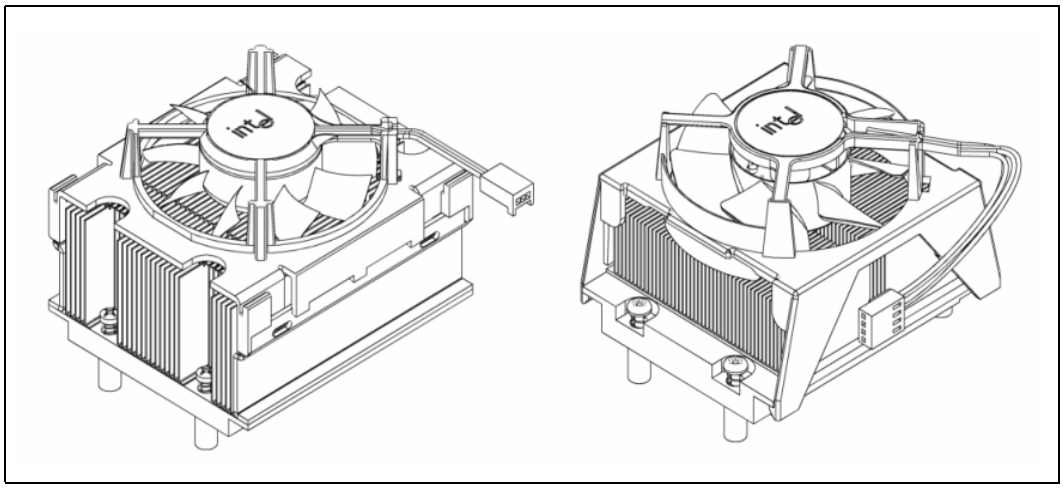
In addition to the 1U and 2U passive CEK heatsinks, Intel is developing an active heatsink solution. This heatsink solution is primarily designed to be used in a pedestal chassis where sufficient air inlet space is present and side directional airflow is not an issue. All three heatsinks will be offered as part of boxed Dual-Core Intel Xeon processor 2.80 GHz products. These solutions are intended for system integrators who build systems from components available through distribution channels. The retention solution used for these products is called the Common Enabling Kit, or CEK. The CEK base is compatible with all three heatsink solutions.

Figure 2-17 provides a representation of the active CEK solution. This design is based on a 4-pin PWM/T-diode controlled active fan heatsink solution. This new solution is being offered to help provide better control over pedestal chassis acoustics. This is achieved though accurate measurement of processor temperature through the processor's temperature diode (T-diode). Fan RPM is modulated through the use an ASIC located on the serverboard, that sends out a PWM control signal to the 4th pin of the connector labeled as **Control**.

This heatsink solution also requires a constant +12 V supplied to pin 2 and does not support variable voltage control or 3-pin PWM control. If no PWM signal is detected on the 4$^{th}$ pin this heatsink solution will revert back to thermistor control mode, supporting both the 4-wire PWM and standard 3-wire ambient air control methods.

Intel may make changes to specification and product descriptions at any time, without notice. The active heatsink solution will not exceed a mass of approximately 1150 grams. Note that this is per processor, so a dual processor system will have up to approximately 2300 grams total mass in the heatsinks. This large mass will require a minimum chassis stiffness to be met in order to withstand force during shock and vibration. Please refer to *Chassis Strength and Stiffness Measurement and Improvement Guidelines, for Direct Chassis Attach Solutions* for more details on chassis requirements.

**Figure 2-17. Boxed Active CEK Heatsink Solutions with PWM/T-diode Control (Representation Only)**



Clearance is required around the heatsink to ensure unimpeded airflow for proper cooling. The physical baseboard keepout requirements for the active solution are the same as the passive CEK solution shown in Appendix A.

### 2.4.8.1 Fan Power Supply

The active heatsink includes a fan, which requires a +12 V power supply. Platforms must provide a matched fan power header to support the boxed processor. Table 2-6 contains specifications for the input and output signals at the heatsink fan connector.

The fan outputs a SENSE signal, an open-collector output, which pulses at a rate of two pulses per fan revolution. A baseboard pull-up resistor provides $V_{CC}$ to match the baseboard-mounted fan speed monitor requirements, if applicable. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 of the connector should be tied to GND.

It is recommended that a 4 pin fan header be used on the baseboard, in addition to, a control ASIC that can send a PWM signal to the active fan heatsink solution on the 4$^{th}$ pin, at a nominal 25 KHz frequency. If a 3-pin CPU fan header is used instead, the active fan heatsink solution will revert back to an automatic ambient air temperature control mode.

The fan will include an integrated fan speed control circuit that will alter the fan speed based on the temperature sensed by the fan. This fan requires a constant +12 V input, though, and will not function properly with fan headers using fan speed control. It is acceptable for the system fan headers to use some form of fan speed control, but since the CEK fan will have it's own, it will require a constant +12 V supply to operate properly.

The fan power header on the baseboard must be positioned to allow the fan heatsink power cable to reach it. The fan power header identification and location must be documented in the supplier's platform documentation, or on the baseboard itself. The baseboard fan power header should be positioned within 177.8 mm [7 in.] from the center of the processor socket.

**Table 2-6. Fan Specifications (Boxed 4-wire PWM/T-diode Heatsink Solution)**

| Description | Min | Typ Steady | Max Steady | Max Startup | Unit | Notes |
|---|---|---|---|---|---|---|
| +12V: 12 Volt Fan Power Supply | 10.8 | 12 | 12 | 13.2 | V | |
| IC: Fan Current Draw | N/A | 1.5 | 1.7 | 2.0 | A | |
| SENSE: SENSE Frequency | 2 | 2 | 2 | 2 | Pulses per fan revolution | 1 |

**NOTE:**
1. System board should pull this pin up to $V_{CC}$ with a resistor.

**Figure 2-18. Fan Cable Connection (Active CEK)**

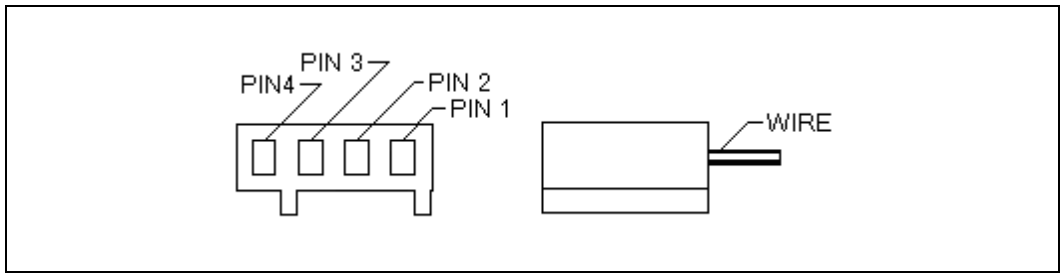


**Table 2-7. Fan Cable Connector Pin Out (Active CEK)**

| Pin Number | Signal | Color |
|---|---|---|
| 1 | Ground (Constant) | Black |
| 2 | Power (+12V) | Yellow |
| 3 | Signal: 2 pulses per revolution | Green |
| 4 | Control | Blue |

### 2.4.8.2 Systems Considerations Associated with the Active CEK

This heatsink was designed to help pedestal chassis users to meet the thermal processor requirements without the use of chassis ducting. It may be necessary to implement some form of chassis air guide or air duct to meet the $T_{LA}$ temperature of 40 °C depending on the pedestal chassis layout. Also, while the active heatsink solution is designed to mechanically fit into a 2U chassis, it may require additional space at the top of the heatsink to allow sufficient airflow into the heatsink fan. Therefore, additional design criteria may need to be considered if this heatsink is used in a 2U rack mount chassis, or in a chassis that has drive bay obstructions above the inlet to the fan heatsink.

Thermal Profile A should be used to help determine the thermal performance of the platform. The active fan utilizes PWM fan speed control technology to automatically adjust fan RPM conforming to the correct thermal load line. It is critical to supply a constant +12 V to the fan header so that the active CEK heat sink solution can operate properly. If a system board has a jumper setting to select either a constant +12 V power to the fan header or a variable voltage, it is strongly recommended that the jumper be set by default to the constant +12 V setting.

It is recommended that the ambient air temperature outside of the chassis be kept at or below 35 °C. The air passing directly over the processor heatsink should not be preheated by other system components. Meeting the processor's temperature specification is the responsibility of the system integrator.

### 2.4.8.3 Boxed Processor Contents

A direct chassis attach method must be used to avoid problems related to shock and vibration, due to the weight of the heatsink required to cool the processor. The board must not bend beyond specification in order to avoid damage. The boxed processor contains the components necessary to solve both issues. The boxed processor will include the following items:

- Dual-Core Intel Xeon processor 2.80 GHz
- Unattached (Active or Passive) Heatsink
- 4 screws, 4 springs, and 4 heatsink standoffs (all captive to the heatsink)
- Thermal Interface Material (TIM)
- Certificate of Authenticity (COA) and Manual
- Intel Inside® Logo

The other items listed in Figure 2-8 that are required to complete this solution will be shipped with either the chassis or boards. They are as follows:

- CEK Spring (supplied by baseboard vendors)
- Chassis standoffs (supplied by chassis vendors)

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# A Mechanical Drawings

The mechanical drawings included in this appendix refer to the thermal mechanical enabling components for the Dual-Core Intel Xeon processor 2.80 GHz Processor.

***Note:*** Intel reserves the right to make changes and modifications to the design as necessary.

**Table A-1. Mechanical Drawing List**

| Drawing Description | Figure Number |
|---|---|
| "2U CEK Heatsink (Sheet 1 of 4)" | Figure A-1 |
| "2U CEK Heatsink (Sheet 2 of 4)" | Figure A-2 |
| "2U CEK Heatsink (Sheet 3 of 4)" | Figure A-3 |
| "2U CEK Heatsink (Sheet 4 of 4)" | Figure A-4 |
| "CEK Spring (Sheet 1 of 3)" | Figure A-5 |
| "CEK Spring (Sheet 2 of 3)" | Figure A-6 |
| "CEK Spring (Sheet 3 of 3)" | Figure A-7 |
| "Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 1 of 6)" | Figure A-8 |
| "Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 2 of 6)" | Figure A-9 |
| "Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 3 of 6)" | Figure A-10 |
| "Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 4 of 6)" | Figure A-11 |
| "Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 5 of 6)" | Figure A-12 |
| "Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 6 of 6)" | Figure A-13 |
| "1U CEK Heatsink (Sheet 1 of 4)" | Figure A-14 |
| "1U CEK Heatsink (Sheet 2 of 4)" | Figure A-15 |
| "1U CEK Heatsink (Sheet 3 of 4)" | Figure A-16 |
| "1U CEK Heatsink (Sheet 4 of 4)" | Figure A-17 |

**Figure A-1. 2U CEK Heatsink (Sheet 1 of 4)**

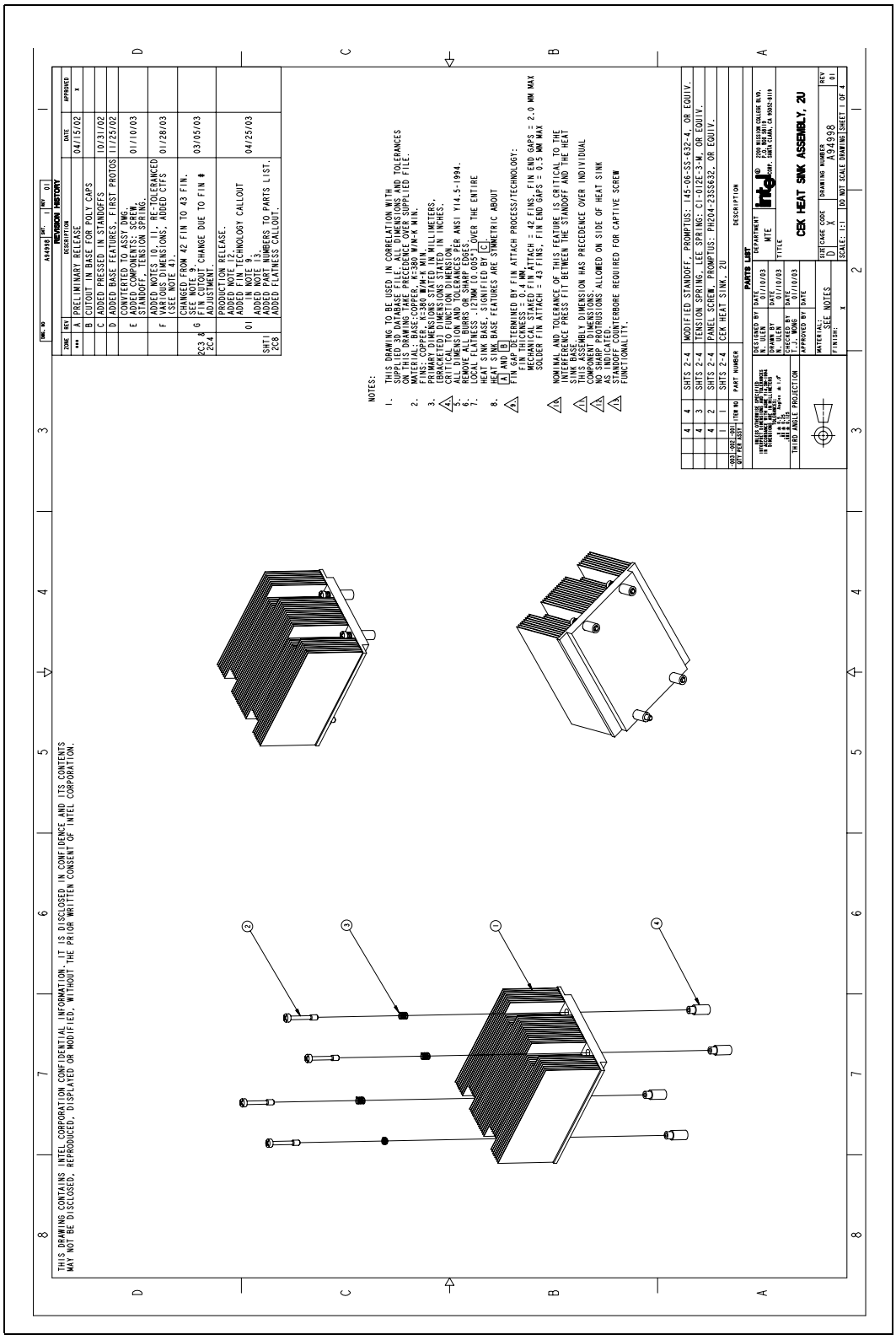


**Figure A-2. 2U CEK Heatsink (Sheet 2 of 4)**

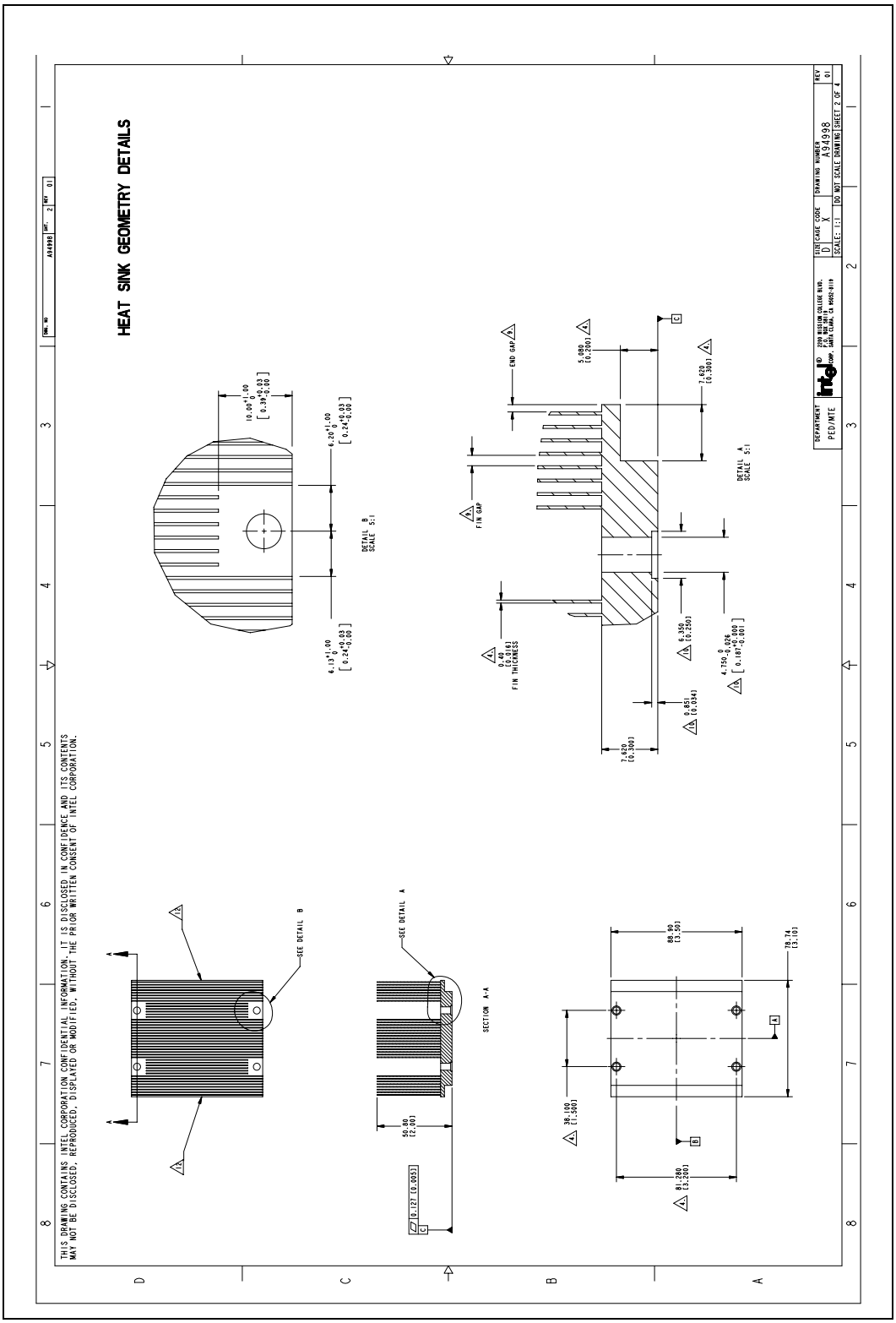


**Figure A-3. 2U CEK Heatsink (Sheet 3 of 4)**

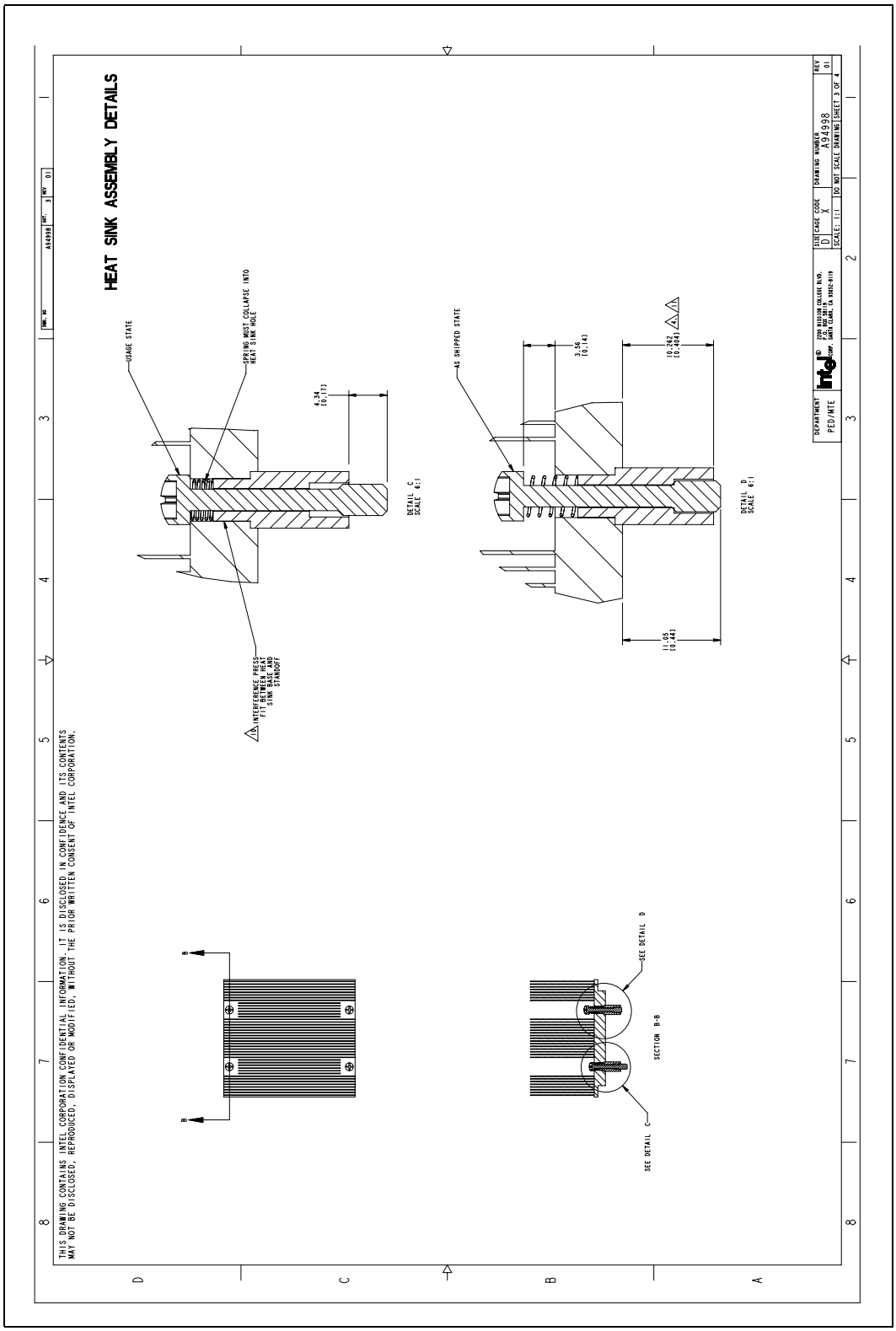


**Figure A-4. 2U CEK Heatsink (Sheet 4 of 4)**

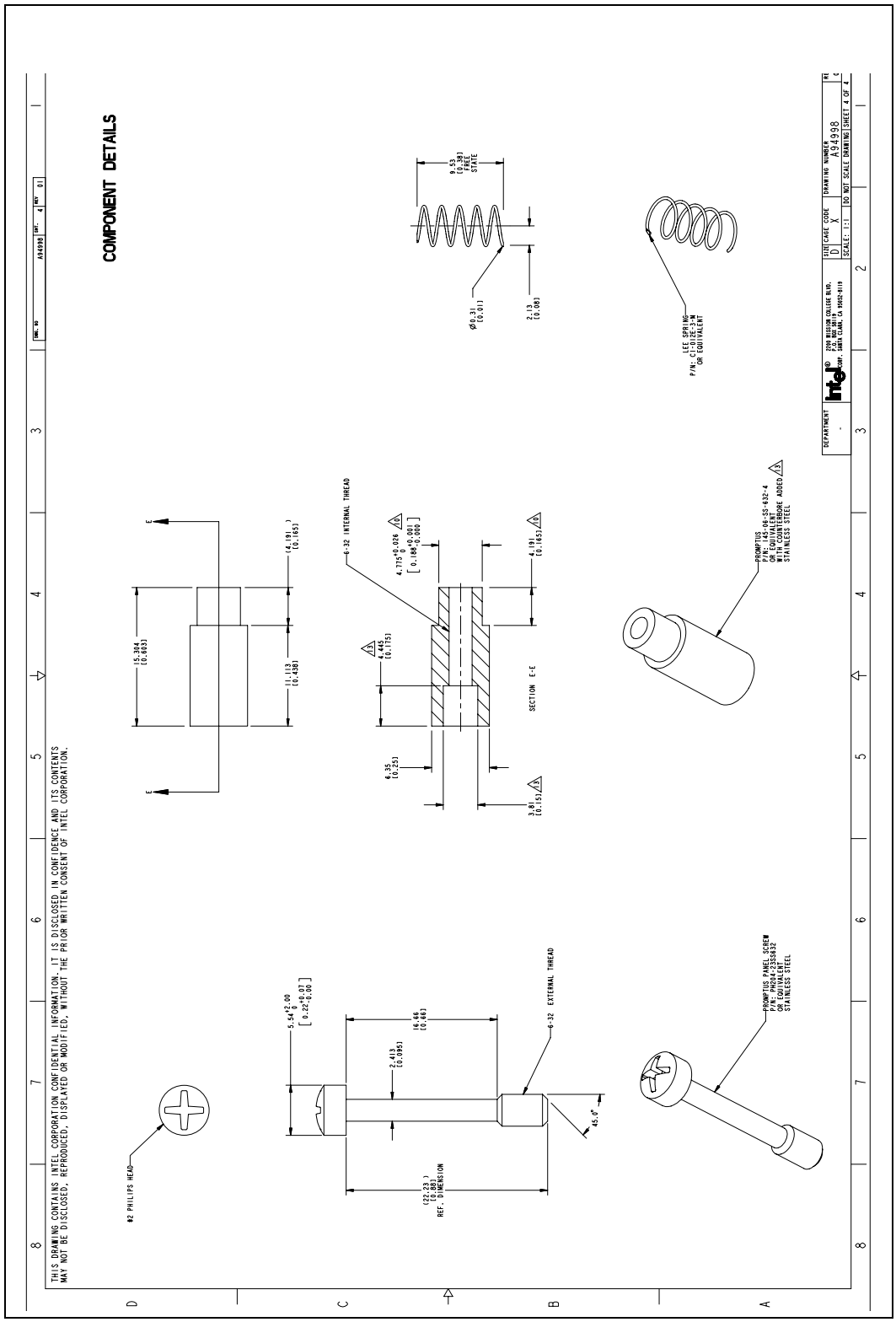


**Figure A-5. CEK Spring (Sheet 1 of 3)**

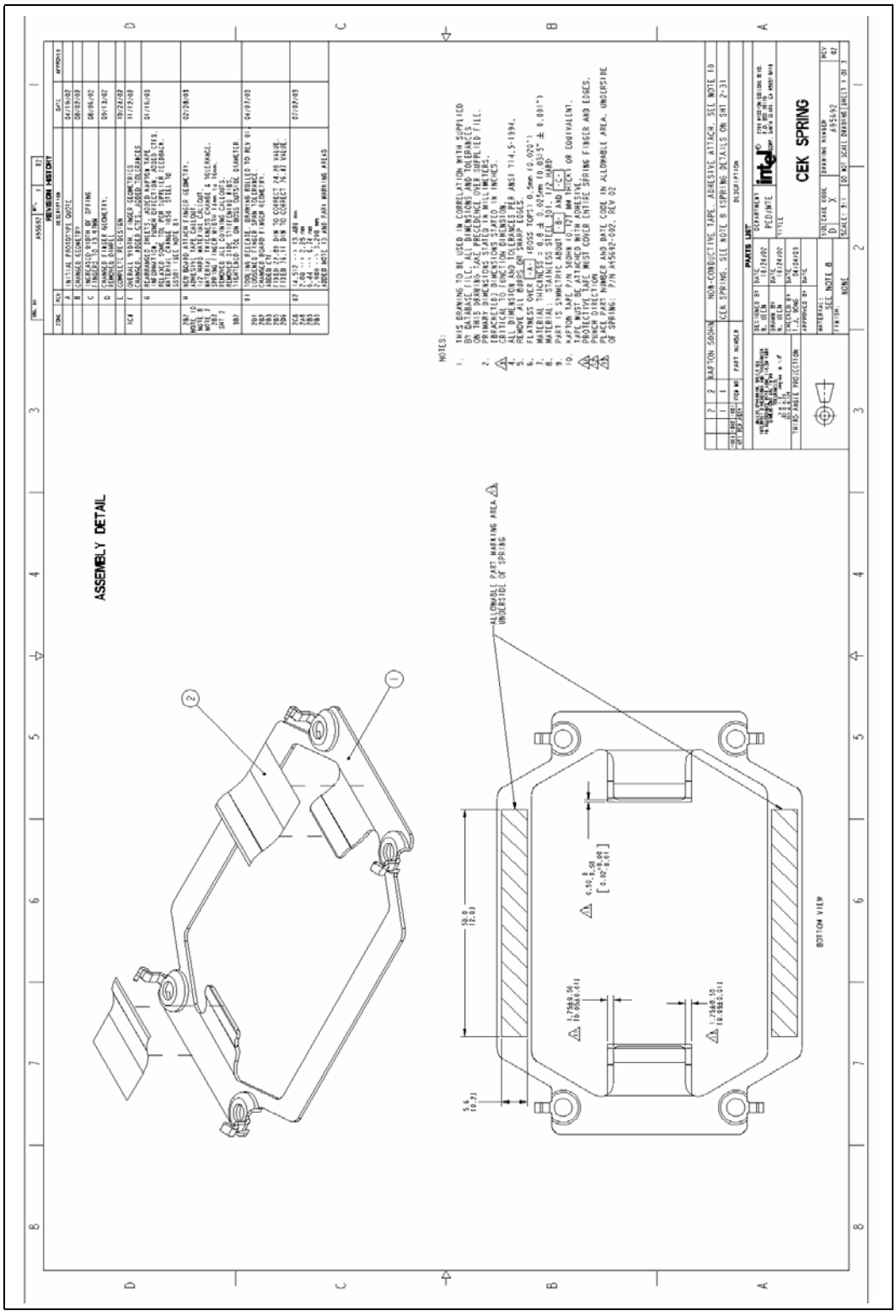


**Figure A-6. CEK Spring (Sheet 2 of 3)**

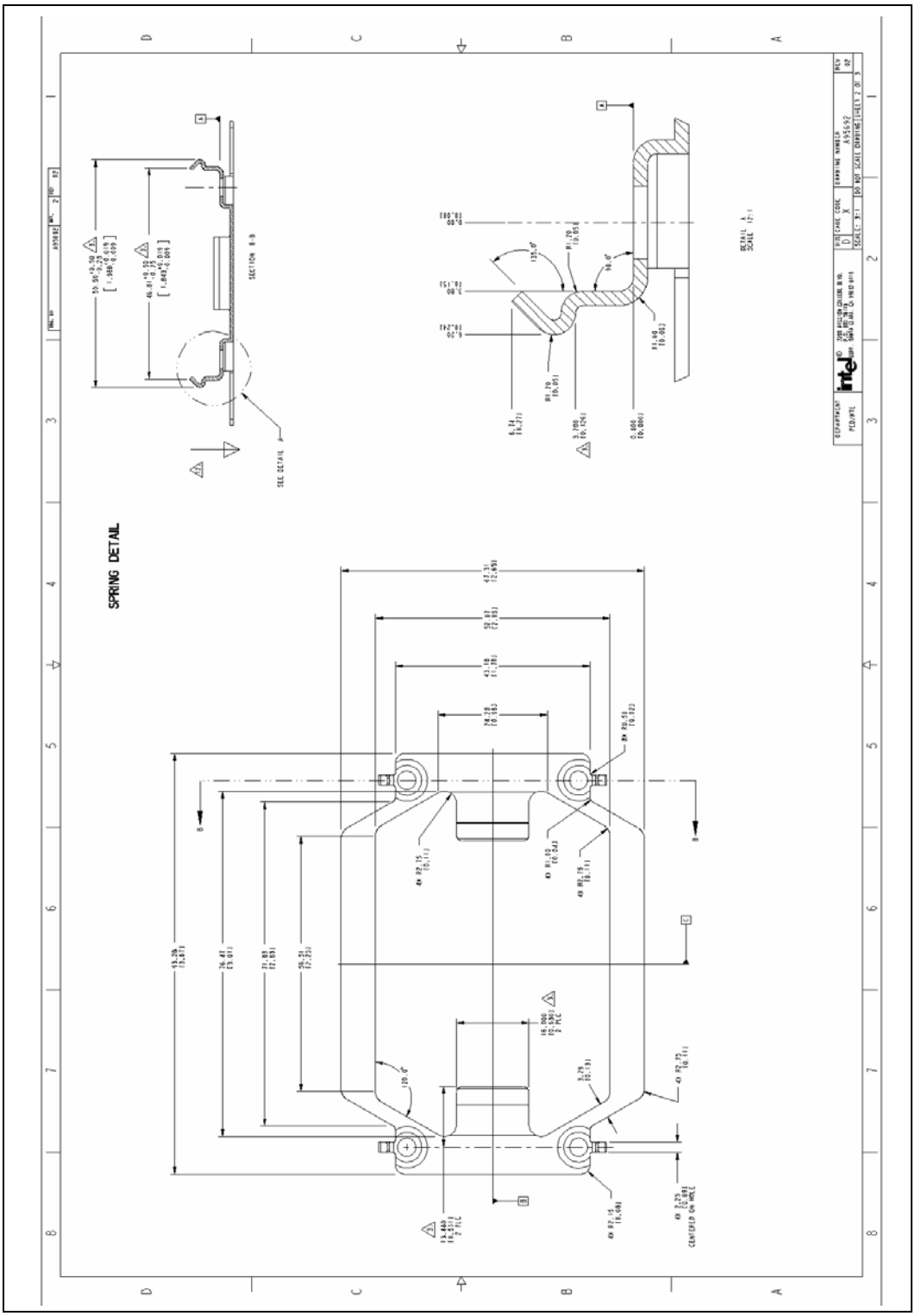


**Figure A-7. CEK Spring (Sheet 3 of 3)**

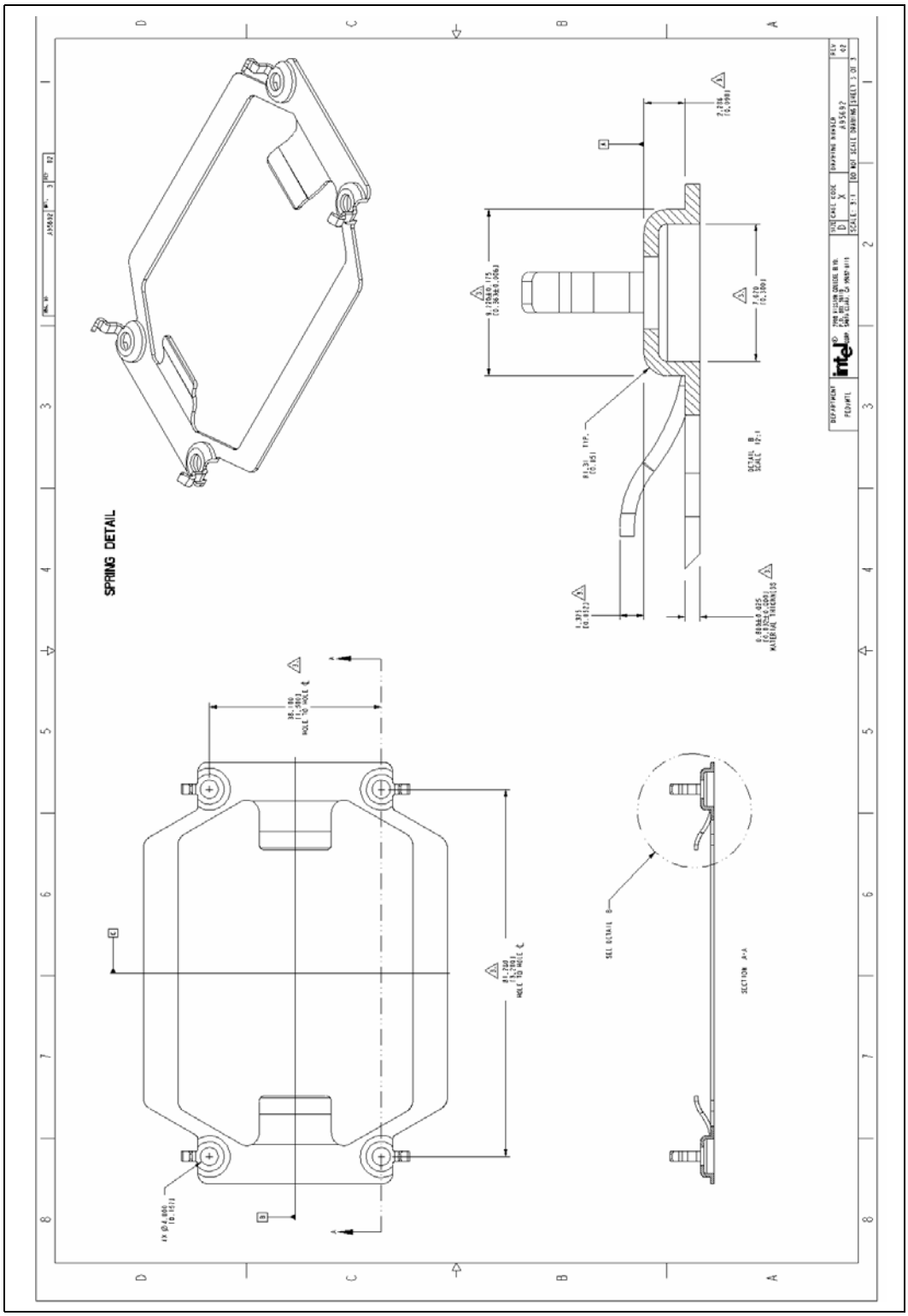


**Figure A-8. Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 1 of 6)**

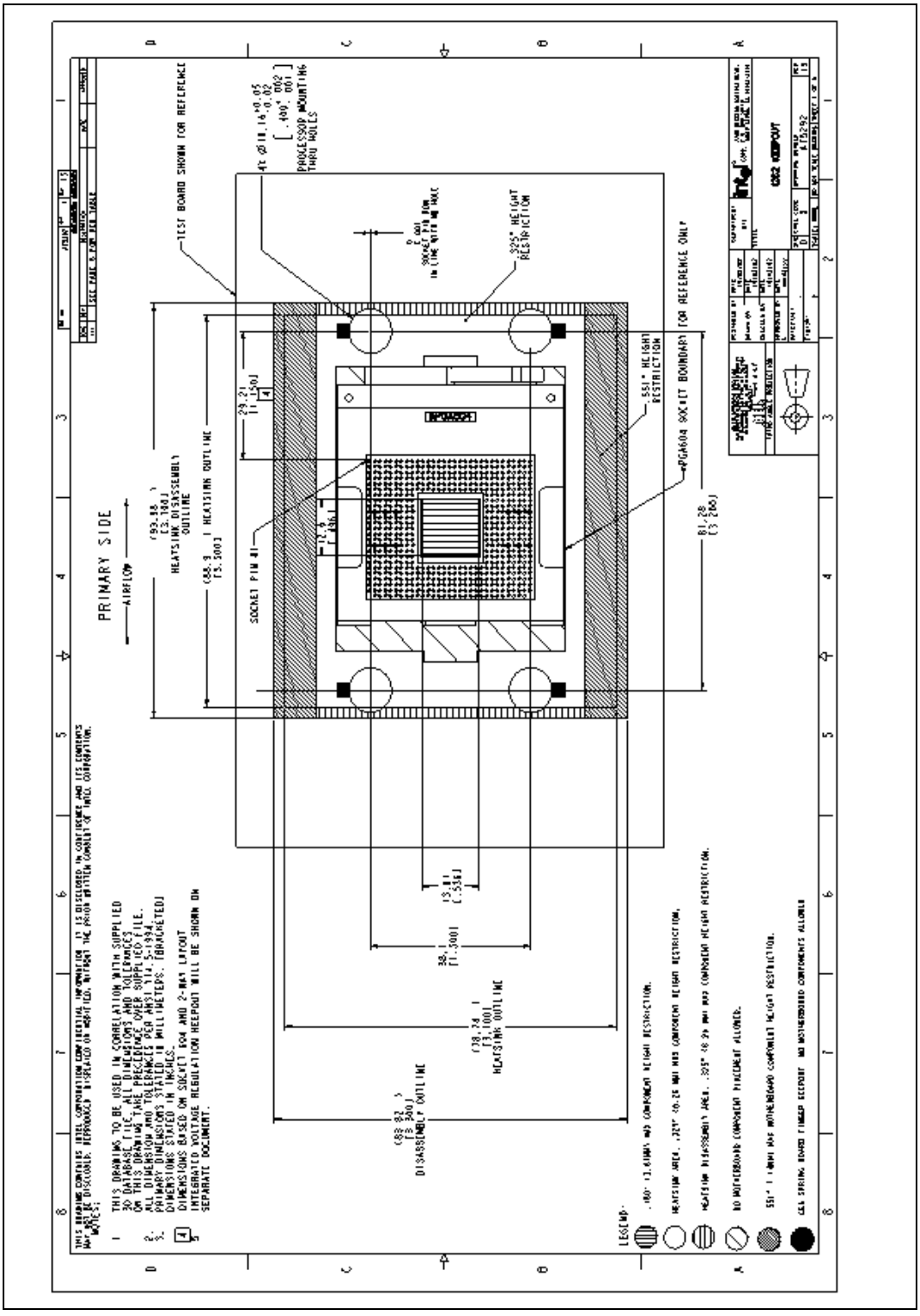


**Figure A-9. Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 2 of 6)**

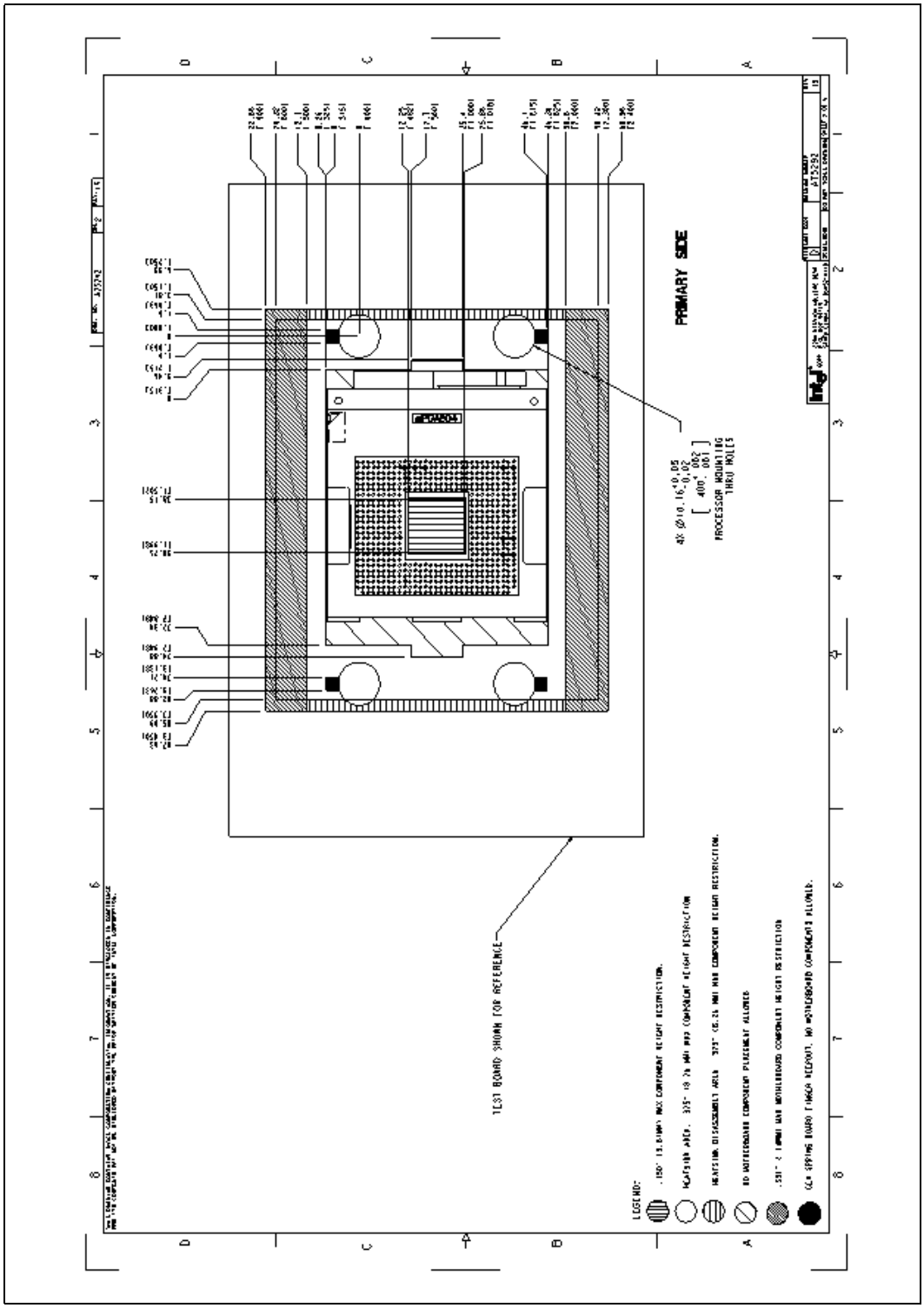


**Figure A-10. Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 3 of 6)**

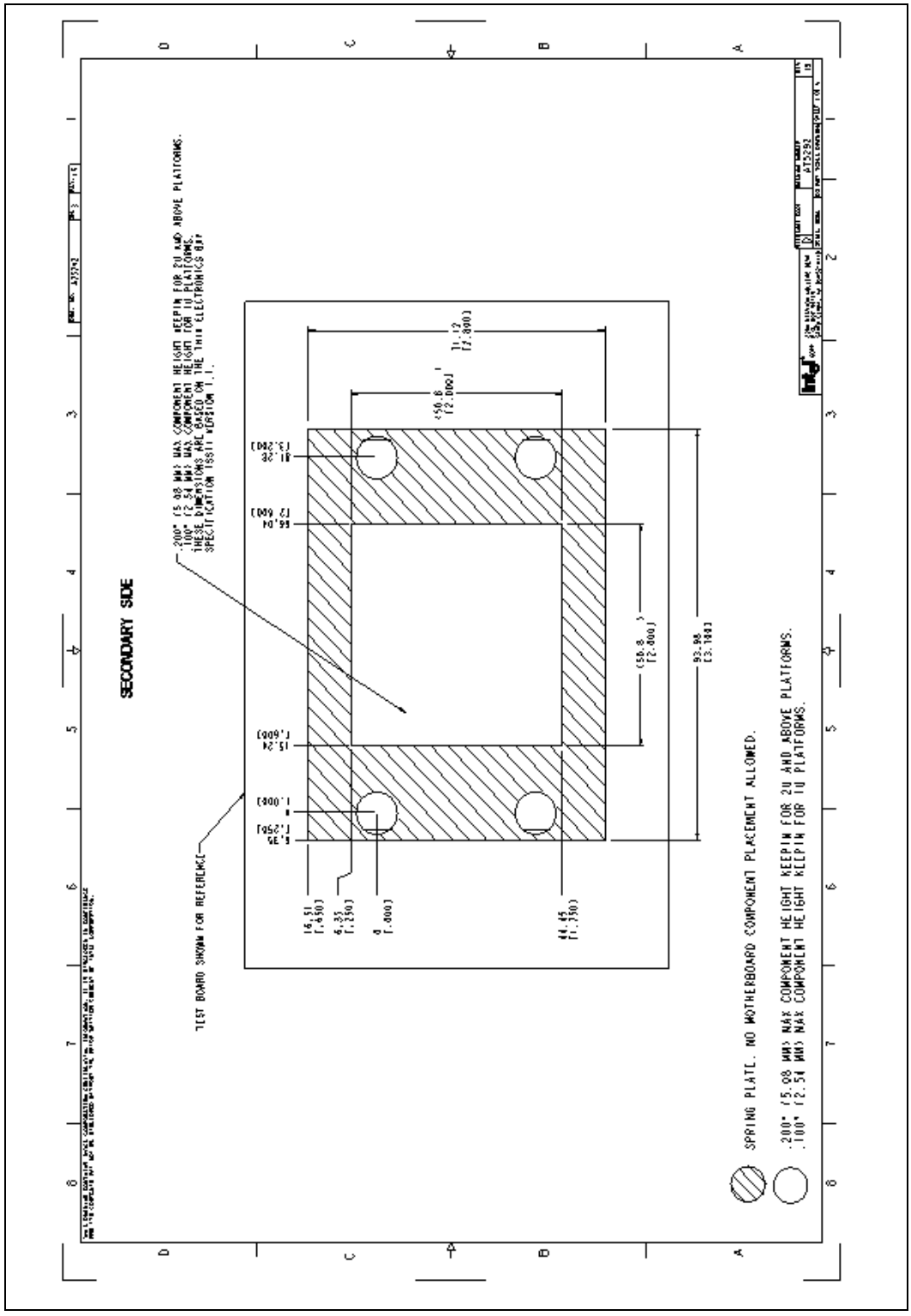


**Figure A-11. Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 4 of 6)**

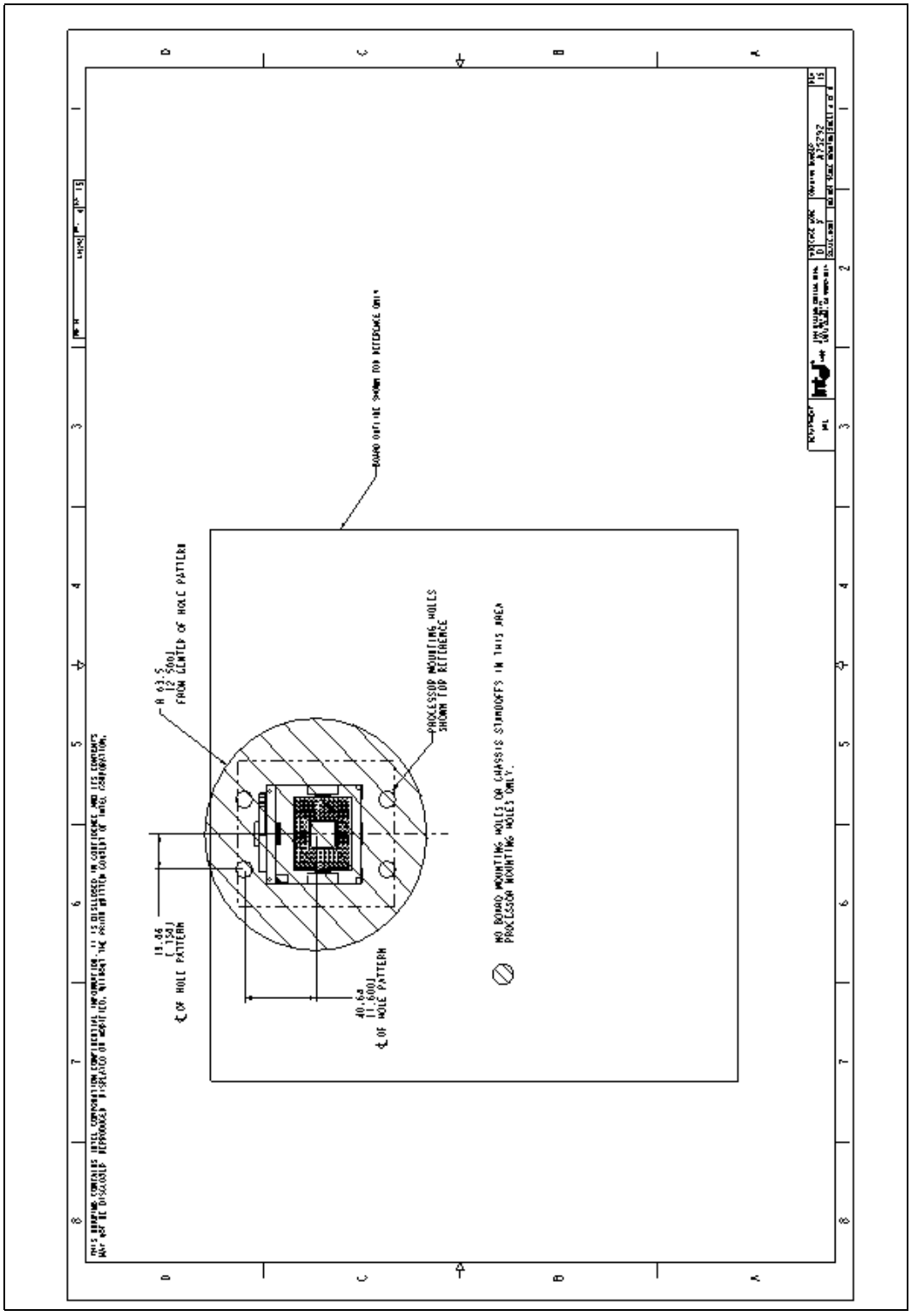


**Figure A-12. Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 5 of 6)**

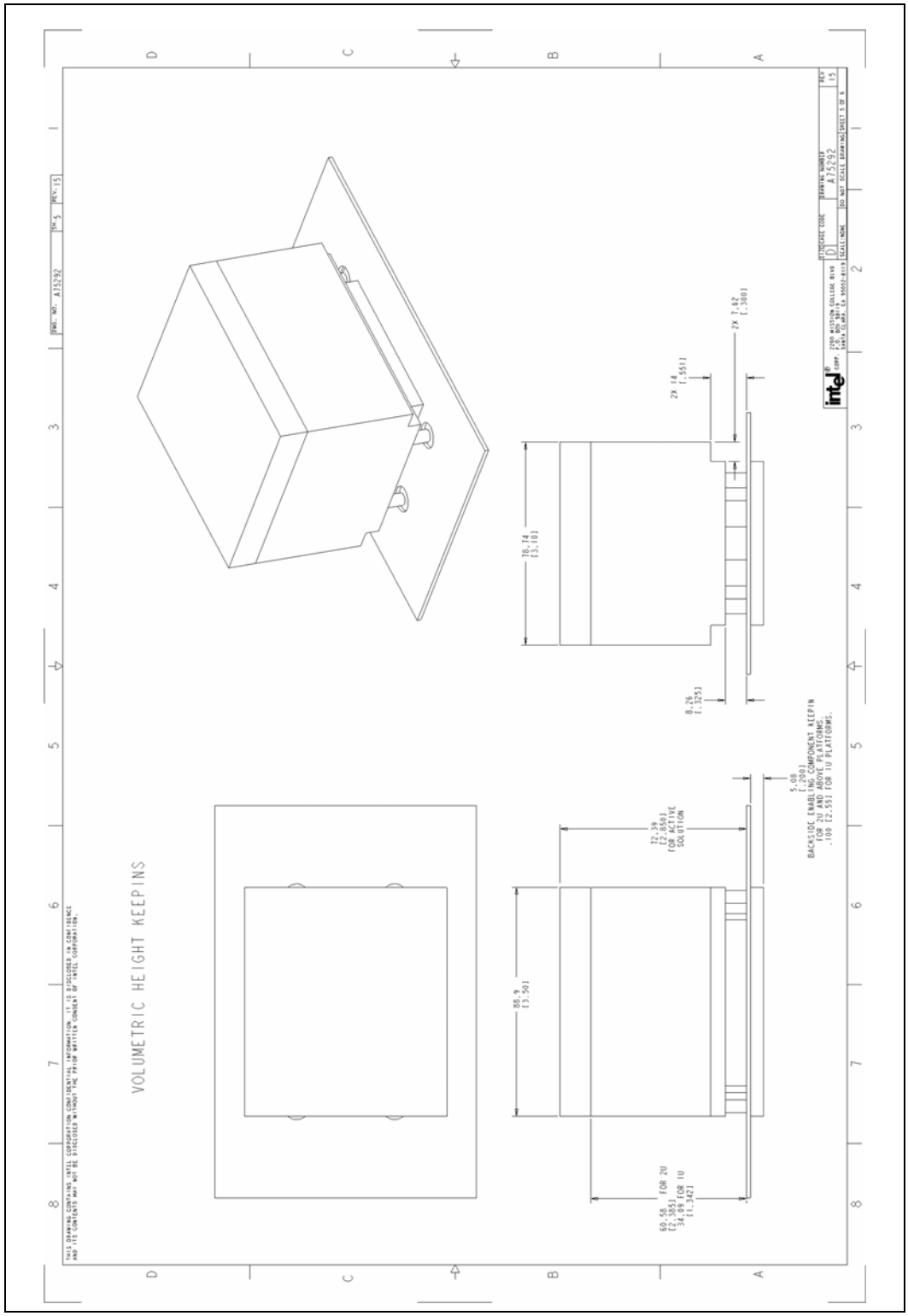


**Figure A-13. Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 6 of 6)**

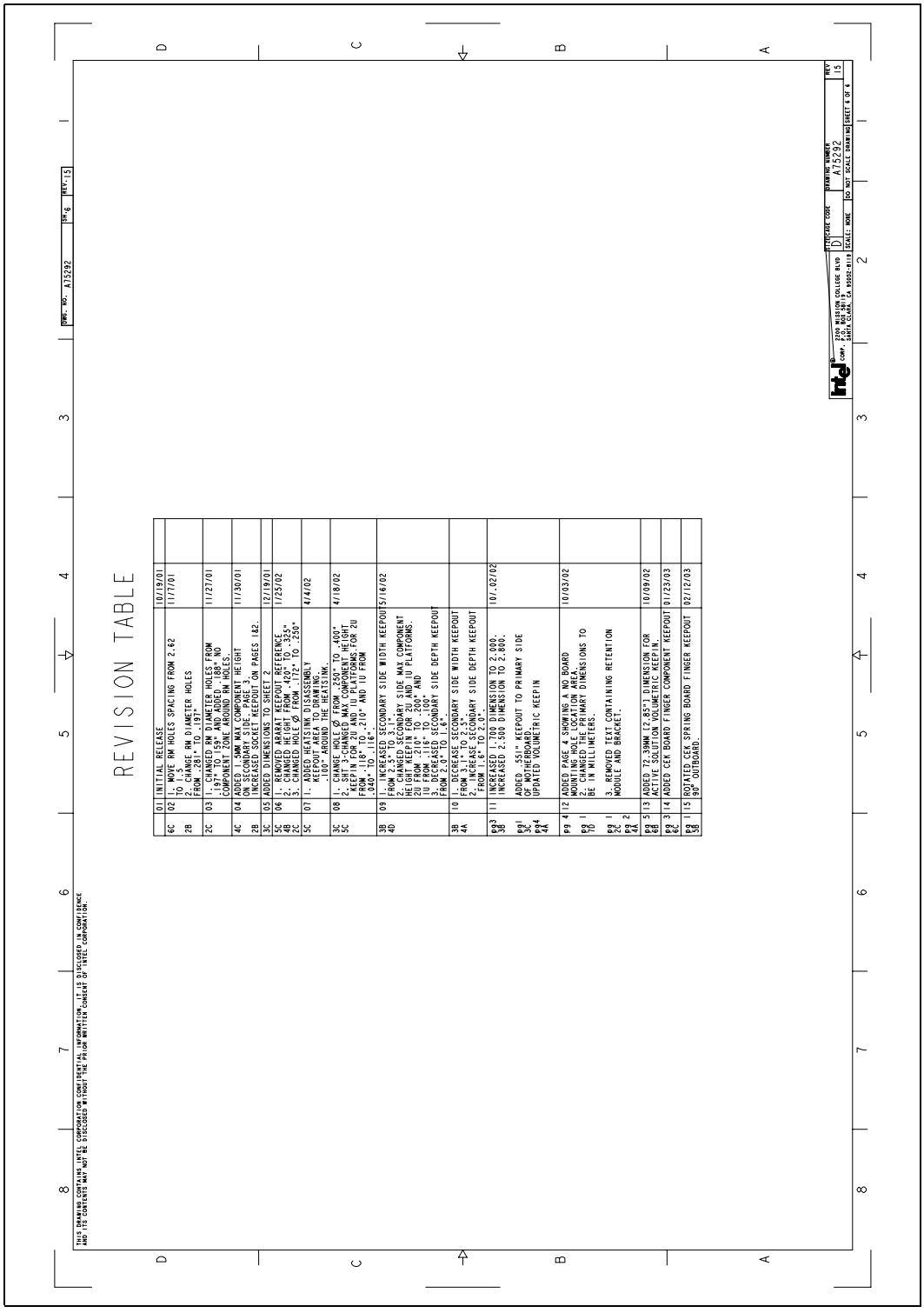


**Figure A-14. 1U CEK Heatsink (Sheet 1 of 4)**

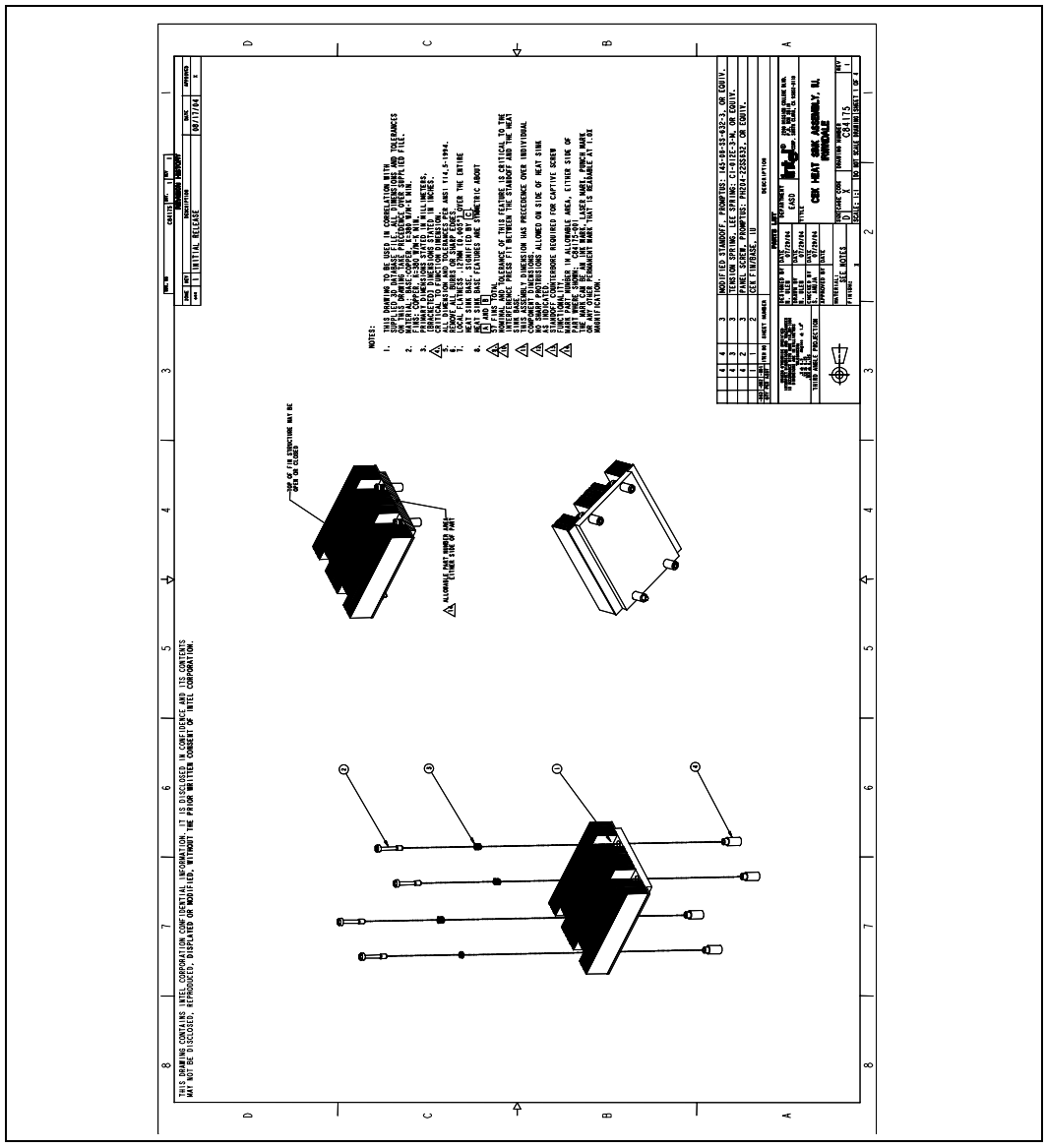


**Figure A-15. 1U CEK Heatsink (Sheet 2 of 4)**

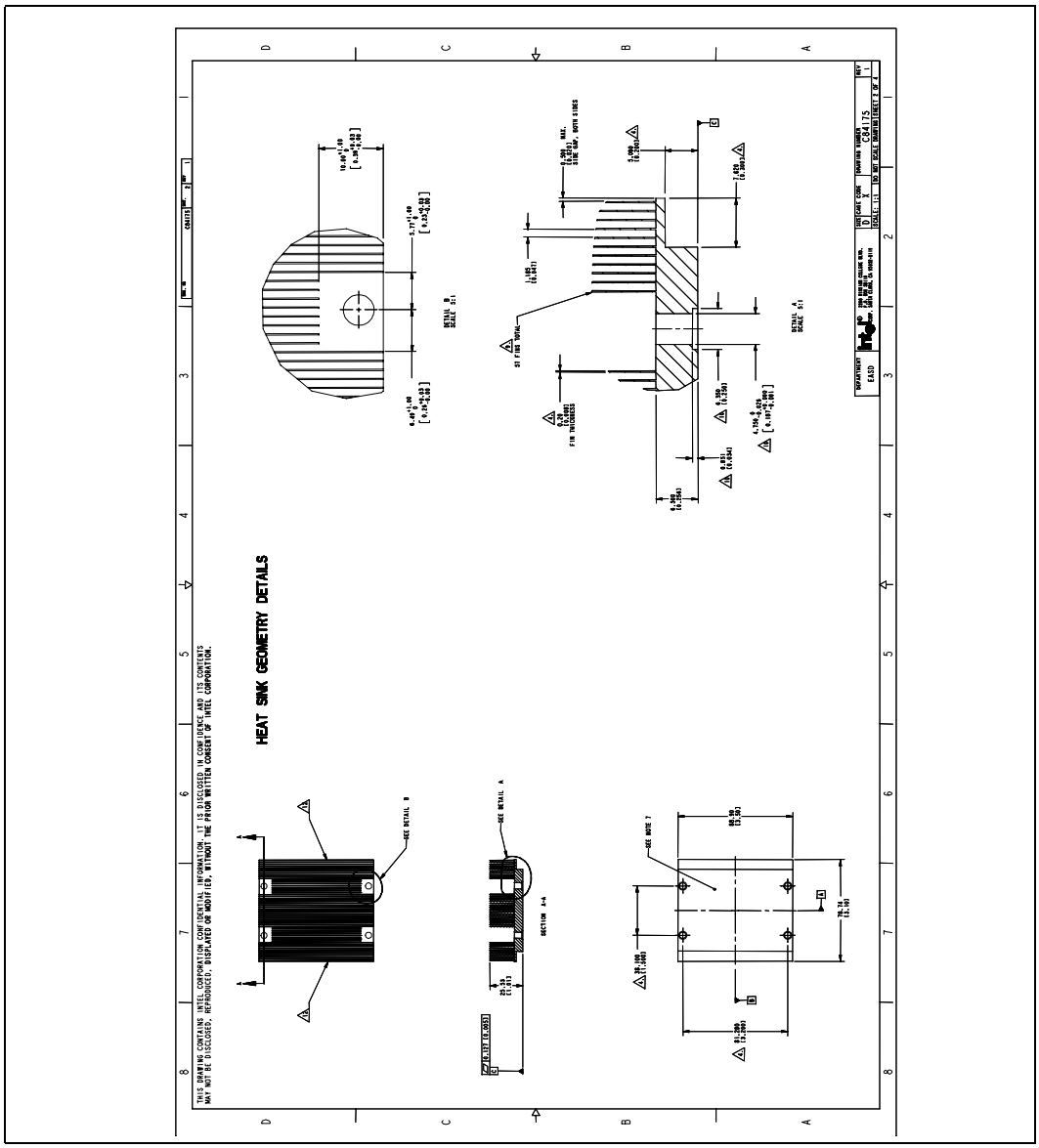


**Figure A-16. 1U CEK Heatsink (Sheet 3 of 4)**

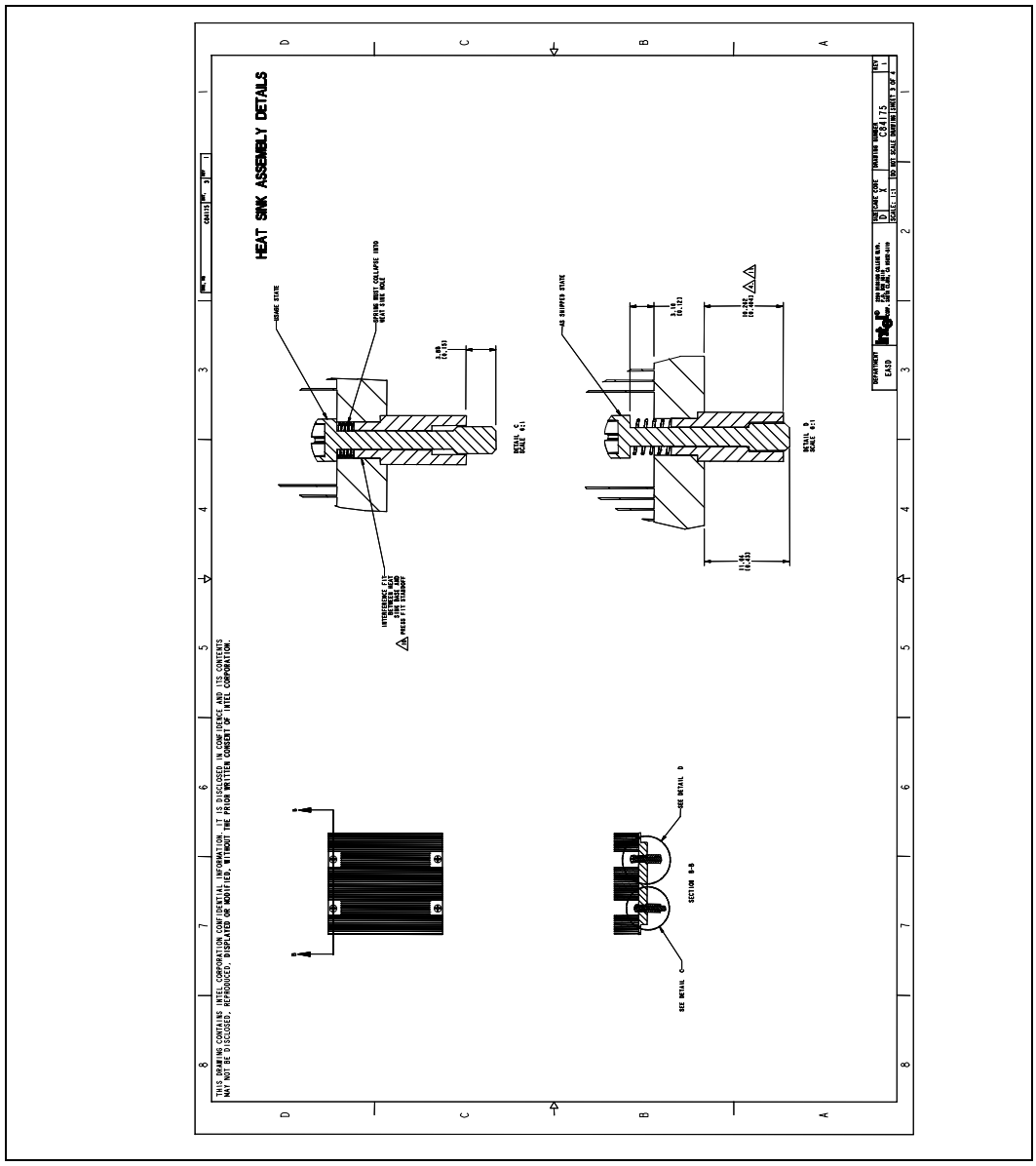
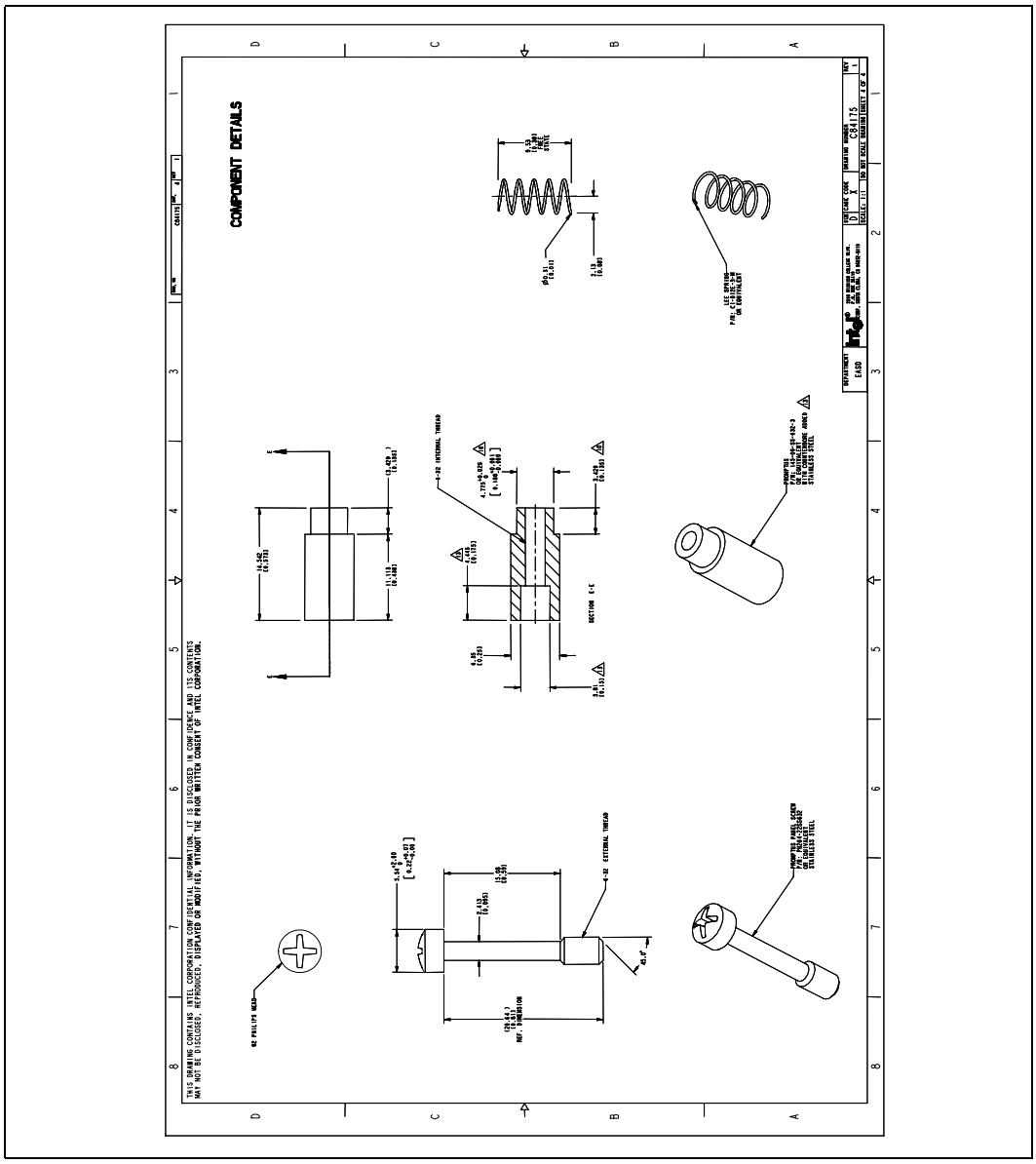


**Figure A-17. 1U CEK Heatsink (Sheet 4 of 4)**

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# B Dual-Core Intel® Xeon® Processor 2.80 GHz Safety Requirements

Heatsink and attachment assemblies shall be consistent with the manufacture of units that meet the safety standards:

1. UL Recognition-approved for flammability at the system level. All mechanical and thermal enabling components must be a minimum UL94V-2 approved.
2. CSA Certification. All mechanical and thermal enabling components must have CSA certification.
3. Heatsink fins must meet the test requirements of UL1439 for sharp edges.

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# C Quality and Reliability Requirements

## C.1 Intel Verification Criteria for the Reference Designs

### C.1.1 Reference Heatsink Thermal Verification

The Intel reference heatsinks will be verified within specific boundary conditions based on the methodology described in *Intel® Xeon® Processor Family Thermal Test Vehicle User's Guide*.

The test results, for a number of samples, are reported in terms of a worst-case mean + 3σ value for thermal characterization parameter using real processors (based on the TTV correction offset).

### C.1.2 Environmental Reliability Testing

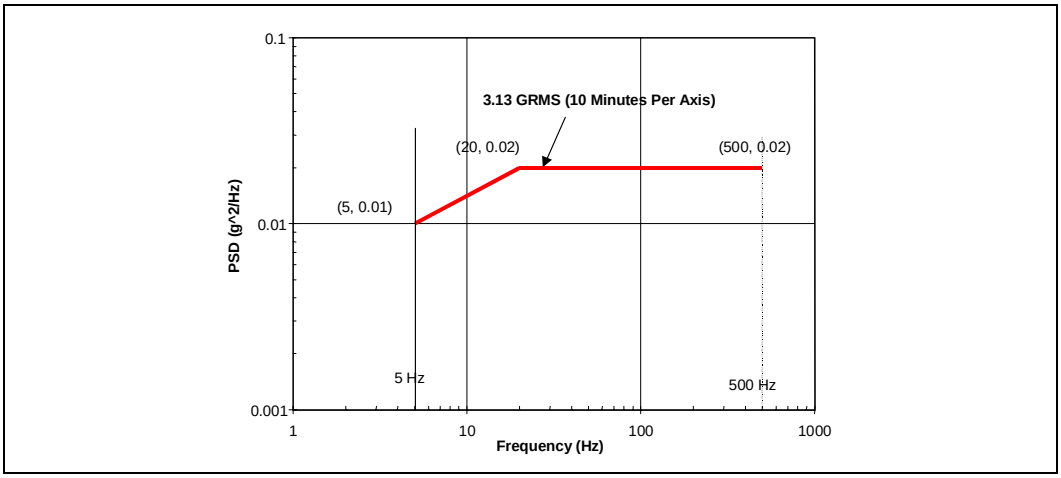
#### C.1.2.1 Structural Reliability Testing

Structural reliability tests consist of unpackaged, board-level vibration and shock tests of a given thermal solution in assembled state, as well as long-term reliability testing (temperature cycling, bake test). The thermal solution should be capable of sustaining thermal performance after these tests are conducted; however, the conditions of the tests outlined here may differ from the customers' system requirements.

#### C.1.2.2 Random Vibration Test Procedure

- Duration: 10 min/axis, 3 axes
- Frequency Range: 5 Hz to 500 Hz
- Power Spectral Density (PSD) Profile: 3.13 G RMS (refer to Figure C-1).

**Figure C-1. Random Vibration PSD**



### C.1.2.3 Shock Test Procedure

Recommended performance requirement for a baseboard:

- Quantity: 3 drops for + and – directions in each of 3 perpendicular axes (i.e. total 18 drops).
- Profile: 50 G trapezoidal waveform, 11 ms duration, 4.32 m/sec minimum velocity change.
- Setup: Mount sample board on test fixture.

**Figure C-2. Shock Acceleration Curve**


### C.1.2.4 Recommended Test Sequence

Each test sequence should start with components (i.e. baseboard, heatsink assembly, etc.) that have not been previously submitted to any reliability testing.

The test sequence should always start with a visual inspection after assembly, and BIOS/Processor/memory test. The stress test should be then followed by a visual inspection and then BIOS/Processor/memory test.

### C.1.2.5 Post-Test Pass Criteria

The post-test pass criteria are:

1. No significant physical damage to the heatsink and retention hardware.
2. Heatsink remains seated and its bottom remains mated flatly against the IHS surface. No visible gap between the heatsink base and processor IHS. No visible tilt of the heatsink with respect to the retention hardware.
3. No signs of physical damage on baseboard surface due to impact of heatsink.
4. No visible physical damage to the processor package.
5. Successful BIOS/Processor/memory test of post-test samples.
6. Thermal compliance testing to demonstrate that the case temperature specification can be met.

### C.1.2.6 Recommended BIOS/Processor/Memory Test Procedures

This test is to ensure proper operation of the product before and after environmental stresses, with the thermal mechanical enabling components assembled. The test shall be conducted on a fully operational baseboard that has not been exposed to any battery of tests prior to the test being considered.

Testing setup should include the following components, properly assembled and/or connected:

- Appropriate system baseboard.
- Processor and memory.
- All enabling components, including socket and thermal solution parts.

The pass criterion is that the system under test shall successfully complete the checking of BIOS, basic processor functions and memory, without any errors. *Intel PC Diags* is an example of software that can be utilized for this test.

## C.1.3 Material and Recycling Requirements

Material shall be resistant to fungal growth. Examples of non-resistant materials include cellulose materials, animal and vegetable based adhesives, grease, oils, and many hydrocarbons. Synthetic materials such as PVC formulations, certain polyurethane compositions (e.g. polyester and some polyethers), plastics which contain organic fillers of laminating materials, paints, and varnishes also are susceptible to fungal growth. If materials are not fungal growth resistant, then MIL-STD-810E, Method 508.4 must be performed to determine material performance.

Material used shall not have deformation or degradation in a temperature life test.

Any plastic component exceeding 25 grams must be recyclable per the European Blue Angel recycling standards.

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# D Supplier Information

## D.1 Intel Enabled Suppliers

The Intel reference solutions have been verified to meet the criteria outlined in Table D-1. Customers can purchase the Intel reference thermal solution components from the suppliers listed in Table D-1.

**Table D-1. Suppliers for the Dual-Core Intel Xeon Processor 2.80 GHz Intel Reference Solution**

| Assembly | Component | Description | Development Suppliers | Supplier Contact Info |
|---|---|---|---|---|
| **CEK604-2U-01 (for 2U, 2U+)** | CEK Heatsink | Copper Fin, Copper Base | Fujikura<br>CNDA 36187<br>(stacked fin)<br><br>Furukawa<br>CNDA 65755<br>(crimped fin) | Mechatronics<br>Steve Carlson<br>800-453-4569 x205<br>steve@mechatronics.com<br><br>Furukawa America<br>Katsu Mizushima<br>(408) 232-9306<br>katsumizushima@mindspring.com |
| | Thermal Interface Material | Grease | Shin-Etsu G751<br>CNDA 75610 | Donna Hartigan<br>(480) 893-8898 |
| | CEK Spring | Stainless Steel 301, Kapton* Tape on Spring Fingers | ITW Fastex*<br>CNDA 78538<br><br>AVC<br>CNDA 2085011<br><br>Foxconn<br>CNDA 11251 | Ron Schmidt<br>(847) 299-2222<br>rschmidt@itwfastex.com<br><br>Felicia Lee<br>886-2-22996390 x144<br>felicia@avc.com.tw |

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