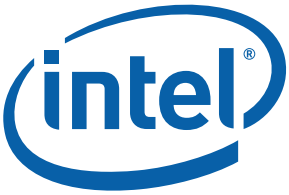
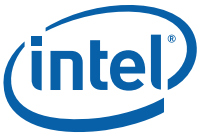


Dual-Core Intel® Xeon® Processor LV and ULV

Datasheet

September 2006

311391-002US



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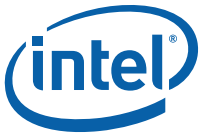


Revision History

Date	Revision	Description
September 2006	002	• Replaced all occurrences of Enhanced HALT State with Extended HALT State • Added references to Dual-Core Intel® Xeon® Processor ULV • Table 7: Added line for Icc at 1.66 GHz • Table 7: Updated HFM VID for LV parts • Table 11: Updated BR0# and BR1# description • Table 14: Added line for TDP at 1.66 GHz • Add Table 8: DC Specification for ULV part • Add Table 15: Thermal Specification for ULV part
March 2006	001	Initial public release.

1.0 Introduction

The Dual-Core Intel® Xeon® Processor LV and ULV on 65 nanometer process is the next generation high-performance, low-power processor for embedded, communications infrastructure, storage and server applications.

This document provides specifications for the following processors:

- Dual-Core Intel® Xeon® Processor LV
- Dual-Core Intel® Xeon® Processor ULV

Note: All references to "processor" applies to all the processors mentioned in the above list unless specific exceptions are mentioned.

The following list provides some of the key features on this processor:

- Dual processing (DP) support, with two cores per processor, allowing up to four execution threads per system
- 36-bit physical addressing
- Address, Data, and Response Parity on the Front Side Bus (FSB)
- Supports Intel Architecture with Dynamic Execution
- On-die, 32 kB Level 1 instruction cache and 32 kB write-back data cache (per execution core)
- On-die, 2 MB, ECC protected, Level 2 cache with Advanced Transfer Cache Architecture (shared between the two execution cores)
- Data Prefetch Logic
- Streaming SIMD Extensions 2 (SSE2) and streaming Single Instruction Multiple Data (SIMD) Extensions 3 (SSE3)
- 667 MT/s, Source-Synchronous FSB
- Advanced Power Management features including Enhanced Intel SpeedStep® Technology
- Digital Thermal Sensor (DTS)
- Intel® Thermal Monitor 1 (TM1) and Thermal Monitor 2 (TM2)
- Micro-FCPGA packaging technologies
- Execute Disable Bit support for enhanced security
- Intel Virtualization Technology

The processor is manufactured on Intel's advanced 65 nanometer process technology with copper interconnect. The processor maintains support for MMX™ Technology and Streaming SIMD instructions and full compatibility with IA32 software. The on-die, 32 kB Level 1 instruction and data caches and the 2 MB Level 2 cache with Advanced Transfer Cache Architecture enable performance improvement over existing low power processors. The processor's Data Prefetch Logic speculatively fetches data to the L2 cache before an L1 cache request occurs, resulting in reduced bus cycle penalties and improved performance. The processor includes the Data Cache Unit Streamer, which enhances the performance of the L2 prefetcher by requesting L1 warm-ups earlier. In addition, Write Order Buffer depth is enhanced to help with write-back latency performance.

In addition to supporting all the existing Streaming SIMD Extensions 2 (SSE2), there are 13 new instructions, which further extend the capabilities of Intel processor technology. These new instructions are called Streaming SIMD Extensions 3 (SSE3).

These new instructions enhance the performance of optimized applications such as video, image processing and media compression technology. 3D graphics and other video intense applications have the opportunity to take advantage of these new instructions as platforms with the processor and SSE3 become available in the marketplace.

The processor's front side bus (FSB) utilizes a split-transaction, deferred reply protocol. The FSB uses Source-Synchronous Transfer (SST) of address and data to improve performance by transferring data four times per bus clock (4X data transfer rate, as in AGP 4X). Along with the 4X data bus, the address bus can deliver addresses two times per bus clock and is referred to as a "double-clocked" or 2X address bus. Working together, the 4X data bus and 2X address bus provide a data bus bandwidth of up to 5.33 GB/second. The FSB uses Advanced Gunning Transceiver Logic (AGTL+) signalling technology, a variant of GTL+ signaling technology with low power enhancements.

The processor features Enhanced Intel SpeedStep® Technology, which enables real-time dynamic switching between multiple voltage and frequency points. This results in optimal performance without compromising low power. The processor also features the Auto Halt low power state.

The processor utilizes socketable Micro Flip-Chip Pin Grid Array (Micro-FCPGA) package technology. The Micro-FCPGA package plugs into a 478-hole, surface-mount, Zero Insertion Force (ZIF) socket, which is referred to as the mPGA478 socket.

The processor supports the Execute Disable Bit capability. This feature combined with a support operating system allows memory to be marked as executable or non executable. If code attempts to run in non-executable memory the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can thus help improve the overall security of the system. See the Intel® Architecture Software Developer's Manual for more detailed information.

Intel® Virtualization Technology (VT) is a set of hardware enhancements to Intel server and client systems if combined with the appropriate software, will enable enhanced virtualization robustness and performance for both enterprise and consumer uses, VT forms the foundation of Intel technologies focused on improving virtualization, safer computing and system stability. For client systems, VT's hardware-based isolation helps provide the foundation for highly available and more secure client virtualization partitions.

1.1 Terminology

Table 1. Terminology

Term	Definition
#	A "#" symbol after a signal name refers to an active low signal, indicating a signal is in the active state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the "#" symbol implies that the signal is inverted. For example, D[3:0] = "HLHL" refers to a hex 'A', and D[3:0]# = "LHLH" also refers to a hex "A" (H= High logic level, L= Low logic level). XXXX means that the specification or value is yet to be determined.
AGTL+	Advanced Gunning Transceiver Logic. Used to refer to Assisted GTL+ signaling technology on some Intel processors.
Dual Core Processor	A single package that contains two complete execution cores.
Dual Processor	Used to specify a system configuration that supports up to two physical processor packages on the FSB.

Table 1. Terminology

Term	Definition
Front Side Bus (FSB)	The electrical interface that connects the processor to the chipset. Also referred to as the processor system bus or the system bus. All memory and I/O transactions as well as interrupt messages pass between the processor and chipset over the FSB.
GTLREF	A reference voltage level used on the system bus to determine the logical state of a signal.
MT/s	Megatransfers/second
Overshoot	The maximum voltage observed for a signal at the device pad, measured with respect to the buffer reference voltage.
Pad	The electrical contact point of a semiconductor die to the package substrate. A pad is only observable in simulations.
Processor	A single package that contains one or more complete execution cores.
RASUM	Reliability, Availability, Serviceability, Usability, and Manageability.
Ringback	The voltage to which a signal transitions to just after reaching its maximum absolute value. Ringback may be caused by reflections, driver oscillations, or other transmission line phenomena.
Undershoot	The minimum voltage extending below VSS observed for a signal at the device pad.
VRD	Voltage Regulator-Down for the processor that supplies the required voltage and current to a single processor.

1.2 References

Material and concepts available in the following documents may be beneficial when reading this document.

Table 2. References

Document	Order Number[1]
Dual-Core Intel® Xeon processor LV and ULV Specification Update	developer.intel.com
Intel® 6300ESB I/O Controller Datasheet	developer.intel.com
Embedded Voltage Regulator-Down (EmVRD) 11.0 Design Guidelines for Embedded Implementations Supporting PGA478	developer.intel.com
ITP700 Debug Port Design Guide	249679 (developer.intel.com)
Intel® E7520 Memory Controller Hub (MCH) Datasheet	303006 (developer.intel.com)
Intel® 3100 Chipset Datasheet	313458 (developer.intel.com)
Dual-Core Intel® Xeon® Processor LV and ULV Thermal Design Guideline for Embedded Applications	developer.intel.com/
Intel® Architecture Software Developer's Manual	developer.intel.com/ design/pentium4/ manuals/ index_new.htm
Volume 1: Basic Architecture	253665
Volume 2A/2B: Instruction Set Reference	253666 / 253667
Volume 3A/3B: System Programming Guide	253668 / 253669
Intel ® Processor Identification and CPUID Instruction application note (AP-485)	www.intel.com/ support/processors/sb/ cs-009861.htm

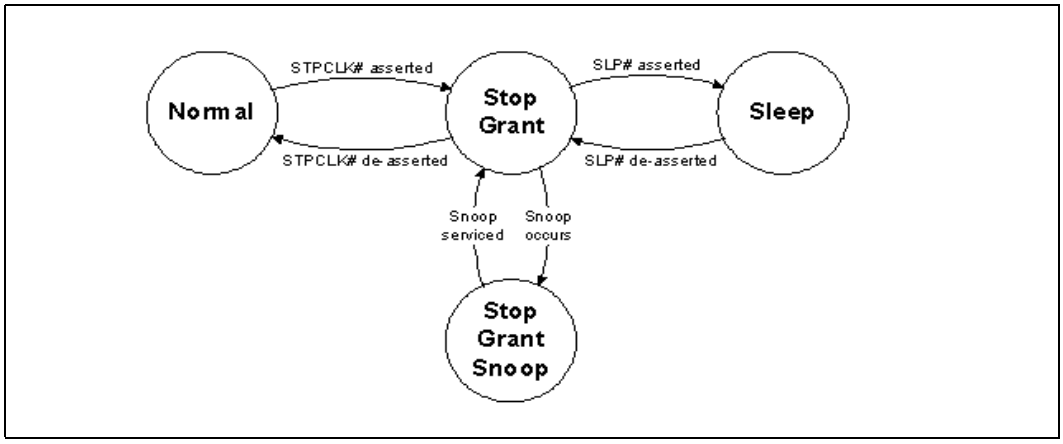
1. Order numbers are subject to change.

2.0 Low Power Features

2.1 Clock Control and Low Power States

The Dual-Core Intel® Xeon® Processor LV and ULV supports the C1/AutoHALT, C1/MWAIT, Stop Grant and Sleep states for optimal power management. C1/AutoHALT and C1/MWAIT are core-level low power states only, they do not have package-level behavior. See Figure 1 for a visual representation of package level low-power states for a Dual-Core Intel® Xeon® Processor LV. Each core of the processor can enter the C1/AutoHALT/MWAIT state independent of the other core.

Figure 1. Package-Level Low Power States



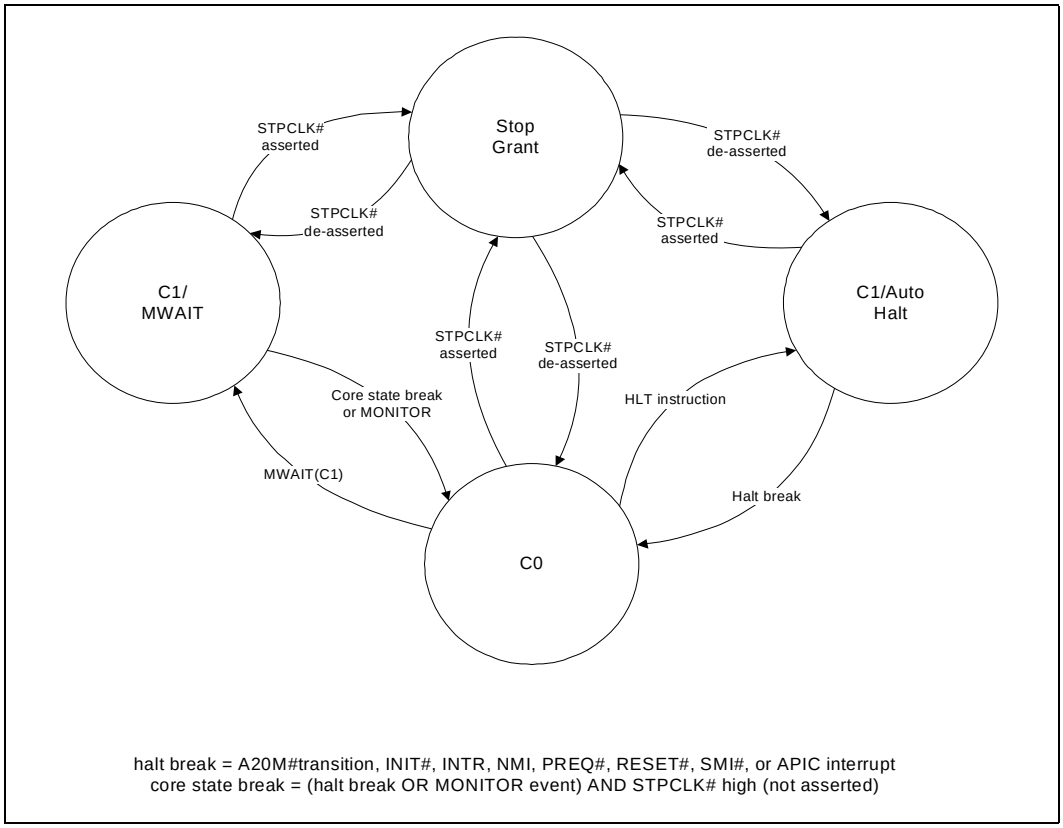
Refer to Figure 2 for a visual representation of the core low-power states for the processor.

The processor implements two software interfaces for requesting low power states: the I/O mapped ACPI P_BLK register block and the C-state extension to the MWAIT instruction. Either interface can be used at any time. Each core in the processor presents an independent low power state request interface (ACPI P_BLK or MWAIT). Requests from the software running on one core puts that core into a core-level low power state. The processor has logic for coordinating low power state requests from each core. This logic will put the processor into a package-level low power state based on the highest common core low power state.

Due to the inability of processors to recognize bus transactions during the Sleep state, multiprocessor systems are not allowed to simultaneously have one processor in Sleep state and the other processors in Normal or Stop-Grant state.

If a core encounters a break event while STPCLK# is asserted, it returns to C0 state by asserting the PBE# output signal. PBE# assertion signals to system logic that the processor needs to return to the Normal package-level state. This will allow individual cores to return to the C0 state.

Figure 2. Core Low Power States



2.1.1 Core Low Power States

2.1.1.1 C0 State - Normal State

This is the normal operating state for the processor.

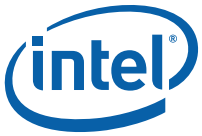
2.1.1.2 C1/AutoHALT Powerdown State

AutoHALT is a low power state entered when the processor executes the HALT instruction. The processor transitions to the Normal state upon the occurrence of SMI#, BINIT#, INIT#, LINT[1:0] (NMI, INTR), or an interrupt delivered over the system bus. RESET# causes the processor to immediately initialize itself.

The return from a System Management Interrupt (SMI) handler can be to either Normal Mode or the AutoHALT Power Down state. See the Intel Architecture Software Developer's Manual, Volume 3: System Programmer's Guide for more information.

The system can generate a STPCLK# while the processor is in the AutoHALT Power Down state. When the system deasserts the STPCLK# interrupt, the processor returns execution to the HALT state.

While in AutoHALT Power Down state, the processor processes system bus snoops and snoops from the other core.



2.1.1.3 C1/MWAIT Powerdown State

MWAIT is a low power state entered when the processor core executes the MWAIT instruction. Processor behavior in the MWAIT state is identical to the AutoHALT state except that there is an additional event that can cause the processor core to return to the C0 state: the Monitor event. See the *Intel Architecture Software Developer's Manual, Volume 2A/2B: Instruction Set Reference* for more information.

2.1.2 Package Low Power States

The following sections describe all package-level low power states for the processor.

2.1.2.1 Normal State

This is the normal operating state for the processor. processor enters the normal state when at least one of its cores is in the Normal, AutoHALT, or MWAIT state.

2.1.2.2 Stop-Grant State

When the STPCLK# pin is asserted, the Stop-Grant state of the processor is entered 20 bus clocks after the response phase of the processor-issued Stop Grant Acknowledge special bus cycle. Once the STPCLK# pin has been asserted, it may only be deasserted once the processor is in the Stop Grant state. For the processor, both processor cores must be in the Stop Grant state before the deassertion of STPCLK#.

Since the AGTL+ signal pins receive power from the system bus, these pins should not be driven (allowing the level to return to V_{CCP}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the system bus should be driven to the inactive state.

BINIT# is not serviced while the processor is in Stop-Grant state. The event is latched and can be serviced by software upon exit from the Stop Grant state.

RESET# causes the processor to immediately initialize itself, but the processor stays in Stop-Grant state. A transition back to the Normal state occurs with the deassertion of the STPCLK# signal. When re-entering the Stop-Grant state from the Sleep state, STPCLK# should only be deasserted one or more bus clocks after the deassertion of SLP#.

A transition to the HALT/Grant Snoop state occurs when the processor detects a snoop on the system bus A transition to the Sleep state occurs with the assertion of the SLP# signal.

While in the Stop-Grant state, SMI#, INIT#, BINIT# and LINT[1:0] is latched by the processor, and only serviced when the processor returns to the Normal state. Only one occurrence of each event is recognized upon return to the Normal state.

While in Stop-Grant state, the processor processes snoops on the system bus and it latches interrupts delivered on the system bus.

The PBE# signal can be driven when the processor is in Stop-Grant state. PBE# is asserted if there is any pending interrupt latched within the processor. Pending interrupts that are blocked by the EFLAGS.IF bit being clear still causes assertion of PBE#. Assertion of PBE# indicates to system logic that it should return the processor to the Normal state.

2.1.2.3 Stop Grant Snoop State

The processor will respond to snoop or interrupt transactions on the FSB while in Stop-Grant state. During a snoop or interrupt transaction, the processor enters the Stop Grant Snoop state. The processor will stay in this state until the snoop on the FSB has been serviced (whether by the processor or another agent on the FSB) or the interrupt has been latched. After the snoop is serviced or the interrupt is latched, the processor will return to the Stop-Grant state.

2.1.2.4 Sleep State

The Sleep state is a very low power state in which each processor maintains its context, maintains the phase-locked loop (PLL), and has stopped most of internal clocks. The Sleep state can only be entered from Stop-Grant state. Once in the Stop-Grant state, the processor enters the Sleep state upon the assertion of the SLP# signal. The SLP# pin has a minimum assertion of one BCLK period. The SLP# pin should only be asserted when the processor is in the Stop Grant state. For the processor, the SLP# pin may only be asserted when all processor cores are in the Stop-Grant state. SLP# assertions while the processors are not in the Stop-Grant state are out of specification and may results in illegal operation.

Snoop events that occur while in Sleep state or during a transition into or out of Sleep state causes unpredictable behavior.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP# or RESET#) are allowed on the system bus while the processor is in Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state results in unpredictable behavior.

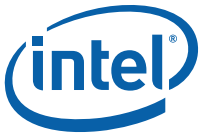
If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, then the processor resets itself, ignoring the transition through Stop-Grant state. If RESET# is driven active while the processor is in the Sleep state, the SLP# and STPCLK# signals should be deasserted immediately after RESET# is asserted to ensure the processor correctly executes the reset sequence.

When the processor is in Sleep state, it does not respond to interrupts or snoop transactions.

2.2 Enhanced Intel SpeedStep® Technology

The processors feature Enhanced Intel SpeedStep® Technology. Following are the key features:

- Multiple voltage/frequency operating points provide optimal performance at the lowest power.
- Voltage/Frequency selection is software controlled by writing to processor MSR's (Model Specific Registers).
  - If the target frequency is higher than the current frequency, V_{CC} is ramped up in steps by placing new values on the VID pins and the PLL then locks to the new frequency.
  - If the target frequency is lower than the current frequency, the PLL locks to the new frequency and the V_{CC} is changed through the VID pin mechanism.
  - Software transitions are accepted at any time. If a previous transition is in progress, the new transition is deferred until the previous transition completes.
- The processor controls voltage ramp rates internally to ensure smooth transitions.
- Low transition latency and large number of transitions possible per second.



  - — Processor core (including L2 cache) is unavailable for up to 10 µs during the frequency transition
  - — The bus protocol (BNR# mechanism) is used to block snooping
- Intel® Thermal Monitor 2 (TM2)
  - — When the on-die thermal sensor indicates that the die temperature is too high, the processor can automatically perform a transition to a lower frequency/ voltage specified in a software programmable MSR.
  - — The processor waits for a fixed time period. If the die temperature is down to acceptable levels, an up transition to the previous frequency/voltage point occurs.
  - — A software interrupt is generated for each Intel Thermal Monitor transition, enabling better system level thermal management.

Note: VID ranges supported by the Enhanced Intel SpeedStep Technology (EIST) may be different among processor family of processors.

Each core in the processor implements an independent MSR for controlling Enhanced Intel SpeedStep Technology, but both cores must operate at the same frequency and voltage. The processor has performance state coordination logic to resolve frequency and voltage requests from the two cores into a single frequency and voltage request for the package as a whole. If both cores request the same frequency and voltage, then the processor transitions to the requested common frequency and voltage. If the two cores have different frequency and voltage requests, then the processor takes the highest of the two frequencies and voltages as the resolved request and transitions to that frequency and voltage.

2.3 Extended Halt State (C1E)

The processor combines Enhanced Intel SpeedStep Technology with the low power states to reduce processor power even further. Extended HALT state is a low power state entered when both processor cores have executed the HALT or MWAIT instructions and Extended HALT state has been enabled via the BIOS. When one of the processor cores executes the HALT instruction, that processor core is halted; however, the other processor core continues normal operation. The Extended HALT state is a lower power state than the HALT state or Stop Grant state.

The Extended HALT state must be enabled for the processor to remain within its specifications. The Extended HALT state requires support for dynamic VID transitions in the platform.

The processor will automatically transition to a lower core frequency and voltage operating point before entering the Extended HALT state. Note that the processor FSB frequency is not altered; only the internal core frequency is changed. When entering the low power state, the processor will first switch to the lower bus to core frequency ratio and then transition to the lower voltage (VID).

While in the Extended HALT state, the processor will process bus snoops. The processor exits the Extended HALT state when a break event occurs. When the processor exits the Extended HALT state, it will first transition the VID to the original value and then change the bus to core frequency ratio back to the original value.

3.0 Electrical Specifications

3.1 Front Side Bus and GTLREF

Most Dual-Core Intel® Xeon® Processor LV and ULV FSB signals use Advanced Gunning Transceiver Logic (AGTL+) signalling technology. This signalling technology provides improved noise margins and reduced ringing through low-voltage swings and controlled edge rates. The termination voltage level for the processor AGTL+ signals is V_{CCP}= 1.05 V (nominal). Due to speed improvements to data and address bus, signal integrity and platform design methods have become more critical than with previous processor families.

The AGTL+ inputs require a reference voltage (GTLREF) that is used by the receivers to determine if a signal is a logical 0 or a logical 1. GTLREF must be generated on the system board. Termination resistors are provided on the processor silicon and are terminated to its I/O voltage (V_{CCP}).

The AGTL+ bus depends on incident wave switching. Therefore, timing calculations for AGTL+ signals are based on flight time as opposed to capacitive deratings. Analog signal simulation of the FSB, including trace lengths, is highly recommended when designing a system.

3.2 Power and Ground Pins

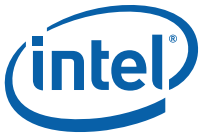
For clean, on-chip power distribution, the processor has a large number of V_{CC} (power) and V_{SS} (ground) inputs. All power pins must be connected to V_{CC} power planes while all V_{SS} pins must be connected to system ground planes. Use of multiple power and ground planes is recommended to reduce I*R drop. The processor V_{CC} pins must be supplied with the voltage determined by the VID (Voltage ID) pins.

3.3 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large average current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Care must be taken in the board design to ensure that the voltage provided to the processor remains within the specifications listed in Table 7. Failure to do so can result in timing violations or reduced lifetime of the component.

3.3.1 V_{CC} Decoupling

Regulator solutions need to provide bulk capacitance with a low effective series resistance (ESR) and keep a low interconnect resistance from the regulator to the socket. Bulk decoupling for the large current swings when the part is powering on, or entering/exiting low-power states, must be provided by the voltage regulator solution. For more details on decoupling recommendations, please refer to the *Embedded Voltage Regulator-Down (EmVRD) 11.0 Design Guidelines for Embedded Implementations Supporting PGA478.* It is strongly recommended that the layout and decoupling recommendations in the design guide be followed.



3.3.2 FSB AGTL+ Decoupling

The processor integrates signal termination on the die as well as incorporate high frequency decoupling capacitance on the processor package. Decoupling must also be provided by the system motherboard for proper AGTL+ bus operation.

3.3.3 FSB Clock (BCLK[1:0]) and Processor Clocking

BCLK[1:0] directly controls the FSB interface speed as well as the core frequency of the processor. As in previous generation processors, the processor core frequency is a multiple of the BCLK[1:0] frequency. The processor bus ratio multiplier is set at its default ratio at manufacturing. The processor uses a differential clocking implementation.

3.3.4 Mixed Frequency in Dual Processor Systems

While Intel has done nothing to specifically prevent processors operating at differing frequencies from functioning within a multiprocessor system, there may be uncharacterized errata that exist in such configurations. Intel does not support such configurations. In mixed stepping systems, all processors must operate at identical frequencies (i.e., the highest frequency rating commonly supported by all processors).

3.3.5 Mixed Steppings in Dual Processor Systems

Intel fully supports mixed steppings of the processor. Mixed steppings are only supported with processors that have identical family numbers as indicated by the CPUID instruction.

3.4 Voltage Identification and Power Sequencing

The VID specification for the processor is defined by the *Embedded Voltage Regulator-Down (EmVRD) 11.0 Design Guidelines for Embedded Implementations Supporting PGA478*.

The processor uses six voltage identification pins, VID[5:0], to support automatic selection of power supply voltages. The VID pins for processor are CMOS outputs driven by the processor VID circuitry. Table 3 specifies the voltage level corresponding to the state of VID[5:0]. A 1 in this refers to a high-voltage level and a 0 refers to low-voltage level. For more details about VR design to support the processor power supply requirements, please refer to the *Embedded Voltage Regulator-Down (EmVRD) 11.0 Design Guidelines for Embedded Implementations Supporting PGA478.*

Power source characteristics must be stable whenever the supply to the voltage regulator is stable.

Table 3. Processor VID Map (Sheet 1 of 3)

VID5	VID4	VID3	VID2	VID1	VID0	Vcc (V)
0	0	0	0	0	0	OFF
0	0	0	0	0	1	1.6000
0	0	0	0	1	0	1.5875
0	0	0	0	1	1	1.5750
0	0	0	1	0	0	1.5625
0	0	0	1	0	1	1.5500
0	0	0	1	1	0	1.5375

Table 3. Processor VID Map (Sheet 2 of 3)

VID5	VID4	VID3	VID2	VID1	VID0	Vcc (V)
0	0	0	1	1	1	1.5250
0	0	1	0	0	0	1.5125
0	0	1	0	0	1	1.5000
0	0	1	0	1	0	1.4875
0	0	1	0	1	1	1.4750
0	0	1	1	0	0	1.4625
0	0	1	1	0	1	1.4500
0	0	1	1	1	0	1.4375
0	0	1	1	1	1	1.4250
0	1	0	0	0	0	1.4125
0	1	0	0	0	1	1.4000
0	1	0	0	1	0	1.3875
0	1	0	0	1	1	1.3750
0	1	0	1	0	0	1.3625
0	1	0	1	0	1	1.3500
0	1	0	1	1	0	1.3375
0	1	0	1	1	1	1.3250
0	1	1	0	0	0	1.3125
0	1	1	0	0	1	1.3000
0	1	1	0	1	0	1.2875
0	1	1	0	1	1	1.2750
0	1	1	1	0	0	1.2625
0	1	1	1	0	1	1.2500
0	1	1	1	1	0	1.2375
0	1	1	1	1	1	1.2250
1	0	0	0	0	0	1.2125
1	0	0	0	0	1	1.2000
1	0	0	0	1	0	1.1875
1	0	0	0	1	1	1.1750
1	0	0	1	0	0	1.1625
1	0	0	1	0	1	1.1500
1	0	0	1	1	0	1.1375
1	0	0	1	1	1	1.1250
1	0	1	0	0	0	1.1125
1	0	1	0	0	1	1.1000
1	0	1	0	1	0	1.0875
1	0	1	0	1	1	1.0750
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1	0	1	1	1	0	1.0375

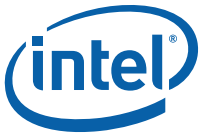


Table 3. Processor VID Map (Sheet 3 of 3)

VID5	VID4	VID3	VID2	VID1	VID0	Vcc (V)
1	0	1	1	1	1	1.0250
1	1	0	0	0	0	1.0125
1	1	0	0	0	1	1.0000
1	1	0	0	1	0	0.9875
1	1	0	0	1	1	0.9750
1	1	0	1	0	0	0.9625
1	1	0	1	0	1	0.9500
1	1	0	1	1	0	0.9375
1	1	0	1	1	1	0.9250
1	1	1	0	0	0	0.9125
1	1	1	0	0	1	0.9000
1	1	1	0	1	0	0.8875
1	1	1	0	1	1	0.8750
1	1	1	1	0	0	0.8625
1	1	1	1	0	1	0.8500
1	1	1	1	1	0	0.8375
1	1	1	1	1	1	0.8250

3.5 Catastrophic Thermal Protection

The processor supports the THERMTRIP# signal for catastrophic thermal protection. An external thermal sensor should also be used to protect the processor and the system against excessive temperatures. Even with the activation of THERMTRIP#, which halts all processor internal clocks and activity, leakage current can be high enough such that the processor cannot be protected in all conditions without the removal of power to the processor. If the external thermal sensor detects a catastrophic processor temperature of approximately 125 °C (maximum), or if the THERMTRIP# signal is asserted, the V_{CC} supply to the processor must be turned off within 500 ms to prevent permanent silicon damage due to thermal runaway of the processor.

3.6 Signal Terminations and Unused Pins

All RSVD (RESERVED) pins must remain unconnected. Connection of these pins to V_{CC}, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future processors. See Table 14 for a pin listing of the processor and the location of all RSVD pins.

For reliable operation, always connect unused inputs or bidirectional signals to an appropriate signal level. Unused active low AGTL+ inputs may be left as no connects if AGTL+ termination is provided on the processor silicon. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs can be left unconnected.

TAP signal termination requirements are also discussed in *ITP700 Debug Port Design Guide.*

Note: The TEST1 and TEST2 pins have unique signal termination requirements. It is mandatory that the TEST2 pin have a 51 Ω +/-5% pull down resistor to Vss. Please refer to Table 12 for details.

3.7 FSB Frequency Select Signals (BSEL[2:0])

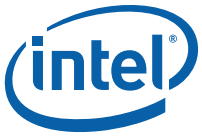
The BSEL[2:0] signals are used to select the frequency of the processor input clock (BCLK[1:0]). These signals should be connected to the clock chip on the platform. The BSEL encoding for BCLK[1:0] is shown in Table 4.

Table 4. BSEL[2:0] Encoding for BCLK Frequency

BSEL[2]	BSEL[1]	BSEL[0]	BCLK frequency
L	L	L	RESERVED
L	L	H	RESERVED
L	H	H	166 MHz
L	H	L	RESERVED

3.8 FSB Signal Groups

In order to simplify the following discussion, the FSB signals have been combined into groups by buffer type. AGTL+ input signals have differential input buffers, which use GTLREF as a reference level. In this document, the term "AGTL+ Input" refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, "AGTL+ Output" refers to the AGTL+ output group as well as the AGTL+ I/O group when driving.



With the implementation of a source synchronous data bus comes the need to specify two sets of timing parameters. One set is for common clock signals which are dependant upon the rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.) and the second set is for the source synchronous signals which are relative to their respective strobe lines (data and address) as well as the rising edge of BCLK0. Asychronous signals are still present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle. Table 5 identifies which signals are common clock, source synchronous, and asynchronous.

Table 5. FSB Pin Groups

Signal Group	Type	Signals[1]
AGTL+ Common Clock Input	Synchronous to BCLK[1:0]	BPRI#, DEFER#, PREQ#, RESET#, RS[2:0]#, RSP#, TRDY#, BR[1]#
AGTL+ Common Clock I/O	Synchronous to BCLK[1:0]	ADS#, AP[1:0]#,BINIT#, BNR#, BPM[3:0]#[3], BR[0]#, DBSY#, DP[3:0], DRDY#, HIT#, HITM#, LOCK#, MCERR#, PRDY#[3]
AGTL+ Source Synchronous I/O	Synchronous to assoc. strobe	<table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>REQ[4:0]#, A[16:3]#</td><td>ADSTB[0]#</td></tr><tr><td>A[35:17]#</td><td>ADSTB[1]#</td></tr><tr><td>D[15:0]#, DINV0#</td><td>DSTBP0#, DSTBN0#</td></tr><tr><td>D[31:16]#, DINV1#</td><td>DSTBP1#, DSTBN1#</td></tr><tr><td>D[47:32]#, DINV2#</td><td>DSTBP2#, DSTBN2#</td></tr><tr><td>D[63:48]#, DINV3#</td><td>DSTBP3#, DSTBN3#</td></tr></table>
AGTL+ Strobes	Synchronous to BCLK[1:0]	ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#
CMOS Input	Asynchronous	A20M#, FORCEPR#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, SLP#, STPCLK#
Open Drain Output	Asynchronous	FERR#, IERR#, THERMTRIP#, PROCHOT#
CMOS Output	Asynchronous	VID[5:0], BSEL[2:0]
CMOS Input	Synchronous to TCK	TCK, TDI, TMS, TRST#
Open Drain Output	Synchronous to TCK	TDO
FSB Clock	Clock	BCLK[1:0]
Power/Other		COMP[3:0], DBR#[2], GTLREF, RSVD, TEST2, TEST1, THERMDA, THERMDC, ODTEN, V_{CC}, V_{CCA}, V_{CCP}, V_{CC_SENSE}, V_{SS}, V_{SS_SENSE}

Notes:
1. Refer to Chapter 4.0 for signal descriptions and termination requirements.
2. In processor systems where there is no debug port implemented on the system board, these signals are used to support a debug port interposer. In systems with the debug port implemented on the system board, these signals are no connects.
3. BPM[2:1]# and PRDY# are AGTL+ output only signals.

3.9 CMOS Signals

CMOS input signals are shown in Table 5. Legacy output FERR#, IERR# and other non-AGTL+ signals (THERMTRIP# and PROCHOT#) utilize Open Drain output buffers. These signals do not have setup or hold time specifications in relation to BCLK[1:0]. However,

all of the CMOS signals are required to be asserted for at least three BCLKs in order for the processor to recognize them. See Section 3.12 for the DC specifications for the CMOS signal groups.

3.10 Test Access Port (TAP) Connection

Please refer to *ITP700 Debug Port Design Guide* for detailed information on TAP signal connections.

3.11 Maximum Ratings

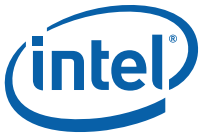
Table 6 lists the processor's maximum environmental stress ratings. The processor should not receive a clock while subjected to these conditions. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the processor contains protective circuitry to resist damage from Electro-Static Discharge (ESD), one should always take precautions to avoid high static voltages or electric fields.

Table 6. Processor DC Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
$T_{STORAGE}$	Processor storage temperature	-40	85	°C	2
V_{CC}	Any processor supply voltage with respect to V_{SS}	-0.3	1.6	V	1
$V_{inAGTL+}$	AGTL+ buffer DC input voltage with respect to V_{SS}	-0.1	1.6	V	1, 2
$V_{inAsynch\_CMOS}$	CMOS buffer DC input voltage with respect to V_{SS}	-0.1	1.6	V	1, 2

Notes:

1. For functional operation, all processor electrical, signal quality, mechanical and thermal specifications must be satisfied.
2. Overshoot and undershoot voltage guidelines for input, output, and I/O signals are outlined in Section 4.0. Excessive overshoot or undershoot on any signal will likely result in permanent damage to the processor.
3. Storage temperature is applicable to storage conditions only. In this scenario, the processor must not receive a clock, and no pins can be connected to a voltage bias. Storage within these limits will not affect the long term reliability of the device. For functional operation, please refer to the processor case temperature specifications.



3.12 Processor DC Specifications

Note: The processor DC specifications in this section are defined at the processor core (pads) unless noted otherwise.

See Table 5 for the pin signal definitions and signal pin assignments. Most of the signals on the FSB are in the AGTL+ signal group. The DC specifications for these signals are listed in Table 9. DC specifications for the CMOS group are listed in Table 10.

Table 7 through Table 11 list the DC specifications for the processor and are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. The Highest Frequency Mode (HFM) and Lowest Frequency Mode (LFM) refer to the highest and lowest core operating frequencies supported on the processor. Active mode load line specifications apply in all states. $V_{CC,BOOT}$ is the default voltage driven by the voltage regulator at power up in order to set the VID values. Unless specified otherwise, all specifications for the processor are at Tjunction = 100°C. Care should be taken to read all notes associated with each parameter.

Table 7. Dual-Core Intel® Xeon® Processor LV Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{CCHFM}	V_{CC} at Highest Frequency Mode (HFM)	1.1125		1.275	V	1, 2
V_{CCLFM}	Vcc at Lowest Frequency Mode (LFM)	0.825		1.1	V	1, 2
$V_{CC,BOOT}$	Default V_{CC} Voltage for initial power up		1.1		V	2, 8
V_{CCP}	AGTL+ Termination Voltage	0.997	1.05	1.102	V	2
V_{CCA}	PLL supply voltage	1.425	1.5	1.575	V	2
I_{CCDES}	I_{CC} for Dual-Core Intel® Xeon® Processor LV Recommended Design Target			36	A	5
I_{CC}	I_{CC} for Dual-Core Intel® Xeon® Processor LV 2.00 GHz and HFM Vcc 1.66 GHz and HFM Vcc 1.00 GHz and LFM Vcc			 36 36 22	A	3,10
I_{AH}, I_{SGNT}	I_{CC} Auto-Halt & Stop-Grant LFM HFM			 15.2 23.8	A	3,4
I_{SLP}	I_{SLP} LFM HFM			 15.1 23.6	A	3,4
$dI_{CC/DT}$	V_{CC} power supply current slew rate			600	A/us	6, 7
I_{CCA}	I_{CC} for V_{CCA} supply			120	mA	
I_{CCP}	I_{CC} for V_{CCP} supply before $V_{CC\ STABLE}$ I_{CC} for V_{CCP} supply after $V_{CC\ STABLE}$			6.0 2.5	A	9

Notes:

1. These are VID values. Individual processor VID values may be calibrated during manufacturing such that two devices at the same speed may have different VID settings. Actual voltage supplied to the processor should be as specified in the load lines in Figure 3. Adherence to load line specifications is required to ensure reliable processor operation. Note that this differs from the VID employed by the processor during a power management event (Thermal Monitor 2, Enhanced Intel SpeedStep® Technology, or Extended Halt State).
2. The voltage specifications are assumed to be measured across $V_{CCSENSE}$ and $V_{SSSENSE}$ pins at socket with a 100 MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1-Mohm minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
3. Specified at 100 C T_J.
4. Specified at the VID voltage.
5. The I_{CCDES}(max) specification comprehends only Standard Voltage processor HFM frequencies. Platforms should be designed to this specification.
6. Based on simulations and averaged over the duration of any change in current. Specified by design/ characterization at nominal V_{CC}. Not 100% tested.
7. Measured at the bulk capacitors on the motherboard.
8. V_{CC}, boot tolerance is shown in Figure 3.
9. I_{CCP} specification refers to a each processor package on the front side bus.
10. Specified at the nominal voltage based on the loadline slope.

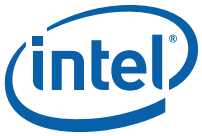


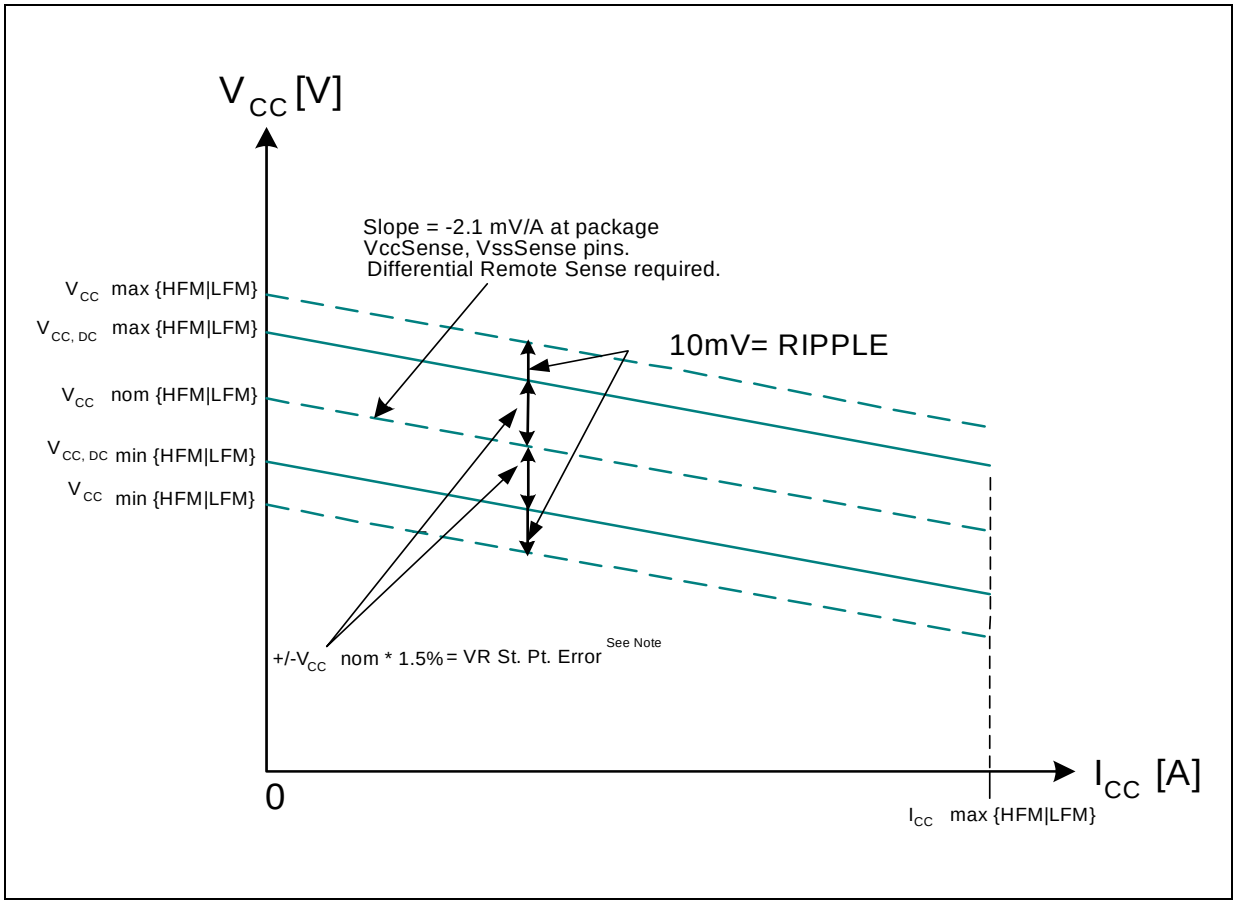
Table 8. Dual-Core Intel® Xeon®Processor ULV Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{CCHFM}	Vcc at Highest Frequency Mode (HFM)	1.0		1.2125	V	1, 2
V_{CCLFM}	Vcc at Lowest Frequency Mode (LFM)	0.825		1.1	V	1, 2
$V_{CC,BOOT}$	Default V_{CC} Voltage for initial power up		1.1		V	2, 8
V_{CCP}	AGTL+ Termination Voltage	0.997	1.05	1.102	V	2
V_{CCA}	PLL supply voltage	1.425	1.5	1.575	V	2
I_{CCDES}	I_{CC} for Dual-Core Intel® Xeon®Processor ULV Recommended Design Target			19	A	5
I_{CC}	I_{CC} for Dual-Core Intel® Xeon®Processor ULV 1.66 GHz and HFM Vcc >1.66 GHz and HFM Vcc 1GHz and LFM Vcc			 19 19 15.5	A	3,10
$I_{AH,}$ I_{SGNT}	I_{CC} Auto-Halt & Stop-Grant LFM HFM			 12.5 13.5	A	3,4
I_{SLP}	$I_{CC\ SLEEP}$ LFM HFM			 12.4 13.3	A	3,4
$dI_{CC/DT}$	V_{CC} power supply current slew rate			600	A/us	6, 7
I_{CCA}	I_{CC} for V_{CCA} supply			120	mA	
I_{CCP}	I_{CC} for V_{CCP} supply before $V_{CC\ STABLE}$ I_{CC} for V_{CCP} supply after $V_{CC\ STABLE}$			6.0 2.5	A	9

Notes:

1. These are VID values. Individual processor VID values may be calibrated during manufacturing such that two devices at the same speed may have different VID settings. Actual voltage supplied to the processor should be as specified in the load lines in Figure 3. Adherence to load line specifications is required to ensure reliable processor operation. Note that this differs from the VID employed by the processor during a power management event (Thermal Monitor 2, Enhanced Intel SpeedStep® Technology, or Extended Halt State).
2. The voltage specifications are assumed to be measured across VCCSENSE and VSSSENSE pins at socket with a 100 MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1-Mohm minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
3. Specified at 100 C TJ.
4. Specified at the VID voltage.
5. The ICCDES (max) specification comprehends only processor HFM frequencies. Platforms should be designed to this specification.
6. Based on simulations and averaged over the duration of any change in current. Specified by design/characterization at nominal VCC. Not 100% tested.
7. Measured at the bulk capacitors on the motherboard.
8. VCC, boot tolerance is shown in Figure 3.
9. Iccp specification refers to a each processor package on the front side bus.
10. Specified at the nominal voltage based on the loadline slope.

Figure 3. Processor Active V_{CC} and I_{CC} Load Line



Note: Vcc > 0.8250V (VID 111111)

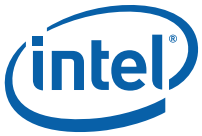


Table 9. AGTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes [1]
V_{CCP}	I/O Voltage	0.997	1.05	1.102	V	
GTLREF	Reference Voltage	2/3 V_{CCP} - 2%	2/3 V_{CCP}	2/3 V_{CCP} + 2%	V	6
V_{IH}	Input High Voltage	GTLREF+0.1	V_{CCP}	V_{CCP}+0.1	V	3,6
V_{IL}	Input Low Voltage	-0.1	0	GTLREF-0.1	V	2,4
V_{OH}	Output High Voltage	V_{CCP} - 0.1		V_{CCP}		6
R_{TT}	Termination Resistance	45	50	55	Ω	7,10
R_{ON}	Buffer On Resistance	20.0	22.5	25.0	Ω	5
I_{LI}	Input Leakage Current			± 100	µA	8
Cpad	Pad Capacitance	1.80	2.30	2.75	pF	9

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that is interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that is interpreted as a logical high value.
4. V_{IH} and V_{OH} may experience excursions above V_{CCP}. However, input signal drivers must comply with the signal quality specifications.
5. This is the pull down driver resistance. Refer to processor I/O Buffer Models for I/V characteristics. Measured at 0.31*V_{CCP}. R_{ON} (min) = 0.40*R_{TT}, R_{ON} (typ) = 0.45*R_{TT}, R_{ON} (max) = 0.50*R_{TT}.
6. GTLREF should be generated from V_{CCP} with a 1% tolerance resistor divider. The V_{CCP} referred to in these specifications is the instantaneous V_{CCP}.
7. R_{TT} is the on-die termination resistance measured at V_{OL} of the AGTL+ output driver. Measured at 0.33*V_{CCP}. R_{TT} is connected to V_{CCP} on die. Refer to processor I/O buffer models for I/V characteristics.
8. Specified with on die R_{TT} and R_{ON} are turned off.
9. Cpad includes die capacitance only. No package parasitics are included.
10. R_{TT} for PREQ# is between 1.5kΩ and 6.0kΩ

Table 10. CMOS Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{CCP}	I/O Voltage	0.997	1.05	1.102	V	
V_{IL}	Input Low Voltage CMOS	-0.1	0	0.33	V	2, 3
V_{IH}	Input High Voltage	0.7	1.05	1.20	V	2
V_{OL}	Output Low Voltage	-0.1	0	0.11	V	2
V_{OH}	Output High Voltage	0.9	V_{CCP}	1.2	V	2
I_{OL}	Output Low Current	1.3		4.1	mA	4
I_{OH}	Output High Current	1.3		4.1	mA	5

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The V_{CCP} referred to in these specifications refers to instantaneous V_{CCP}.
3. Refer to the processor I/O Buffer Models for I/V characteristics.
4. Measured at 0.1*V_{CCP}.
5. Measured at 0.9*V_{CCP}.
6. For Vin between 0V and V_{CCP}. Measured when the driver is tristated.
7. Cpad1 includes die capacitance only for PWRGOOD. No package parasitics are included.
8. Cpad2 includes die capacitance for all other CMOS input signals. No package parasitics are included.

Table 10. CMOS Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
I_{LI}	Leakage Current			± 100	µA	6
Cpad1	Pad Capacitance	1.8	2.3	2.75	pF	7
Cpad2	Pad Capacitance for CMOS Input	0.95	1.2	1.45	pF	8

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The V_{CCP} referred to in these specifications refers to instantaneous V_{CCP}.
3. Refer to the processor I/O Buffer Models for I/V characteristics.
4. Measured at $0.1*V_{CCP}$.
5. Measured at $0.9*V_{CCP}$.
6. For Vin between 0V and V_{CCP}. Measured when the driver is tristated.
7. Cpad1 includes die capacitance only for PWRGOOD. No package parasitics are included.
8. Cpad2 includes die capacitance for all other CMOS input signals. No package parasitics are included.

Table 11. Open Drain Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{OH}	Output High Voltage	1.0	1.05	1.10	V	3
V_{OL}	Output Low Voltage	0		0.20	V	
I_{OL}	Output Low Current	11.4		50	mA	2
I_{LEAK}	Leakage Current			± 200	µA	4
Cpad	Pad Capacitance	1.8	2.3	2.75	pF	5

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Measured at 0.2 V
3. V_{OH} is determined by value of the external pull-up resistor to V_{CCP}.
4. For Vin between 0 V and V_{OH}.
5. Cpad includes die capacitance only. No package parasitics are included.

4.0 Package Mechanical Specifications and Pin Information

4.1 Package Mechanical Specifications

The Dual-Core Intel® Xeon® Processor LV and ULV is available in 478 pin Micro-FCPGA package.

4.1.1 Package Mechanical Drawings

Different views of the Micro-FCPGA package are shown in Figure 4, Figure 5, and Figure 6.

Figure 4. Micro-FCPGA Package Top and Bottom Views

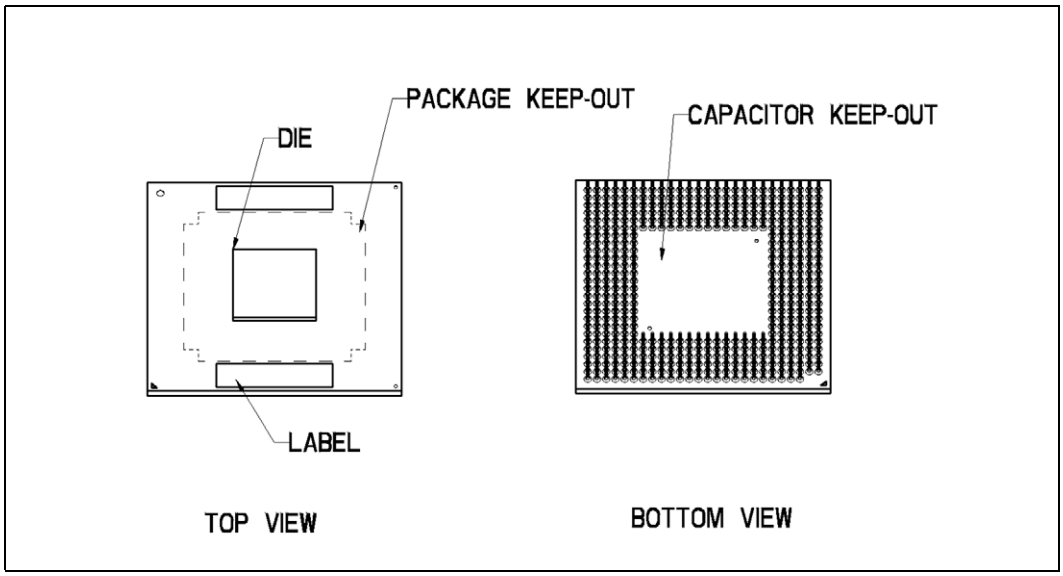
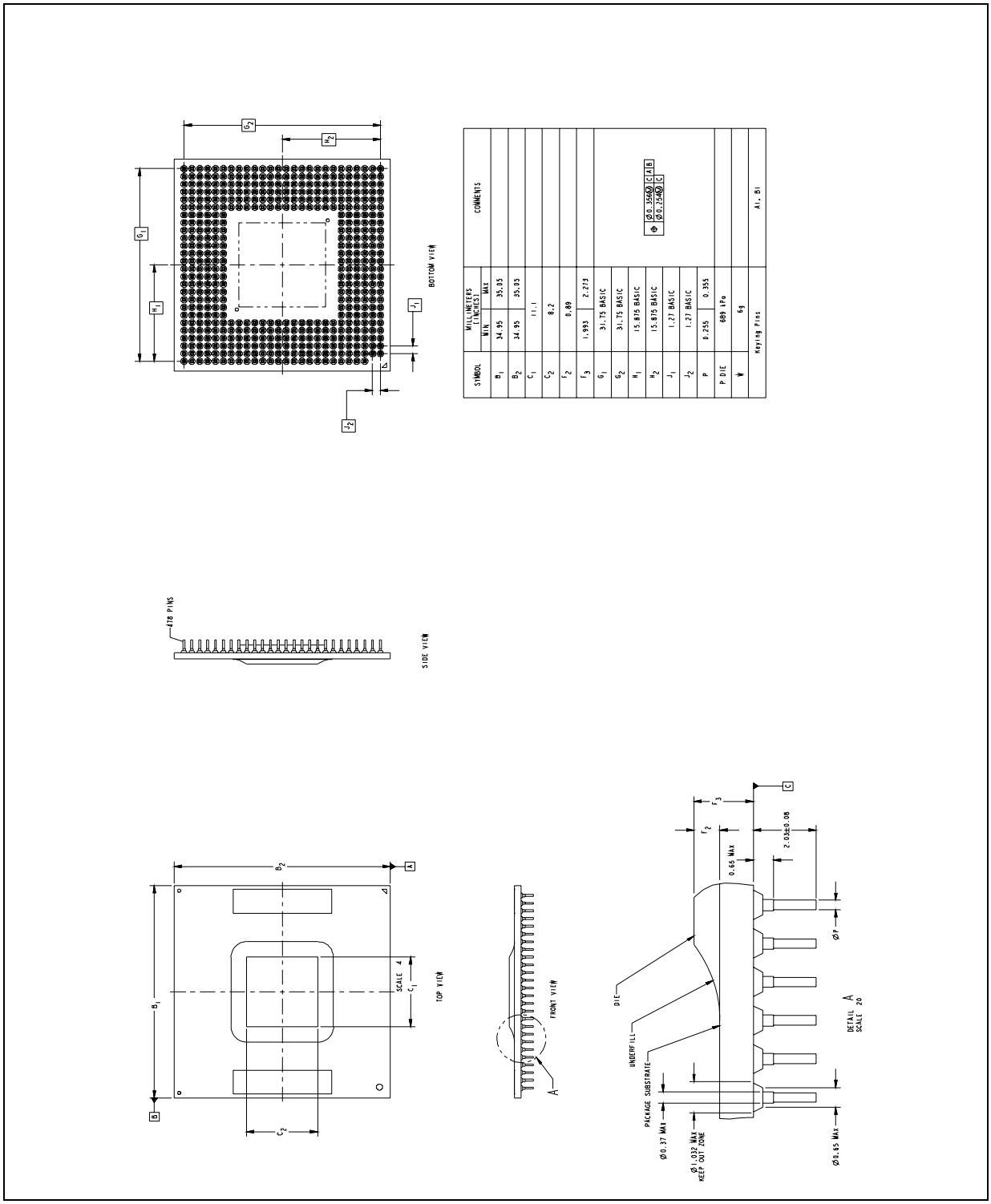


Figure 5. Micro-FCPGA Processor Package Drawing (Sheet 1)

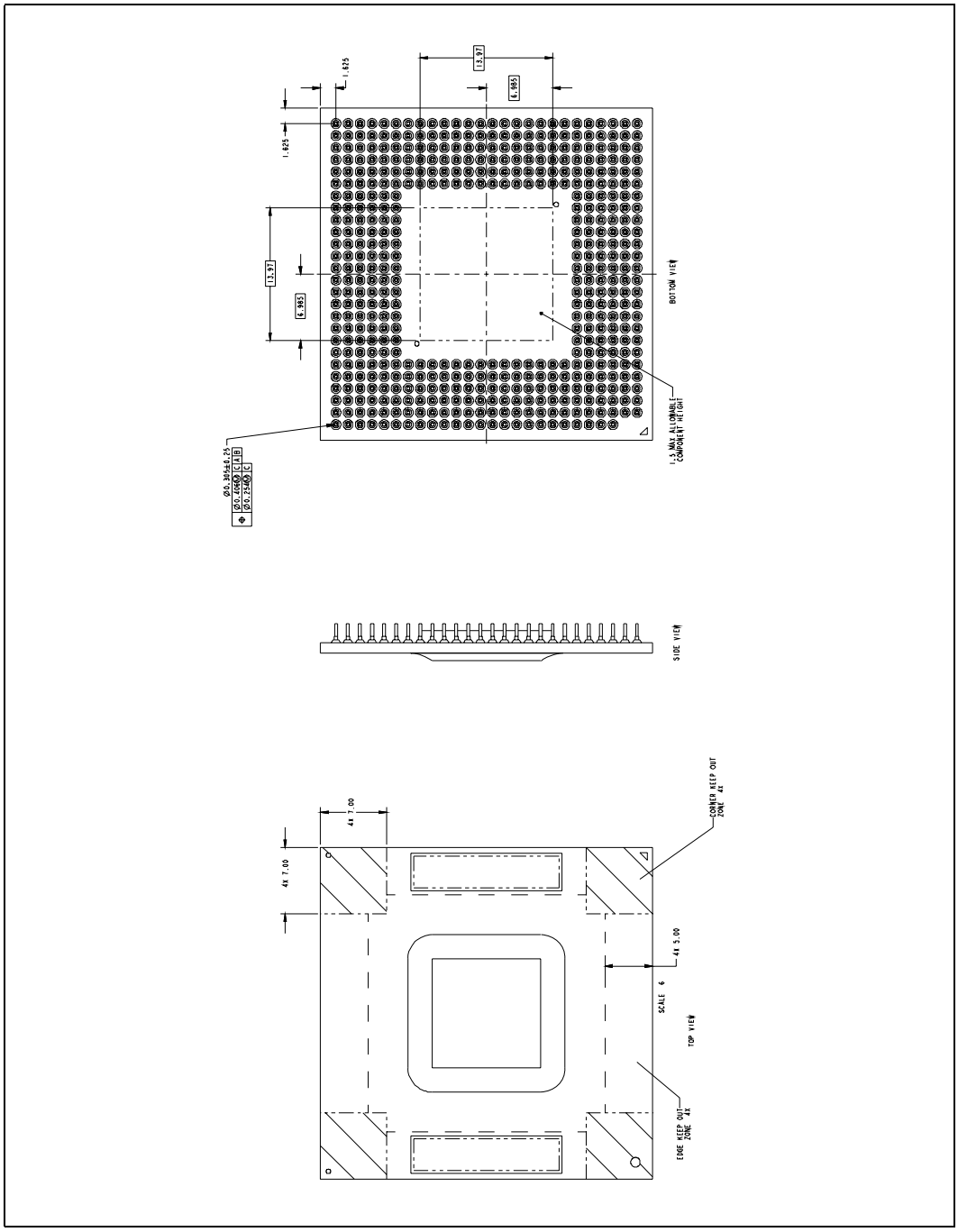


SYMBOL	MILLIMETERS / INCHES MIN	MAX	COMMENTS
B_1	34.95	35.05	
B_2	34.95	35.05	
C_1	11.1		
C_2	8.2		
F_2	0.89		
F_3	1.993	2.273	
G_1	31.75 BASIC		
G_2	31.75 BASIC		
H_1	15.875 BASIC		
H_2	15.875 BASIC		
J_1	1.27 BASIC		
J_2	1.27 BASIC		
P	0.255	0.355	
P DIE	689 lb_m		
W	68		keying pins

Ø0.356 M C A B
Ø0.254 M C

Note: All dimensions are in millimeters [inches]. Values shown for reference only.

Figure 6. Micro-FCPGA Processor Package Drawing (Sheet 2)



Note: All dimensions are in millimeters [inches]. Values shown for reference only.

4.1.2 Processor Component Keep-Out Zones

The processor may contain components on the substrate that define component keep-out zone requirements. A thermal and mechanical solution design must not intrude into the required keep-out zones. Decoupling capacitors are typically mounted in the keep-out areas. The location and quantity of the capacitors may change, but will remain within the component keep-in. See Figure 4, Figure 5, and Figure 6 for keep-out zones.

4.1.3 Package Loading Specifications

Maximum mechanical package loading specifications are given in Figure 6. These specifications are static compressive loading in the direction normal to the processor. This maximum load limit should not be exceeded during shipping conditions, standard use condition, or by thermal solution. In addition, there are additional load limitations against transient bend, shock, and tensile loading. These limitations are more platform specific, and should be obtained by contacting your field support. Moreover, the processor package substrate should not be used as a mechanical reference or load-bearing surface for thermal and mechanical solution.

4.1.4 Processor Mass Specifications

The typical mass of the processor is given in Figure 6. This mass includes all the components that are included in the package.

4.2 Processor Pin-Out and Pin List

Figure 7 shows the top view pinout of the processor. The alphabetical pin listing is shown in Table 13. The alphabetical signal listing is shown in Table 14.

Figure 7. The Coordinates of the Processor Pins as Viewed From the Top of the Package

	AF	AE	AD	AC	AB	AA	Y	W	V	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
1	VID[5]	SKTOCC#	VSS	A[35]#	A[34]#	VSS	A[29]#	A[30]#	VSS	A[14]#	A[10]#	VSS	COMP[2]	COMP[3]	A[8]#	VSS	A[5]#	A[4]#	VSS	A[3]#	RS[0]#	VSS	RSVD	RSVD		
2	VID[3]	VID[4]	A[31]#	VSS	A[27]#	A[21]#	VSS	A[28]#	A[25]#	VSS	A[13]#	A[12]#	VSS	RSVD	VSS	REQ[0]#	A[7]#	VSS	REQ[2]#	REQ[4]#	VSS	RS[1]#	RESET#	VSS	RSVD	FORCEPR#
3	VID[1]	VID[2]	A[32]#	A[33]#	VSS	A[26]#	A[20]#	VSS	A[23]#	A[24]#	VSS	A[16]#	A[9]#	VSS	RSVD	A[6]#	VSS	REQ[3]#	REQ[1]#	VSS	BNR#	HIT#	VSS	RSVD	RSVD	VSS
4	PREQ#	VID[0]	VSS	TDI	TDO	VSS	RSP#	AP[1]#	VSS	A[22]#	A[19]#	VSS	A[15]#	A[11]#	BR0#	VSS	MCERR#	HITM#	VSS	RS[2]#	LOCK#	VSS	STPCLK#	RSVD	LINT0	PWRGOOD
5	VSS	BPM[3]#	PRDY#	VSS	TMS	TCK	VSS	BINIT#	AP[0]#	VSS	A[18]#	RSVD	VSS	A[17]#	VSS	BR1#	BPRI#	VSS	TRDY#	DRDY#	VSS	SMI#	INIT#	VSS	FERR#	THERMTRIP#
6	BPM[0]#	VSS	BPM[1]#	BPM[2]#	VSS	TRST#	V_{CCP}	VSS	V_{CCP}	V_{CCP}	VSS	ADSTB[1]#	RSVD	VSS	ADSTB[0]#	ADS#	VSS	DEFER#	DBSY#	VSS	ODTEN	IGNNE#	VSS	A20M#	LINT1	VSS
7	VCC	VCC	VCC	VCC	VSSSENSE	VCCSENSE															VCC	VCC	RSVD	SLP#	VCC	VCC
8	VSS	VSS	VSS	VSS	VSS	VSS															VSS	VSS	VSS	VSS	VSS	VSS
9	VCC	VCC	VCC	VCC	VCC	VCC															VCC	VCC	VCC	VCC	VCC	VCC
10	VCC	VCC	VCC	VCC	VCC	VCC															VCC	VCC	VCC	VCC	VCC	VCC
11	VSS	VSS	VSS	VSS	VSS	VSS															VSS	VSS	VSS	VSS	VSS	VSS
12	VCC	VCC	VCC	VCC	VCC	VCC															VCC	VCC	VCC	VCC	VCC	VCC
13	VSS	VCC	VSS	VCC	VSS	VCC															VSS	VCC	VSS	VCC	VSS	VCC
14	VCC	VSS	VCC	VSS	VCC	VSS															VCC	VSS	VCC	VSS	VCC	VSS
15	VCC	VCC	VCC	VCC	VCC	VCC															VCC	VCC	VCC	VCC	VCC	VCC
16	VSS	VSS	VSS	VSS	VSS	VSS															VSS	VSS	VSS	VSS	VSS	VSS
17	VCC	VCC	VCC	VCC	VCC	VCC															VCC	VCC	VCC	VCC	VCC	VCC
18	VCC	VCC	VCC	VCC	VCC	VCC															VCC	VCC	VCC	VCC	VCC	VCC
19	VSS	VSS	VSS	VSS	VSS	VSS															VSS	VSS	VSS	VSS	VSS	VSS
20	VCC	VCC	VCC	VCC	V_{CCP}	V_{CCP}															VCC	VCC	BSEL[1]	BSEL[0]	VCC	VCC
21	VSS	V_{CCP}	V_{CCP}	VSS	V_{CCP}	D[62]#	VSS	DSTBP[3]#	DSTBN[3]#	VSS	DSTBP[2]#	DSTBN[2]#	VSS	DSTBP[1]#	DSTBN[1]#	VSS	DSTBP[0]#	DSTBN[0]#	VSS	D[5]#	D[2]#	VSS	D[0]#	IERR#	VSS	BSEL[2]
22	V_{CCP}	V_{CCP}	VSS	V_{CCP}	D[61]#	VSS	D[54]#	D[53]#	VSS	D[48]#	D[49]#	VSS	D[33]#	VSS	D[24]#	D[15]#	VSS	D[11]#	D[10]#	VSS	D[6]#	D[3]#	VSS	D[1]#	THRMDA	THRMDC
23	V_{CCP}	VSS	D[63]#	V_{CCP}	VSS	DINV[3]#	D[55]#	VSS	D[51]#	D[52]#	VSS	D[37]#	D[32]#	D[31]#	VSS	D[14]#	D[12]#	VSS	D[13]#	D[9]#	VSS	D[8]#	D[7]#	VSS	TEST2	VCCA
24	VSS	D[60]#	D[59]#	VSS	D[56]#	D[47]#	VSS	D[43]#	D[41]#	VSS	D[50]#	RSVD	VSS	D[36]#	DP[3]#	VSS	D[25]#	D[26]#	VSS	D[23]#	D[20]#	VSS	D[17]#	DINV[0]#	VSS	TEST1
25	V_{CCP}	RSVD	VSS	D[57]#	D[46]#	VSS	D[45]#	D[40]#	VSS	D[38]#	D[39]#	VSS	DP[2]#	VSS	DP[1]#	D[30]#	VSS	D[29]#	DINV[1]#	VSS	D[21]#	D[18]#	VSS	D[4]#	PROCHOT#	VSS
26	V_{CCP}	VSS	GTLREF	D[58]#	VSS	D[44]#	D[42]#	VSS	DINV[2]#	D[35]#	VSS	COMP[1]	COMP[0]	D[34]#	VSS	DP[0]#	D[28]#	VSS	D[27]#	D[22]#	VSS	D[19]#	D[16]#	VSS	BCLK[0]	BCLK[1]

4.2.1 Alphabetical Signals Reference

Table 12. Signal Description (Sheet 1 of 8)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>A[35:3]#</td><td>Input/ Output</td><td>A[35:3]# (Address) define a 2^{36}-byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of both agents on the Dual-Core Intel® Xeon® Processor LV FSB. A[35:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. Address signals are used as straps which are sampled before RESET# is deasserted.</td></tr>
<tr><td>A20M#</td><td>Input</td><td>If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode.
A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.</td></tr>
<tr><td>ADS#</td><td>Input/ Output</td><td>ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.</td></tr>
<tr><td>ADSTB[1:0]#</td><td>Input/ Output</td><td>Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below.
<table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>REQ[4:0]#, A[16:3]#</td><td>ADSTB[0]#</td></tr><tr><td>A[35:17]#</td><td>ADSTB[1]#</td></tr></table></td></tr>
<tr><td>AP[1:0]#</td><td>Input/ Output</td><td>AP[1:0]# (Address Parity) are driven by the request initiator along with ADS#, A[35:3]#, and the transaction type on the REQ[4:0]# pins. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should connect the appropriate pins of all front side bus agents. The following table defines the coverage model of these signals.
<table><tr><th>Request Signals</th><th>Subphase 1</th><th>Subphase 2</th></tr><tr><td>A[35:24]#</td><td>AP0#</td><td>AP1#</td></tr><tr><td>A[23:3]#</td><td>AP1#</td><td>AP0#</td></tr><tr><td>REQ[4:0]#</td><td>AP1#</td><td>AP0#</td></tr></table></td></tr>
<tr><td>BCLK[1:0]</td><td>Input</td><td>The differential pair BCLK (Bus Clock) determines the FSB frequency. All FSB agents must receive these signals to drive their outputs and latch their inputs.
All external timing parameters are specified with respect to the rising edge of BCLK0 crossing V_{CROSS}.</td></tr>
</table>

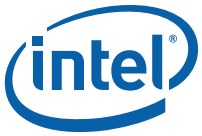


Table 12. Signal Description (Sheet 2 of 8)

Name	Type	Description
BINIT#	Input/ Output	BINIT# (Bus Initialization) may be observed and driven by all processor front side bus agents and if used, must connect the appropriate pins of all such agents. If the BINIT# driver is enabled during power on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future information. If BINIT# observation is enabled during power-on configuration and BINIT# is sampled asserted, symmetric agents reset their bus LOCK# activity and bus request arbitration state machines. The bus agents **do not** reset their IOQ and transaction tracking state machines upon observation of BINIT# assertion. Once the BINIT# assertion has been observed, the bus agents re-arbitrate for the front side bus and attempt completion of their bus queue and IOQ entries. If BINIT# observation is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the error handling architecture of the system.
BNR#	Input/ Output	BNR# (Block Next Request) is used to assert a bus stall by any bus agent it is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.
BPM[2:1]# BPM[3,0]#	Output Input/ Output	BPM[3:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[3:0]# should connect the appropriate pins of all Dual-Core Intel® Xeon® Processor LV FSB agents.This includes debug or performance monitoring tools. Please refer to the platform design guide for more detailed information.
BPRI#	Input	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the FSB. It must connect the appropriate pins of all FSB agents. Observing BPRI# active (as asserted by the priority agent) causes the other agent to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.
BR0# BR1#	Input/ Output Input	The BR0# and BR1#(Bus Request) pins drive the BREQ[1:0]# signals in the system. The BREQ[1:0]# signals are interconnected in a rotating manner to individual processor pins. The following table gives the rotating interconnect between the processor and bus signals. **BR0# (I/O) and BR1# Signals Rotating Interconnect** Bus Signals / Agent 0 Pin / Agent 1 Pin BREQ0# / BR0# / BR1# BREQ1# / BR1# / BR0# During power-on configuration, the central agent must assert the BR0# bus signal. All symmetric agents sample their BR[1:0]# pins on the active-to-inactive transition of RESET#. The pin which the agent samples asserted determines it's agent ID.
BSEL[2:0]	Output	BSEL[2:0] (Bus Select) are used to select the processor input clock frequency. Table 3 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset and clock synthesizer. All agents must operate at the same frequency. The Dual-Core Intel® Xeon® Processor LV operates at 667 MHz system bus frequency (166 MHz BCLK[2:0] frequency respectively).
COMP[3:0]	Analog	COMP[3:0] must be terminated on the system board using precision (1% tolerance) resistors. Refer to the platform design guide for more details on implementation.

Table 12. Signal Description (Sheet 3 of 8)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>D[63:0]#</td><td>Input/ Output</td><td>D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the FSB agents, and must connect the appropriate pins on both agents. The data driver asserts DRDY# to indicate a valid data transfer.
D[63:0]# are quad-pumped signals and is thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DINV#.
Quad-Pumped Signal Groups<table><tr><th>Data Group</th><th>DSTBN# / DSTBP#</th><th>DINV#</th></tr><tr><td>D[15:0]#</td><td>0</td><td>0</td></tr><tr><td>D[31:16]#</td><td>1</td><td>1</td></tr><tr><td>D[47:32]#</td><td>2</td><td>2</td></tr><tr><td>D[63:48]#</td><td>3</td><td>3</td></tr></table>Furthermore, the DINV# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DINV# signal. When the DINV# signal is active, the corresponding data group is inverted and therefore sampled active high.</td></tr>
<tr><td>DBSY#</td><td>Input/ Output</td><td>DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the FSB to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on both FSB agents.</td></tr>
<tr><td>DEFER#</td><td>Input</td><td>DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of all FSB agents.</td></tr>
<tr><td>DP[3:0]#</td><td>Input/ Output</td><td>DP[3:0]# (Data Parity) provide parity protection for the D[63:0]# signals. They are driven by the agent responsible for driving D[63:0]#, and must connect the appropriate pins of all processor front side bus agents.</td></tr>
<tr><td>DINV[3:0]#</td><td>Input/ Output</td><td>DINV[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DINV[3:0]# signals are activated when the data on the data bus is inverted. The bus agent inverts the data bus signals if more than half the bits, within the covered group, would change level in the next cycle.
DINV[3:0]# Assignment To Data Bus<table><tr><th>Bus Signal</th><th>Data Bus Signals</th></tr><tr><td>DINV[3]#</td><td>D[63:48]#</td></tr><tr><td>DINV[2]#</td><td>D[47:32]#</td></tr><tr><td>DINV[1]#</td><td>D[31:16]#</td></tr><tr><td>DINV[0]#</td><td>D[15:0]#</td></tr></table></td></tr>
<tr><td>DRDY#</td><td>Input/ Output</td><td>DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of both FSB agents.</td></tr>
</table>

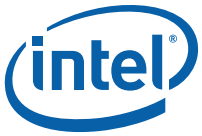


Table 12. Signal Description (Sheet 4 of 8)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>DSTBN[3:0]#</td><td>Input/ Output</td><td>Data strobe used to latch in D[63:0]#.
<table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>D[15:0]#, DINV[0]#</td><td>DSTBN[0]#</td></tr><tr><td>D[31:16]#, DINV[1]#</td><td>DSTBN[1]#</td></tr><tr><td>D[47:32]#, DINV[2]#</td><td>DSTBN[2]#</td></tr><tr><td>D[63:48]#, DINV[3]#</td><td>DSTBN[3]#</td></tr></table></td></tr>
<tr><td>DSTBP[3:0]#</td><td>Input/ Output</td><td>Data strobe used to latch in D[63:0]#.
<table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>D[15:0]#, DINV[0]#</td><td>DSTBP[0]#</td></tr><tr><td>D[31:16]#, DINV[1]#</td><td>DSTBP[1]#</td></tr><tr><td>D[47:32]#, DINV[2]#</td><td>DSTBP[2]#</td></tr><tr><td>D[63:48]#, DINV[3]#</td><td>DSTBP[3]#</td></tr></table></td></tr>
<tr><td>FERR#/PBE#</td><td>Output</td><td>FERR# (Floating-point Error) PBE# (Pending Break Event) is a multiplexed signal and its meaning is qualified with STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating point error when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it remains asserted until STPCLK# is deasserted. Assertion of PREQ# when STPCLK# is active also causes an FERR# break event.
For additional information on the pending break event functionality, including identification of support of the feature and enable/disable information, refer to Volume 3 of the *Intel® Architecture Software Developer's Manual* and the *Intel® Processor Identification and CPUID Instruction* application note.
For termination requirements please refer to the platform design guide.</td></tr>
<tr><td>FORCEPR#</td><td>Input</td><td>The FORCEPR# input can be used by the platform to force the Dual-Core Intel® Xeon® Processor LV system bus to activate the Thermal Control Circuit (TCC). The TCC remains active until the system deasserts FORCEPR#.</td></tr>
<tr><td>GTLREF</td><td>Input</td><td>GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 V_{CCP}. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1. Please refer to the platform design guide for details on GTLREF implementation.</td></tr>
<tr><td>HIT#

HITM#</td><td>Input/ Output

Input/ Output</td><td>HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Either FSB agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.</td></tr>
<tr><td>IERR#</td><td>Output</td><td>IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the FSB. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor keeps IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.
For termination requirements please refer to the platform design guide.</td></tr>
</table>

Table 12. Signal Description (Sheet 5 of 8)

Name	Type	Description
IGNNE#	Input	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute non-control floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
INIT#	Input	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output Write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction. INIT# must connect the appropriate pins of both FSB agents. For termination requirements please refer to the platform design guide.
LINT[1:0]	Input	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Intel® Pentium® processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	Input/ Output	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of both FSB agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the FSB, it waits until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the FSB throughout the bus locked operation and ensure the atomicity of lock.
MCERR#	Input/ Output	MCERR# (Machine Check Error) is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all processor front side bus agents. MCERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options: • Enabled or disabled. • Asserted, if configured, for internal errors along with IERR#. • Asserted, if configured, by the request initiator of a bus transaction after it observes an error. • Asserted by any bus agent when it observes an error in a bus transaction. For more details regarding machine check architecture, refer to the *IA-32 Software Developer's Manual, Volume 3: System Programming Guide*. Since multiple agents may drive this signal at the same time, MCERR# is a wire-OR signal which must connect the appropriate pins of all processor front side bus agents. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, MCERR# is activated on specific clock edges and sampled on specific clock edges.
ODTEN	Input	ODTEN (On-die termination enable) should be connected to VCC to enable on-die termination for end bus agents. For middle bus agents, pull this signal down via a resistor to ground to disable on-die termination. Whenever ODTEN is high, on-die termination is active, regardless of other states of the bus.
PRDY#	Output	Probe Ready signal used by debug tools to determine processor debug readiness. Please refer to the platform design guide for more implementation details.
PREQ#	Input	Probe Request signal used by debug tools to request debug operation of the processor. Please refer to the platform design guide for more implementation details.

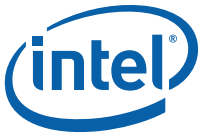


Table 12. Signal Description (Sheet 6 of 8)

Name	Type	Description
PROCHOT#	Output	PROCHOT# (Processor Hot) goes active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, For termination requirements please refer to the platform design guide. This signal may require voltage translation on the motherboard. Please refer to the platform design guide for more details.
PWRGOOD	Input	PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal remains low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation. For termination requirements please refer to the platform design guide.
REQ[4:0]#	Input/ Output	REQ[4:0]# (Request Command) must connect the appropriate pins of both FSB agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[0]#.
RESET#	Input	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least two milliseconds after V_{CC} and BCLK have reached their proper specifications. On observing active RESET#, both FSB agents deasserts their outputs within two clocks. All processor straps must be valid within the specified setup time before RESET# is deasserted. Please refer to the platform design guide for termination requirements and implementation details. There is a 55 ohm (nominal) on die pullup resistor on this signal.
RS[2:0]#	Input	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all FSB agents.
RSP#	Input	RSP# (Response Parity) is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect to the appropriate pins of all processor front side bus agents. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. While RS[2:0]# = 000, RSP# is also high, since this indicates it is not being driven by any agent guaranteeing correct parity.
RSVD	Reserved/ No Connect	These pins are RESERVED and must be left unconnected on the board. However, it is recommended that routing channels to these pins on the board be kept open for possible future use. Please refer to the platform design guide for more details.
SKTOCC#	Output	SKTOCC# (Socket occupied) is pulled to ground by the processor to indicate that the processor is present.
SLP#	Input	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state does not recognize snoops or interrupts. The processor recognizes only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units.

Table 12. Signal Description (Sheet 7 of 8)

Name	Type	Description
SMI#	Input	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor tristates its outputs.
STPCLK#	Input	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the FSB and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	Input	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port). Please refer to the platform design guide for termination requirements and implementation details.
TDI	Input	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support. Please refer to the platform design guide for termination requirements and implementation details.
TDO	Output	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support. Please refer to the platform design guide for termination requirements and implementation details.
TEST1	Input	TEST1 must have a stuffing option of separate pull down resistors to V_{SS}. Please refer to the platform design guide for more details.
TEST2	Input	TEST2 must have a 51Ω +/- 5% pull down resistor to V_{SS}. Please refer to the platform design guide for more details.
THERMDA	Other	Thermal Diode Anode.
THERMDC	Other	Thermal Diode Cathode.
THERMTRIP#	Output	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor stops all execution when the junction temperature exceeds approximately 125°C. This is signalled to the system by the THERMTRIP# (Thermal Trip) pin. For termination requirements please refer to the platform design guide.
TMS	Input	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools. Please refer to the platform design guide for termination requirements and implementation details.
TRDY#	Input	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of both FSB agents.
TRST#	Input	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. Please refer to the platform design guide for termination requirements and implementation details.
V_{CC}	Input	Processor core power supply.
V_{CCA}	Input	V_{CCA} provides isolated power for the internal processor core PLLs. Refer to the platform design guide for complete implementation details.
V_{CCP}	Input	Processor I/O Power Supply.

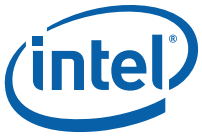


Table 12. Signal Description (Sheet 8 of 8)

Name	Type	Description
$V_{CCSENSE}$	Output	$V_{CCSENSE}$ is an isolated low impedance connection to processor core power (V_{CC}). It can be used to sense or measure power near the silicon with little noise. Please refer to the platform design guide for termination recommendations and more details.
VID[5:0]	Output	VID[5:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (V_{CC}). Unlike some previous generations of processors, these are CMOS signals driven by the Dual-Core Intel® Xeon® Processor LV. The voltage supply (V_{CCP}) for these pins must be valid before the VR can supply V_{CC} to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations. See Table 4 for definitions of these pins. The VR must supply the voltage that is requested by the pins, or disable itself.
$V_{SSSENSE}$	Output	$V_{SSSENSE}$ is an isolated low impedance connection to processor core V_{SS}. It can be used to sense or measure ground near the silicon with little noise. Please refer to the platform design guide for termination recommendations and more details.

Table 13. Alphabetical Signal Listing (Sheet 1 of 13)

Pin Name	Pin Number	Signal Buffer Type	Direction
A[10]#	T1	Source Sync	Input/Output
A[11]#	N4	Source Sync	Input/Output
A[12]#	R2	Source Sync	Input/Output
A[13]#	T2	Source Sync	Input/Output
A[14]#	U1	Source Sync	Input/Output
A[15]#	P4	Source Sync	Input/Output
A[16]#	R3	Source Sync	Input/Output
A[17]#	N5	Source Sync	Input/Output
A[18]#	T5	Source Sync	Input/Output
A[19]#	T4	Source Sync	Input/Output
A[20]#	Y3	Source Sync	Input/Output
A[21]#	AA2	Source Sync	Input/Output
A[22]#	U4	Source Sync	Input/Output
A[23]#	V3	Source Sync	Input/Output
A[24]#	U3	Source Sync	Input/Output
A[25]#	V2	Source Sync	Input/Output
A[26]#	AA3	Source Sync	Input/Output
A[27]#	AB2	Source Sync	Input/Output
A[28]#	W2	Source Sync	Input/Output
A[29]#	Y1	Source Sync	Input/Output
A[3]#	G1	Source Sync	Input/Output
A[30]#	W1	Source Sync	Input/Output
A[31]#	AD2	Source Sync	Input/Output
A[32]#	AD3	Source Sync	Input/Output
A[33]#	AC3	Source Sync	Input/Output
A[34]#	AB1	Source Sync	Input/Output

Table 13. Alphabetical Signal Listing (Sheet 2 of 13)

Pin Name	Pin Number	Signal Buffer Type	Direction
A[35]#	AC1	Source Sync	Input/Output
A[4]#	J1	Source Sync	Input/Output
A[5]#	K1	Source Sync	Input/Output
A[6]#	L3	Source Sync	Input/Output
A[7]#	K2	Source Sync	Input/Output
A[8]#	M1	Source Sync	Input/Output
A[9]#	P3	Source Sync	Input/Output
A20M#	C6	CMOS	Input
ADS#	L6	Common Clock	Input/Output
ADSTB#[0]	M6	Source Sync	Input/Output
ADSTB#[1]	R6	Source Sync	Input/Output
AP[0]#	V5	Common Clock	Input/Output
AP[1]#	W4	Common Clock	Input/Output
BCLK[0]	B26	Bus Clock	Input
BCLK[1]	A26	Bus Clock	Input
BINIT#	W5	Common Clock	Input/Output
BNR#	F3	Common Clock	Input/Output
BPM[0]#	AF6	Common Clock	Input/Output
BPM[1]#	AD6	Common Clock	Output
BPM[2]#	AC6	Common Clock	Output
BPM[3]#	AE5	Common Clock	Input/Output
BPRI#	K5	Common Clock	Input
BR0#	M4	Common Clock	Input/Output
BR1#	L5	Common Clock	Input
BSEL[0]	C20	CMOS	Output
BSEL[1]	D20	CMOS	Output
BSEL[2]	A21	CMOS	Output
COMP[0]	P26	Power/Other	Input/Output
COMP[1]	R26	Power/Other	Input/Output
COMP[2]	P1	Power/Other	Input/Output
COMP[3]	N1	Power/Other	Input/Output
D[0]#	D21	Source Sync	Input/Output
D[1]#	C22	Source Sync	Input/Output
D[10]#	H22	Source Sync	Input/Output
D[11]#	J22	Source Sync	Input/Output
D[12]#	K23	Source Sync	Input/Output
D[13]#	H23	Source Sync	Input/Output
D[14]#	L23	Source Sync	Input/Output
D[15]#	L22	Source Sync	Input/Output
D[16]#	D26	Source Sync	Input/Output

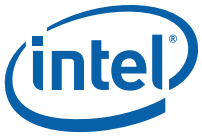


Table 13. Alphabetical Signal Listing (Sheet 3 of 13)

Pin Name	Pin Number	Signal Buffer Type	Direction
D[17]#	D24	Source Sync	Input/Output
D[18]#	E25	Source Sync	Input/Output
D[19]#	E26	Source Sync	Input/Output
D[2]#	F21	Source Sync	Input/Output
D[20]#	F24	Source Sync	Input/Output
D[21]#	F25	Source Sync	Input/Output
D[22]#	G26	Source Sync	Input/Output
D[23]#	G24	Source Sync	Input/Output
D[24]#	M22	Source Sync	Input/Output
D[25]#	K24	Source Sync	Input/Output
D[26]#	J24	Source Sync	Input/Output
D[27]#	H26	Source Sync	Input/Output
D[28]#	K26	Source Sync	Input/Output
D[29]#	J25	Source Sync	Input/Output
D[3]#	E22	Source Sync	Input/Output
D[30]#	L25	Source Sync	Input/Output
D[31]#	N23	Source Sync	Input/Output
D[32]#	P23	Source Sync	Input/Output
D[33]#	P22	Source Sync	Input/Output
D[34]#	N26	Source Sync	Input/Output
D[35]#	U26	Source Sync	Input/Output
D[36]#	N24	Source Sync	Input/Output
D[37]#	R23	Source Sync	Input/Output
D[38]#	U25	Source Sync	Input/Output
D[39]#	T25	Source Sync	Input/Output
D[4]#	C25	Source Sync	Input/Output
D[40]#	W25	Source Sync	Input/Output
D[41]#	V24	Source Sync	Input/Output
D[42]#	Y26	Source Sync	Input/Output
D[43]#	W24	Source Sync	Input/Output
D[44]#	AA26	Source Sync	Input/Output
D[45]#	Y25	Source Sync	Input/Output
D[46]#	AB25	Source Sync	Input/Output
D[47]#	AA24	Source Sync	Input/Output
D[48]#	U22	Source Sync	Input/Output
D[49]#	T22	Source Sync	Input/Output
D[5]#	G21	Source Sync	Input/Output
D[50]#	T24	Source Sync	Input/Output
D[51]#	V23	Source Sync	Input/Output
D[52]#	U23	Source Sync	Input/Output

Table 13. Alphabetical Signal Listing (Sheet 4 of 13)

Pin Name	Pin Number	Signal Buffer Type	Direction
D[53]#	W22	Source Sync	Input/Output
D[54]#	Y22	Source Sync	Input/Output
D[55]#	Y23	Source Sync	Input/Output
D[56]#	AB24	Source Sync	Input/Output
D[57]#	AC25	Source Sync	Input/Output
D[58]#	AC26	Source Sync	Input/Output
D[59]#	AD24	Source Sync	Input/Output
D[6]#	F22	Source Sync	Input/Output
D[60]#	AE24	Source Sync	Input/Output
D[61]#	AB22	Source Sync	Input/Output
D[62]#	AA21	Source Sync	Input/Output
D[63]#	AD23	Source Sync	Input/Output
D[7]#	D23	Source Sync	Input/Output
D[8]#	E23	Source Sync	Input/Output
D[9]#	G23	Source Sync	Input/Output
DBSY#	H6	Common Clock	Input/Output
DEFER#	J6	Common Clock	Input
DINV#[0]	C24	Source Sync	Input/Output
DINV#[1]	H25	Source Sync	Input/Output
DINV#[2]	V26	Source Sync	Input/Output
DINV#[3]	AA23	Source Sync	Input/Output
DP[0]#	L26	Common Clock	Input/Output
DP[1]#	M25	Common Clock	Input/Output
DP[2]#	P25	Common Clock	Input/Output
DP[3]#	M24	Common Clock	Input/Output
DRDY#	G5	Common Clock	Input/Output
DSTBN[0]#	J21	Source Sync	Input/Output
DSTBN[1]#	M21	Source Sync	Input/Output
DSTBN[2]#	R21	Source Sync	Input/Output
DSTBN[3]#	V21	Source Sync	Input/Output
DSTBP[0]#	K21	Source Sync	Input/Output
DSTBP[1]#	N21	Source Sync	Input/Output
DSTBP[2]#	T21	Source Sync	Input/Output
DSTBP[3]#	W21	Source Sync	Input/Output
FERR#	B5	Open Drain	Output
FORCEPR#	A2	CMOS	Input
GTLREF	AD26	Power/Other	Input
HIT#	E3	Common Clock	Input/Output
HITM#	J4	Common Clock	Input/Output
IERR#	C21	Open Drain	Output

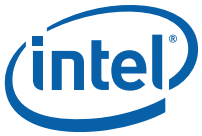


Table 13. Alphabetical Signal Listing (Sheet 5 of 13)

Pin Name	Pin Number	Signal Buffer Type	Direction
IGNNE#	E6	CMOS	Input
INIT#	D5	CMOS	Input
LINT0	B4	CMOS	Input
LINT1	B6	CMOS	Input
LOCK#	F4	Common Clock	Input/Output
MCERR#	K4	Common Clock	Input/Output
ODTEN	F6	Power/Other	Input
PRDY#	AD5	Common Clock	Output
PREQ#	AF4	Common Clock	Input
PROCHOT#	B25	Open Drain	Output
PWRGOOD	A4	CMOS	Input
REQ[0]#	L2	Source Sync	Input/Output
REQ[1]#	H3	Source Sync	Input/Output
REQ[2]#	H2	Source Sync	Input/Output
REQ[3]#	J3	Source Sync	Input/Output
REQ[4]#	G2	Source Sync	Input/Output
RESET#	D2	Common Clock	Input
RS[0]#	F1	Common Clock	Input
RS[1]#	E2	Common Clock	Input
RS[2]#	G4	Common Clock	Input
RSP#	Y4	Common Clock	Input
RSVD	M3	Reserved	
RSVD	N2	Reserved	
RSVD	P6	Reserved	
RSVD	R5	Reserved	
RSVD	B3	Reserved	
RSVD	C4	Reserved	
RSVD	D7	Reserved	
RSVD	R24	Reserved	
RSVD	AE25	Reserved	
RSVD	D1	Reserved	
RSVD	C1	Reserved	
RSVD	B2	Reserved	
RSVD	C3	Reserved	
SKTOCC#	AE1	Power/Other	Output
SLP#	C7	CMOS	Input
SMI#	E5	CMOS	Input
STPCLK#	D4	CMOS	Input
TCK	AA5	CMOS	Input
TDI	AC4	CMOS	Input

Table 13. Alphabetical Signal Listing (Sheet 6 of 13)

Pin Name	Pin Number	Signal Buffer Type	Direction
TDO	AB4	Open Drain	Output
TEST1	A24	Test	
TEST2	B23	Test	
THERMTRIP#	A5	Open Drain	Output
THRMDA	B22	Power/Other	
THRMDC	A22	Power/Other	
TMS	AB5	CMOS	Input
TRDY#	H5	Common Clock	Input
TRST#	AA6	CMOS	Input
VCC	AC20	Power/Other	
VCC	AD20	Power/Other	
VCC	AE20	Power/Other	
VCC	AF20	Power/Other	
VCC	AA17	Power/Other	
VCC	AA18	Power/Other	
VCC	AB17	Power/Other	
VCC	AB18	Power/Other	
VCC	AC17	Power/Other	
VCC	AC18	Power/Other	
VCC	AD17	Power/Other	
VCC	AD18	Power/Other	
VCC	AE17	Power/Other	
VCC	AE18	Power/Other	
VCC	AF17	Power/Other	
VCC	AF18	Power/Other	
VCC	AA15	Power/Other	
VCC	AB15	Power/Other	
VCC	AC15	Power/Other	
VCC	AD15	Power/Other	
VCC	AE15	Power/Other	
VCC	AF15	Power/Other	
VCC	AA13	Power/Other	
VCC	AB14	Power/Other	
VCC	AC13	Power/Other	
VCC	AD14	Power/Other	
VCC	AE13	Power/Other	
VCC	AF14	Power/Other	
VCC	AA12	Power/Other	
VCC	AB12	Power/Other	
VCC	AC12	Power/Other	

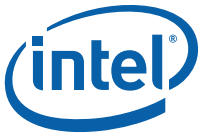


Table 13. Alphabetical Signal Listing (Sheet 7 of 13)

Pin Name	Pin Number	Signal Buffer Type	Direction
VCC	AD12	Power/Other	
VCC	AE12	Power/Other	
VCC	AF12	Power/Other	
VCC	AA9	Power/Other	
VCC	AA10	Power/Other	
VCC	AB9	Power/Other	
VCC	AB10	Power/Other	
VCC	AC9	Power/Other	
VCC	AC10	Power/Other	
VCC	AD9	Power/Other	
VCC	AD10	Power/Other	
VCC	AE9	Power/Other	
VCC	AE10	Power/Other	
VCC	AF9	Power/Other	
VCC	AF10	Power/Other	
VCC	AC7	Power/Other	
VCC	AD7	Power/Other	
VCC	AE7	Power/Other	
VCC	AF7	Power/Other	
VCC	A20	Power/Other	
VCC	B20	Power/Other	
VCC	E20	Power/Other	
VCC	F20	Power/Other	
VCC	A17	Power/Other	
VCC	A18	Power/Other	
VCC	B17	Power/Other	
VCC	B18	Power/Other	
VCC	C17	Power/Other	
VCC	C18	Power/Other	
VCC	D17	Power/Other	
VCC	D18	Power/Other	
VCC	E17	Power/Other	
VCC	E18	Power/Other	
VCC	F17	Power/Other	
VCC	F18	Power/Other	
VCC	A15	Power/Other	
VCC	B15	Power/Other	
VCC	C15	Power/Other	
VCC	D15	Power/Other	
VCC	E15	Power/Other	

Table 13. Alphabetical Signal Listing (Sheet 8 of 13)

Pin Name	Pin Number	Signal Buffer Type	Direction
VCC	F15	Power/Other	
VCC	A13	Power/Other	
VCC	B14	Power/Other	
VCC	C13	Power/Other	
VCC	D14	Power/Other	
VCC	E13	Power/Other	
VCC	F14	Power/Other	
VCC	A12	Power/Other	
VCC	B12	Power/Other	
VCC	C12	Power/Other	
VCC	D12	Power/Other	
VCC	E12	Power/Other	
VCC	F12	Power/Other	
VCC	A9	Power/Other	
VCC	A10	Power/Other	
VCC	B9	Power/Other	
VCC	B10	Power/Other	
VCC	C9	Power/Other	
VCC	C10	Power/Other	
VCC	D9	Power/Other	
VCC	D10	Power/Other	
VCC	E9	Power/Other	
VCC	E10	Power/Other	
VCC	F9	Power/Other	
VCC	F10	Power/Other	
VCC	A7	Power/Other	
VCC	B7	Power/Other	
VCC	E7	Power/Other	
VCC	F7	Power/Other	
VCCA	A23	Power/Other	
V_{CCP}	AC23	Power/Other	
V_{CCP}	U6	Power/Other	
V_{CCP}	AF25	Power/Other	
V_{CCP}	AF26	Power/Other	
V_{CCP}	AF23	Power/Other	
V_{CCP}	AB21	Power/Other	
V_{CCP}	AC22	Power/Other	
V_{CCP}	AD21	Power/Other	
V_{CCP}	AE21	Power/Other	
V_{CCP}	AE22	Power/Other	

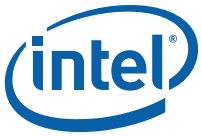


Table 13. Alphabetical Signal Listing (Sheet 9 of 13)

Pin Name	Pin Number	Signal Buffer Type	Direction
V_{CCP}	AF22	Power/Other	
V_{CCP}	AA20	Power/Other	
V_{CCP}	AB20	Power/Other	
V_{CCP}	V6	Power/Other	
V_{CCP}	Y6	Power/Other	
VCCSENSE	AA7	Power/Other	
VID[0]	AE4	CMOS	Output
VID[1]	AF3	CMOS	Output
VID[2]	AE3	CMOS	Output
VID[3]	AF2	CMOS	Output
VID[4]	AE2	CMOS	Output
VID[5]	AF1	CMOS	Output
VSS	AA25	Power/Other	
VSS	AB26	Power/Other	
VSS	AD25	Power/Other	
VSS	AE26	Power/Other	
VSS	AB23	Power/Other	
VSS	AC24	Power/Other	
VSS	AE23	Power/Other	
VSS	AF24	Power/Other	
VSS	AA22	Power/Other	
VSS	AC21	Power/Other	
VSS	AD22	Power/Other	
VSS	AF21	Power/Other	
VSS	AA19	Power/Other	
VSS	AB19	Power/Other	
VSS	AC19	Power/Other	
VSS	AD19	Power/Other	
VSS	AE19	Power/Other	
VSS	AF19	Power/Other	
VSS	AA16	Power/Other	
VSS	AB16	Power/Other	
VSS	AC16	Power/Other	
VSS	AD16	Power/Other	
VSS	AE16	Power/Other	
VSS	AF16	Power/Other	
VSS	AA14	Power/Other	
VSS	AB13	Power/Other	
VSS	AC14	Power/Other	
VSS	AD13	Power/Other	

Table 13. Alphabetical Signal Listing (Sheet 10 of 13)

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	AE14	Power/Other	
VSS	AF13	Power/Other	
VSS	AA11	Power/Other	
VSS	AB11	Power/Other	
VSS	AC11	Power/Other	
VSS	AD11	Power/Other	
VSS	AE11	Power/Other	
VSS	AF11	Power/Other	
VSS	AA8	Power/Other	
VSS	AB8	Power/Other	
VSS	AC8	Power/Other	
VSS	AD8	Power/Other	
VSS	AE8	Power/Other	
VSS	AF8	Power/Other	
VSS	AB6	Power/Other	
VSS	AC5	Power/Other	
VSS	AE6	Power/Other	
VSS	AF5	Power/Other	
VSS	AA4	Power/Other	
VSS	AB3	Power/Other	
VSS	AD4	Power/Other	
VSS	AA1	Power/Other	
VSS	AC2	Power/Other	
VSS	AD1	Power/Other	
VSS	A6	Power/Other	
VSS	C5	Power/Other	
VSS	D6	Power/Other	
VSS	F5	Power/Other	
VSS	G6	Power/Other	
VSS	J5	Power/Other	
VSS	K6	Power/Other	
VSS	M5	Power/Other	
VSS	N6	Power/Other	
VSS	P5	Power/Other	
VSS	T6	Power/Other	
VSS	U5	Power/Other	
VSS	W6	Power/Other	
VSS	Y5	Power/Other	
VSS	A3	Power/Other	
VSS	D3	Power/Other	

Table 13. Alphabetical Signal Listing (Sheet 11 of 13)

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	E4	Power/Other	
VSS	G3	Power/Other	
VSS	H4	Power/Other	
VSS	K3	Power/Other	
VSS	L4	Power/Other	
VSS	N3	Power/Other	
VSS	R4	Power/Other	
VSS	T3	Power/Other	
VSS	V4	Power/Other	
VSS	W3	Power/Other	
VSS	C2	Power/Other	
VSS	E1	Power/Other	
VSS	F2	Power/Other	
VSS	H1	Power/Other	
VSS	J2	Power/Other	
VSS	L1	Power/Other	
VSS	M2	Power/Other	
VSS	P2	Power/Other	
VSS	R1	Power/Other	
VSS	U2	Power/Other	
VSS	V1	Power/Other	
VSS	Y2	Power/Other	
VSS	A25	Power/Other	
VSS	C26	Power/Other	
VSS	D25	Power/Other	
VSS	F26	Power/Other	
VSS	B24	Power/Other	
VSS	C23	Power/Other	
VSS	E24	Power/Other	
VSS	F23	Power/Other	
VSS	B21	Power/Other	
VSS	D22	Power/Other	
VSS	E21	Power/Other	
VSS	A19	Power/Other	
VSS	B19	Power/Other	
VSS	C19	Power/Other	
VSS	D19	Power/Other	
VSS	E19	Power/Other	
VSS	F19	Power/Other	
VSS	A16	Power/Other	

Table 13. Alphabetical Signal Listing (Sheet 12 of 13)

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	B16	Power/Other	
VSS	C16	Power/Other	
VSS	D16	Power/Other	
VSS	E16	Power/Other	
VSS	F16	Power/Other	
VSS	A14	Power/Other	
VSS	B13	Power/Other	
VSS	C14	Power/Other	
VSS	D13	Power/Other	
VSS	E14	Power/Other	
VSS	F13	Power/Other	
VSS	A11	Power/Other	
VSS	B11	Power/Other	
VSS	C11	Power/Other	
VSS	D11	Power/Other	
VSS	E11	Power/Other	
VSS	F11	Power/Other	
VSS	A8	Power/Other	
VSS	B8	Power/Other	
VSS	C8	Power/Other	
VSS	D8	Power/Other	
VSS	E8	Power/Other	
VSS	F8	Power/Other	
VSS	G25	Power/Other	
VSS	J26	Power/Other	
VSS	K25	Power/Other	
VSS	M26	Power/Other	
VSS	N25	Power/Other	
VSS	R25	Power/Other	
VSS	T26	Power/Other	
VSS	V25	Power/Other	
VSS	W26	Power/Other	
VSS	H24	Power/Other	
VSS	J23	Power/Other	
VSS	L24	Power/Other	
VSS	M23	Power/Other	
VSS	P24	Power/Other	
VSS	T23	Power/Other	
VSS	U24	Power/Other	
VSS	W23	Power/Other	

Table 13. Alphabetical Signal Listing (Sheet 13 of 13)

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	Y24	Power/Other	
VSS	G22	Power/Other	
VSS	H21	Power/Other	
VSS	K22	Power/Other	
VSS	L21	Power/Other	
VSS	N22	Power/Other	
VSS	P21	Power/Other	
VSS	R22	Power/Other	
VSS	U21	Power/Other	
VSS	V22	Power/Other	
VSS	Y21	Power/Other	
VSSSENSE	AB7	Power/Other	Output

Table 14. Alphabetical Pin Listing (Sheet 1 of 12)

Pin Number	Pin Name	Signal Buffer Type	Direction
A2	FORCEPR#	CMOS	Input
A3	VSS	Power/Other	
A4	PWRGOOD	CMOS	Input
A5	THERMTRIP#	Open Drain	Output
A6	VSS	Power/Other	
A7	VCC	Power/Other	
A8	VSS	Power/Other	
A9	VCC	Power/Other	
A10	VCC	Power/Other	
A11	VSS	Power/Other	
A12	VCC	Power/Other	
A13	VCC	Power/Other	
A14	VSS	Power/Other	
A15	VCC	Power/Other	
A16	VSS	Power/Other	
A17	VCC	Power/Other	
A18	VCC	Power/Other	
A19	VSS	Power/Other	
A20	VCC	Power/Other	
A21	BSEL[2]	CMOS	Output
A22	THRMDC	Power/Other	
A23	VCCA	Power/Other	
A24	TEST1	Test	
A25	VSS	Power/Other	
A26	BCLK[1]	Bus Clock	Input
AA1	VSS	Power/Other	
AA2	A[21]#	Source Sync	Input/Output
AA3	A[26]#	Source Sync	Input/Output
AA4	VSS	Power/Other	
AA5	TCK	CMOS	Input
AA6	TRST#	CMOS	Input
AA7	VCCSENSE	Power/Other	
AA8	VSS	Power/Other	
AA9	VCC	Power/Other	
AA10	VCC	Power/Other	
AA11	VSS	Power/Other	
AA12	VCC	Power/Other	
AA13	VCC	Power/Other	
AA14	VSS	Power/Other	

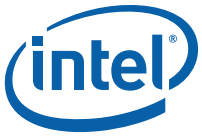


Table 14. Alphabetical Pin Listing (Sheet 2 of 12)

Pin Number	Pin Name	Signal Buffer Type	Direction
AA15	VCC	Power/Other	
AA16	VSS	Power/Other	
AA17	VCC	Power/Other	
AA18	VCC	Power/Other	
AA19	VSS	Power/Other	
AA20	VCCP	Power/Other	
AA21	D[62]#	Source Sync	Input/Output
AA22	VSS	Power/Other	
AA23	DINV#[3]	Source Sync	Input/Output
AA24	D[47]#	Source Sync	Input/Output
AA25	VSS	Power/Other	
AA26	D[44]#	Source Sync	Input/Output
AB1	A[34]#	Source Sync	Input/Output
AB2	A[27]#	Source Sync	Input/Output
AB3	VSS	Power/Other	
AB4	TDO	Open Drain	Output
AB5	TMS	CMOS	Input
AB6	VSS	Power/Other	
AB7	VSSSENSE	Power/Other	Output
AB8	VSS	Power/Other	
AB9	VCC	Power/Other	
AB10	VCC	Power/Other	
AB11	VSS	Power/Other	
AB12	VCC	Power/Other	
AB13	VSS	Power/Other	
AB14	VCC	Power/Other	
AB15	VCC	Power/Other	
AB16	VSS	Power/Other	
AB17	VCC	Power/Other	
AB18	VCC	Power/Other	
AB19	VSS	Power/Other	
AB20	VCCP	Power/Other	
AB21	VCCP	Power/Other	
AB22	D[61]#	Source Sync	Input/Output
AB23	VSS	Power/Other	
AB24	D[56]#	Source Sync	Input/Output
AB25	D[46]#	Source Sync	Input/Output
AB26	VSS	Power/Other	
AC1	A[35]#	Source Sync	Input/Output
AC2	VSS	Power/Other	

Table 14. Alphabetical Pin Listing (Sheet 3 of 12)

Pin Number	Pin Name	Signal Buffer Type	Direction
AC3	A[33]#	Source Sync	Input/Output
AC4	TDI	CMOS	Input
AC5	VSS	Power/Other	
AC6	BPM[2]#	Common Clock	Output
AC7	VCC	Power/Other	
AC8	VSS	Power/Other	
AC9	VCC	Power/Other	
AC10	VCC	Power/Other	
AC11	VSS	Power/Other	
AC12	VCC	Power/Other	
AC13	VCC	Power/Other	
AC14	VSS	Power/Other	
AC15	VCC	Power/Other	
AC16	VSS	Power/Other	
AC17	VCC	Power/Other	
AC18	VCC	Power/Other	
AC19	VSS	Power/Other	
AC20	VCC	Power/Other	
AC21	VSS	Power/Other	
AC22	VCCP	Power/Other	
AC23	VCCP	Power/Other	
AC24	VSS	Power/Other	
AC25	D[57]#	Source Sync	Input/Output
AC26	D[58]#	Source Sync	Input/Output
AD1	VSS	Power/Other	
AD2	A[31]#	Source Sync	Input/Output
AD3	A[32]#	Source Sync	Input/Output
AD4	VSS	Power/Other	
AD5	PRDY#	Common Clock	Output
AD6	BPM[1]#	Common Clock	Output
AD7	VCC	Power/Other	
AD8	VSS	Power/Other	
AD9	VCC	Power/Other	
AD10	VCC	Power/Other	
AD11	VSS	Power/Other	
AD12	VCC	Power/Other	
AD13	VSS	Power/Other	
AD14	VCC	Power/Other	
AD15	VCC	Power/Other	
AD16	VSS	Power/Other	

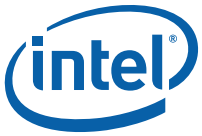


Table 14. Alphabetical Pin Listing (Sheet 4 of 12)

Pin Number	Pin Name	Signal Buffer Type	Direction
AD17	VCC	Power/Other	
AD18	VCC	Power/Other	
AD19	VSS	Power/Other	
AD20	VCC	Power/Other	
AD21	VCCP	Power/Other	
AD22	VSS	Power/Other	
AD23	D[63]#	Source Sync	Input/Output
AD24	D[59]#	Source Sync	Input/Output
AD25	VSS	Power/Other	
AD26	GTLREF	Power/Other	Input
AE1	SKTOCC#	Power/Other	Output
AE2	VID[4]	CMOS	Output
AE3	VID[2]	CMOS	Output
AE4	VID[0]	CMOS	Output
AE5	BPM[3]#	Common Clock	Input/Output
AE6	VSS	Power/Other	
AE7	VCC	Power/Other	
AE8	VSS	Power/Other	
AE9	VCC	Power/Other	
AE10	VCC	Power/Other	
AE11	VSS	Power/Other	
AE12	VCC	Power/Other	
AE13	VCC	Power/Other	
AE14	VSS	Power/Other	
AE15	VCC	Power/Other	
AE16	VSS	Power/Other	
AE17	VCC	Power/Other	
AE18	VCC	Power/Other	
AE19	VSS	Power/Other	
AE20	VCC	Power/Other	
AE21	VCCP	Power/Other	
AE22	VCCP	Power/Other	
AE23	VSS	Power/Other	
AE24	D[60]#	Source Sync	Input/Output
AE25	RSVD	Reserved	
AE26	VSS	Power/Other	
AF1	VID[5]	CMOS	Output
AF2	VID[3]	CMOS	Output
AF3	VID[1]	CMOS	Output
AF4	PREQ#	Common Clock	Input

Table 14. Alphabetical Pin Listing (Sheet 5 of 12)

Pin Number	Pin Name	Signal Buffer Type	Direction
AF5	VSS	Power/Other	
AF6	BPM[0]#	Common Clock	Output
AF7	VCC	Power/Other	
AF8	VSS	Power/Other	
AF9	VCC	Power/Other	
AF10	VCC	Power/Other	
AF11	VSS	Power/Other	
AF12	VCC	Power/Other	
AF13	VSS	Power/Other	
AF14	VCC	Power/Other	
AF15	VCC	Power/Other	
AF16	VSS	Power/Other	
AF17	VCC	Power/Other	
AF18	VCC	Power/Other	
AF19	VSS	Power/Other	
AF20	VCC	Power/Other	
AF21	VSS	Power/Other	
AF22	VCCP	Power/Other	
AF23	VCCP	Power/Other	
AF24	VSS	Power/Other	
AF25	VCCP	Power/Other	
AF26	VCCP	Power/Other	
B2	RSVD	Reserved	
B3	RSVD	Reserved	
B4	LINT0	CMOS	Input
B5	FERR#	Open Drain	Output
B6	LINT1	CMOS	Input
B7	VCC	Power/Other	
B8	VSS	Power/Other	
B9	VCC	Power/Other	
B10	VCC	Power/Other	
B11	VSS	Power/Other	
B12	VCC	Power/Other	
B13	VSS	Power/Other	
B14	VCC	Power/Other	
B15	VCC	Power/Other	
B16	VSS	Power/Other	
B17	VCC	Power/Other	
B18	VCC	Power/Other	
B19	VSS	Power/Other	

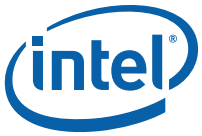


Table 14. Alphabetical Pin Listing (Sheet 6 of 12)

Pin Number	Pin Name	Signal Buffer Type	Direction
B20	VCC	Power/Other	
B21	VSS	Power/Other	
B22	THRMDA	Power/Other	
B23	TEST2	Test	
B24	VSS	Power/Other	
B25	PROCHOT#	Open Drain	Output
B26	BCLK[0]	Bus Clock	Input
C1	RSVD	Reserved	
C2	VSS	Power/Other	
C3	RSVD	Reserved	
C4	RSVD	Reserved	
C5	VSS	Power/Other	
C6	A20M#	CMOS	Input
C7	SLP#	CMOS	Input
C8	VSS	Power/Other	
C9	VCC	Power/Other	
C10	VCC	Power/Other	
C11	VSS	Power/Other	
C12	VCC	Power/Other	
C13	VCC	Power/Other	
C14	VSS	Power/Other	
C15	VCC	Power/Other	
C16	VSS	Power/Other	
C17	VCC	Power/Other	
C18	VCC	Power/Other	
C19	VSS	Power/Other	
C20	BSEL[0]	CMOS	Output
C21	IERR#	Open Drain	Output
C22	D[1]#	Source Sync	Input/Output
C23	VSS	Power/Other	
C24	DINV#[0]	Source Sync	Input/Output
C25	D[4]#	Source Sync	Input/Output
C26	VSS	Power/Other	
D1	RSVD	Reserved	
D2	RESET#	Common Clock	Input
D3	VSS	Power/Other	
D4	STPCLK#	CMOS	Input
D5	INIT#	CMOS	Input
D6	VSS	Power/Other	
D7	RSVD	Reserved	

Table 14. Alphabetical Pin Listing (Sheet 7 of 12)

Pin Number	Pin Name	Signal Buffer Type	Direction
D8	VSS	Power/Other	
D9	VCC	Power/Other	
D10	VCC	Power/Other	
D11	VSS	Power/Other	
D12	VCC	Power/Other	
D13	VSS	Power/Other	
D14	VCC	Power/Other	
D15	VCC	Power/Other	
D16	VSS	Power/Other	
D17	VCC	Power/Other	
D18	VCC	Power/Other	
D19	VSS	Power/Other	
D20	BSEL[1]	CMOS	Output
D21	D[0]#	Source Sync	Input/Output
D22	VSS	Power/Other	
D23	D[7]#	Source Sync	Input/Output
D24	D[17]#	Source Sync	Input/Output
D25	VSS	Power/Other	
D26	D[16]#	Source Sync	Input/Output
E1	VSS	Power/Other	
E2	RS[1]#	Common Clock	Input
E3	HIT#	Common Clock	Input/Output
E4	VSS	Power/Other	
E5	SMI#	CMOS	Input
E6	IGNNE#	CMOS	Input
E7	VCC	Power/Other	
E8	VSS	Power/Other	
E9	VCC	Power/Other	
E10	VCC	Power/Other	
E11	VSS	Power/Other	
E12	VCC	Power/Other	
E13	VCC	Power/Other	
E14	VSS	Power/Other	
E15	VCC	Power/Other	
E16	VSS	Power/Other	
E17	VCC	Power/Other	
E18	VCC	Power/Other	
E19	VSS	Power/Other	
E20	VCC	Power/Other	
E21	VSS	Power/Other	

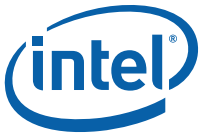


Table 14. Alphabetical Pin Listing (Sheet 8 of 12)

Pin Number	Pin Name	Signal Buffer Type	Direction
E22	D[3]#	Source Sync	Input/Output
E23	D[8]#	Source Sync	Input/Output
E24	VSS	Power/Other	
E25	D[18]#	Source Sync	Input/Output
E26	D[19]#	Source Sync	Input/Output
F1	RS[0]#	Common Clock	Input
F2	VSS	Power/Other	
F3	BNR#	Common Clock	Input/Output
F4	LOCK#	Common Clock	Input/Output
F5	VSS	Power/Other	
F6	ODTEN	Power/Other	Input
F7	VCC	Power/Other	
F8	VSS	Power/Other	
F9	VCC	Power/Other	
F10	VCC	Power/Other	
F11	VSS	Power/Other	
F12	VCC	Power/Other	
F13	VSS	Power/Other	
F14	VCC	Power/Other	
F15	VCC	Power/Other	
F16	VSS	Power/Other	
F17	VCC	Power/Other	
F18	VCC	Power/Other	
F19	VSS	Power/Other	
F20	VCC	Power/Other	
F21	D[2]#	Source Sync	Input/Output
F22	D[6]#	Source Sync	Input/Output
F23	VSS	Power/Other	
F24	D[20]#	Source Sync	Input/Output
F25	D[21]#	Source Sync	Input/Output
F26	VSS	Power/Other	
G1	A[3]#	Source Sync	Input/Output
G2	REQ[4]#	Source Sync	Input/Output
G3	VSS	Power/Other	
G4	RS[2]#	Common Clock	Input
G5	DRDY#	Common Clock	Input/Output
G6	VSS	Power/Other	
G21	D[5]#	Source Sync	Input/Output
G22	VSS	Power/Other	
G23	D[9]#	Source Sync	Input/Output

Table 14. Alphabetical Pin Listing (Sheet 9 of 12)

Pin Number	Pin Name	Signal Buffer Type	Direction
G24	D[23]#	Source Sync	Input/Output
G25	VSS	Power/Other	
G26	D[22]#	Source Sync	Input/Output
H1	VSS	Power/Other	
H2	REQ[2]#	Source Sync	Input/Output
H3	REQ[1]#	Source Sync	Input/Output
H4	VSS	Power/Other	
H5	TRDY#	Common Clock	Input
H6	DBSY#	Common Clock	Input/Output
H21	VSS	Power/Other	
H22	D[10]#	Source Sync	Input/Output
H23	D[13]#	Source Sync	Input/Output
H24	VSS	Power/Other	
H25	DINV#[1]	Source Sync	Input/Output
H26	D[27]#	Source Sync	Input/Output
J1	A[4]#	Source Sync	Input/Output
J2	VSS	Power/Other	
J3	REQ[3]#	Source Sync	Input/Output
J4	HITM#	Common Clock	Input/Output
J5	VSS	Power/Other	
J6	DEFER#	Common Clock	Input
J21	DSTBN[0]#	Source Sync	Input/Output
J22	D[11]#	Source Sync	Input/Output
J23	VSS	Power/Other	
J24	D[26]#	Source Sync	Input/Output
J25	D[29]#	Source Sync	Input/Output
J26	VSS	Power/Other	
K1	A[5]#	Source Sync	Input/Output
K2	A[7]#	Source Sync	Input/Output
K3	VSS	Power/Other	
K4	MCERR#	Common Clock	Input/Output
K5	BPRI#	Common Clock	Input
K6	VSS	Power/Other	
K21	DSTBP[0]#	Source Sync	Input/Output
K22	VSS	Power/Other	
K23	D[12]#	Source Sync	Input/Output
K24	D[25]#	Source Sync	Input/Output
K25	VSS	Power/Other	
K26	D[28]#	Source Sync	Input/Output
L1	VSS	Power/Other	

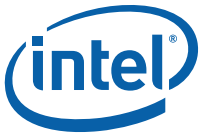


Table 14. Alphabetical Pin Listing (Sheet 10 of 12)

Pin Number	Pin Name	Signal Buffer Type	Direction
L2	REQ[0]#	Source Sync	Input/Output
L3	A[6]#	Source Sync	Input/Output
L4	VSS	Power/Other	
L5	BR1#	Common Clock	Input
L6	ADS#	Common Clock	Input/Output
L21	VSS	Power/Other	
L22	D[15]#	Source Sync	Input/Output
L23	D[14]#	Source Sync	Input/Output
L24	VSS	Power/Other	
L25	D[30]#	Source Sync	Input/Output
L26	DP[0]#	Common Clock	Input/Output
M1	A[8]#	Source Sync	Input/Output
M2	VSS	Power/Other	
M3	RSVD	Reserved	
M4	BR0#	Common Clock	Input/Output
M5	VSS	Power/Other	
M6	ADSTB#[0]	Source Sync	Input/Output
M21	DSTBN[1#]	Source Sync	Input/Output
M22	D[24]#	Source Sync	Input/Output
M23	VSS	Power/Other	
M24	DP[3]#	Common Clock	Input/Output
M25	DP[1]#	Common Clock	Input/Output
M26	VSS	Power/Other	
N1	COMP[3]	Power/Other	Input/Output
N2	RSVD	Reserved	
N3	VSS	Power/Other	
N4	A[11]#	Source Sync	Input/Output
N5	A[17]#	Source Sync	Input/Output
N6	VSS	Power/Other	
N21	DSTBP[1]#	Source Sync	Input/Output
N22	VSS	Power/Other	
N23	D[31]#	Source Sync	Input/Output
N24	D[36]#	Source Sync	Input/Output
N25	VSS	Power/Other	
N26	D[34]#	Source Sync	Input/Output
P1	COMP[2]	Power/Other	Input/Output
P2	VSS	Power/Other	
P3	A[9]#	Source Sync	Input/Output
P4	A[15]#	Source Sync	Input/Output
P5	VSS	Power/Other	

Table 14. Alphabetical Pin Listing (Sheet 11 of 12)

Pin Number	Pin Name	Signal Buffer Type	Direction
P6	RSVD	Reserved	
P21	VSS	Power/Other	
P22	D[33]#	Source Sync	Input/Output
P23	D[32]#	Source Sync	Input/Output
P24	VSS	Power/Other	
P25	DP[2]#	Common Clock	Input/Output
P26	COMP[0]	Power/Other	Input/Output
R1	VSS	Power/Other	
R2	A[12]#	Source Sync	Input/Output
R3	A[16]#	Source Sync	Input/Output
R4	VSS	Power/Other	
R5	RSVD	Reserved	
R6	ADSTB[1]#	Source Sync	Input/Output
R21	DSTBN[2]#	Source Sync	Input/Output
R22	VSS	Power/Other	
R23	D[37]#	Source Sync	Input/Output
R24	RSVD	Reserved	
R25	VSS	Power/Other	
R26	COMP[1]	Power/Other	Input/Output
T1	A[10]#	Source Sync	Input/Output
T2	A[13]#	Source Sync	Input/Output
T3	VSS	Power/Other	
T4	A[19]#	Source Sync	Input/Output
T5	A[18]#	Source Sync	Input/Output
T6	VSS	Power/Other	
T21	DSTBP[2]#	Source Sync	Input/Output
T22	D[49]#	Source Sync	Input/Output
T23	VSS	Power/Other	
T24	D[50]#	Source Sync	Input/Output
T25	D[39]#	Source Sync	Input/Output
T26	VSS	Power/Other	
U1	A[14]#	Source Sync	Input/Output
U2	VSS	Power/Other	
U3	A[24]#	Source Sync	Input/Output
U4	A[22]#	Source Sync	Input/Output
U5	VSS	Power/Other	
U6	VCCP	Power/Other	
U21	VSS	Power/Other	
U22	D[48]#	Source Sync	Input/Output
U23	D[52]#	Source Sync	Input/Output

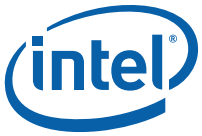


Table 14. Alphabetical Pin Listing (Sheet 12 of 12)

Pin Number	Pin Name	Signal Buffer Type	Direction
U24	VSS	Power/Other	
U25	D[38]#	Source Sync	Input/Output
U26	D[35]#	Source Sync	Input/Output
V1	VSS	Power/Other	
V2	A[25]#	Source Sync	Input/Output
V3	A[23]#	Source Sync	Input/Output
V4	VSS	Power/Other	
V5	AP[0]#	Common Clock	Input/Output
V6	VCCP	Power/Other	
V21	DSTBN[3]#	Source Sync	Input/Output
V22	VSS	Power/Other	
V23	D[51]#	Source Sync	Input/Output
V24	D[41]#	Source Sync	Input/Output
V25	VSS	Power/Other	
V26	DINV[2]#	Source Sync	Input/Output
W1	A[30]#	Source Sync	Input/Output
W2	A[28]#	Source Sync	Input/Output
W3	VSS	Power/Other	
W4	AP[1]#	Common Clock	Input/Output
W5	BINIT#	Common Clock	Input/Output
W6	VSS	Power/Other	
W21	DSTBP[3]#	Source Sync	Input/Output
W22	D[53]#	Source Sync	Input/Output
W23	VSS	Power/Other	
W24	D[43]#	Source Sync	Input/Output
W25	D[40]#	Source Sync	Input/Output
W26	VSS	Power/Other	
Y1	A[29]#	Source Sync	Input/Output
Y2	VSS	Power/Other	
Y3	A[20]#	Source Sync	Input/Output
Y4	RSP#	Common Clock	Input
Y5	VSS	Power/Other	
Y6	VCCP	Power/Other	
Y21	VSS	Power/Other	
Y22	D[54]#	Source Sync	Input/Output
Y23	D[55]#	Source Sync	Input/Output
Y24	VSS	Power/Other	
Y25	D[45]#	Source Sync	Input/Output
Y26	D[42]#	Source Sync	Input/Output

5.0 Thermal Specifications and Design Considerations

The processor requires a thermal solution to maintain temperatures within operating limits as set forth in Section 5.1. Any attempt to operate the processor outside these operating limits may result in permanent damage to the processor and potentially other components in the system. As processor technology changes, thermal management becomes increasingly crucial when building computer systems. Maintaining the proper thermal environment is key to reliable, long-term system operation. A complete thermal solution includes both component and system level thermal management features. Component level thermal solutions include active or passive heatsinks or heat exchangers attached to the processor exposed die. The solution should make firm contact to the die while maintaining processor mechanical specifications such as pressure. A typical system level thermal solution may consist of a processor fan. A secondary fan or air from the processor fan may also be used to cool other platform components or to lower the internal ambient temperature within the system.

To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed such that the processor remains within the minimum and maximum junction temperature (T_J) specifications at the corresponding thermal design power (TDP) value listed in Table 15. Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system.

Refer to the *Dual-Core Intel® Xeon® Processor LV and ULV Thermal Design Guideline for Embedded Applications* document for more details on processor and system level cooling approaches.

The maximum junction temperature is defined by an activation of the processor Intel® Thermal Monitor. Refer to Section 5.1.3 for more details. Analysis indicates that real applications are unlikely to cause the processor to consume the theoretical maximum power dissipation for sustained time periods. Intel recommends that complete thermal solution designs target the TDP indicated in Table 15. The Intel Thermal Monitor feature is designed to help protect the processor in the unlikely event that an application exceeds the TDP recommendation for a sustained period of time. For more details on the usage of this feature, refer to Section 5.1.3. In all cases the Intel thermal monitor feature must be enabled for the processor to remain within specification.

Table 15. Dual-Core Intel® Xeon® Processor LV Power Specifications

Symbol	Processor Number	Core Frequency & Voltage	Thermal Design Power			Unit	Notes
TDP	Not Applicable	2.00GHz and HFM Vcc 1.66 GHz and HFM Vcc 1 GHz and LFM Vcc	31 31 19.4			W	1, 4
Symbol	**Parameter**		**Min**	**Typ**	**Max**	**Unit**	**Notes**
P_{AH}, P_{SGNT}	Auto Halt, Stop Grant Power at LFM Vcc at HFM Vcc				7.8 14.4	W	2

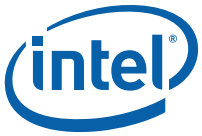


Table 15. Dual-Core Intel® Xeon® Processor LV Power Specifications

Symbol	Processor Number	Core Frequency & Voltage	Thermal Design Power			Unit	Notes
P_{SLP}	Sleep Power at LFM Vcc at HFM Vcc				7.7 14.2	W	2
T_J	Junction Temperature		0		100	°C	3

Notes:
1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating to 50°C.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum T_J has been reached. Refer to Section 5.1 for more details.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.

Table 16. Dual-Core Intel® Xeon® Processor ULV Power Specifications

Symbol	Processor Number	Core Frequency & Voltage	Thermal Design Power	Unit	Notes
TDP	Not Applicable	1.66GHz and HFM Vcc >1.66 GHz and HFM Vcc 1 GHz and LFM Vcc	15 15 13.1	W	1, 4

Symbol	Parameter	Min	Typ	Max	Unit	Notes
P_{AH}, P_{SGNT}	Auto Halt, Stop Grant Power at LFM Vcc at HFM Vcc			4.8 6.0	W	2
P_{SLP}	Sleep Power at LFM Vcc at HFM Vcc			4.7 5.8	W	2
T_J	Junction Temperature	0		100	°C	3

Notes:
1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating to 50°C.
3. As measured by the activation of the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum T_J has been reached. Refer to Section 5.1 for more details.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.

5.1 Thermal Specifications

The processor incorporates three methods of monitoring die temperature, the Digital thermal sensor, Intel thermal monitor and the thermal diode. The Intel Thermal Monitor (detailed in Section 5.1.3) must be used to determine when the maximum specified processor junction temperature has been reached.

5.1.1 Thermal Diode

The processor incorporates an on-die PNP transistor whose base emitter junction is used as a thermal "diode", with its collector shorted to Ground. The thermal diode, can be read by an off-die analog/digital converter (a thermal sensor) located on the

motherboard, or a stand-alone measurement kit. The thermal diode may be used to monitor the die temperature of the processor for thermal management or instrumentation purposes but is not a reliable indication that the maximum operating temperature of the processor has been reached. When using the thermal diode, a temperature offset value must be read from a processor Model Specific Register (MSR) and applied. See Section 5.1.2 for more details. Please see Section 5.1.3 for thermal diode usage recommendation when the PROCHOT# signal is not asserted.

Note: The reading of the external thermal sensor (on the motherboard) connected to the processor thermal diode signals, will not necessarily reflect the temperature of the hottest location on the die. This is due to inaccuracies in the external thermal sensor, on-die temperature gradients between the location of the thermal diode and the hottest location on the die, and time based variations in the die temperature measurement. Time based variations can occur when the sampling rate of the thermal diode (by the thermal sensor) is slower than the rate at which the T_J temperature can change.

Offset between the thermal diode based temperature reading and the Intel Thermal Monitor reading may be characterized using the Intel Thermal Monitor's Automatic mode activation of thermal control circuit. This temperature offset must be taken into account when using the processor thermal diode to implement power management events. This offset is different than the diode Toffset value programmed into the processor Model Specific Register (MSR).

Table 17, Table 18, Table 19, and Table 20 provide the "diode" interface and specifications. Two different sets of "diode" parameters are listed in Table 18 and Table 19. The Diode Model parameters (Table 18) apply to traditional thermal sensors that use the Diode Equation to determine the processor temperature. Transistor Model parameters (Table 19) have been added to support thermal sensors that use the transistor equation method. The Transistor Model may provide more accurate temperature measurements when the diode ideality factor is closer to the maximum or minimum limits. Please contact your external thermal sensor supplier for their recommendation. This thermal "diode" is separate from the Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

Table 17. Thermal Diode Interface

Signal Name	Pin/Ball Number	Signal Description
THERMDA	B22	Thermal diode anode
THERMDC	A22	Thermal diode cathode

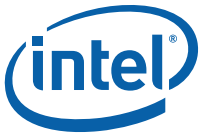


Table 18. Thermal "Diode" Parameters using Diode Mode

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{FW}	Forward Bias Current	5		200	µA	1
n	Diode Ideality Factor	1.000	1.009	1.050	-	2, 3, 4
R_T	Series Resistance	2.79	4.52	6.24	Ω	2, 3, 5

Notes:

1. Intel does not support or recommend operation of the thermal diode under reverse bias. Intel does not support or recommend operation of the thermal diode when the processor power supplies are not within their specified tolerance range.
2. Characterized across a temperature range of 50 - 100°C.
3. Not 100% tested. Specified by design characterization.
4. The ideality factor, n, represents the deviation from ideal diode behavior as exemplified by the diode equation:

$$I_{FW} = I_S * (e^{qV_D/nkT} - 1)$$

where I_S = saturation current, q = electronic charge, V_D = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin).

5. The series resistance, R_T, is provided to allow for a more accurate measurement of the junction temperature. R_T, as defined, includes the lands of the processor but does not include any socket resistance or board trace resistance between the socket and the external remote diode thermal sensor. R_T can be used by remote diode thermal sensors with automatic series resistance cancellation to calibrate out this error term. Another application is that a temperature offset can be manually calculated and programmed into an offset register in the remote diode thermal sensors as exemplified by the equation:

$$T_{error} = [R_T * (N-1) * I_{FWmin}] / [nk/q * \ln N]$$

where T_{error} = sensor temperature error, N = sensor current ratio, k = Boltzmann Constant, q = electronic charge.

Table 19. Thermal "Diode" Parameters using Transistor Mode

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{FW}	Forward Bias Current	5	-	200	µA	1, 2
I_E	Emitter Current	5		200	µA	
n_Q	Transistor Ideality	0.997	1.001	1.005	-	3, 4, 5
Beta		0.3		0.760		3, 4
R_T	Series Resistance	2.79	4.52	6.24	Ω	3, 6

Notes:

1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. Same as I_{FW} in Table 17.
3. Characterized across a temperature range of 50 - 100 °C.
4. Not 100% tested. Specified by design characterization.
5. The ideality factor, nQ, represents the deviation from ideal transistor model behavior as exemplified by the equation for the collector current:

$$I_C = I_S * (e^{qV_{BE}/n_Q kT} - 1)$$

Where I_S = saturation current, q = electronic charge, V_{BE} = voltage across the transistor base emitter junction (same nodes as VD), k = Boltzmann Constant, and T = absolute temperature (Kelvin).

6. The series resistance, R_T, provided in the Diode Model Table (Table 18) can be used for more accurate readings as needed.

When calculating a temperature based on thermal diode measurements, a number of parameters must be either measured or assumed. Most devices measure the diode ideality and assume a series resistance and ideality trim value, although some are capable of also measuring the series resistance. Calculating the temperature is then accomplished using the equations listed under Table 17. In most temperature sensing devices, an expected value for the diode ideality is designed-in to the temperature calculation equation. If the designer of the temperature sensing device assumes a perfect diode the ideality value (also called n_{trim}) will be 1.000. Given that most diodes

are not perfect, the designers usually select an n_{trim} value that more closely matches the behavior of the diodes in the processor. If the processors diode ideality deviates from that of n_{trim}, each calculated temperature will be offset by a fixed amount. This temperature offset can be calculated with the equation:

$$T_{error(nf)} = T_{measured} X (1 - n_{actual}/n_{trim})$$

Where $T_{error(nf)}$ is the offset in degrees C, $T_{measured}$ is in Kelvin, n_{actual} is the measured ideality of the diode, and n_{trim} is the diode ideality assumed by the temperature sensing device.

5.1.2 Thermal Diode Offset

In order to improve the accuracy of diode based temperature measurements, a temperature offset value (specified as Toffset) will be programmed into a processor Model Specific Register (MSR) which will contain thermal diode characterization data. During manufacturing each processors thermal diode will be evaluated for its behavior relative to a theoretical diode. Using the equation above, the temperature error created by the difference between n_{trim} and the actual ideality of the particular processor will be calculated.

If the n_{trim} value used to calculate Toffset differs from the n_{trim} value used in a temperature sensing device, the $T_{error(nf)}$ may not be accurate. If desired, the Toffset can be adjusted by calculating n_{actual} and then recalculating the offset using the actual n_{trim} as defined in the temperature sensor manufacturers' datasheet.

The n_{trim} used to calculate the Diode Correction Toffset are listed in Table 20.

Table 20. Thermal "Diode" n_{trim} and Diode Correction Toffset

Symbol	Parameter	Unit
n_{trim}	Diode ideality used to calculate Toffset	1.01

5.1.3 Intel® Thermal Monitor

The Intel Thermal Monitor helps control the processor temperature by activating the TCC (Thermal Control Circuit) when the processor silicon reaches its maximum junction temperature. The temperature at which the Intel Thermal Monitor activates the TCC is not user configurable. Bus traffic is snooped in the normal manner, and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

A thermal solution that is significantly under designed may not be capable of cooling the processor even when the TCC is active continuously.

The Intel Thermal Monitor controls the processor temperature by modulating (starting and stopping) the processor core clocks or by initiating an Enhanced Intel SpeedStep® Technology transition when the processor silicon reaches its maximum operating temperature. The Intel Thermal Monitor uses two modes to activate the TCC: Automatic mode and on-demand mode. If both modes are activated, Automatic mode takes precedence.

Note: The Intel thermal monitor automatic mode must be enabled through BIOS for the processor to be operating within specifications.

There are two automatic modes called Intel Thermal Monitor 1 and Intel Thermal Monitor 2. These modes are selected by writing values to the Model Specific Registers (MSRs) of the processor. After Automatic mode is enabled, the TCC activates only when the internal die temperature reaches the maximum allowed value for operation.

TM1 and TM2 can co-exist within the processor. If both TM1 and TM2 bits are enabled in the auto-throttle MSR, TM2 will take precedence over TM1. However, if TM2 is not sufficient to cool the processor below the maximum operating temperature, then TM1 will also activate to help cool down the processor.

Note: Intel recommends Thermal Monitor 1 and Thermal Monitor 2 to be simultaneously enabled on processors.

Likewise, when Intel Thermal Monitor 2 is enabled, and a high temperature situation exists, the processor performs an Enhanced Intel SpeedStep® Technology transition to a lower operating point. When the processor temperature drops below the critical level, the processor makes an Enhanced Intel SpeedStep Technology transition to the last requested operating point.

If a processor load based Enhanced Intel SpeedStep Technology transition (through MSR write) is initiated when an Intel Thermal Monitor 2 period is active, there are two possible results:

1. If the processor load based Enhanced Intel SpeedStep Technology transition target frequency is **higher** than the Intel® Thermal Monitor 2 transition based target frequency, the processor load-based transition is deferred until the Intel Thermal Monitor 2 event has been completed.
2. If the processor load-based Enhanced Intel SpeedStep Technology transition target frequency is **lower** than the Intel Thermal Monitor 2 transition based target frequency, the processor transitions to the processor load-based Enhanced Intel SpeedStep® Technology target frequency point.

When Intel Thermal Monitor 1 is enabled, and a high temperature situation exists, the clocks are modulated by alternately turning the clocks off and on at an MSR-controlled percent duty cycle. Cycle times are processor speed dependent and decreases linearly as processor core frequencies increase. Once the temperature has returned to a non-critical level, modulation ceases and TCC goes inactive. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near the trip point. The duty cycle is factory configured and cannot be modified. Also, automatic mode does not require any additional hardware, software drivers, or interrupt handling routines. Processor performance is decreased by the same amount as the duty cycle when the TCC is active.

The TCC may also be activated via on-demand mode. If bit 4 of the ACPI Intel thermal monitor control register is written to a 1, the TCC is activated immediately, independent of the processor temperature. When using on-demand mode to activate the TCC, the duty cycle of the clock modulation is programmable via bits 3:1 of the same ACPI Intel Thermal Monitor control register. In automatic mode, the duty cycle is fixed at 50% on, 50% off, however in on-demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off, to 87.5% on/12.5% off in 12.5% increments. On-demand mode may be used at the same time automatic mode is enabled, however, if the system tries to enable the TCC via on-demand mode at the same time automatic mode is enabled and a high temperature condition exists, automatic mode takes precedence

An external signal, PROCHOT# (processor hot) is asserted when the processor detects that its temperature is above the thermal trip point. Bus snooping and interrupt latching are also active while the TCC is active.

Besides the thermal sensor and thermal control circuit, the Intel Thermal Monitor also includes one ACPI register, one performance counter register, three model specific registers (MSR), one output pin (PROCHOT#), and one input pin (FORCEPR#). All are available to monitor and control the state of the Intel thermal monitor feature. The Intel thermal monitor can be configured to generate an interrupt upon the assertion or deassertion of PROCHOT#.

Note: PROCHOT# is not asserted when the processor is in the Stop Grant, and Sleep, low power states (internal clocks stopped), hence the thermal diode reading must be used as a safeguard to maintain the processor junction temperature within maximum specification. If the platform thermal solution is not able to maintain the processor junction temperature within the maximum specification, the system must initiate an orderly shutdown to prevent damage. If the processor enters a low power states with PROCHOT# already asserted, PROCHOT# remains asserted until the processor exits the low power state and the processor junction temperature drops below the thermal trip point.

If Thermal Monitor automatic mode is disabled, the processor is operating out of specification. Regardless of enabling the automatic or on-demand modes, in the event of a catastrophic cooling failure, the processor automatically shuts down when the silicon has reached a temperature of approximately 125°C. At this point the THERMTRIP# signal goes active. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. When THERMTRIP# is asserted, the processor core voltage must be shut down within the time specified in Chapter 3.0.

5.1.4 Digital Thermal Sensor (DTS)

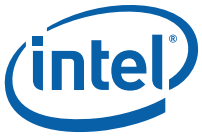
The processor also contains an on-die digital thermometer that can be read via a MSR (no I/O interface). The digital thermometer shares the thermal sensor of the Intel Thermal Monitor. In a dual core implementation of the processor, each core has a unique digital thermometer whose temperature is accessible via processor MSR. The digital sensor is the preferred method of reading the processor die temperature since it can be located much closer to the hottest portions of the die and can thus more accurately track the die temperature and potential activation of processor throttling via the Thermal Monitor.

Unlike traditional thermal devices, the Digital Thermometer outputs a temperature relative to the maximum supported operating temperature of the processor ($T_{J,max}$). It is the responsibility of software to convert the relative temperature to an absolute temperature. The temperature returned by the Digital Thermometer is always at or below $T_{J,max}$. Over temperature conditions are detectable via an Out Of Spec status bit. This bit is also part of the Digital Thermometer MSR. When this bit is set, the processor is operating out of specification and immediate shutdown of the system should occur. The processor operation and code execution is not guaranteed once the activation of the Out of Spec status bit is set.

The Digital Thermal Sensor (DTS) relative temperature readout corresponds to the thermal monitor (TM1/TM2) trigger point. When the DTS indicates maximum processor core temperature has been reached the TM1 or TM2 hardware thermal control mechanism will activate. The DTS and TM1/TM2 temperature may not correspond to the thermal diode reading since the thermal diode is located in a separate portion of the die and thermal gradient between the individual core DTS. Additionally, the thermal gradient from DTS to thermal diode can vary substantially due to changes in processor power, mechanical and thermal attach and software application. The system designer is required to use the DTS to guarantee proper operation of the processor within its temperature operating specifications

5.1.5 Out of Specification Detection

Overheat detection is performed by monitoring the processor temperature and temperature gradient. This feature is intended for graceful shut down before the THERMTRIP# is activated. If the processor's TM1 or TM2 are triggered and the temperature remains high, an "Out Of Spec" status and sticky bit are latched in the status MSR register and generates thermal interrupt.



5.1.6 PROCHOT# Signal Pin

An external signal, PROCHOT# (processor hot), is asserted when the processor die temperature has reached its maximum operating temperature. If the Intel Thermal Monitor 1 or Intel Thermal Monitor 2 is enabled (note that the Thermal Monitor 1 or Thermal Monitor 2 must be enabled for the processor to be operating within specification), the TCC is active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or deassertion of PROCHOT#. Refer to the *Intel® Architecture Software Developer's Manuals* for specific register and programming details.

In a dual core implementation, only a single PROCHOT# pin exists at a package level. When either core's thermal sensor trips, the PROCHOT# signal will be driven by the processor package. If only TM1 is enabled, PROCHOT# will be asserted and only the core that is above the TCC temperature trip point will have its core clocks modulated. If TM2 is enabled, then regardless of which core(s) are above the TCC temperature trip point, both cores will enter the lowest programmed TM2 performance state. It is important to note that Intel recommends both TM1 and TM2 be enabled.

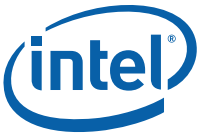
5.1.7 FORCEPR# Signal Pin

The FORCEPR# (force power reduction) input can be used by the platform to cause the processor to activate the TCC. If the Thermal Monitor is enabled, the TCC is activated upon the assertion of the FORCEPR# signal. The TCC remains active until the system deasserts FORCEPR#. FORCEPR# is an asynchronous input.

FORCEPR# can be used to thermally protect other system components. Using the VR as an example, when the FORCEPR# pin is asserted, the TCC circuit in the processor activates reducing the current consumption of the processor and the corresponding temperature of the VR. It should be noted that assertion of the FORCEPR# does not automatically assert PROCHOT#. As mentioned previously, the PROCHOT# signal is asserted when a high temperature situation is detected. A minimum pulse width of 500 µs is recommend when the FORCEPR# is asserted by the system. Sustained activation of the FORCEPR# pin may cause noticeable platform performance degradation.

5.1.8 THERMTRIP# Signal Pin

Regardless of whether or not Thermal Monitor is enabled, in the event of a catastrophic cooling failure, the processor automatically shuts down when the silicon has reached an elevated temperature (refer to the THERMTRIP# definition in Table 13). At this point, the system bus signal THERMTRIP# goes active and stay active as described in Table 13. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles.



6.0 Debug Tools Specifications

The ITP700 debug port connector is the recommended debug port for Dual-Core Intel® Xeon® Processor LV and ULV platforms. Refer to the *ITP700 Debug Port Design Guide* documentation for more information.

6.1 Logic Analyzer Interface (LAI)

Intel has worked with logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging systems with this processor. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of systems with this processor, the LAI is critical in providing the ability to probe and capture Front Side Bus signals. There are two sets of considerations to keep in mind when designing a system that can make use of an LAI: mechanical and electrical.

6.1.1 Mechanical Considerations

The LAI is installed between the processor socket and the processor. The LAI pins plug into the socket, while the processor pins plug into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the processor and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system.

6.1.2 Electrical Considerations

The LAI also affects the electrical performance of the FSB; therefore, it is critical to obtain electrical load models from each of the logic analyzers to be able to run system level simulations to prove that their tool works in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide.