Embedded Voltage Regulator-Down (EmVRD) 11.0
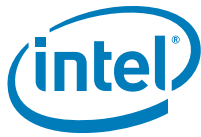
Design Guidelines for Embedded Implementations Supporting PGA478

January 2007

Order Number: 311395-005

Contents

Figures

Tables

Revision History

Date	Revision	Description
January 2007	005	• Added support for Intel® Celeron® Processor 1.83 GHz
November 2006	004	• Added support for Intel® Celeron® Processor 1.66 GHz information
August 2006	003	• Added support for Dual-Core Intel® Xeon® Processor ULV • Revised wording on VR11 PWM controller support for 10.x VID table • Revised Table 9 to include values
April 2006	002	Grammatical edits.
March 2006	001	Initial Public Release

1.0 Introduction

1.1 About This Document

This design guide defines the power delivery features necessary to support Intel processors' power delivery requirements for embedded computer applications using the following family of processors:

- Dual-Core Intel® Xeon® Processor LV
- Dual-Core Intel® Xeon® Processor ULV
- Intel® Celeron® Processor 1.66 GHz / 1.83 GHz

All references to "processor(s)" include all of the above processors unless specific exclusions are mentioned.

This includes design recommendations for DC to DC regulators, which convert the input supply voltage to a processor consumable voltage (V_{CC}) and additional specific feature set implementation, such as thermal monitoring and dynamic voltage identification.

EmVRD - The Embedded Voltage Regulator-Down (EmVRD) designation of this document refers to a regulator with all components mounted directly on the motherboard for intent of supporting a single embedded processor. For platforms supporting dual embedded processor designs, an additional EmVRD regulator will be required.

Note: This document does *not* describe the use of a Voltage Regulator Module (VRM), a modular pluggable converter.

The EmVRD 11.0 is based on the previous generation enterprise/server VRM/EVRD 10.x specification, but incorporates several functional changes. Hardware solutions for the voltage regulator are dependent upon the microprocessors to be supported in a specific motherboard. The EmVRD 11.0 is used to support the Dual-Core Intel® Xeon® Processor LV, and Dual-Core Intel® Xeon® Processor ULV and Intel® Celeron® Processor 1.66 GHz / 1.83 GHz family of processors.

The EmVRD 11.0 controller offers two modes of operation which allows it to incorporate all of the VRD 10.x and VRM/EVRD 10.x functions plus the following enhancements:

- Extended VRM/EVRD 10.x VID table with a seventh bit for 6.25 mV resolution, processor will only use VR11.0 VID mode
- Support for a second linear 8-bit VID table with 6.25 mV resolution, 1.6 V maximum VID, and minimum VID defined as 31.25 mV. The processor will only use 12.5 mV of VID resolution.
- New power-on sequence definition
- Load-line regulation tolerance of ±19 mV
- Integrated thermal monitor circuitry
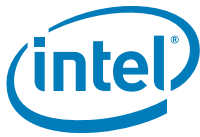
This document describes the following areas of implementation in support of the processor:

- Processor Load-Line
- Tolerance Band (TOB)
- Voltage and Current Requirements
- Bypass Capacitor Details
- Layout Considerations
- EmVRD Controller Details

This document does not describe the implementation of a enterprise/server VRM/EVRD 10.x or desktop VRD10.x compatible voltage regulator, because they are not compatible with this family of processors.

1.2 Terminology

Table 1. Glossary (Sheet 1 of 2)

Term	Description
σ	Sigma – standard deviation
AVP	Adaptive Voltage Positioning
D-VID	Dynamic Voltage Identification. A low power mode of operation where the processor instructs the EmVRD to operate at a lower voltage.
DAC	Digital to Analog Converter
DCR	Direct Current Resistance
ESL	Effective Series Inductance
ESR	Effective Series Resistance
FET	Field Effect Transistor
FORCEPR#	Under thermal monitoring, the EmVRD asserts this processor input to indicate an over-temperature condition has occurred. Assertion of this signal sets the processor in a low-power state, thereby cooling the voltage regulator.
FR4	A type of printed circuit board (PCB) material.
HVM	High Volume Manufacturing
V_{CC}	EmVRD output voltage or the processor's main input voltage.
I_{CC}	EmVRD output current or the processor's main input current.
VTT	Voltage Test Tool
Vtt	Processor Termination Voltage
Itt	Bus current associated with the V_{CCP} (Vtt) supply.
PGA478 Socket	The surface-mount Zero Insertion Force (ZIF) socket designed to accept several Intel processors, including the Dual-Core Intel Xeon processor LV family
RLL	A linear equation that describes a voltage to current relationship resulting in system impedance. The load-line equations is Vcc = VID − Icc*RLL +/- Offset, also known as Load Line Impedance
MLCC	Multi-Layer Ceramic Cap
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
OCP	Output Current Protection
OVP	Output Voltage Protection

Table 1.   Glossary (Sheet 2 of 2)
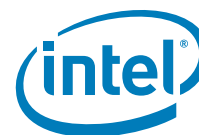
Term	Description
EMTS	A document that defines the processor electrical, mechanical, and thermal specifications. See your Intel representative for access to EMTS documents.
Processor Load Line	The ratio of voltage drop/current load as measured across the processor Vccsense and Vsssense pins. The Dual-Core Intel Xeon processor LV specifies the processor load-line value, RLL which incorporates a component the processor package, processor socket and the motherboard impedance. Load Line references in this document assume Processor Load Line in not explicitly noted otherwise.
PWM	Pulse Width Modulation, EmVRD voltage resultor controller
RDS-ON	MOSFET source to drain conduction resistance when biased
RSS	Root Sum Square. A method of adding statistical variables.
Socket Load Line	Processor Loadline minus the Package and Socket impedance = the motherboard impedance. The characteristic impedance of the motherboard power delivery circuit, in conjunction with high frequency decoupling, bulk decoupling, and power plane impedance. Design compliance to this parameter ensures that the processor motherboard voltage specifications minus the processor socket are satisfied.
Dual-Core Intel® Xeon® Processor LV, and Dual-Core Intel® Xeon® Processor ULV and Intel® Celeron® Processor 1.66 GHz / 1.83 GHz processor families	The embedded dual core, dual-processor/single-core, single processor (Intel® Celeron® Processor 1.66 GHz / 1.83 GHz) capable IA32 microprocessors.
Static Load Line	DC resistance at the defined regulation node. Defined as the quotient of voltage and current (V/I) under steady state conditions. This value is configured by proper tuning of the PWM controller voltage positioning circuit. In this document, the static load line is referenced at the socket unless otherwise stated.
TDC	Voltage Regulator Thermal Design Current. The sustained DC current the voltage regulator must support under the system defined cooling solution.
Thermal Monitor	A feature of the voltage regulator that sets the processor in a low power state when critical EmVRD temperatures are reached, thereby reducing power and EmVRD temperature.
TOB	Vcc regulation tolerance band. Defines the voltage regulator's $3*\sigma$ voltage variation across temperature, manufacturing variation, and age factors. Must be guaranteed by design through component selection. Defined at processor maximum current and maximum VID levels.
TOS	Time Overshoot
Dynamic Load Line	Transient Response equal to dV/di or Vdroop/Istep and is controlled by switching frequency, decoupling capacitor selection, and motherboard layout parasitics. In this document, the transient load line is referenced at the Vccsense and Vsssense unless otherwise stated.
V_{CCP}	Voltage provided to the processor to initiate power up and drive I/O buffer circuits
VID	Voltage Identification: A binary code supplied by the processor that determines the a reference output voltage to the EmVRD controller. At zero amperes and the tolerance band at $+ 3*\sigma$, VID is the voltage at the processor.
VOS	V_{CC} Overshoot
VRD	Desktop Voltage Regulator Down. A Desktop VR circuit resident on the motherboard.
VRM	Enterprise/Server Voltage Regulator Module that is socketed/pluggable to a motherboard.
EVRD	Enterprise/Server Voltage Regulator Down circuit resident on the motherboard.
EmVRD	Embedded Voltage Regulator Down. An Embedded VR circuit resident on the motherboard.
Vtt	See V_{CCP}

1.3 Related Documentation

Table 2. Related Documentation

Title	Location
Dual-Core Intel® Xeon® Processor LV and ULV Thermal Design Guide for Embedded Systems	http://www.intel.com/design/intarch/designgd/311374.htm
Dual-Core Intel® Xeon® Processor LV and ULV Datasheet	http://www.intel.com/design/intarch/datashts/311391.htm
Intel® Celeron® Processor 1.66 GHz / 1.83 GHz Datasheet	http://developer.intel.com/design/intarch/datashts/315876.pdf

2.0 Processor V$_{CC}$ Requirements

2.1 Voltage and Current

A six-bit VID code supplied by the processor to the EmVRD controller determines the reference output voltage as described in Section 6.1. The processor load lines in Section 2.2 show the relationship between V$_{CC}$ and I$_{CC}$ for the processor at the processor cores.

Intel performs exhaustive testing against multiple software applications and software test vectors to identify valid processor V$_{CC}$ operating ranges. Failure to satisfy the processor load line (RLL), load line tolerance band (TOB), and overshoot voltage specifications (VOS) as shown in Section 2.3 and Section 2.6 may invalidate Intel warranties and lead to premature processor failure, intermittent system lock-up (blue screen), and/or data corruption.

2.2 Processor Load Line Definitions

To ensure processor reliability and performance, platform static and dynamic voltage regulation must always be contained within the V$_{CCMAX}$ and V$_{CCMIN}$ processor load line boundaries (known as the load line window). Processor load line compliance must be guaranteed across 3*σ component manufacturing tolerances, thermal variation, and age degradation. Processor load line boundaries are defined by the equations in Table 3 and in conjunction with the processor design parameter values defined in Table 4. Load line voltage tolerance is defined in Section 2.3. In the equations in Table 3, VID, RLL, and TOB are known. Plotting V$_{CC}$ while varying I$_{CC}$ from 0 A to I$_{CCMAX}$ establishes the V$_{CCMAX}$ and V$_{CCMIN}$ processor load lines, see Figure 1. V$_{CCMAX}$ establishes the maximum DC processor load line boundary. Short AC transient bursts above the V$_{CCMAX}$ load line are permitted; this condition is defined in Section 2.6. V$_{CCMIN}$ establishes the minimum AC and DC voltage boundary.

Table 3.   Processor Load Line Equations

Processor Load Line	Equation
Equation 1. V$_{CCMAX}$ processor load line	$V_{CC} = VID + TOB - (RLL * I_{CC})$
Equation 2. V$_{CCTYP}$ processor load line	$V_{CC} = VID - (RLL * I_{CC})$
Equation 3. V$_{CCMIN}$ processor load line	$V_{CC} = VID - TOB - (RLL * I_{CC})$

Table 4. **V$_{CC}$ Regulator Design Parameters**

VR Configuration	I$_{CCMAX}$	Dynamic I$_{cc}$	RLL	TOB	Maximum VID	Minimum VID
Dual-Core Intel® Xeon® Processor LV	36 A	12.4 A	2.1 mΩ	19 mV	1.25	1.1125
Dual-Core Intel® Xeon® Processor ULV	19 A	5.7A	2.1 mΩ	19 mV	1.2125	1.0
Intel® Celeron® Processor 1.66 GHz / 1.83 GHz	36 A	12.4 A	2.1 mΩ	19 mV	1.275	1.1125

Figure 1. **Processor Load Line**
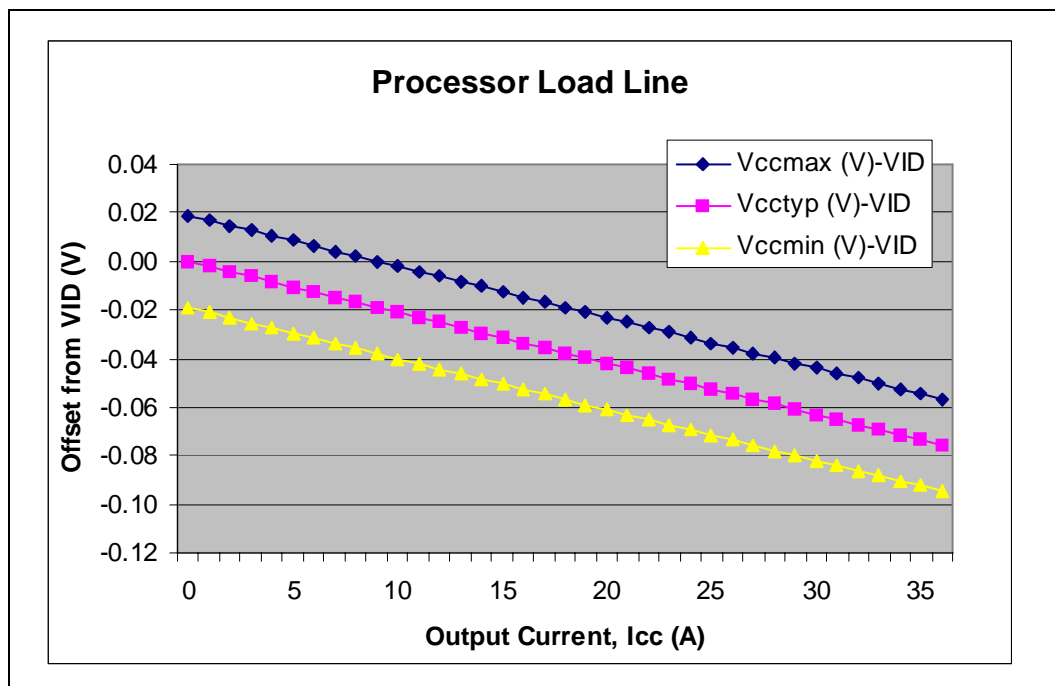
Notes:
1. Presented as a deviation from VID
2. Processor load line Slope = 2.1 mΩ, TOB = 19 mV
3. Dual-Core Intel® Xeon® Processor ULV IccMAX is limited to 19A and Intel® Celeron® Processor 1.66 GHz / 1.83 GHz is limited to 36A, consult Table 4 for maximum current values

A EmVRD transient processor load line circuit should be designed to meet or exceed rated conditions defined in Table 4. For example, the processor requires a processor load-line slope of 2.1 mΩ. A transient processor load line slope can vary from the static load-line, but it should always reside within the TOB range. However, the static load line condition must be set to the recommended value unless explicitly stated otherwise in the processor datasheet.

Figure 2. Processor Load Transient Limits
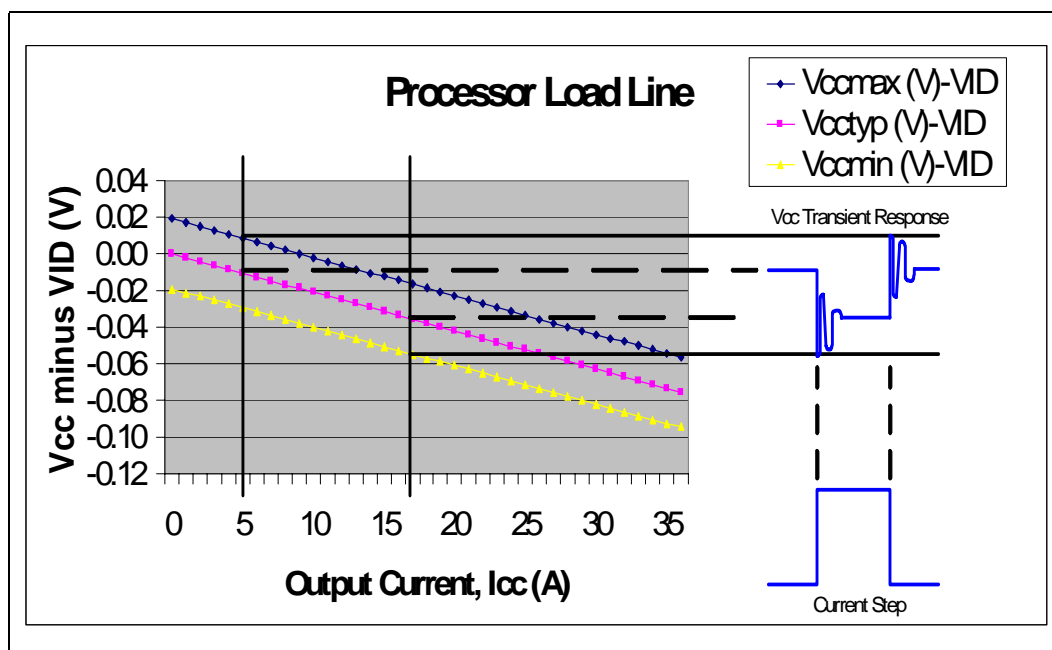
Operating at a low load-line resistance results in higher processor operating temperature, which can result in damage or a reduced processor life span. Processor temperature increases from higher functional voltages can lead to operation at low power states, which may force the platform to induce a reduction in processor performance. Operating at a higher load-line resistance results in minimum voltage violations which can result in system lock-up, "blue screening", or data corruption.

Table 4 lists the EmVRD voltage regulator design configuration intended to support the Dual-Core Intel Xeon processor LV. It is common for a motherboard to support processors that require different EmVRD configurations. In this case, the voltage regulator design must meet the specifications of all processors supported by that board. For example, if a motherboard is targeted to support this family of processors, the voltage regulator must have the ability to support the highest power requirements amongst the twothree processors in this family. Detailed processor configuration requirements are defined in the processor datasheets.

Figure 1 and Table 3 describe minimum and maximum voltage boundaries for each processor load line design configuration defined in Table 4. V_{CCTYP} processor load lines are provided for design reference. Designers should calibrate the processor load line to this case (centered in the load line window, at the mean of the tolerance band). The reader should not assume that processors with similar characteristics will have the same VID value. Typical values will range from 1.1 V to 1.5 V in 12.5 mV increments. A single load line chart and figure for each EmVRD design configuration can represent functionality for each possible VID value. Figure 1 and Table 3 presented as voltage deviation from VID provide the necessary information to identify voltage requirements at any reference VID. This avoids the redundancy of publishing tables and figures for each of the multiple cases.

Table 5.   Processor Load-Line Window

I$_{CC}$ (A)	V$_{CCMAX}$ (V)	V$_{CCTYP}$ (V)	V$_{CCMIN}$ (V)
0	0.019	0.000	-0.019
5	0.009	-0.011	-0.030
10	-0.002	-0.021	-0.040
15	-0.013	-0.032	-0.051
20	-0.023	-0.042	-0.061
25	-0.034	-0.053	-0.072
30	-0.044	-0.063	-0.082
35	-0.055	-0.074	-0.093
40	-0.065	-0.084	-0.103
45	-0.076	-0.095	-0.114

Notes:
1. Presented as a deviation from VID
2. Processor load line slope = 2.1 mΩ, TOB = 19 mV
3. Consult Table 4 for maximum current values
4. Consult Table 3 for linear equations for V$_{CC}$MAX, V$_{CC}$TYP, and V$_{CC}$MIN

Since each processor uses a processor load line, the voltage measurement points for accurate load line determination is at the processor V$_{CCSENSE}$ and V$_{SSSENSE}$ pins. The use of a BGA type socket for the processor would dictate that the load line measurements be taken on the back side of the circuit board on the vias connected to the sense signals.
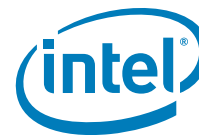
To properly calibrate the processor load line parameter, the EmVRD designer must excite the processor socket with a current step that generates a voltage response which must be checked against the load line window requirements as shown in Figure 2.

Table 6 identifies the steady state and transient current values to use for this calibration. For additional information, consult the processor load line calculator for the appropriate Intel processor.

Table 6.   Current Step Values for Transient Processor Load Line Testing

VR Configuration	Starting Current	Ending Current	Dynamic Current Step
Dual-Core Intel® Xeon® Processor LV	23.6 A	36 A	12.4 A
Dual-Core Intel® Xeon® Processor ULV	13.3A	19A	5.7 A
Intel® Celeron® Processor 1.66 GHz / 1.83 GHz	23.6 A	36A	12.4 A

EmVRD designs must be processor load-line compliant across the full tolerance band window to avoid data corruption, system lock-up, and reduced performance. When validating a system's processor load line, a single measurement is statistically insignificant and cannot represent the response variation seen across the entire high volume manufacturing population of EmVRD designs. A typical processor load line may fit in the specification window; although designs residing elsewhere in the tolerance band distribution may violate the specifications.

Example A in Figure 3 shows a load line that is contained in the specification window and in this instance, complies with V_{CCMIN} and V_{CCMAX} specifications. The positioning of this processor load line will shift up and down as the tolerance drifts from typical to the design limits.

Example B in Figure 3 shows that V_{CCMAX} limits will be violated as the component tolerances shift the load line to the upper tolerance band limits.

Example C in Figure 3 shows that the V_{CCMIN} limits will be violated as the component tolerances shift the load line to the lower tolerance band limits.

Figure 3.   Examples of High Volume Manufacturing Load Line Violations

Example A: This load line satisfies voltage limits, but will violate specifications as the VR TOB varies across the minimum to maximum range

Example B: Vccmax violation when component tolerance shift Load Line to the upper TOB limits

Example C: Vccmin violation when component tolerance shift Load Line to the lower TOB limits
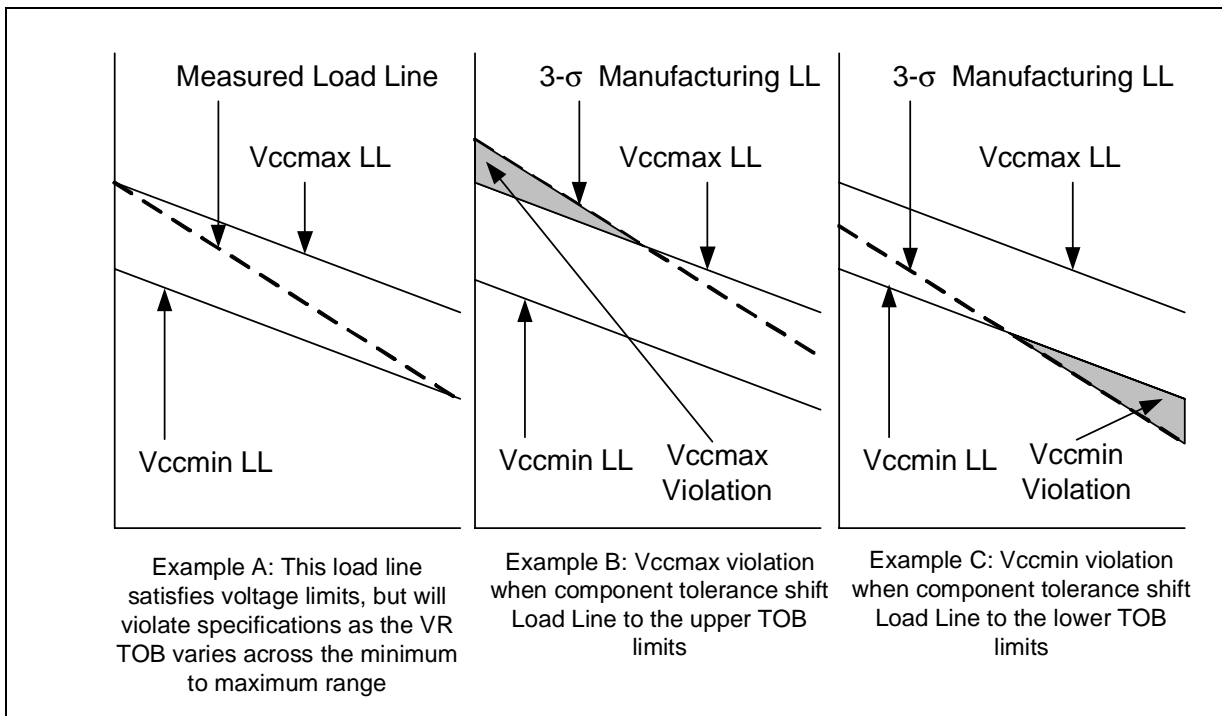
To satisfy specifications across high volume manufacturing variation, a typical processor load line must be centered in the load line window and have a slope equal to the value specified in Figure 3. Example A in Figure 4 shows a processor load line that meets this condition. Under full $3*\sigma$ tolerance band variation, the load line slope will intercept the V_{CCMIN} load line (Figure 4 Example B) or V_{CCMAX} load line (Figure 4 Example C) limits.

Figure 4. Examples of High Volume Manufacturing Compliant Load Lines

Example A: Measured load line satisfies slope specification and is centered in the LL window

Example B: When component tolerances shift the load line to the lower TOB limits, the 3-σ manufacturing LL is bounded by the Vccmin LL

Example C: When component tolerances shift the load line to the upper TOB limits, the 3-σ manufacturing load line is bounded by the Vccmax LL
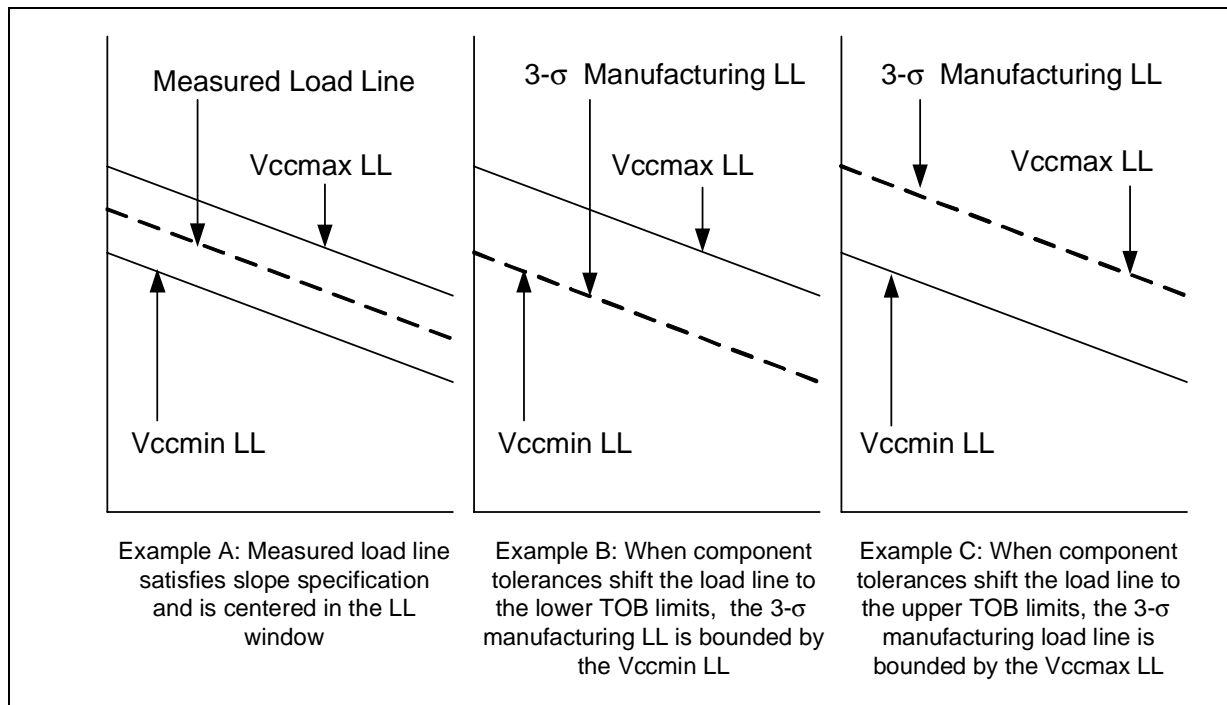
2.3 Voltage Tolerance Band (TOB)

Processor load line specifications must be guaranteed across component process variation, system temperature extremes, and age degradation limits. The EmVRD topology and component selection must maintain a $3*\sigma$ tolerance of the EmVRD Tolerance Band around the typical load line. The critical parameters include voltage ripple, EmVRD controller tolerance, and current sense tolerance under both static and transient conditions. Individual tolerance components vary among designs; the processor requires only that the total error stack-up stay within the defined EmVRD configuration tolerance band under the conditions defined in Table 4.

2.3.1 EmVRD Controller Requirements

The vendor for the chosen EmVRD controller, typically a pulse width modulator controller (PWM) should publish data and collateral that is critical for satisfying design requirements. This includes support of the following:

- The controller vendors are to define equations for calculating the EmVRD TOB with Inductor DCR for current sensing and/or output series resistor sensing. The equations are to include all parameter dependencies such as adaptive voltage positioning (AVP) tolerances, age degradations, thermal drifts, sense element's DC and AC accuracy, etc. under $3*\sigma$ variation. These equations should be published in the controller datasheet. The vendor is to distribute and support a tolerance band calculator that communicates the voltage regulator TOB for each valid VID.

- Total controller DC set point accuracy is to be <0.5% over temperature, component age, and lot to lot variation over the 1.0 – 1.5 V VID range. DAC accuracy may be larger for voltages below 1V under the assumption that the required Vmin TOB requirements are always satisfied. Typical low voltage accuracy is ±5 mV for 0.8 V – 1.0 V and ±8 mV < 0.8 V. Each vendor is to publish their controller DAC accuracy by VID value in the component datasheet.

- The controller should support voltage amplitudes read across sense elements with a DCR of 0.1 – 2.0 mΩ. Controller vendors should define the minimum sense signal voltage necessary to satisfy their controller signal to noise ratio requirements. These requirements are to be published by the vendor in their controller datasheet.

- Vendors should establish an inductor DCR sense topology that supports a ±19 mV TOB @ 1.25 VID, 36 A I_{CCMAX}, 2.1 mΩ processor load line slope including voltage ripple. The topology and component values are to be published in the controller datasheet.

2.3.2   Dynamic Voltage Identification (D-VID) TOB

During the D-VID mode of operation (see Section 2.5), EmVRD minimum voltage tolerance band requirements must be satisfied. The minimum voltage cannot fall below the values predicted by Equation 3 assuming any possible VID setting along with the RLL at TOB values defined in Table 3. Dynamic VID max/min limits are expanded during VID transition and are a function of the starting VID and the final VID.

For low to higher VID transitions, the max/min limits can be calculated by:

- $V_{CC}START\_LOWER\_TOB = VIDSTARTING - RLL*Icc - TOB$
- $V_{CC}FINAL\_UPPER\_TOB = VIDFINAL - RLL*Icc$

For high to low VID transitions, the max/min limits are calculated by:

- $V_{CC}START\_UPPER\_TOB = VIDSTARTING - RLL*Icc$
- $V_{CC}FINAL\_LOWER\_TOB = VIDFINAL - RLL*Icc - TOB$

V_{CCMAX} EmVRD TOB can be relaxed during dynamic VID. Positive tolerance variation is permitted and is to be bounded by the voltages predicted by Equation 1 in Table 3, where VID is the standard VID value in regulation when not in the D-VID mode.

2.3.3   Ripple Voltage

To meet tolerance band specifications, high and low frequency ripple is to be limited to 10 mV peak-to-peak. Measurements must be taken carefully to ensure that superposition of high frequency with low frequency oscillations do not sum to a value greater than 10 mV peak-to-peak. Measurements are to be taken with a 20 MHz band limited oscilloscope. Ripple is to be measured under both VTT and processor loading conditions. VTT testing is to be performed at 5 A minimum loading and at VR_TDC.

Processor testing is to be evaluated while running the *MaxPower* application and with the operating system in an idle state with no other applications running.

Contact your Intel field sales representative for the version of *MaxPower* that applies to this processor family.

2.3.4   Sense Topology Requirements

EmVRD designers must construct a sense topology that guarantees compliance to tolerance band specifications under standard operation and under the D-VID mode of operation. This includes selection of sense elements and supporting components that satisfy tolerance requirements with the chosen EmVRD controller and ripple amplitude.

Inductor DCR or resistor current sensing topologies are required to satisfy tolerance band requirements. Current sensing across MOSFET RDSon is not recommended for load line AVP functions due to the large variation in this parameter. Evaluation of this sense method has shown that the TOB requirements cannot be satisfied unless expensive <10% tolerance MOSFETs are chosen.

2.3.5 Error Amp Specification

The EmVRD controller chosen should provide an error amp with a sufficient gain BW product to ensure duty cycle saturation does not occur with large signal current transients. Typical target closed loop VR bandwidths of 30-200 kHz (20% of switching frequency target) are expected in EmVRD 11.0 system designs. The output of the error amp should also have high slew rates to avoid duty cycle saturation. Performance limitations must be included in the EmVRD TOB equations.

2.4 Stability

The EmVRD chosen should be unconditionally stable under all DC and transient conditions across the voltage and current ranges defined in Table 4 and Figure 1. The EmVRD must also operate in a no-load condition: i.e., with no processor installed. Normally the no-processor VID code will be 00000, disabling the EmVRD output voltage.

2.5 Dynamic Voltage Identification

2.5.1 Dynamic-Voltage Identification Functionality

EmVRD 11.0 architecture includes the Dynamic Voltage Identification (D-VID) feature set, which enables the processor to reduce power consumption and processor temperature. Reference VID codes are dynamically updated by the processor to the EmVRD controller via the VID bus when a low power state is initiated. VID codes are updated sequentially in 12.5 mV steps and are transmitted every 5 microseconds until the final voltage code is encountered. Intel processors are capable of transitioning from standard operational VID levels to the EmVRD 11.0 table minimum values. They are also capable of returning to a higher VID code in a similar manner. The low voltage code will be held for a minimum of 50 microseconds prior to sequentially transitioning through the VID table to a new voltage reference which can be any higher VID code, but is generally the original reference VID.

Figure 5 illustrates processor-operating states as the VID level is lowered. The diagram assumes steady state, maximum current during the transition for ease of illustration. In this figure, the processor begins in a high-load condition. Upon entering D-VID, the processor will shift to a low power state and stop executing code (sequence 1 => 2). After reaching state 2, the processor encounters a brief delay to prepare for low power operation then re-initiates code, resulting in current draw and a load line IR drop to state 3. Sequencing from state 3 to 4 is a simplification of the multiple steps from the original VID load line window to the low-voltage VID window. Transition from state 4 to state 5 is an example of a load change during normal operation in the low voltage VID setting. Transition from a low to high VID reference follows the reverse sequence.

During a D-VID transition, V_{CC} must always reside above the minimum load line of the current VID setting (see Figure 5). The load line values of each VID increment are required to match the slope defined in Table 4. In addition, the voltage tolerance band and ripple specifications defined in Table 4 and Section Voltage Tolerance Band (TOB) must be satisfied in this state. To expedite power reduction and processor cooling, the EmVRD must lower the maximum V_{CC} value to reside within the low voltage VID window within 50 microseconds of the final VID code transmission (see Figure 5). The EmVRD must respond to a transition from low VID to high VID by regulating the V_{CC} output to the range defined by the new VID code within 50 microseconds of the final code transmission. Note: the minimum VID is not constant among all processors; the value will vary with frequency and standard VID settings. This results in numerous possible D-VID states. A simple and direct D-VID validation method is defined at the end of this section.

During a D-VID event, the processor load may not be capable of absorbing output capacitor energy when the VID reference is lowered. As a result, reverse current may flow into the AC-DC regulator's input filter, potentially charging the input filter to a voltage above the over voltage value. Upon detection of this condition, the AC-DC regulator will react by shutting down the AC-DC regulator supply voltage. The EmVRD and AC-DC filter must be designed to ensure this condition does not occur. In addition, reverse current into the AC-DC regulator must not impair the operation of the EmVRD, the AC-DC supply, or any other part of the system.

Under all functional conditions, including D-VID, the Vcc supply must satisfy load line and overshoot constraints to avoid data corruption, system lock-up events, or system blue-screen failures.

Figure 5.   Processor D-VID Load Line Transition States
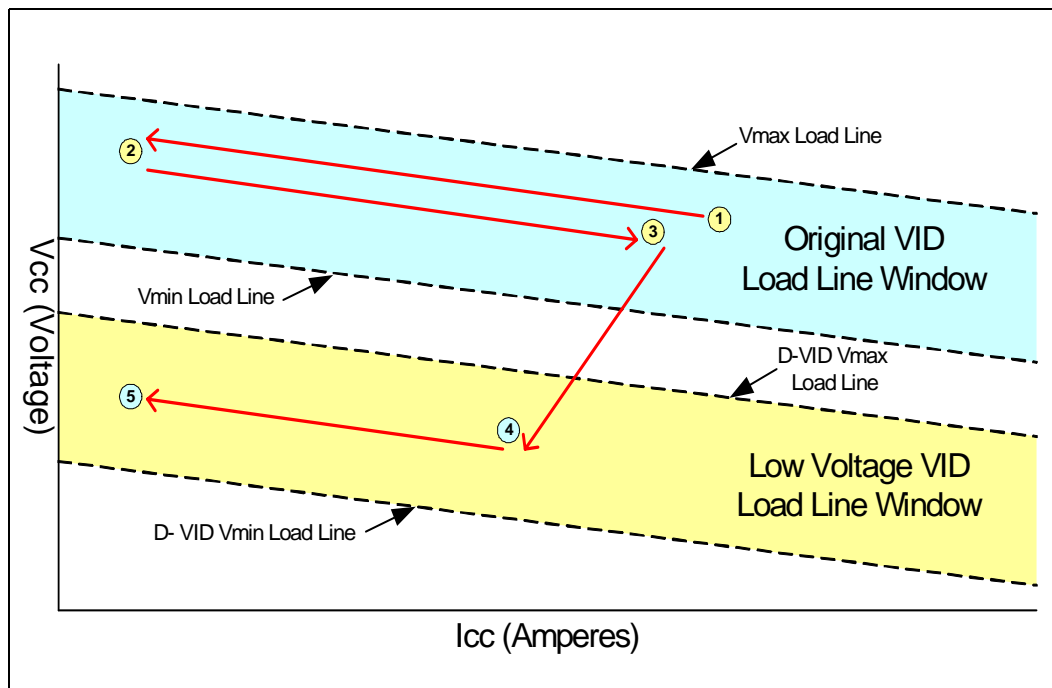
2.5.2   D-VID Validation

Note: Performance tests and ratings are measured using specific computer systems and/or components and reflect the approximate performance of Intel products as measured by those tests. Any difference in system hardware or software design or configuration may affect actual performance. Buyers should consult other sources of information to evaluate the performance of systems or components they are considering purchasing. For more information on performance tests and on the performance of Intel products, visit Intel Performance Benchmark Limitations.

Intel processors are capable of generating numerous D-VID states and the EmVRD must be designed to properly transition to and function at each possible VID voltage. However, exhaustive validation of each state is unnecessary and impractical. Validation can be simplified by verifying the EmVRD conforms to processor load line requirements, tolerance band specifications, and D-VID timing requirements. Then, by default, each processor D-VID state will be valid. The key variables for V_{CC} under D-VID conditions are processor loading, starting VID, ending VID, and V_{CC} slew rate. The V_{CC} slew rate is defined by EmVRD bulk decoupling, the output inductors, the switching FET resistance and the processor load. This indicates that the V_{CC} slewing will have an exponential behavior, where the response to code 'n+1' takes longer to settle than code 'n'. As a result, a test from maximum to minimum and from minimum to maximum will be sufficient to guarantee slew rate requirements and VID code regulation.

To ensure support for any valid VID reference, testing should be performed from the maximum EmVRD 11.0 voltage of 1.5 V to the minimum VID table value. For Embedded VR11, use 0.825 V for the minimum value.

The EmVRD must ensure that the full table transition occurs within 50 microseconds of the final VID code transmission. Slew rate timing is referenced from 0.4 V on the rising edge of the initial VID code to the time the final voltage is settled within 5 mV of the final Vcc value. Intel testing has noted a 10% change to the V_{CC} slew rate between EmVRD no load (5 A) and full load (VR_TDC) conditions. For this reason, the V_{CC} slewing must be tested under both loading conditions.

During the D-VID test defined in the previous paragraph, V_{CC} droop and undershoot amplitudes must be limited to avoid processor damage and performance failures. If the processor experiences a voltage undershoot due to D-VID transitions, an application initiated di/dt droop can superimpose with this event and potentially violate minimum voltage specifications. Droop during this D-VID test must be limited to 5 mV. This value was derived by calculating EmVRD tolerance band improvements at the low D-VID current and voltage values. If the processor experiences an overshoot due to D-VID transitions, an application initiated di/dt overshoot can superimpose with this event and potentially violate overshoot specifications. Overshoot is permitted, but must be properly budgeted with respect to the specifications defined in Section 2.6. Superposition of the dynamic VID overshoot event and the overshoot resulting from the transient test defined in Section 2.6, must not exceed the amplitude and time requirements defined in the overshoot specification.

2.5.2.1   VR11 Validation Summary

This exercise tests the EmVRD 11.0 functionality with 12.5 mV VID resolution. The use of the Voltage Test Tool (VTT) is recommended to provide the synthetic loads and D-VID control. Consult Figure 6 and Figure 7 for graphic representation of validation requirements.

1. Constraints:

    a. The 662.5 mV +/-5 mV transition must occur within 315 s (see Figure 6).

    b. Start time is referenced to 0.4 V on the rising edge of the initial D-VID code.

    c. End time is referenced to the steady state Vcc voltage after the final D-VID code.
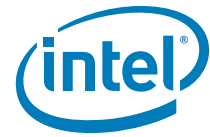
d. Undershoot during maximum to minimum VID transition must be limited to 5 mV. This 5 mV is included within the +/-5 mV tolerance on the final VID value defined under test condition A.

e. Overshoot observed when transitioning from minimum to maximum VID must conform to overshoot specifications. Specifically, superposition of the dynamic VID overshoot event and the overshoot resulting from the transient test defined in Section 2.6 must not exceed the overshoot amplitude and time requirements defined in the overshoot specification.

f. Care must be taken to avoid motherboard and component heat damage resulting from extended operations with high current draw.

2. Validation exercises:

a. D-VID transition must be validated against above constraints from a starting VID of 1.5 V to an ending VID of 0.8375 V with an applied 5 A Load.

b. D-VID transition must be validated against above constraints from a starting VID of 1.5 V to an ending VID of 0.8375 V with an applied VR_TDC Load.

c. D-VID transition must be validated against above constraints from a starting VID of 0.8375 V to an ending VID of 1.5 V with an applied 5 A Load.

d. D-VID transition must be validated against above constraints from a starting VID of 0.8375 V to an ending VID of 1.5 V with an applied VR_TDC Load.

Figure 6.   EmVRD 11.0 D-VID Transition Timing States (12.5 mV VID Resolution)
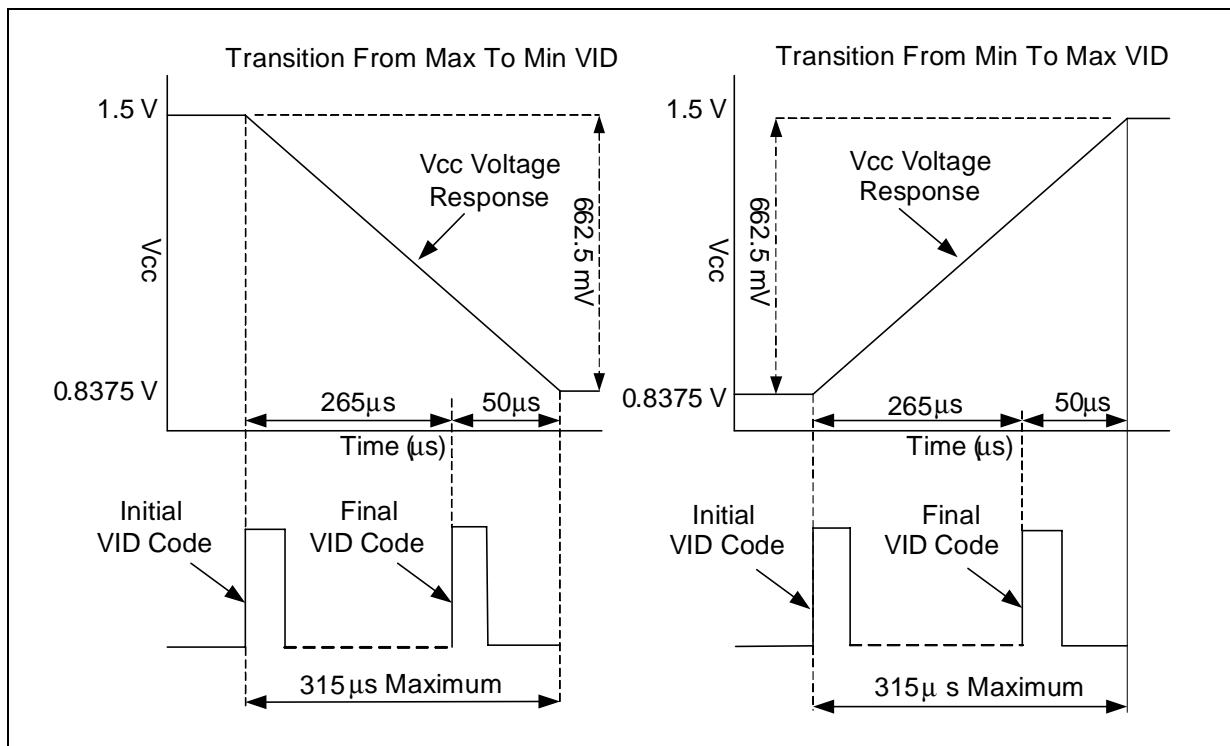
Figure 7. Overshoot and Undershoot During Dynamic VID Validation
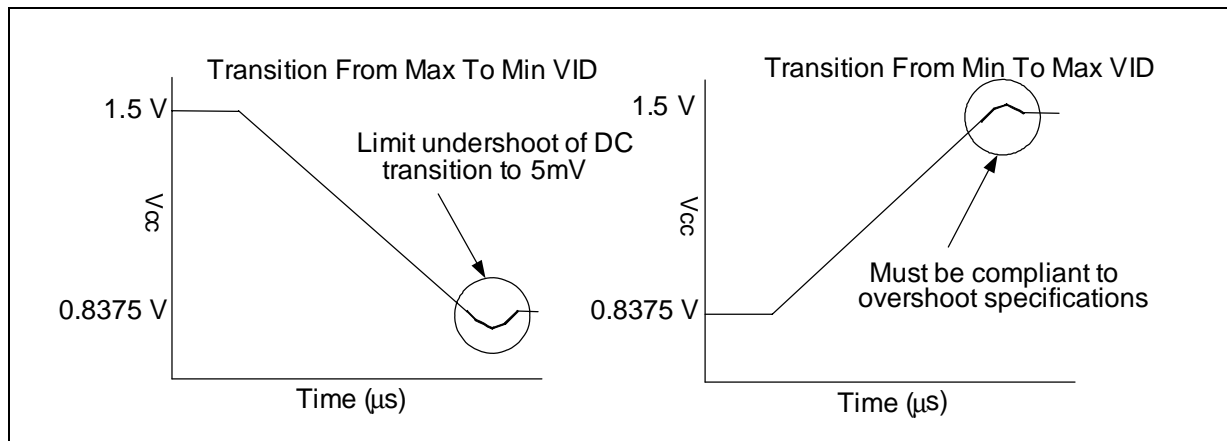
Table 7. D-VID Validation Summary Table

Parameter	Minimum	Typical	Maximum
VID	0.8375 V	-	1.5000 V[1]
Voltage Transition	0.6575 V	0.6625 V	0.6675 V
Transition Time	-	-	315s[2]
Current Load	5A	-	VR_TDC

Notes:
1. The absolute maximum core voltage for Dual-Core Intel® Xeon® Processor LV is 1.5 V. The maximum voltage supported by the VR11 specification is 1.6V.
2. Time is measured from 0.4 V on rising edge of the first D-VID input code to the convergent Vcc voltage value after the final D-VID code is transmitted. Includes 50 us for final code settling.
3. Please see the Datasheet for nominal voltage values.

2.6 Processor V$_{CC}$ Overshoot

2.6.1 Specification Overview

Intel embedded processors in EmVRD 11.0 systems are capable of tolerating short transient overshoot events above VID on the Vcc supply that will not impact processor life span or reliability. Maximum processor Vcc overshoot, VOS, cannot exceed VID+VOS-MAX. Overshoot duration, TOS, cannot stay above VID for a time more than TOS-MAX. See Table 9 and Table 10 for details.

Table 8.   **V$_{CC}$ Overshoot Terminology**

Parameter	Definition
VOS	Measured peak overshoot voltage
VOSMAX	Maximum specified overshoot voltage allowed above VID
TOS	Measured overshoot time duration
TOSMAX	Maximum specified overshoot time duration above VID
Vzc	Zero current voltage: The voltage where the measured load line intercepts the voltage axis
Vzco	Zero current offset from VID: Vzco = VID – Vzc

Table 9.   **V$_{CC}$ Overshoot Specifications**

Parameter	Specification
VOS_MAX	mV
TOS_MAX	µs
VOS	Maximum = VID + VOS_MAX
TOS	Maximum = TOS_MAX

Maximum overshoot is validated by monitoring the voltage across the recommended test pins (defined in Section 2.2) while applying a current load release across the socket V$_{CC}$ and V$_{SS}$ pin field. Amperage values for performing this validation under each EmVRD design configuration are identified in Table 6. The platform voltage regulator output filter must be stuffed with a sufficient quality and number of capacitors to ensure that overshoot stays above VID for a time no longer than TOS_MAX and never exceeds the maximum amplitude of VID+VOS_MAX. Measurements are to be taken using an oscilloscope with a 20 MHz bandwidth. Boards in violation must be redesigned for compliance to avoid processor damage.

Table 10.   **Intel Processor Current Release Values for Overshoot Testing**

VR Configuration	Starting Current	Ending Current	Dynamic Current Step
Dual-Core Intel® Xeon® Processor LV	23.6 A	36 A	12.4 A
Dual-Core Intel® Xeon® Processor ULV	13.3A	19A	6.6 A
Intel® Celeron® Processor 1.66 GHz / 1.83 GHz	23.6 A	36 A	12.4 A

To prevent processor damage, EmVRD designs should comply to overshoot specifications across the full processor load line tolerance band window (see Section 2.2). When validating a system's overshoot, a single measurement is statistically insignificant and cannot represent the response variation seen across the entire high volume manufacturing population of EmVRD designs. A typical design may fit in the processor load line window; however designs residing elsewhere in the tolerance band distribution may violate the V$_{CC}$ overshoot specifications. Figure 8 provides an illustration of this concept.

A typical board will have the Vcc zero current voltage (Vzc) centered in the processor load line window at VID-TOB; for this example consider waveform A and assume TOB is 20 mV. Now assume that the EmVRD has maximum overshoot amplitude of VOS_MAX = 50 mV above VID. Under this single case, the overshoot aligns with the specification limit and there is zero margin to violation. Under manufacturing variation Vzc can drift to align with VID (waveform B). This drift will shift the overshoot waveform by the

same voltage level. Since waveform A has zero overshoot amplitude margin, this increase in Vzc due to manufacturing drift will yield a 20 mV overshoot violation which will reduce the processor life span. To address this issue in validation, a voltage margining technique can be employed to ensure overshoot amplitudes stay below a safe value. This technique translates the specification baseline from VID to a EmVRD validation baseline of Vzc + VOS_MAX, which defines a test limit for specification compliance across the full TOB range:

Equation 4. Overshoot Voltage Limit

$$VOS < Vzc + VOS\_MAX$$

Equation 4 is to be used during validation to ensure overshoot is in compliance to specifications across high volume manufacturing variation. In addition, the overshoot duration must be referenced to Vzc and cannot exceed this level by more than 25 µs.

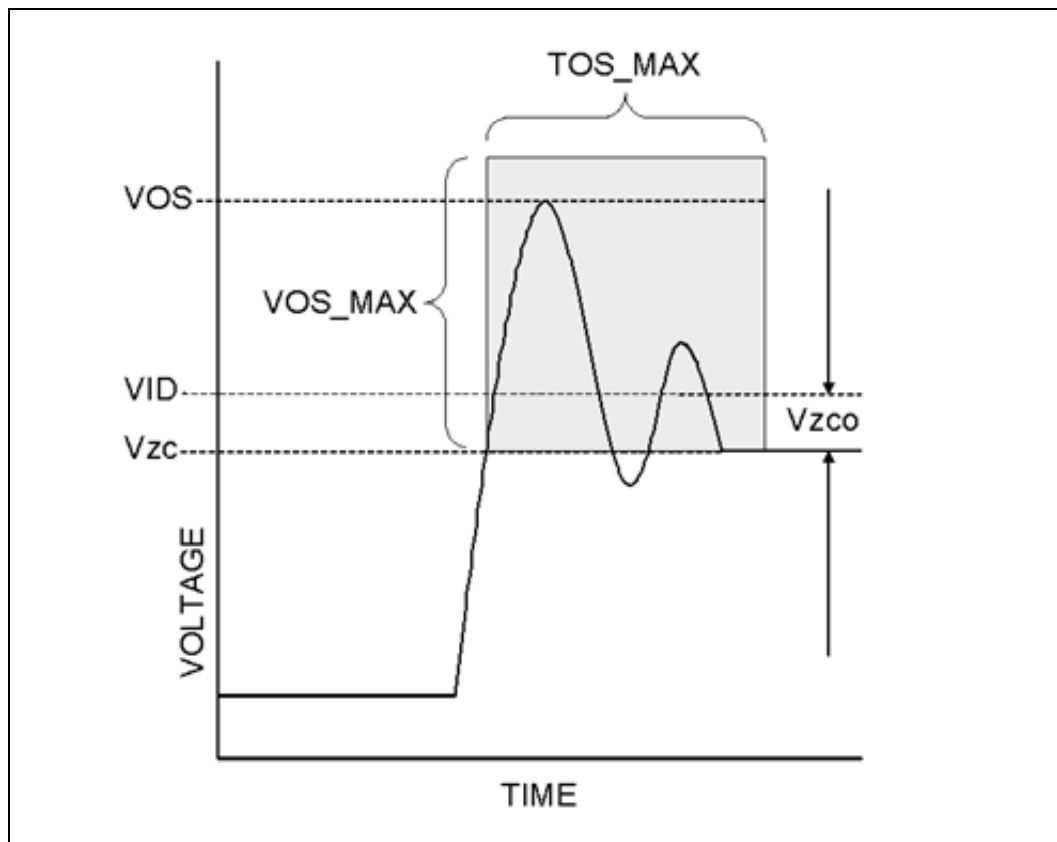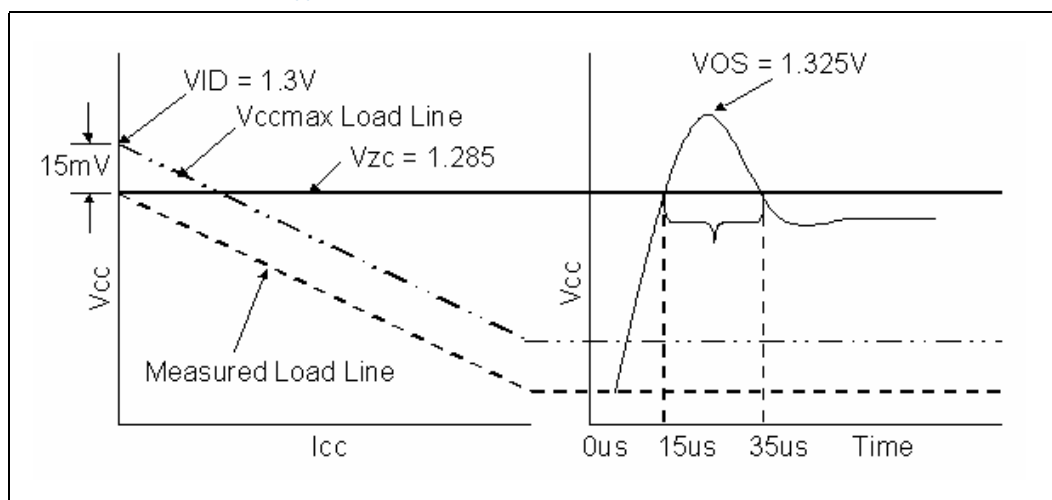**Figure 8. Graphical Representation of Overshoot Parameters**

Figure 9.   Example Processor V$_{CC}$ Overshoot Waveform

2.6.2   Example: Processor V$_{CC}$ Overshoot Test

To pass the overshoot specification, the amplitude constraint of Equation 4 and time duration requirement of TOS_MAX must be satisfied. This example references Figure 9.

Amplitude Test Constraint: Overshoot amplitude, VOS, must be less than Vzc + VOS_MAX

Input parameters:

- VOS= 1.325V: Obtained from direct measurement
- VZC = 1.285V: Obtained from direct measurement
- VOS_MAX = 0.050V: An Intel specified value

Amplitude Analysis:

- VZC + VOS_MAX = 1.285 V + 50 mV = 1.335 V
- VOS = 1.325 < 1.335 V

Amplitude Test Satisfied:

- Time Duration Test Constraint: Overshoot duration above Vzc must be less than 25 µs

Input Parameters:

- Initial crossing of overshoot: 15 µs: Obtained from direct measurement
- Final crossing of overshoot: 35 µs: Obtained from direct measurement
- TOS_MAX = 25 µs: An Intel specified value

Overshoot Duration Analysis:

- TOS = Final Crossing of Vzc: Initial Crossing of Vzc
- TOS = 35 µs − 15 µs = 20 µs < 25 µs = TOS_MAX

Time duration test passed:

- Amplitude and Time Duration Tests Passed => Overshoot specification is satisfied

Note: EmVRD processor load line calibration with the VTT does not guarantee adequate high frequency decoupling to reduce package noise. This noise is directly dependent upon the processor core frequency, so the filter must guarantee adequate decoupling to support all frequencies the board is to support.

Table 11.   Board Decoupling Requirements per CPU

Bypass Caps	Value	Quantity	ESR	ESL	Style	Notes
High Frequency	22 µF	30	3 mΩ	700 pH	0805 Package	Ceramic
Bulk	330 µF	6	9 mΩ	1.8 nH	3 pin SMT	Poscap

3.0 V_{CCP} Requirements

The V_{CCP} regulator provides power to the processor VID pull-up resistors, the chipset - processor front side bus, and miscellaneous buffer signals. This rail voltage must converge to the amplitude defined in Table 9 to begin power sequencing. The EmVRD controller will sense the amplitude of the V_{CCP} rail and initiate power sequencing upon crossing a defined threshold voltage. The V_{CCP} regulator controller start up can be inhibited until various system checks can be verified, usually by way of discrete logic. In a dual-processor design this could include ensuring a boot processor is installed. Once the V_{CCP} regulator is allowed to start, valid output voltage of Table 9 must be guaranteed by the timing protocol defined in Figure 10.

Note: Note: V_{CCP} is often referred to as V_{TT} on other Intel Processors.

3.1 Electrical Specifications

If a system design will use only one embedded processor a linear regulator is recommended for the V_{CCP} supply. If the system design will use two embedded processors, a switching regulator is recommended. With either supply method, the design must have adequate decoupling capacitors to ensure the sum of AC bus noise and DC tolerance satisfies limits identified in Table 9. The processor and chipset V_{CCP} supply must be maintained within these tolerance limits across full operational thermal limits, part-to-part component variation, age degradation, and regulator accuracy. Full bandwidth bus noise amplitude must be guaranteed across all V_{CC}/V_{SS} pin pairs defined in Table 10.

The V_{CCP} supply must be unconditionally stable under all DC and transient conditions across the voltage and current ranges defined in Table 9. The V_{CCP} supply must also operate in a no-load condition: i.e., with no processor installed.

Table 12.   V$_{CCP}$ Specifications

Number of CPU Sockets	Processor	V$_{CCP}$ Min	V$_{CCP}$ Typ	V$_{CCP}$ Max	Itt Min[1]	Itt Max[2]	Itt Max[3]
One Socket Design[2]	Dual-Core Intel® Xeon® Processor LV, and Dual-Core Intel® Xeon® Processor ULV and Intel® Celeron® Processor 1.66 GHz / 1.83 GHz	0.9975 V	1.05 V	1.1025 V	0.15 A	6 A	2.5 A
Two Socket Design[2]	Dual-Core Intel® Xeon® Processor LV and Dual-Core Intel® Xeon® Processor ULV and Intel® Celeron® Processor 1.66 GHz / 1.83 GHz	0.9975 V	1.05 V	1.1025 V	0.3 A	12 A	5 A

Notes:
1.   These values are pre-silicon estimates and are subject to change.
2.   Before V$_{CC}$ is stable.
3.   After V$_{CC}$ is stable.
4.   Includes the MCH and other circuitry.
5.   Itt and I$_{CCP}$ are synonymous.

Table 13 lists test pins for V$_{CCP}$ at the processor and Intel® E7520 Chipset.

Table 13.   V$_{CCP}$ Measurement Pins

Device	Supply	Pins
Processor	V$_{CCP}$	AF26
Processor	Vss	AE26
Intel® E7520 Chipset	V$_{CCP}$ (V$_{TT}$)	A31
Intel® E7520 Chipset	V$_{SS}$	B32

3.2   V$_{CCP}$ Bypass Recommendations

The values and placement recommendations for the V$_{CCP}$ decoupling capacitors are in Table 14. These values and quantities are for a switching regulator. In all cases the capacitors should be placed as close as possible to the device.

Table 14.   V$_{CCP}$ Bypass Capacitors TD7: Regulation to Power Down Delay

Cap Location	CPU Socket	MCH	Regulator
0.1 uF	8	4	2
330 uF	1	1	1

4.0 Power Sequencing

EmVRD 11.0 features a power sequence that is compatible with both VR11 and VR10 processors. To avoid compatibility problems with VR11 architecture, EmVRD 11.0 systems must not use the legacy VR10 start sequence.

Embedded VR11 systems can use a pull-up resistor tied to the V_{CCP} supply as an enable signal or provide additional sequencing or check circuits before enabling. Once the PWM V_{CC} voltage is above its UVLO threshold and out of reset or configuration states and a valid enable signal is received, the PWM can initiate the start up sequence with TD1.

The EmVRD should ramp V_{CC} to the default 'Vboot' value and start its internal timer. It will remain at the Vboot voltage during TD3 and then read in the VID lines and ramp to the VID programming voltage. Vboot is a DC voltage state with no load line or AVP function. See timing diagram Figure 12 for details on the power-on sequence requirements.

4.1 VR_ENABLE

VR_ENABLE pin is a level sensitive logic input that is externally pulled up to the front side bus termination voltage rail (V_{CCP}) rail in the system. The threshold for turn on is 0.85 V +/- 50 mV with a 100 mV +/- 30 mV hysteresis. The VR_ENABLE input should have a 3 dB bandwidth of approximately 20 MHz to reject high frequency noise. If enable goes low during the start up sequence the EmVRD should re-start the start up sequence.

When VR_ENABLE is pulled low or disabled, VR_READY should be de-asserted and the DC-DC output should be in a high-impedance state and should not sink current. During the shut down process, no negative voltage below −100 mV may be present at the DC-DC output when loaded with a resistive load or microprocessor in the system. Some electronic loads with long leads may cause false readings at turn off.

4.2 Vboot Voltage Level

Vboot is a default power-on V_{CC} value. Upon detection of a valid Vccp supply, the EmVRD controller is to regulate the output to this value until VID codes are read. The Vboot voltage is 1.1 V. During Vboot, the output should operate with no load line and as if the VID code represents 1.1 V.

4.3 Under Voltage Lock Out (UVLO)

The EmVRD controller should detect the V_{CC} input and remain in the disabled state until valid V_{CC} level is available or reached. Typically 3.0 V in a 3.3 V system, 4.0 V in a 5 V system or 7 V to 8 V in a 12 V system. Ultimately the controller vendor should set the level to meet applicable market segment requirements. However, the controller and driver chips (in not integrated in the controller) should coordinate start up such that both the EmVRD V_{CC} and power conversion rail (typically +12 V) of the buck converter are both up and valid prior to enabling the controller function. The controller and driver combination need to be tolerant of any sequencing combination of 3.3 V, 5 V or 12 V

input rails. If either the Vcc or power conversion rail fall below the UVLO thresholds, the controller should shut down in an orderly manner and restart the start up sequence.

4.4 Soft Start (SS)

The EmVRD controller will have a soft start function to limit inrush current into the output capacitor bank and prevent false over current protection (OCP) trips. The soft start should have a ramp of 500 s as an internally programmed default. A SS pin for user programmability of SS ramp to extend the ramp to 1-5 ms is required. Consult TD2 and TD4 parameters in Figure 10 and Section 15 for further details.

Figure 10.   Start-Up Sequence
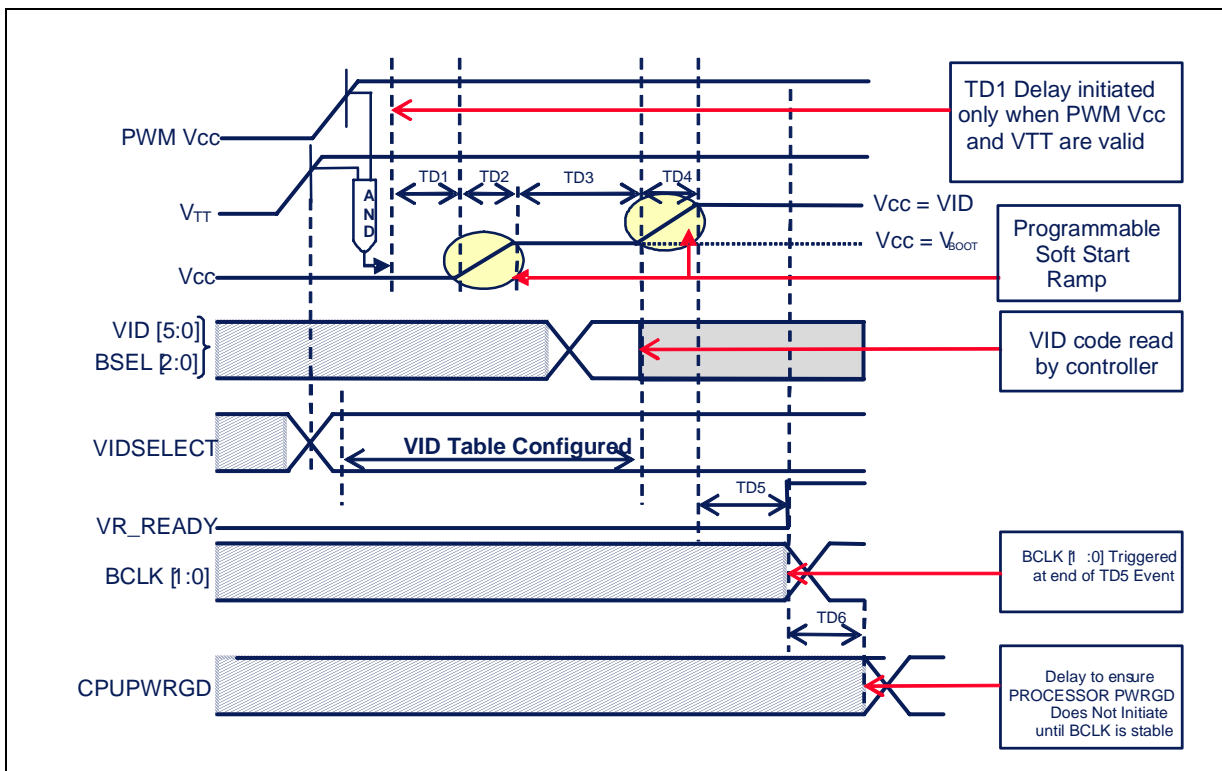
Notes:
1.   TD2, TD4 voltage slopes are determined by soft start logic.
2.   Timing not to scale.

Figure 11. Power-Off Timing Sequence
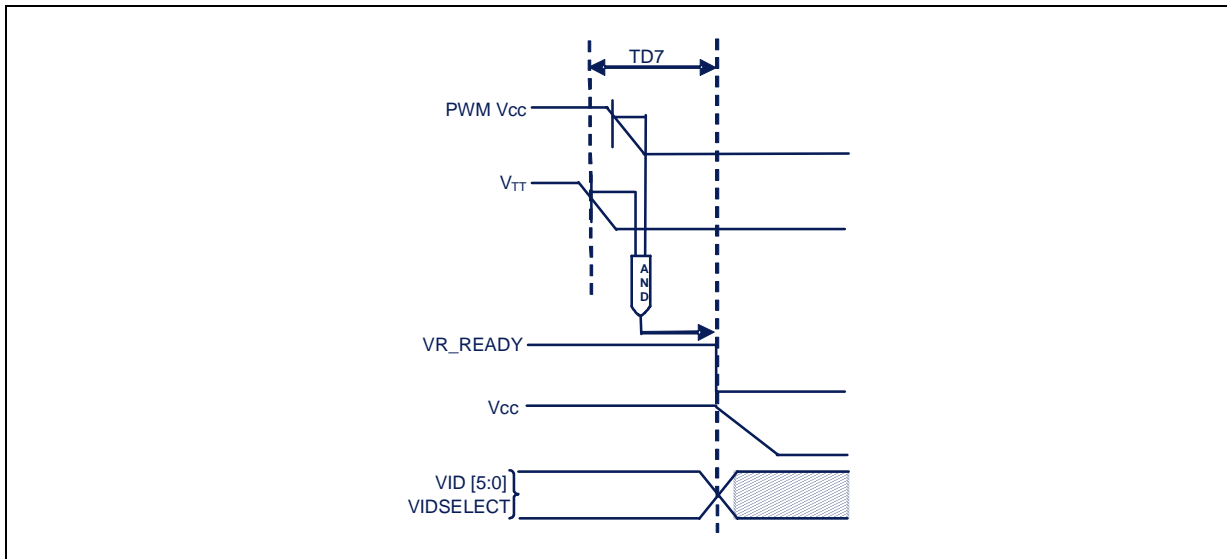
Note: Timing is not to scale.

Table 15. Start-Up and Power-Off Sequence Timing

Start up Delay Parameters			
Parameter	**Minimum**	**Typical, Default**	**Maximum**
TD1	1 ms	-	5 ms
TD2	0 ms	500 µs	5 ms
TD3	50 µs	-	3 ms
TD4	0 µs	250 µs	2.5 ms
TD5	0 ms	-	3 ms
TD6	500 µs		
TD7	0 ms	-	1 ms

Figure 12.   Start-Up Sequence Functional Block Diagram

B5813-01
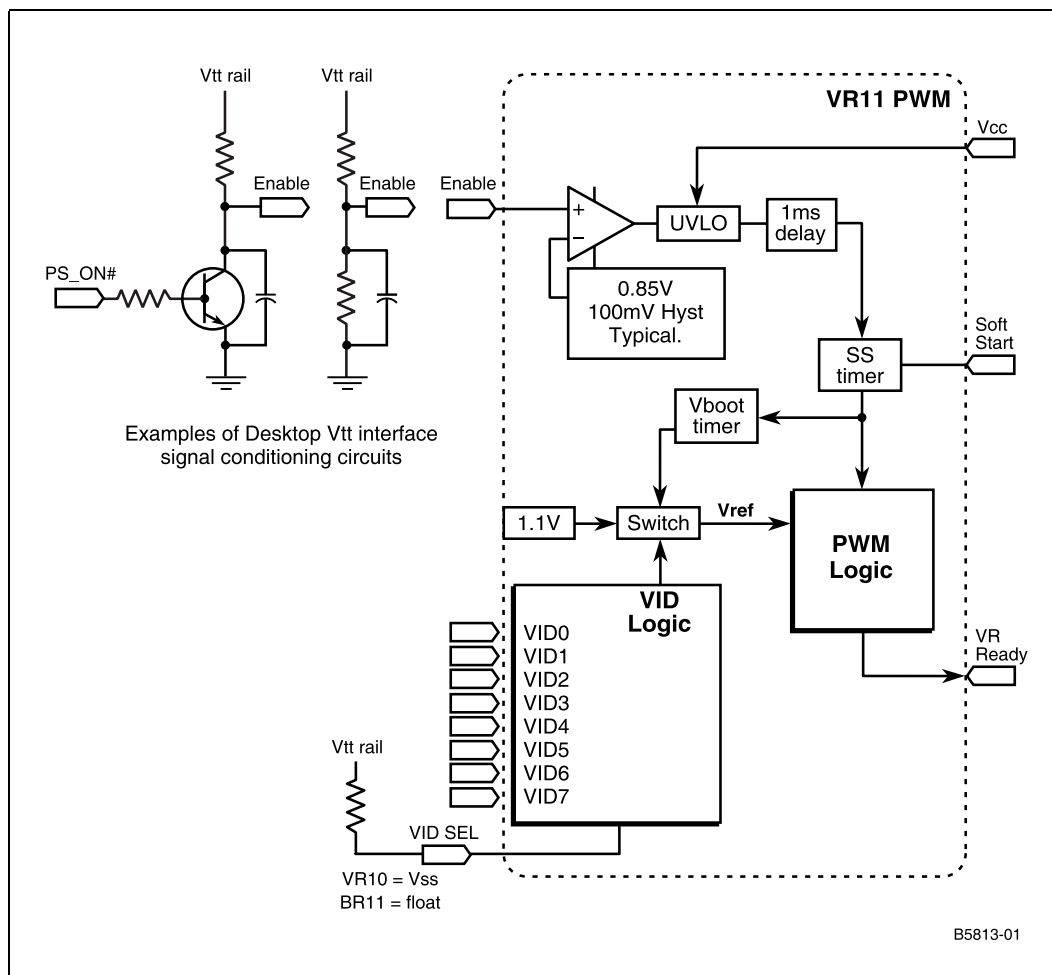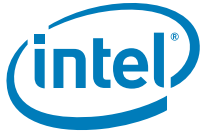
5.0 EmVRD Current Support

System boards supporting processors must have voltage regulator designs compliant to electrical and thermal standards defined in Table 4. This includes full electrical support of Iccmax specifications and regulator layout, processor fan selection, ambient temperature, chassis configuration, etc. Consult Table 4 and Table 9 for processor V_{CC} and V_{CCP} current limits.

To avoid heat related failures, embedded computer systems should be validated for thermal compliance under the envelope of system operating conditions using metrology in the Dual-Core Intel® Xeon® Processor LV *and ULV Thermal Design Guide for Embedded Systems* (see Section 1.3).

5.1 Phase Count Requirement

A EmVRD controller will be used in DC-DC converters that support processors up to 36A I_{CC}. It is expected that the controller chip manufacturer will determine the optimal number of phases for a low-cost design and allow for flexible implementations to meet various market segment requirements. Initial Intel studies show that a two or three phase VR design should meet all the requirements. The specific design environment should dictate which approach is used.

6.0 Control Inputs

6.1 Voltage Identification (CPU VID [5:0], EmVRD [6:1])

The EmVRD controller must accept an 8-bit code transmitted by the processor to establish the reference V_{CC} operating voltage. VR 11.0 based controllers support both VR10.x and VR11.0 VID tables, only the VR11.0 will be used by the processors and will be discussed in this document.

The processors use six VID pins. To match the VID resolution least significant bit in the processor to EmVRD controller, the VID signals are shifted up by one from CPU to EmVRD controller. The two unused VID inputs should be grounded. The VID connections are shown at the top of Table 17.

When an 'OFF' VID code appears at the input to the EmVRD controller, the DC-DC should turn off the V_{CC} output within 0.5 seconds and latch off until power is cycled. Since the processor VID map uses all zeros as the only off condition, the VID bits should use pull down resistors. This will keep the VR off with an empty processor socket.

While operating in the D-VID mode, the processor can transmit VID codes across the six bit bus with a 5 ms data transmission rate. To properly design this bus against timing and signal integrity requirements, the following information is provided. The VID buffer circuit in the processor use a push-pull CMOS circuit configuration. The worst-case settling time requirement for code transmission at each load is 400 ns, including line-to-line skew. EmVRD controller VID inputs will contain circuitry to detect a change and prevent false tripping or latching of VID codes during this 400-nanosecond window.

Intel recommends use of the D-VID bus topology described in Figure 13 and Table 16. Under these conditions, traces can be routed with microstrip, stripline, or a combination with a maximum of four layer transitions. The main trace length can vary between ½ inch and 15 inches with a maximum recommended line to line skew of 1 inch. The 2 kΩ +/-10% pull-down resistor can be placed at any location on the trace with a maximum stub length of 1 inch.

Some designs may require additional VID bus loads. In this case, care should be taken to design the topology to avoid excessive undershoot and overshoot at each load. Failure to comply with these limits may lead to component damage or cause premature failure. The responsible engineer must identify minimum and maximum limits of each component and design a topology that ensures voltages stay within these limits at all times.

Figure 13. **D-VID Bus Topology**
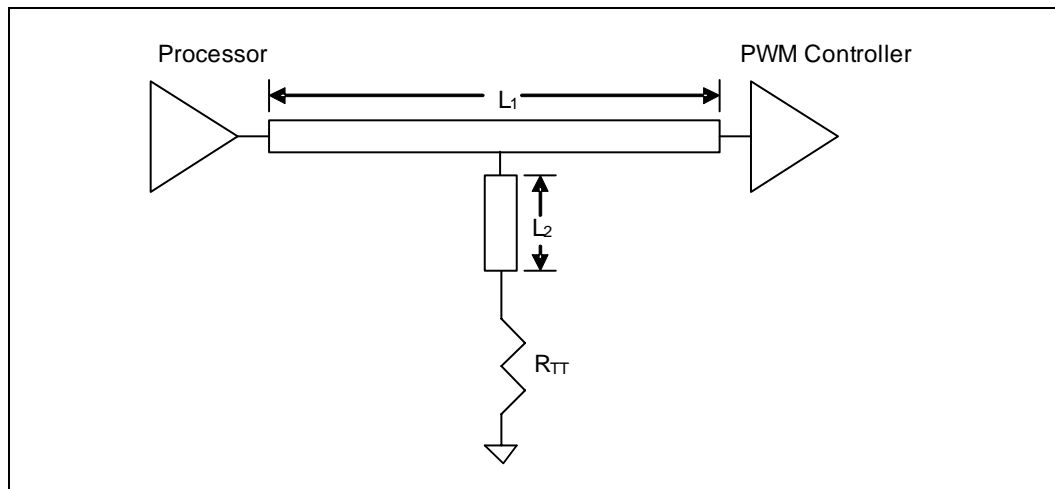
Table 16. **VID Buffer And VID Bus Electrical Parameters**

Design Parameter	Minimum	Typical	Maximum
VID Bus Voltage	-	Vccp[1]	-
Voltage Limits At Processor VID Pins	- 0.100	-	Vccp[2]
VIH	0.8 V	-	-
VIL	-	-	0.3 V
L1, VID trace length	0.5 inch	-	15 inches
L2, Vccp Stub Length	0 inch	-	1 inch
VID trace length skew	-	1.0 inch	-
VID trace width	5 mil	-	-
VID trace separation	5 mil	-	-
RTT, Pull-Down Resistor	1900 Ω[3]	2000 Ω	2100 Ω[4]

Notes:
1. Consult Table 9 for Vccp specifications.
2. Consult the processor datasheet for signal overshoot limits.
3. Value represents minimum resistance at tolerance limits.
4. Value represents maximum resistance at tolerance limits.

6.1.1 Voltage Identification Table

The VID table in Table 17 has the mapping of the VID pins between the CPU and the VR controller and the codes that the processors use. The table also has codes from 1.6 V to 1.5125 V that processors will not use.

Table 17.   **VR11 VID Table from 1.5 V to 0.81875 V (Sheet 1 of 2)**

VR	7	6	5	4	3	2	1	0	VID<7-0>
CPU			5	4	3	2	1	0	VID<5-0>
	0	0	0	0	0	0	0	0	OFF
		0	0	1	0	0	1		1.50000
		0	0	1	0	1	0		1.48750
		0	0	1	0	1	1		1.47500
		0	0	1	1	0	0		1.46250
		0	0	1	1	0	1		1.45000
		0	0	1	1	1	0		1.43750
		0	0	1	1	1	1		1.42500
		0	1	0	0	0	0		1.41250
		0	1	0	0	0	1		1.40000
		0	1	0	0	1	0		1.38750
		0	1	0	0	1	1		1.37500
		0	1	0	1	0	0		1.36250
		0	1	0	1	0	1		1.35000
		0	1	0	1	1	0		1.33750
		0	1	0	1	1	1		1.32500
		0	1	1	0	0	0		1.31250
		0	1	1	0	0	1		1.30000
		0	1	1	0	1	0		1.28750
		0	1	1	0	1	1		1.27500
		0	1	1	1	0	0		1.26250
		0	1	1	1	0	1		1.25000
		0	1	1	1	1	0		1.23750
		0	1	1	1	1	1		1.22500
		1	0	0	0	0	0		1.21250
		1	0	0	0	0	1		1.20000
		1	0	0	0	1	0		1.18750
		1	0	0	0	1	1		1.17500
		1	0	0	1	0	0		1.16250
		1	0	0	1	0	1		1.15000
		1	0	0	1	1	0		1.13750
		1	0	0	1	1	1		1.12500
		1	0	1	0	0	0		1.11250
		1	0	1	0	0	1		1.10000
		1	0	1	0	1	0		1.08750
		1	0	1	0	1	1		1.07500
		1	0	1	1	0	0		1.06250
		1	0	1	1	0	1		1.05000

Table 17.   VR11 VID Table from 1.5 V to 0.81875 V (Sheet 2 of 2)

VR	7	6	5	4	3	2	1	0	VID<7-0>
CPU			5	4	3	2	1	0		VID<5-0>
		1	0	1	1	1	0		1.03750
		1	0	1	1	1	1		1.02500
		1	1	0	0	0	0		1.01250
		1	1	0	0	0	1		1.00000
		1	1	0	0	1	0		0.98750
		1	1	0	0	1	1		0.97500
		1	1	0	1	0	0		0.96250
		1	1	0	1	0	1		0.95000
		1	1	0	1	1	0		0.93750
		1	1	0	1	1	1		0.92500
		1	1	1	0	0	0		0.91250
		1	1	1	0	0	1		0.90000
		1	1	1	0	1	0		0.88750
		1	1	1	0	1	1		0.87500
		1	1	1	1	0	0		0.86250
		1	1	1	1	0	1		0.85000
		1	1	1	1	1	0		0.83750
		1	1	1	1	1	1		0.82500

6.2   VID_SEL: VID Table Selection

VID_SEL is an input on the VR11 controller determines which VID code table to use. It is a static line that can be strapped or floated based on the particular manufacture's instructions. The VID_SEL pin will map the VID inputs to a VR10.x or VR11.0 voltage definition table. The processor will always select the VR11.0 based VID table and designers need to ensure the proper table is being used. This document assumes that the VR11.0 table has been selected. A logic 0 = VR10 VID mode, logic 1= VR11.0 VID mode. The EmVRD should sample VID_SEL during the TD1 time period at startup and select the proper VID table definition (see Figure 10).
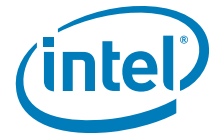
7.0　Input Voltage and Current

7.1　Input Voltages

EmVRD output voltage is supplied via DC-to-DC power conversion. To ensure proper operation, the input supplies to these regulators must satisfy the following conditions.

7.1.1　Platform Input Voltages

The most common power source for the Vcc EmVRD is 12 V ±15% and 3.3 V or 5 V for the V_{CCP} supply. These voltages are supplied by an AC-DC power supply through cabling to the motherboard inputs. For input voltages outside the normal operating range, the EmVRD should either operate properly or shut down. The 1 A/µs slew rate specification for the input current is no longer a design requirement. For the VRD supply Intel recommends a DC-DC regulator input filter with a minimum of 1000 µF to ensure proper loading of the 12 V power source.
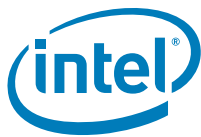
8.0 Output Protection

This section describes features that are built into the EmVRD controller to prevent damage to itself, the processor, validation tools, or other system components. Intel highly recommends that system designers choose a VR11 controller that supports these features.

8.1 Over-Voltage Protection (OVP)

OVP is intended to protect the processor from high voltage damage that may lead to failure, or a reduced processor life span. The OVP circuit is to monitor Vcc for an over-voltage condition at the defined regulation pins. This voltage must never exceed VID+200 mV under any condition and operation above this level defines an OVP violation. In the event of an OVP violation, the V_{CC} VR low side MOSFETs should be driven on to protect the processor and the VR should de-assert VR_READY to shut down the core supply voltage. Power cycling is required to re-start the system.

OVP at start-up should be fully functional with a trip level referenced to the boot VID of 1.1 V.

Operating at lower VID codes during Dynamic VID establishes low (invalid) OVP thresholds which must not be used to initiate a system shut down. For example, there is a time delay from transmission of a VID code to the VR reaction; this time lag may result in a 200 mV delta from the reference VID at a functional voltage that will not damage the processor. Because of these conditions, OVP functionality must be blanked during the Dynamic VID state.

8.2 Over-Current Protection (OCP)

The DC-DC should be capable of withstanding a continuous, abnormally low resistance on the output without damage or over-stress to the DC-DC. The OCP trip level should be programmable by the DC-DC designer, typically 130 percent of rated output current. If an OCP fault is detected, the VR should fold back or shut down, de-assert VR_READY and reset the start up sequence.

Output current under this condition must be limited to avoid component damage and violation of the EmVRD thermal specifications.

9.0 Output Indicators

9.1 VR_READY: V_{CC} Regulator Is 'ON'

VR_READY is an active high output that indicates the start-up sequence is complete and the output voltage has moved to the programmed VID value. This signal is used for start-up sequencing for other voltage regulators, the clock, and microprocessor reset. It is tied to processor PWRGOOD input pin. This signal should not be de-asserted during D-VID operation. The signal should remain asserted during normal DC-DC operating conditions and only de-assert for fault or shutdown conditions. This signal is not a representation of the accuracy of the DC output to its VID value. See Figure 10 for timing and Table 18 for signal specifications.

Table 18. VR_Ready Output Signal Specifications

Signal Type	Open Collector/Drain Logic output from PWM IC, with external pull-up resistor and reference voltage.			
VR_Ready = HIGH	Active / Asserted			
VR_Ready = LOW	Not Active / De-Asserted			

Symbol	Parameter	Min	Max	Units	Remarks
VOH	Output Voltage High	0.8	1.6	V	V_{CCP} rail is expected; Open Coll./Drain Trans. OFF, Imp. >100k depending on system implementation
VOL	Output Voltage Low	0	0.3	V	With external pull-up resistor; Open Coll./Drain Trans. ON
IOL	Output Low Sink Current	1.0	4.0	mA DC	Current limit set by external pull-up resistor
	Transition Edge Rate		150	ns	From 10-90% rise

9.2 FORCEPR# and EmVRD Thermal Monitoring

Each customer is responsible for identifying maximum temperature specifications for all components in the voltage regulator design and ensuring that these specifications are not violated while continuously drawing specified VR_TDC levels. In the event of a catastrophic thermal failure, the thermal monitoring circuit is to assert the VR_HOT signal to drive the processor FORCEPR# input immediately prior to exceeding maximum temperature ratings to prevent heat damage. Assertion of these signals lowers processor power consumption and reduce current draw through the voltage regulator, resulting in lower component temperatures. Assertion of FORCEPR# degrades system performance and must never occur when drawing less than specified thermal design current.

Both VR_HOT and VR_FAN are active high outputs. See the controller IC vendor's datasheets for signal interface specifications (open drain or push-pull). VR_HOT cannot be tied directly to FORCEPR#; the signal must be inverted and buffered. See Figure 14 for buffering information and Table 19 for FORCEPR# signal requirements.

To avoid performance degradation resulting from EmVRD over-temperature conditions, VR11 PWM controllers include a signal called VR_FAN. This signal is activated at 90% of the max VR_HOT trip point. It provides the system designer with options to perform thermal management activities, such as fan speed control, in order to avoid initiating performance degradation.

The controller is located away from the EmVRD 'hot spot'; therefore, external thermistors are needed to sense temperature. Thermistors are placed in the temperature sensitive region of the voltage regulator. The location must be chosen carefully and is to represent the position where initial thermal violations are expected to occur. When exceeded, the thermal monitor circuit is to initiate FORCEPR# to protect the voltage regulator from heat damage.
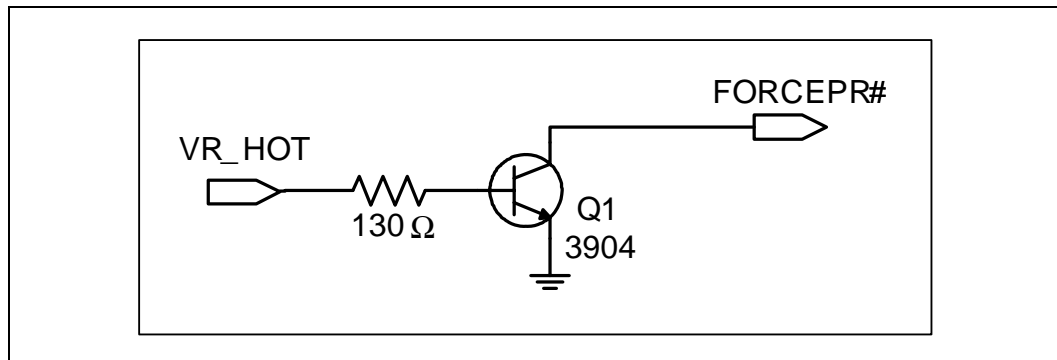
Figure 14. FORCEPR# Buffering

Table 19. FORCEPR# Specifications

Parameter	Minimum	Typical	Maximum
V_{CCP}	-	Vccp[1]	-
V_{CCP} termination resistance	25 Ω	-	70 Ω
FORCEPR# leakage current	-	-	200 mA
FORCEPR# Transition time	1.10 ns	100 ns	-
Minimum time to toggle in and out of D-VID	0.5 ms	-	-

1. Consult Table 12 for V_{CCP} specifications.
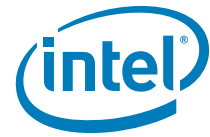
10.0   Mother Board Power Plane Layout

The motherboard layer stack-up must be designed to ensure robust, noise-free power delivery to the processor. Failure to minimize and balance power plane resistance may result in non-compliance to the processor load line specification. A poorly planned stack-up or excessive holes in the power planes may increase system inductance and generate oscillation on the Vcc voltage rail at the processor. Both of these types of design errors can lead to processor failure and must be avoided by careful V_{CC} and V_{SS} plane layout and stack-up. The types of noise introduced by these errors may not be immediately observed on the processor power pins or during system-board voltage transient validation, so issues must be resolved by design, prior to layout, to avoid unexpected failures.

Following basic layout rules can help avoid excessive power plane noise. All motherboard layers in the area surrounding the processor socket should be used for V_{CC} power delivery; copper shapes that encompass the power delivery region of the processor pin field are required. A careful motherboard design will help ensure a well-functioning system that minimizes the noise profile at the processor die. The following subsections provide further guidance.

10.1   Minimize Power Path DC Resistance

Power path resistance can be minimized by ensuring that the copper layout area is balanced between V_{CC} and V_{SS} planes. A good board design will have two V_{CC} layers and a minimum of two Vss layers. Because there is generally more V_{SS} copper in the motherboard stack-up, care should be taken to maximize the copper in V_{CC} floods. This includes care to minimize unnecessary plane splits and holes when locating through hole components, vias, and connection pads.

10.2   Minimize Power Delivery Inductance

At higher frequencies the ordering of the motherboard layers becomes critical as it is V_{CC}/V_{SS} plane pairs which carry current and determine power plane inductance. The layer stack-up should maximize adjacent (layer-to-layer) planes at a minimized spacing to achieve the smallest possible inductance. Care must be taken to minimize unnecessary plane splits and holes when locating through-hole components, vias, and connection pads. Minimized inductance will ensure that the board does not develop low frequency noise which may cause the processor to fail (load line violation).

10.3   Ten Layer Board

In embedded applications, the nominal layer count for a control board is normally much higher than the standard desktop or commodity server boards. An example will be shown for a ten layer board that provides four routing layers, four ground layers, and two outer layers for power. The use of the top and bottom layers for power is becoming increasingly important as the transition speed of current demand has increased. Providing generous voltage planes on the top layer directly from the VR11.0 output inductors to the CPU socket provides the lowest possible resistance and inductance

path to the processors. Using the bottom and internal layers where possible to provide CPU core planes is also recommended. A complete stack-up example of processor reference board is provided in Table 20.

Table 20.   Reference Board Layer Stack-up

| Layers	Material	Thickness (mils)
	Soldermask	1.0
	Plating	1.4
L1 (Top-PWR)	Copper	0.6
	Prepreg	4.0
L2 (Plane-GND)	Copper	1.2
	Core	4.0
L3 (Signal)	Copper	0.6
	Prepreg	6.0
L4 (Plane-GND)	Copper	1.2
	Core	4.0
L5 (Signal)	Copper	0.6
	Prepreg	25.0
L6 (Signal)	Copper	0.6
	Core	4.0
L7 (Plane-GND)	Copper	1.2
	Prepreg	6.0
L8 (Signal)	Copper	0.6
	Core	4.0
L9 (Plane-GND)	Copper	1.2
	Prepreg	4.0
L10 (Bottom-PWR)	Copper	0.6
	Plating	1.4
	Soldermask	1.0

Note: Table does not show the scale of layer thickness.

For further reference board stack-up details see the Intel® E7520 Chipset *Platform Design Guide* (see Section 1.3).

10.3.1   Power Shape Example

Figure 15 shows an example of the V_{CC} shape on the top layer of the processor reference board. To accommodate testing attachments, this design has a larger CPU socket keepout than would be required normal designs. The placement of the VR11.0 inductors and the bulk decoupling capacitors should ideally be as close to the socket as possible. Figure 16 shows the bottom layer for the same CPU socket.

**Figure 15.   Layer 1 V$_{CC}$ Shape For Intel's Reference Ten Layer Motherboard**
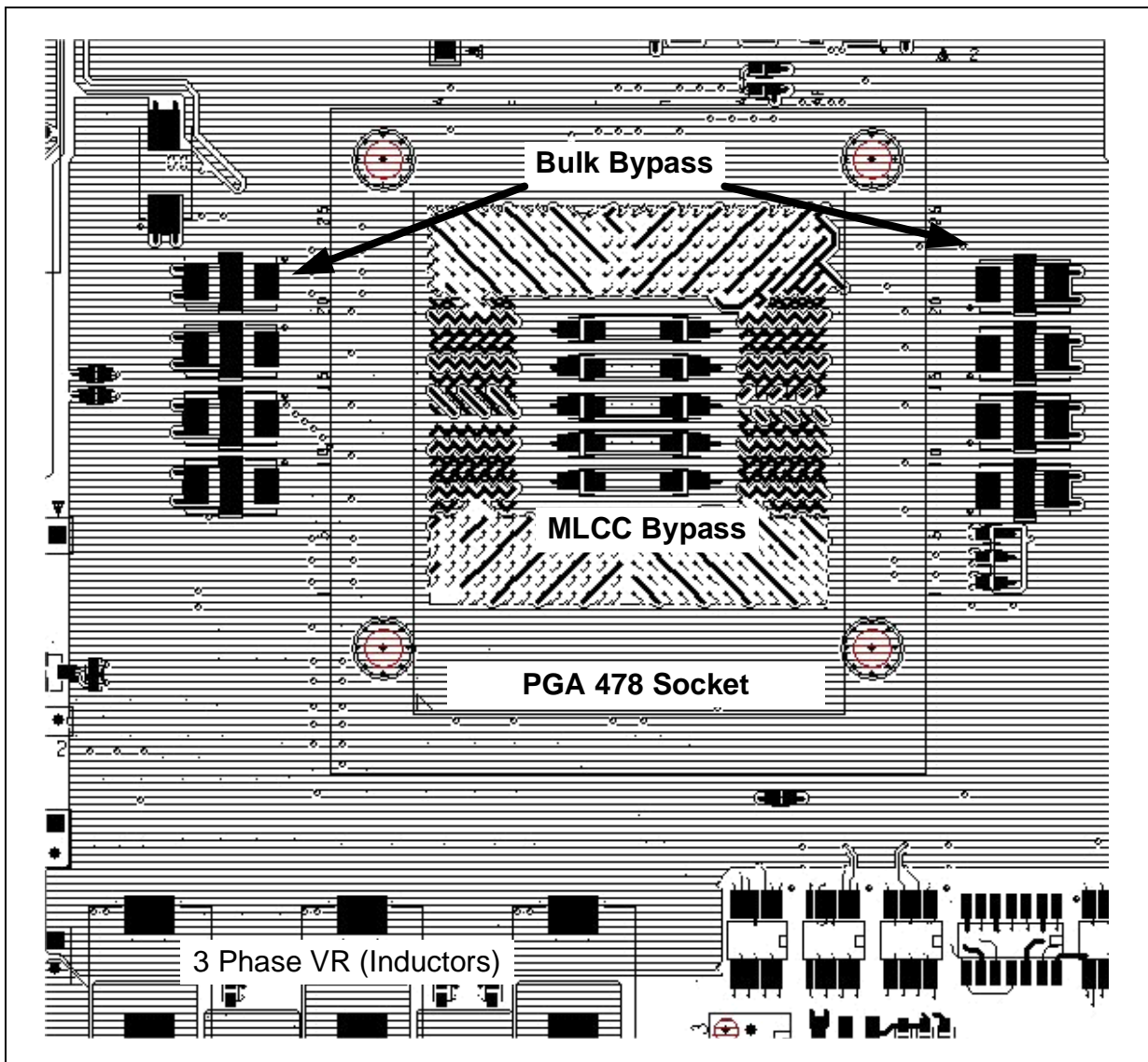
Note: Eight Bulk Bypass Capacitors are shown, two are extra for testing purposes, six are recommended.

Figure 16.   Layer 10 V$_{CC}$ Shape For Intel's Reference Ten Layer Motherboard
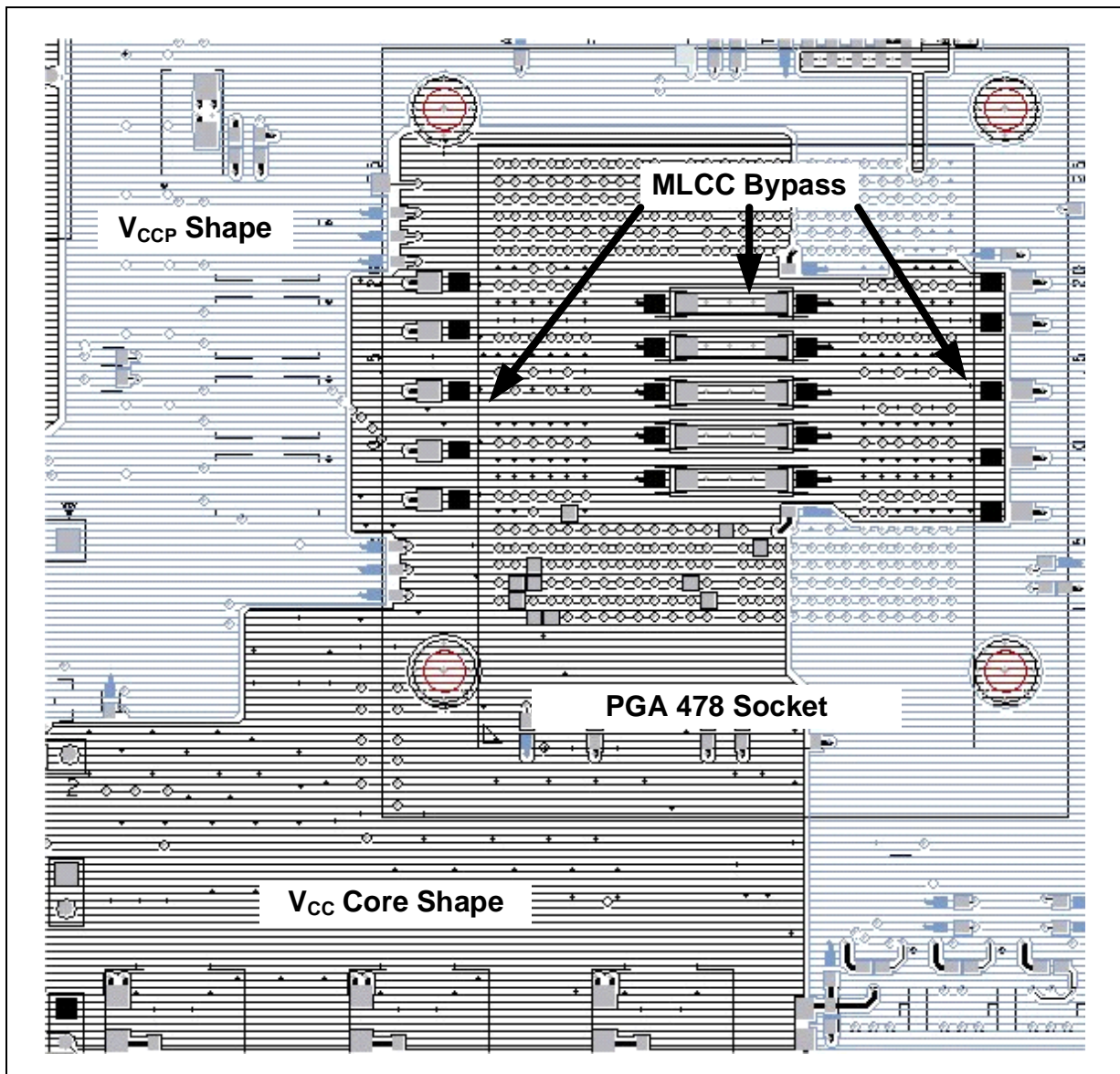
10.3.2   Ganging Common Pins

To maximize the benefit of using the top layer for V$_{CC}$ delivery, the power shape should directly capture all possible socket V$_{CC}$ pads. Using the pattern shown in Figure 17 allows the V$_{CC}$ shape to flow through both sides of the CPU socket and make direct connection with the mid-frequency decoupling capacitors in the socket cavity. Also shown is the ganging of the V$_{SS}$ pads to lower the inductance to the GND layers.
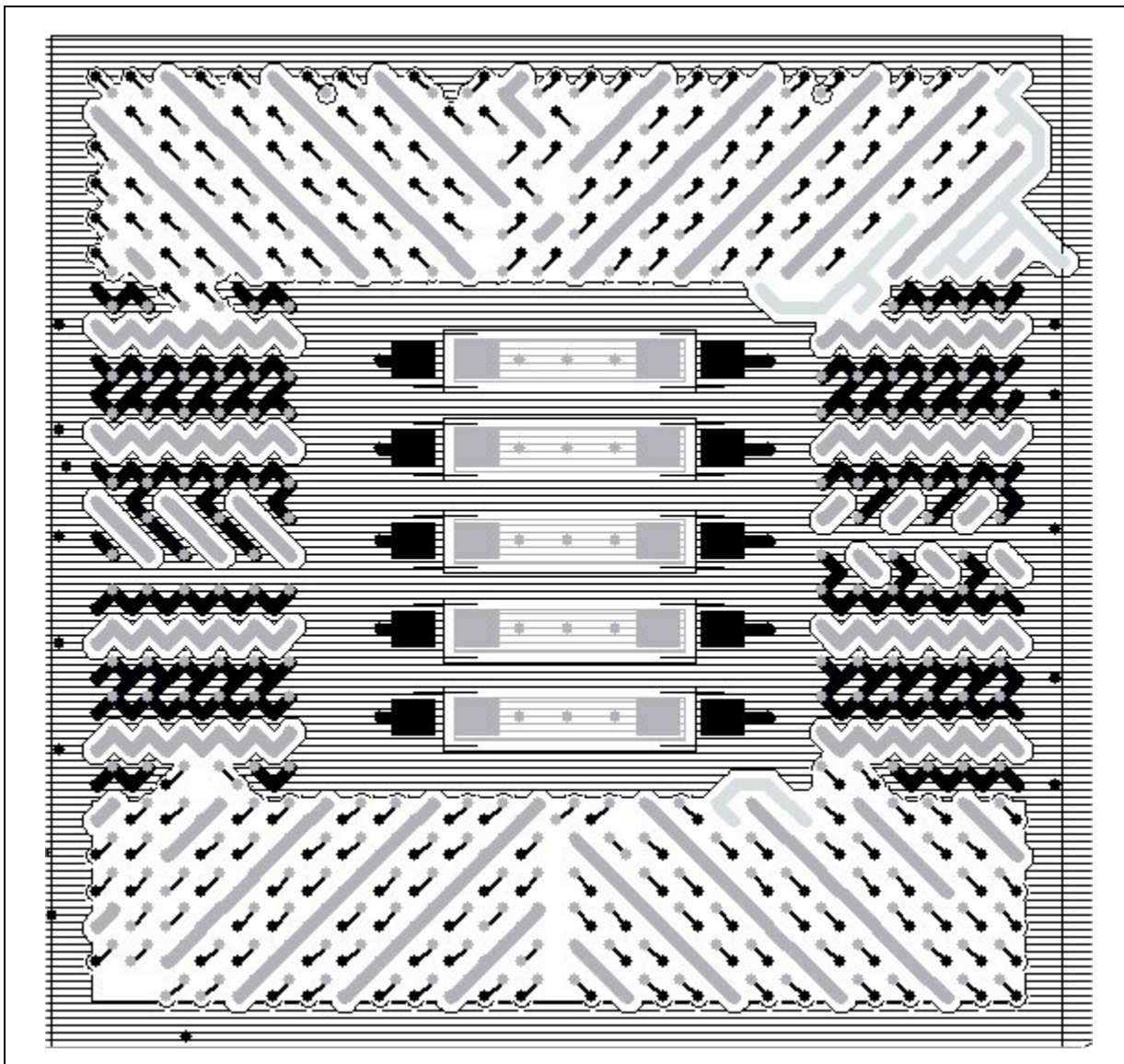
Note: The copper pour and black pins denotes V$_{CC}$, the gray denotes V$_{SS}$

10.4 Resonance Suppression

V$_{CC}$ power delivery designs can be susceptible to resonance phenomena capable of creating droop amplitudes in violation of load line specifications. This is due to the interleaved levels of inductively-separated decoupling capacitance. Furthermore, these resonances may not be detected through standard VTT validation and require engineering analysis to identify and resolve. If not identified and corrected in the design process, these resonant phenomena may yield droop amplitudes in violation of load line specifications by superimposing with standard EmVRD droop behavior. Frequency-dependent power delivery network impedance simulations and validation
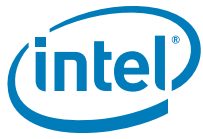
are strongly recommended to identify and resolve power delivery resonances before boards are actually built. Careful modeling and validation can help avoid voltage violations responsible for data corruption, system lock-up, or system 'blue-screening'.