Intel® IP Network Server NSI2U

Technical Product Specification

Intel order number D34973-002

Revision 1.1

November 2007

Modular Communications Platform Division

Revision History

Date	Revision Number	Modifications
September 2005	1.0	Initial release.
November 2007	1.1	Corrected system board identification

Disclaimers

THIS SPECIFICATION IS PROVIDED "AS IS" WITH NO WARRANTIES WHATSOEVER, INCLUDING ANY WARRANTY OF MERCHANTABILITY, NONINFRINGEMENT, FITNESS FOR ANY PARTICULAR PURPOSE, OR ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, SPECIFICATION OR SAMPLE. Intel disclaims all liability, including liability for infringement of any proprietary rights, relating to use of information in this specification. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted herein.

The Intel® IP Network Server NSI2U may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

This document is an intermediate draft for comment only and is subject to change without notice. Readers should not design products based on this document.

I^2C* is a two-wire communications bus/protocol developed by Philips*. SMBus is a subset of the I^2C bus/protocol and was developed by Intel. Implementations of the I^2C bus/protocol or the SMBus bus/protocol may require licenses from various entities, including Philips Electronics N.V. and North American Philips Corporation.

Intel, Pentium and Xeon are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

*Other brands and names are the property of their respective owners.

Table of Contents

List of Figures

List of Tables

1. Introduction

This document provides an overview of the Intel® IP Network Server NSI2U and includes information on chassis hardware, cables, connectors, Intel® Server Board SE7520JR2, system boards, power subsystem, and regulatory requirements.

1.1 Document Structure and Outline

This document is organized into the following chapters:

Chapter 1: Introduction
Provides an overview of this document.

Chapter 2: System Overview
Provides an overview of the chassis hardware.

Chapter 3: Cables and Connectors
Describes the cables and connectors used to interconnect the system board set and the server system components.

Chapter 4: Front Panel I/O Board
Describes the specifications of the front panel I/O board.

Chapter 5: Full Height / Full Length PCI-E / PCI-X Riser Board
Describes the specifications of the 3.3 V FH/FL PCI-E / PCI-X riser board.

Chapter 6: Low Profile / Half Length PCI-X Riser Board
Describes the specifications of the 3.3 V LP/HL PCI-X riser board.

Chapter 7: AC Power Subsystem
Describes the specifications of the AC power subsystem.

Chapter 8: Regulatory Specifications
Describes system compliance to regulatory specifications.

2. System Overview

This chapter describes the features of the NSI2U IP Network Server system chassis.

2.1 System Features

Table 2-1 provides a list and brief description of the features of the NSI2U IP Network Server system.

Table 2-1. NSI2U IP Network Server system Feature List

Feature	Description	
Compact, high-density system	Rack-mount server with a height of 2U (3.5 inches) and a depth of 20.0 inches	
Configuration flexibility	1 or -2 way capability in low profile and cost/value effective packaging Stand-alone system 800 MHz Front Side Bus (FSB) Intel® Xeon™ processor support up to 3.6 GHz	
Serviceability	Back access to hot-swap power supplies Front access to SATA disk drives	
Availability	Two hot-swap 600 W power supplies in a redundant (1+1) configuration RAID 0 and RAID 1 capability using two SATA disk drives.	
Manageability	Remote management Emergency management port (Serial and LAN) IPMI 1.5 compliant Remote diagnostics support	
Upgradeability and investment protection	Designed to support 800 MHz FSB Intel® Xeon™ processor family Multigenerational chassis	
System-level scalability	16 GB DDR2-400 Registered SDRAM DIMM memory support Dual 800 MHz FSB Intel® Xeon™ processor support 2 Full Height / Full Length x4 PCI-E Slots 1 Full Height / Full Length 3.3V 64-bit x 133 MHz PCI-X Slots 3 Low Profile / Half Length 64-bit x 133 MHz PCI-X Slots 2 internal SATA disk drives	
Front panel	Switches: Power switch Reset switch NMI switch ID switch	LEDs: ID LED NIC activity LED Main power LED HDD activity LED Status LED

2.2 Chapter Structure and Outline

This chapter is organized into the following sections. The content of each section is summarized as follows.

Section 2.3: Introduction
Provides an overview and block diagram of the NSI2U IP Network Server system.

Section 2.4: External Chassis Features
Describes features of the NSI2U IP Network Server system chassis in detail (buttons, switches, bezel, etc.).

Section 2.5: Internal Chassis Features
Provides an overview of the components of the NSI2U IP Network Server system.

Section 2.6: Server Management
Describes the server management features of the NSI2U IP Network Server system.

Section 2.7: Specifications
Summarizes the environmental and physical specifications of the NSI2U IP Network Server system.

2.3 Introduction

The IP network server is a compact, high-density, rack mount server system with support for one or two 800 MHz FSB Intel® Xeon™ processors and 16 GB DDR2-400 SDRAM DIMM memory. The NSI2U supports high availability features such as front accessible network connections, front accessible disk drives, and hot-swap and redundant power supply modules. The scalable architecture of the NSI2U supports symmetric multiprocessing (SMP) and a variety of operating systems (OS).

Figure 2-1 shows an isometric view of the system. Figure 2-2 shows the system with the top covers and the front bezel removed.

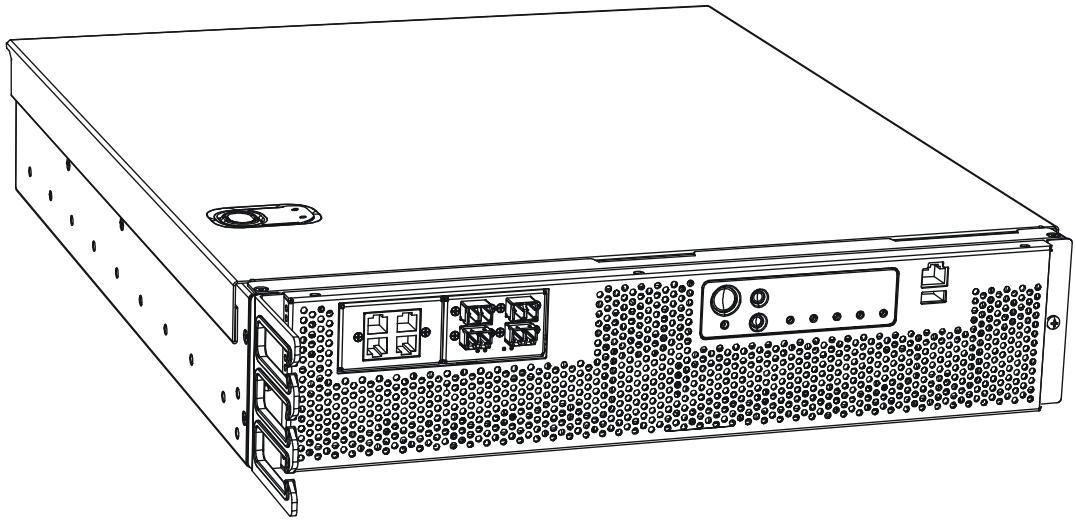
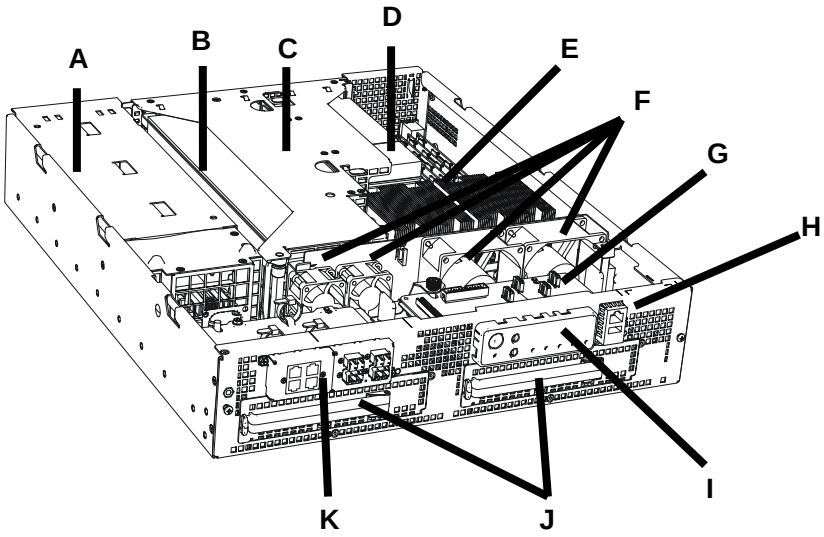


Figure 2-1: NSI2U IP Network Server system

The Intel® IP Network Server NSI2U uses the Intel® Server Board SE7520JR2, which contains dual processor slots for installing up to two 800 MHz FSB Intel® Xeon™ processors utilizing 604-pin zero insertion force (ZIF) processor sockets. The server board has six DIMM slots and supports up to 16 GB error checking and correcting (ECC) SDRAM memory. The server board also contains six PCI slots (implemented via riser cards), input/output (I/O) ports and various controllers.



A. Power Supply	G. FPIO system board
B. PCI card bracket (full-length)	H. RJ45 COM2 and USB port
C. Riser card assembly (full and low profile)	I. Control Panel and Status Indicators
D. PCI card bracket (low-profile)	J. SATA Hard Disk Drive Bays
E. Intel® Server Board SE7520JR2	K. Interconnect Port Panels
F. System Fans	

Figure 2-2: IP Network Server (shown with top covers and bezel removed)

The server board is mounted horizontally toward the rear of the chassis behind the system fan array.

Up to two 3.5” SATA technology hard drives can be mounted in the drive bays, which are located in the bottom front of the chassis. The front bezel must be removed to access the drive bays. Figure 2-2 shows the location of the two SATA drive trays.

Two interconnect port panels can be installed in the system. The interconnect port panels are located above the left hard drive bay. Each of the interconnect port panels can be configured with either a blank panel, a four port copper RJ45 interconnect port panel, or a four port Fiber-LC interconnect port panel. Note that the RJ45 and Fiber-LC interconnect port panels are internally cabled to PCI-Express adapters configured in the full height/full length PCI-E riser board.

The Front Panel I/O board (FPIO board) is located above the right hard drive tray and provides user interface for the system front panel and for system management.

The AC-input power supply modules are installed at the left-rear of the chassis. Up to two hot-swap 600W AC power supply modules may be installed for a 1 + 1 redundant configuration. A filler panel for the empty power supply location is supplied for systems without redundancy.

The system contains a fan array consisting of two 80 x 38mm fans and two 40 x 28mm fans to cool the server board and other components. The fans are installed directly behind the drive bays and are located in front of the server board. Individual fan connectors are located on the FPIO board. A fan failure is indicated by one of the fault light-emitting diodes (LED) located on the FPIO board.

The front bezel can be customized to meet OEM industrial design requirements. The bezel design allows adequate airflow to cool the system components. The front bezel is removed to access the drive tray.

Figure 2-3 shows a block diagram of the IP Network Server with interconnections.

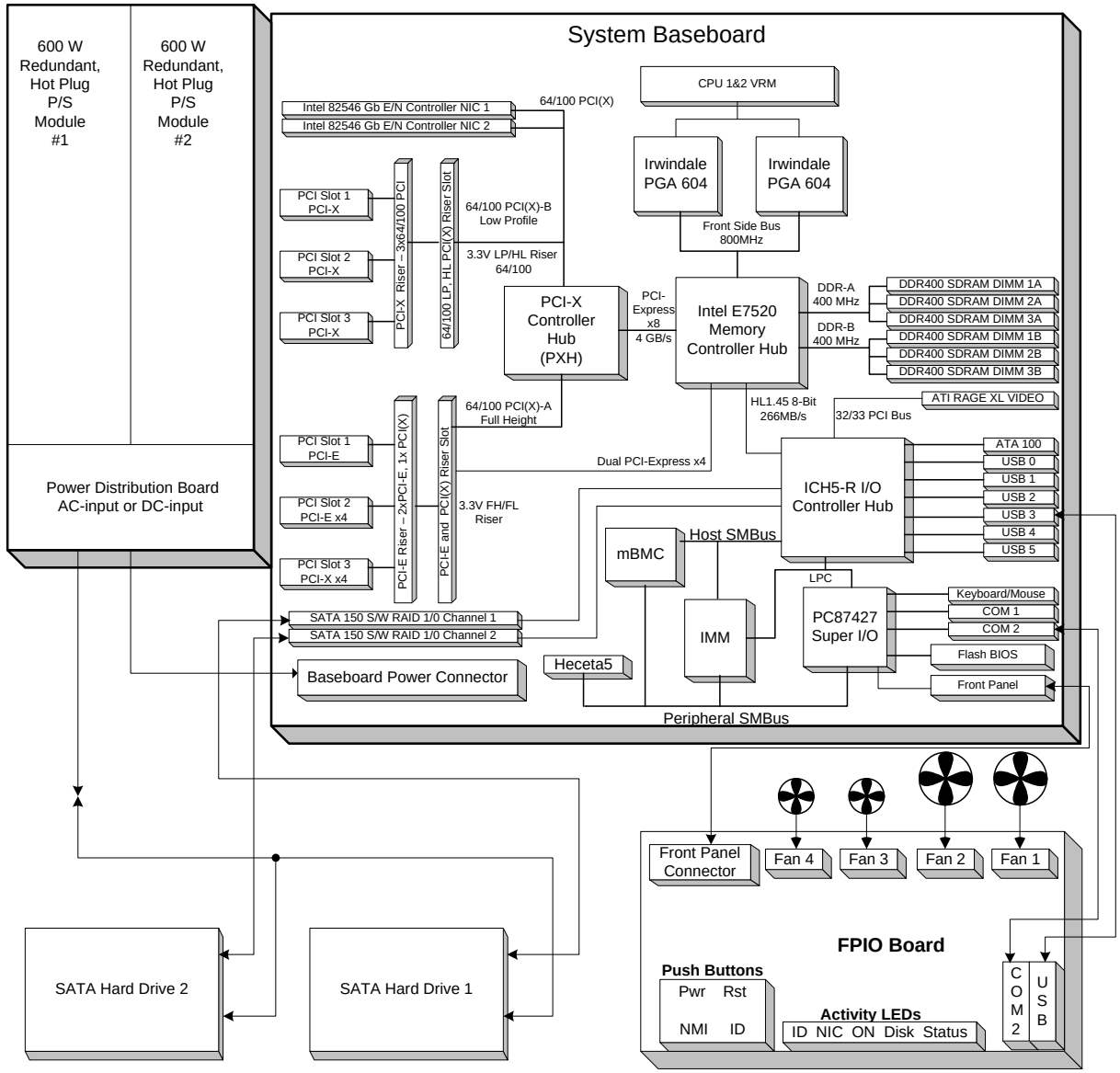


Figure 2-3: IP Network Server Block Diagram

2.4 External Chassis Features

2.4.1 Front View of Chassis

Figure 2-4 shows the front view of the system. Figure 2-5 shows the front view of the system with the front bezel removed. Removing the front bezel provides access to the two hard drive bays. Removing the front bezel also provides access to the interconnect port panels.

Both areas are described in detail in the following sections.

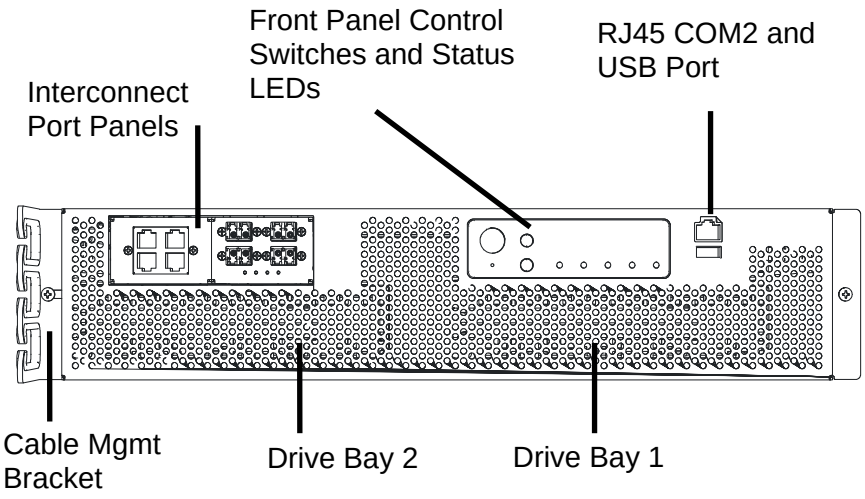


Figure 2-4. Front View of System

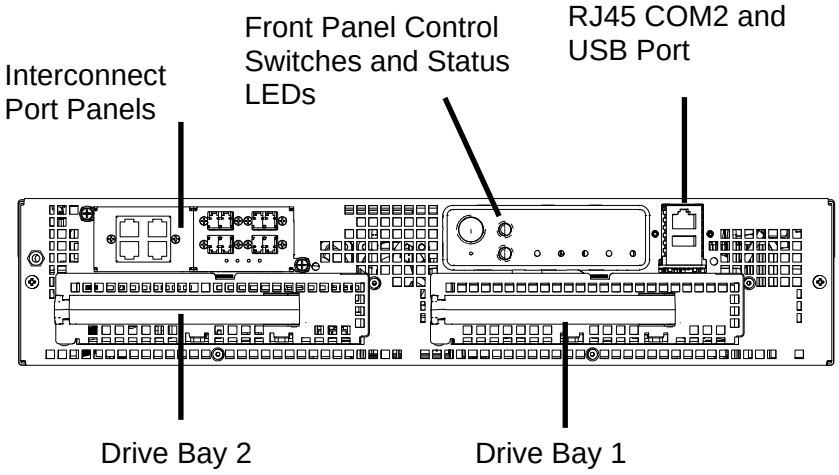


Figure 2-5. Front View of System (shown with bezel removed)

2.4.2 Front Panel

The front panel features are shown in Figure 2-6 and described in Table 2-2. All front panel control switches and status LEDs are contained on the FPIO system board. Please refer to Section 4.4 for a detailed description of the control switches and status LEDs contained on the front panel.

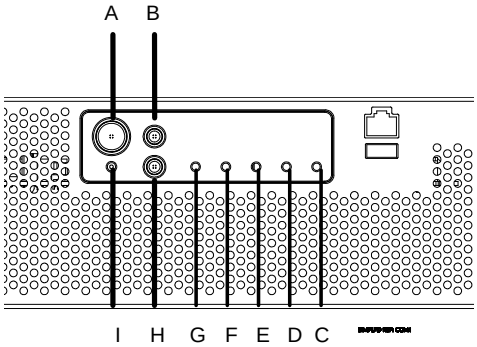


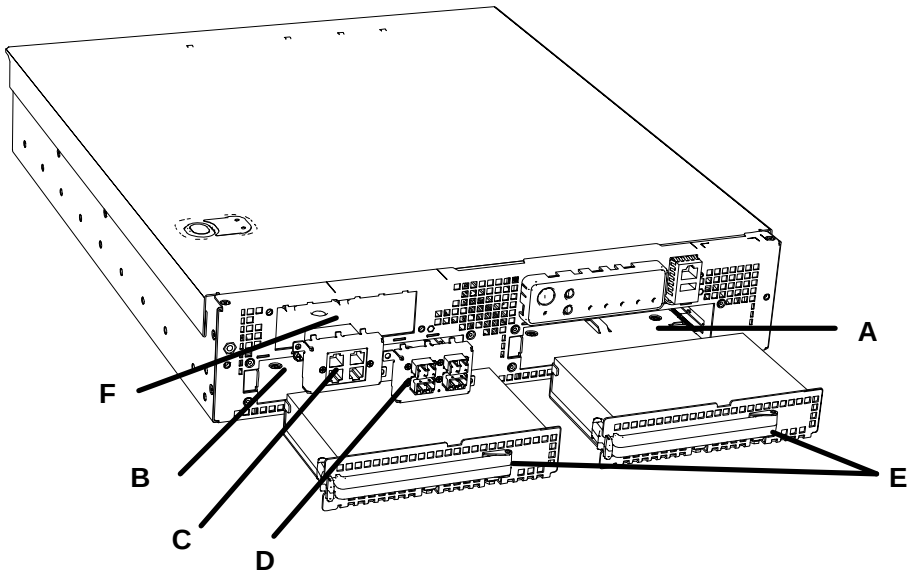
Figure 2-6. Front Panel Details

Table 2-2: Front Panel Features

Item	Feature	Description
Front Panel Switches		
A	Power switch	Toggles the system power
B	Reset switch	Resets the system
H	ID switch	Toggles system ID LED
I	NMI switch	Assert NMI to server board
Front Panel Status LEDs		
C	System Status LED (green/amber)	Indicates system status ok when green, or a system fault when amber
D	Disk Activity/Fault LED (green/amber)	Indicates SATA disk 1 or SATA disk 2 hard drive activity when green, or hard drive fault when amber
E	Main power LED (green)	When continuously lit, indicates the presence of DC power in the server. The LED goes out when the power is turned off or the power source is disrupted
F	NIC0/NIC1 activity LED (green)	Indicates activity on either NIC0 or NIC1
G	System ID LED (white)	Continuously lit when activated by (1) software command to front panel board or (2) by the front panel ID switch

2.4.3 Chassis Interconnect Port Panel Bays and Hard Drive Bays

The IP Network Server provides two hard drive bays at the front of the chassis, along with two bays for interconnect port panels. Both hard drive bays may be populated with a tray-mounted 3.5” SATA hard disk drive.



A. Hard drive bay 1
B. Hard drive bay 2
C. Interconnect Port Panel Bay - Ethernet RJ45 interconnect port panel shown
D. Interconnect Port Panel Bay - Ethernet fiber interconnect port panel shown
E. Hard disk drive modules
F. Interconnect port panel bays

Figure 2-7: Chassis Interconnect Port Panel Bays and Hard Drive Bays

2.4.3.1 Interconnct Port Panel Bays

There are two interconnect port panel bays. Each bay will support the installation of either an Ethernet copper RJ45 interconnect port panel, or an Ethernet fiber interconnect port panel.

As shown by the red dots in Figure 2-8, each interconnect port panel is secured with a screw. The interconnect port panel shown installed in the left bay (2) is an Ethernet RJ45 interconnect port panel, while the interconnect port panel shown installed in the right bay (1) is an Ethernet fiber interconnect port panel. The Ethernet RJ45 interconnect port panel and the Ethernet fiber interconnect port panel can be installed in either interconnect port panel bay.

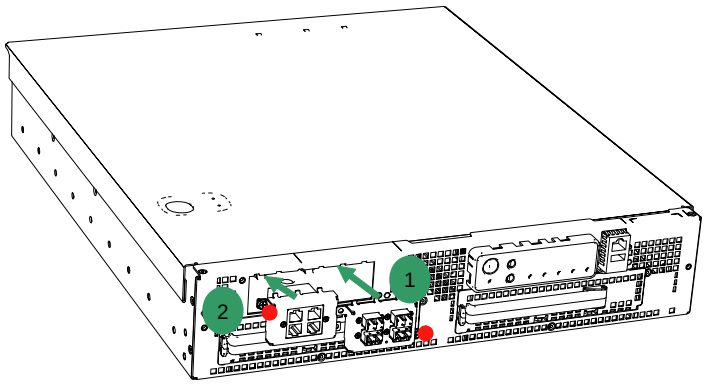


Figure 2-8: Interconnect Port Bays

2.4.3.2 Hard Drive Bays

There are two hard drive bays in the IP network server (see (1) and (2) in the drawing below). Each hard drive bay supports a tray-mounted SATA disk drive. The drive tray is installed into the front of the chassis in the hard drive bay, and then secured in place by pushing in the handle on the drive tray. A small metal bracket on the inside front of the system is then pushed toward the drive to connect the SATA cable signal and power connectors to the SATA signal and power connectors on the drive.

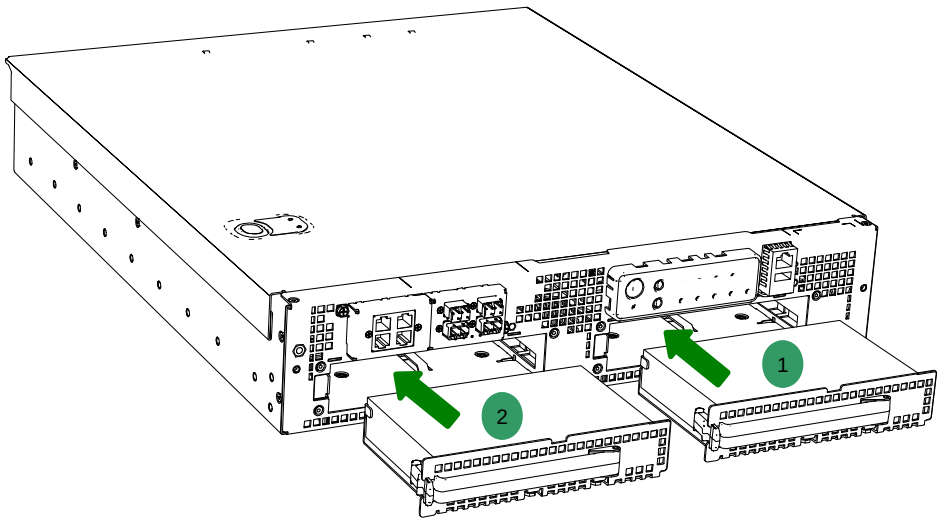


Figure 2-9: SATA Hard Drive Bays

2.4.3.2.1 Hard Drive Tray

Each hard drive used in the system must be mounted to a drive tray using four screws inserted into the bottom of the drive as shown in Figure 2-10.

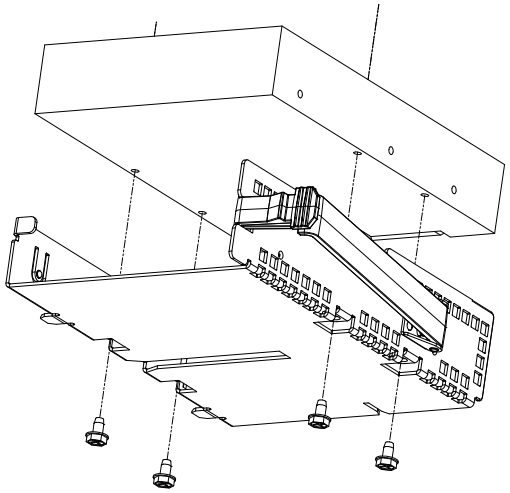


Figure 2-10: SATA Hard Drive Tray

2.4.4 Rear View of System

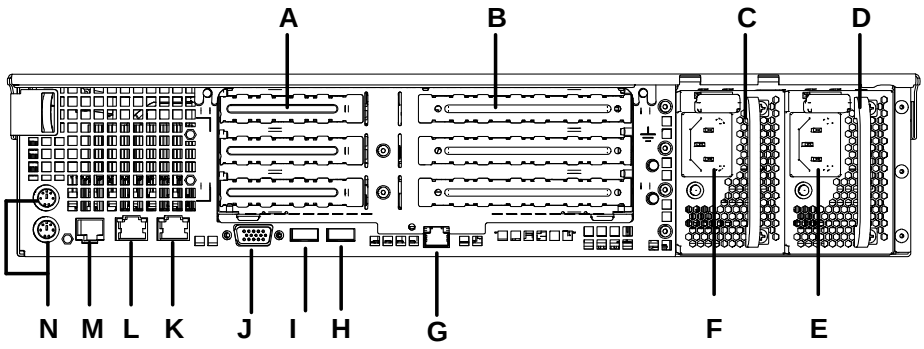


Figure 2-11. Rear View of System

Table 2-3. System Features - Rear

Item	Description
A	PCI card bracket (low profile)
B	PCI card bracket (full-height)
C	Power supply module, redundant (system accessory)
D	Power supply module, primary
E	AC power input (primary
F	AC power input (redundant)
G	RJ45 Server Management (system accessory)
H	USB connector 2
I	USB connector 1
J	Video connector
K	RJ45 NIC 2 connector - Green Status LED / Yellow Status LED
L	RJ45 NIC 1 connector - Green Status LED / Yellow Status LED
M	RJ45 serial 2 port
N	PS/2 mouse/keyboard connectors

2.5 Internal System Features

2.5.1 Intel® Server Board SE7520JR2

The Intel® Server Board SE7520JR2 is a monolithic printed circuit board that can accept one or two 800 MHz FSB Intel® Xeon™ processors using the 604-pin ZIF socket. The figure below shows the functional blocks of the server board and the plug-in modules that it supports in the IP network server.

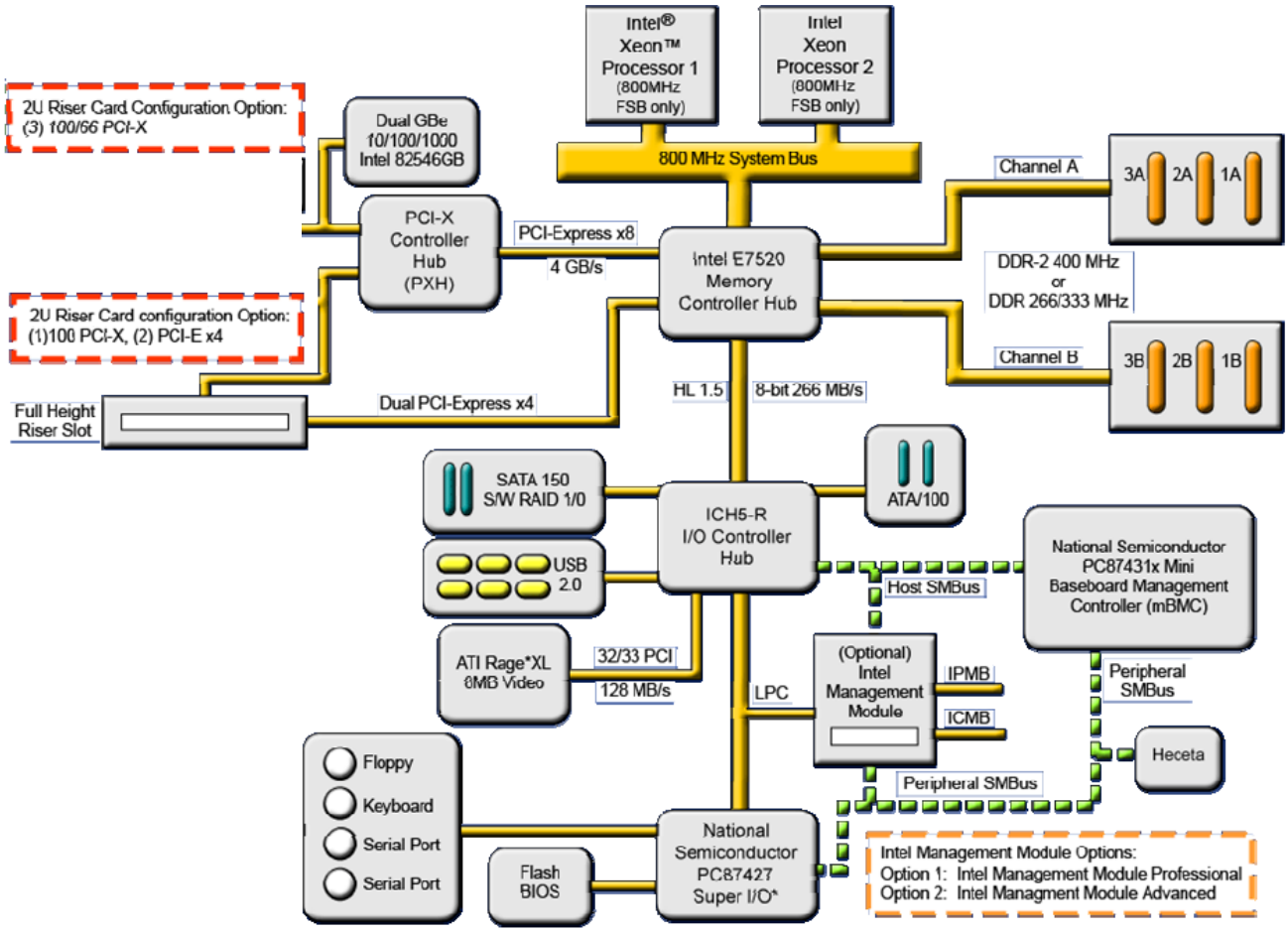


Figure 2-12. Intel® Server Board SE7520JR2 Block Diagram

- Dual processor slots supporting 800MHz Front Side Bus (FSB) Intel® Xeon™ processors
- Intel E7520 Chipset (MCH, PXH, ICH-5R)
- Two PCI riser slots
  - Riser Slot 1: Supports low profile PCI-X 64-bit 100MHz PCI-X cards
  - Riser Slot 2: Supports two x4 PCI-E cards and one full height PCI-X 64-bit 133MHz PCI-X card
- Six DIMM slots supporting DDR2 – 400MHz memory
- Dual Intel® 82546GB 10/100/1000 Network Interface Controllers (NICs)
- On board ATI* Rage XL video controller with 8MB SDRAM
- On-board platform instrumentation using a National* PC87431M mini-BMC.
- External IO connectors
  - Stacked PS2 ports for keyboard and mouse
  - RJ45 Serial B Port
  - Two RJ45 NIC connectors
  - 15-pin video connector
  - Two USB 2.0 ports
- Dual Intel® 800 MHz Front Side Bus
- Intel® E7520 chipset
  - E7520 North Bridge
  - PXH I/O Bridge
  - ICH-5R S South Bridge
- Support for up to six DDR2-400MHz compliant registered ECC DIMMs providing up to 16 GB of memory, when 4G DIMMs become available and have been tested.
- Three separate and independent PCI buses:
  - Segment P32-A: 32-bit, 33 MHz, 5 V with the embedded device:
    - 2D/3D graphics controller: ATI Rage XL Video Controller with 8 MB of memory.
  - Segment P64-A: 64-bit, 133 MHz, 3.3 V, PCI-X supporting the following configuration:
    - One PCI I/O riser slot capable of supporting full length PCI add-in cards

    Segment P64-B: 64-bit, 133 MHz, 3.3 V PCI-X supporting the following devices:
    - One PCI I/O riser slot capable of supporting low-profile PCI add-in cards
    - Dual-channel Intel® 10/100/1000 82546EB Gigabit Ethernet Controller
- LPC (Low Pin Count) bus segment with two embedded devices:
  - Platform Management Controller (BMC) providing monitoring, alerting, and logging of critical system information obtained from embedded sensors on the server board
  - Super I/O controller chip providing all PC-compatible I/O (floppy, serial, keyboard, mouse)
- X-Bus segment with one embedded device:
  - Flash ROM device for system BIOS: Intel® 32-megabit 28F320C3 Flash ROM

- One external Universal Serial Bus (USB) port with an additional internal header providing two optional USB ports for front panel support
- One external low-profile RJ45 serial port. An internal header is also available providing an optional serial port.
- IDE connector for one CDROM drive
- Support for up to four system fans
- Fault/Status LEDs throughout the server board
- Multiple server management headers providing on-board interconnects to server management features

Refer to the Intel® Server Board SE7520JR2 Technical Product Specification for further details.

2.5.2 PCI Adapter Subsystem

A PCI adapter assembly that supports both the full-height PCI riser and the low profile riser and associated PCI adapters is installed in the PCI riser slots located in the middle of the server board. This PCI adapter assembly is configured and installed as shown in figures Figure 2-13 and Figure 2-14. After the PCI adapter assembly is removed from the system, it is configured with PCI adapters by plugging the PCI adapters into the PCI connectors on the riser cards that are part of the PCI adapter assembly. The PCI adapter assembly is then installed into the system by plugging the riser cards into the riser card connectors on the server board. Refer to the Intel® Server Board SE7520JR2 Technical Product Specification for electrical characteristics for this PCI adapter subsystem.

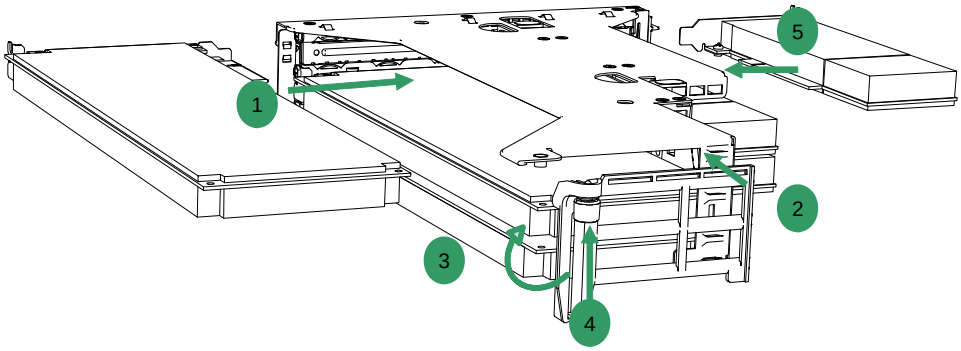


Figure 2-13: PCI Adapter Subsystem Assembly and Installation (A)

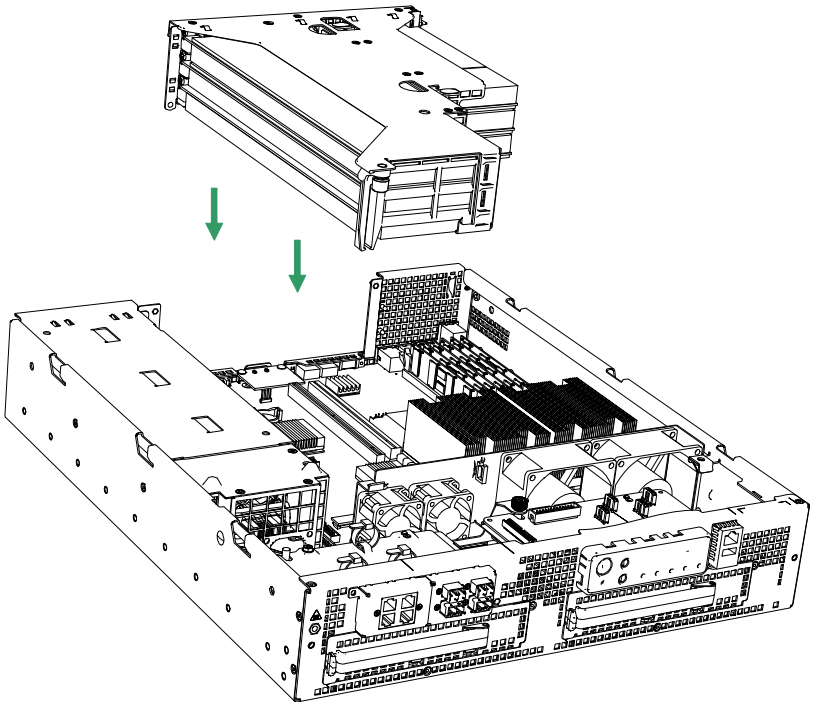


Figure 2-14: PCI Adapter Subsystem Assembly and Installation (B)

The full height riser slot is configured with a 2U three slot riser card which provides two x8 PCI-E connectors each supporting x4 data widths, and a third slot which is a PCI-X slot capable of supporting a bus speed of up to 133MHz.

The low-profile riser slot is configured with a 2U three slot riser card which provides three PCI-X slots. It will support bus speeds of up to 100MHz with one or two PCI-X 100MHz cards installed. The bus speed will drop to 66MHz when three PCI-X 100MHz cards are installed, or will match the card speed of the lowest speed card on the bus. That is, if any PCI card is installed that supports a maximum bus speed of 66MHz, the entire bus will throttle down to 66MHz to match the supported frequency of that card. When populating add-in cards, the add-in cards must be installed starting with the slot furthest from the server board. If only a single PCI-X card is installed, it must be installed in the top PCI slot. If two PCI-X cards are installed, they must be installed in the top two slots. These population rules must be followed to maintain the signal integrity of the bus.

2.5.3 Power Subsystem

The IP Network Server is configured with a 1+1 redundant AC-input power subsystem. The power supply modules are located at the left rear of the chassis. The AC power subsystem may contain up to two power supply modules and can be configured as follows:

- Two power supply modules installed, (1 + 1) power redundancy for maximally loaded system
- One power supply module installed[1], non-redundant for maximally loaded system

When the system is configured with two power supply modules, the hot-swap feature allows the user to replace a failed power supply module without interrupting system functionality. To ensure that all components remain within specification under all system environmental conditions, it is recommended that power supply module hot-swap operations not exceed two minutes in duration.

Power from the power subsystem is carried to internal system boards and peripheral devices via discrete cables from the Power Distribution Board (PDB). One power supply module is capable of handling the worst-case power requirements for a fully configured IP network server. This includes two 800 MHz FSB Intel® Xeon™ processors, 16 GB of memory, two hard drives at 18 W per drive (typical worst case 3.5-inch by 1.0-inch, 15k RPM drive), and a full complement of PCI adapters.

The total power requirement for the IP network server exceeds the 240 VA energy hazard limit, which defines an operator-accessible area. As a result, only qualified technical individuals should access the processor, memory, and I/O areas on the server board while the system is energized.

Refer to *Section 7 AC Power Subsystem* of this document for detailed power specifications.

[1] Proper power subsystem cooling by the power subsystem fan requires the population of both (power supply bay) receptacles either by a power supply module or a filler panel.

2.5.4 Cooling Subsystem

2.5.4.1 Description

All system components except the power supply cage are cooled by a set of fans mounted near the middle of the chassis and behind the hard drive bays. This is shown in Figure 2-2.

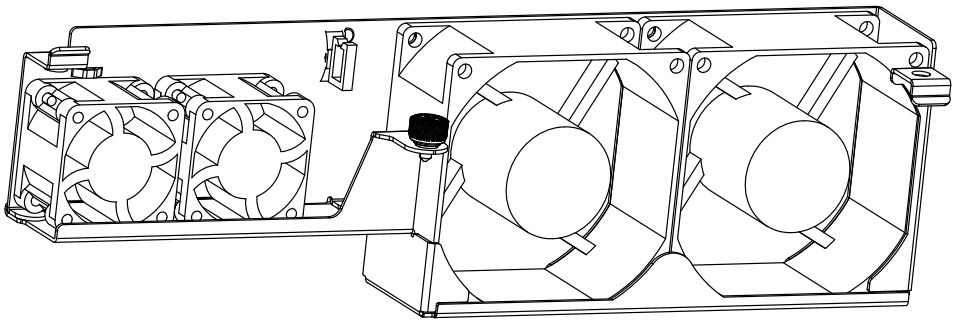


Figure 2-15. Fan Array with Four System Fans Installed

The IP network server comes in a non-redundant, four-fan configuration that consists of two 80mm x 38mm fans and two 40mm x 28mm fans.

Air flows in through the front bezel over the hard drive bays, passes through the fans and over the server board, and exhausts through the rear of the chassis. Each fan provides tachometer signal output to the server board to indicate a fan failure.

2.5.4.2 Ambient Temperature Control

The server board contains two pulse-width-modulation (PWM) circuits, which cycle the 12 Vdc fan voltage to provide quiet operation when system ambient temperature is low and there are no fan failures. One PWM is connected to the two 80x38mm fans and the other to the two 40x28mm fans. Based on the ambient temperature, the fan speeds are set per Table 2-4:

Table 2-4: Fan Speed Control Settings

	40mm	40mm	80mm	80mm
Temperature	**PWM %**	**VDC**	**PWM%**	**VDC**
20c	49% (31h)	5.47v	49% (31h)	5.26v
21c	49% (31h)	5.47v	49% (31h)	5.26v
22c	49% (31h)	5.47v	49% (31h)	5.26v
23c	51% (33h)	6.23v	49% (31h)	5.26v
24c	54% (36h)	6.23v	49% (31h)	5.26v
25c	57% (39h)	6.99v	49% (31h)	5.26v
26c	60% (3Ch)	6.99v	50% (32h)	5.99v
27c	63% (3Fh)	7.47v	51% (33h)	5.99v

28c	66% (42h)	7.47v	52% (34h)	5.99v
29c	69% (45h)	8.53v	54% (36h)	5.99v
30c	72% (48h)	8.53v	55% (37h)	5.99v
31c	76% (4Ch)	9.30v	58% (3Ah)	6.72v
32c	82% (52h)	10.07v	68% (44h)	7.45v
33c	90% (5Ah)	10.84v	74% (4Ah)	8.18v
34c	96% (60h)	11.59v	80% (50h)	8.91v
35c	100% (64h)	12.21v	86% (56h)	9.63v

2.5.4.3 Cooling Summary

The four-fan cooling subsystem is sized to provide cooling for:

- Up to two processors
- 16 GB of SDRAM memory
- Two 15,000 RPM hard drives at a maximum of 18W per drive
- 6 PCI cards

The cooling subsystem is designed to meet acoustic and thermal requirements at the lower fan speed settings. At the higher fan speed settings, thermal requirements are met for the maximum ambient temperatures, but acoustic requirements are not met. The environmental specifications are summarized in 2.7.1.

2.6 Server Management

The server board server management architecture features Intel's Sahalee Baseboard Management Controller (BMC). This autonomously monitors server status and provides the interface to server management control functions. This controller is responsible for controlling system power, resets, monitoring voltages, temperatures, fans, and communicating with secondary controllers on the Intelligent Platform Management Bus (IPMB).

The functions of each controller are summarized in the following sections. The firmware for all of the controllers is field upgradeable using the *Server Management Firmware Update Utility*. Refer to the *SE7520JR2 Server Management External Architecture Specification* for more details.

2.6.1 Baseboard Management Controller

The BMC on the server board provides server management monitoring capabilities. A flash memory is associated with the BMC that holds the operational code, sensor data records (SDR), and system event log (SEL). There is also a serial EEPROM that holds the BMC configuration defaults and field replaceable unit (FRU) information. The various server management functions provided by the BMC are listed as follows:

- Server board voltage monitoring
- Fan failure detection
- Fan speed control
- Processor voltage monitoring
- Processor presence detection
- Processor internal error (IERR) monitoring
- Fault resilient booting (FRB)
- Processor disable control
- Watchdog timer
- Periodic system management interrupt (SMI) timer
- I^2C master controller for the Intelligent Platform Management Bus (IPMB)
- Two private I^2C management bus interfaces
- Server management software (SMS) and server management mode (SMM) IPMB message receiver
- Event message receiver
- System event log (SEL) management and access
- Sensor data record (SDR) repository management and access
- Processor non-maskable interrupt (NMI) monitoring
- Processor SMI monitoring
- Time-stamp clock
- Secure mode, video blank, and floppy write protect
- Software front panel NMI generation

2.7 Specifications

2.7.1 Environmental Specifications

The IP network server will be tested to the environmental specifications as indicated in Table 2-5. All testing will be performed per procedures defined in the *Intel Environmental Standards Handbook*.

Table 2-5. Environmental Specifications Summary

Environment	Specification
Temperature operating	10^{o} C to 35^{o} C (41^{o} F to 104^{o} F)
Temperature non-operating	-40^{o} C to 70^{o} C (-104^{o} F to 158^{o} F)
Humidity non-operating	95%, non-condensing at temperatures of 23^{o} C (73^{o} F) to 40^{o} C (104^{o} F)
Vibration non-operating	2.2 Grms, 10 minutes per axis on all three axes as per the *Intel Environmental Standards Handbook*
Shock operating	Half-sine 2 G, 11 ms pulse, 100 pulses in each direction, on each of the three axes as per the *Intel Environmental Standards Handbook*
Shock non-operating	Trapezoidal, 25 G, 170 inches/sec delta V, three drops in each direction, on each of the three axes as per *Intel Environmental Standards Handbook*
Safety	UL 1950, CSA 950, IEC 950, TUV/GS EN60950
Emissions	Certified to FCC Class A; tested to CISPR 22 Class A, EN 55022 Class A, VCCI Class A ITE, AS/NZS 3548 Class A
Immunity	Verified to comply with EN 50082-1
Electrostatic discharge (ESD)	Tested to ESD levels up to 15 kilovolts (kV) air discharge and up to 8 kV contact discharge without physical damage as per *Intel Environmental Standards Handbook*
Acoustic	Sound power: < 7.0 BA at ambient temperatures < 24°C measured per *Intel Environmental Standards Handbook*

2.7.2 Physical Specifications

Table 2-6 describes the physical specifications of the IP network server.

Table 2-6. Dimensions and Weight – to be updated

Height	3.45 inches (87.6 mm)
Width	17.14 inches (435.3 mm)
Depth	20 inches (508 mm)
Front clearance	2 inches (76 mm)
Side clearance	1 inches (25 mm)
Rear clearance	3.6 inches (92 mm)

3. Cables and Connectors

This chapter describes interconnections between the various components of the Intel® IP Network Server NSI2U. Also, this chapter includes an overview diagram of the IP network server interconnections, as well as tables describing the signals and pin-outs for the system connectors. Refer to the appropriate server board section or system board sections in this document for other connector signal descriptions and pin-outs.

3.1 Chapter Structure and Outline

The information contained in this chapter is organized into three sections. The information is presented in a modular format, with numbered headings for each major topic and subtopic. The content of each section is summarized as follows:

Section 3.2: Interconnect Block Diagram
Provides an overview of system interconnects.

Section 3.3: Cable and System Interconnect Descriptions
Provides a list of all the connectors and cables in the system.

Section 3.4: User-accessible Interconnects
Describes the form-factor and pin-out of user-accessible interconnects.

3.2 Interconnect Block Diagram

Figure 3-1 shows interconnections for all of the boards used in the IP network server.

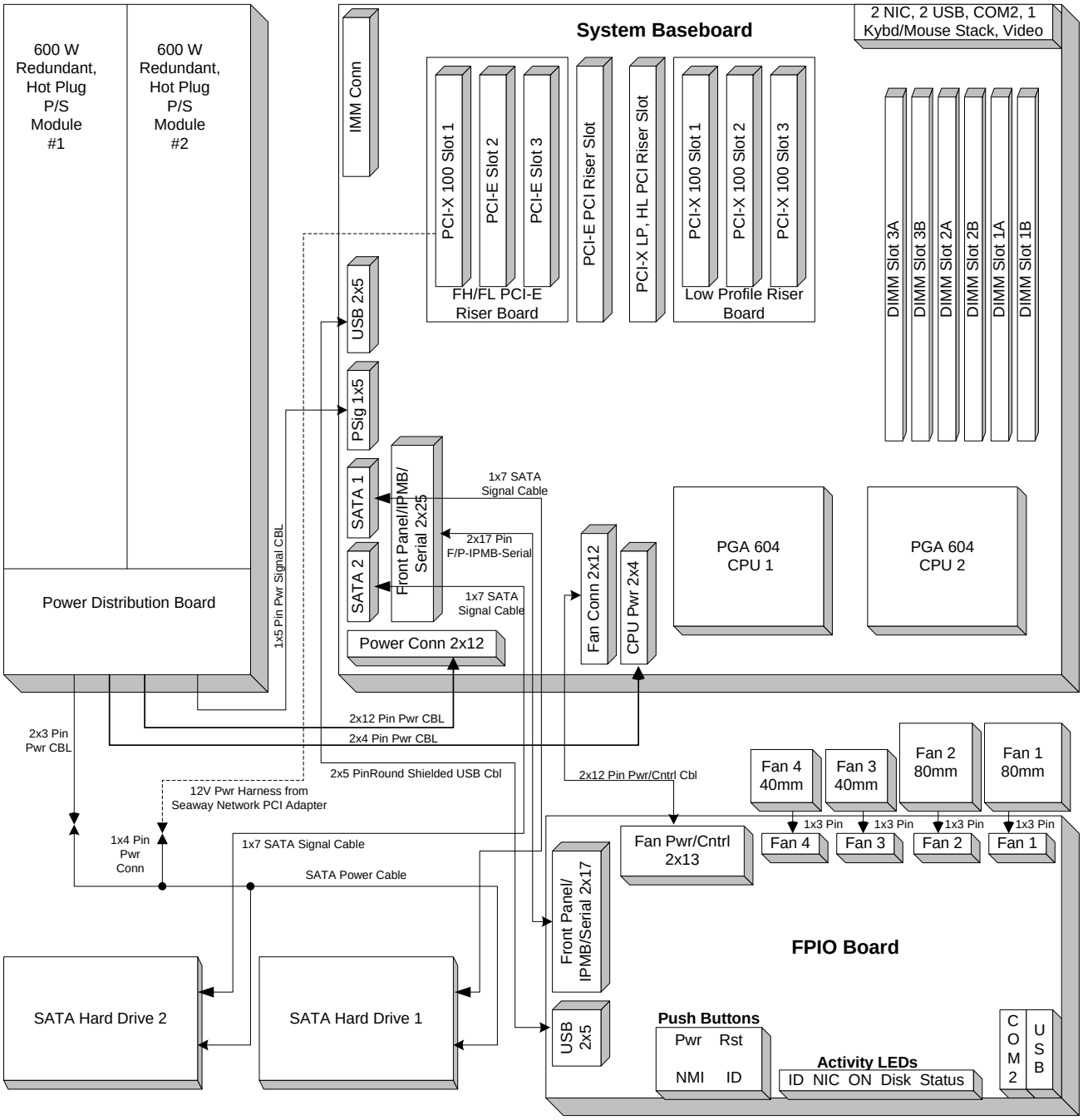


Figure 3-1. Intel® IP Network Server NSI2U Interconnect Block Diagram

3.3 Cable and Interconnect Descriptions

Table 3-1 describes all cables and connectors of the IP network server.

Table 3-1. System Interconnects

System Board	Ref Des	Connector Description	Cable/Device /Board	Ref Des	Connector Description
Jarrell Baseboard Connections					
Baseboard	J1G2	1x5 P/S Signal Connector	P/S Sig Cable	J1G2	1x5 P/S Signal Connector
Baseboard	J3K5	2x12 P/S Power Connector	P/S Pwr Cable	J3K5	2x12 P/S Power Conn
Baseboard	J4J1	2x4 uP Power Connector	P/S uP Pwr Cbl	J9B1	2x4 uP Power Connector
Baseboard	J1F1	1x5 USB Connector	USB Cable	J1F1	2x5 USB Connector
Baseboard	J1J1	2x25 Front Panel Conn	FP Cable	J1J1	2x25 Front Panel Conn
Baseboard	J3K6	2x12 Fan Pwr/Sig Conn	Fan Pwr/Sig Cbl	J3K6	2x12 Fan Pwr/Sig Conn
Baseboard	J1H1	1x4 SATA Signal Conn	SATA Signal Cbl	J1H1	1x4 SATA Signal Conn
Baseboard	J1H2	1x4 SATA Signal Conn	SATA Signal Cbl	J1H2	1x4 SATA Signal Conn
Front Panel Board					
FP Board	J8	2x17 Front Panel Conn	FP Cable	J8	2x17 FP Connector
FP Board	J5	2x5 USB Connector	USB Cable	J5	2x5 USB Connector
FP Board	J7A1	2x12 Fan Pwr/Sig Conn	Fan Pwr/Sig Cbl	J7A1	2x12 Fan Pwr/Sig Conn
FP Board	J1	1x3 Fan Connector	Fan 1		1x3 Fan Connector
FP Board	J2	1x3 Fan Connector	Fan 2		1x3 Fan Connector
FP Board	J3	1x3 Fan Connector	Fan 3		1x3 Fan Connector
FP Board	J4	1x3 Fan Connector	Fan 4		1x3 Fan Connector

3.4 User-accessible Interconnects

3.4.1 Keyboard and Mouse Ports

Two stacked PS/2 ports are provided to support both a keyboard and a mouse. Either PS/2 port can support a mouse or keyboard. The following table details the pin-out of the PS/2 connector.

Table 3-2. Stacked PS/2 Keyboard and Mouse Port Pin-out

Pin	Signal
1	KEYDAT (keyboard data)
2	MSEDAT (mouse data)
3	GND (ground)
4	Fused VCC (+5 V)
5	KEYCLK (keyboard clock)
6	MSECLK (mouse clock)

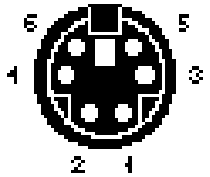


Figure 3-2. Keyboard, Mouse Connector

3.4.2 Serial Port

Two serial ports are provided, one on the front panel and one at the rear I/O using 8-pin RJ-45 connectors.

Table 3-3. Serial Port Connector on rear I/O Port

Pin	Signal Name	Description
1	RTS	Request To Send
2	DTR	Data Terminal Ready
3	TXD	Transmit Data
4	GND	Ground
5	RI	Ring Indicate
6	RXD	Receive Data
7	DSR / DCD	Data Set Ready / Data Carrier Detect1
8	CTS	Clear To Send

Note:

1. A jumper block on the server board will determine whether DSR or DCD is routed to pin 7. The board will have the jumper block configured with DSR enabled at production.

The front panel board has provisions for the COM2 port using a RJ45 connector. This RJ45 connector is accessible behind the front bezel.

Table 3-4. Serial Port Connector on Front Panel

Pin	Signal Name	Description
1	RTS	Request To Send
2	DTR	Data Terminal Ready
3	TXD	Transmit Data
4	GND	Ground
5	In Use	In use signal – when grounded, indicates that COM2 is routed to the front panel RJ45 connector.
6	RXD	Receive Data
7	DSR	Data Set Ready
8	CTS	Clear To Send

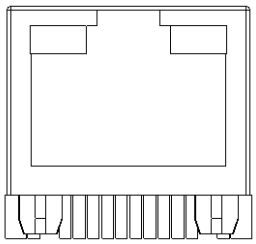


Figure 3-3. Serial Port Connector

3.4.3 Video Port

The video port interface is a standard VGA compatible, 15-pin connector. Onboard video is supplied by an ATI Rage XL video controller with 8 MB of onboard video SGRAM.

Table 3-5. Video Connector

Pin	Signal
1	Red (analog color signal R)
2	Green (analog color signal G)
3	Blue (analog color signal B)
4	No connection
5	GND
6	GND
7	GND
8	GND
9	Fused VCC (+5 V)
10	GND
11	No connection
12	DDCDAT
13	HSYNC (horizontal sync)
14	VSYNC (vertical sync)
15	DDCCLK

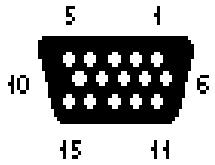


Figure 3-4. Video Connector

3.4.4 Universal Serial Bus (USB) Interface

The server board provides three USB ports. USB ports 0 and 1 are brought out the rear of the unit on the server board, and USB port 2 is routed to the FPIO board. USB port 2 is brought to the front of the system and is accessible without removing the front bezel. The built-in USB ports permit the direct connection of three USB peripherals without an external hub. If more devices are required, an external hub can be connected to any of the built-in ports.

Table 3-6. Single USB Connector

Pin	Signal
1	Fused VCC (+5 V w/over-current monitor of ports 0, 1, and 2)
2	DATAL0 (differential data line paired with DATAH0)
3	DATAH0 (differential data line paired with DATAL0)
4	GND
5	GND
6	GND

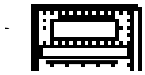


Figure 3-5. USB Connector

3.4.5 Ethernet Connector

The server board provides two NIC RJ45 connectors oriented side by side on the back edge of the board and accessible at the rear I/O panel. The pin-out of each connector is identical and is defined in the following table.

Table 3-7. Ethernet Connector

Pin	Signal Name	Pin	Signal Name
1		9	LAN_MID3N
2	LAN_MID0P	10	P2V5_NIC
3	LAN_MID0N	11	LAN_LINK_1000_L (LED)
4	LAN_MID1P	12	LAN_LINK_100_L_R (LED)
5	LAN_MID2P	13	LAN_ACT_L (LED)
6	LAN_MID2N	14	LAN_LINK_L_R (LED)
7	LAN_MID1N	15	GND
8	LAN_MID3P	16	GND

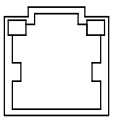


Figure 3-6. Ethernet Connector

3.4.6 AC Power Input for AC-Input Power Supply Cage

A single IEC320-C13 receptacle is provided at the rear of each AC-input power module installed in the system. It is recommended to use an appropriately sized power cord and AC main. Please refer to *Section 7 AC Power Subsystem* of this document for system voltage, frequency, and current draw specifications.

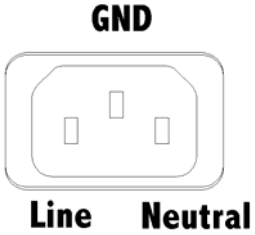


Figure 3-7. AC Power Input Connector

4. Front Panel IO (FPIO) System Board

This chapter describes the basic functions and interface requirements of the Front Panel IO (FPIO) system board that is designed for the IP Network Server.

4.1 Features

- Four switches to control Power-On, Reset, NMI, and the system ID LED
- One system ID LED that can be controlled remotely or by the system ID switch
- Two system activity LEDs that indicate power-on and NIC activity
- One hard drive activity/fault LEDS that indicate activity/fault status for drives 0 and 1
- One system status LED that indicates system status
- Connectors for interfacing to the USB connector, RS232 (via RJ45) port, the front panel connector, and the fan power/control connector on the server board

4.2 Chapter Structure and Outline

The information contained in this chapter is organized into six sections. The information is presented in a modular format, with numbered headings for each major topic and subtopic. The content of each section is summarized as follows:

Section 4.3: Introduction
Provides an overview of the FPIO board, showing primary components and their relationships, and physical board layout diagrams.

Section 4.4: Functional Description of Front Panel Switches and LEDs
Provides a functional description of the front panel switches and LEDs contained on the FPIO board.

Section 4.5: Connector Information
Provides information on all connectors contained on the FPIO board. Gives signal descriptions and the corresponding electrical parameters for each input and output of a given connector.

Section 4.6: Specifications
Describes the electrical, environmental and mechanical specifications.

4.3 Introduction

The FPIO system board provides the means of mounting and electrically connecting switches and indicators for system operation and status. These features are accessible and visible from the front of the chassis. The FPIO system board is designed for use with the SSI compliant server board.

4.4 Functional Description of Front Panel Switches and LEDs

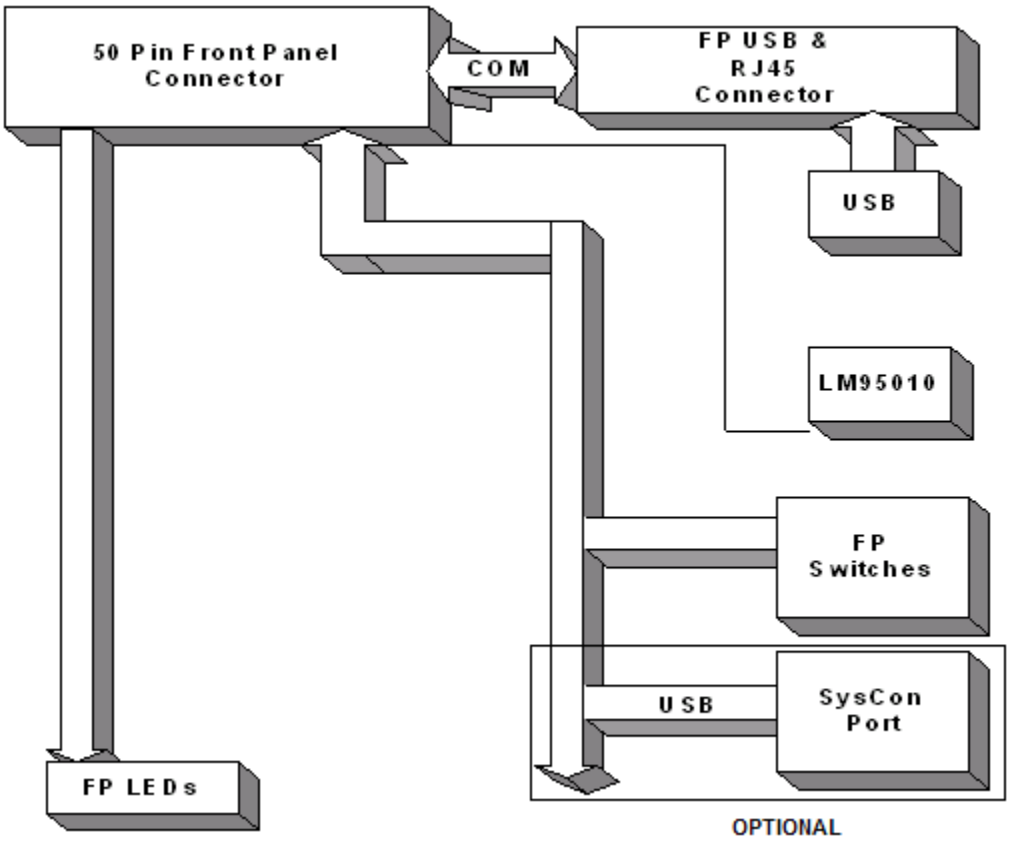


Figure 4-1. Block Diagram of Front Panel Switches and LEDs

4.4.1 Front Panel Switches

The front panel has a power switch, a reset switch, an NMI switch, and a system ID switch. The function of these switches is described in the following table.

Table 4-1. Front Panel Switch Description

Switch	Function
Power Switch	A momentary switch, APCI compliant, used to toggle system power on/off.
Reset Switch	A momentary switch used to reset the system when it is in the power-on state.
NMI Switch	A momentary switch used to instruct the processor to copy system memory to hard disk.
System ID Switch	A momentary switch used to instruct the processor to toggle the state of the system ID LED.

4.4.2 Front Panel LEDs

The following table lists the LED specifications.

Table 4-2. LED Specifications

LED Function	LED Color	Peak Wavelength (nm)	Luminous Intensity Typ(mcd)	Luminous Intensity Min(mcd)
ID	White	N/A	8.9	4.5
NIC	Green	560	4.3	1.7
ON	Green	560	4.3	1.7
DRV 1/0 Activity	Green	568	6.8	4.5
DRV 1/0 Fault	Red	625	7.9	4.0
Status	Green	568	6.8	4.5
Status	Amber	590	11.4	4.5

4.4.3 System Status LED

There are four FPIO system board system status LEDs. The function of these system status LEDs is described in the following table.

Table 4-3. Front Panel System Status LED Description

<table>
<tr><th>Status LED</th><th>Function</th></tr>
<tr><td>On</td><td>The green Power LED indicates that system power is on when it is illuminated continuously. When it is blinking green, it indicates that the system is in ACPI sleep mode.</td></tr>
<tr><td>NIC0/NIC1</td><td>The green NIC activity LED indicates network link presence and activity on either NIC0 or NIC1.</td></tr>
<tr><td>System ID</td><td>The white System ID LED is used to identify a particular system. The LED can be toggled remotely or with the System ID Switch.</td></tr>
<tr><td>Disk 0/Disk 1</td><td>The green/ /red hard drive 0/1 activity/fault LED displays activity or fault status for hard disk drive 0 and hard disk drive 1.</td></tr>
<tr><td>Status</td><td>The green/ /amber status activity/fault LED displays system status for the system as follows:
<table>
<tr><th>Color</th><th>State</th><th>Criticality</th><th>Description</th></tr>
<tr><td>Green</td><td>Solid On</td><td>Ok</td><td>System booted and ready</td></tr>
<tr><td>Green</td><td>~1 Hz blink</td><td>Degraded</td><td>CPU or DIMM disabled</td></tr>
<tr><td>Amber</td><td>~1 Hz blink</td><td>Non-critical</td><td>Redundant fan or power supply failure
Non-critical Fan, Temperature, or Voltage</td></tr>
<tr><td>Amber</td><td>Solid On</td><td>Critical</td><td>Critical Power Supply, Voltage, Fan, or Temperature</td></tr>
<tr><td>Off</td><td>-</td><td>Not Ready</td><td>AC power off, POST error</td></tr>
</table>
</td></tr>
</table>

4.4.3.1 Temperature Sensor

The front panel temperature sensor is an LM95010 SensorPath™ single wire interface temperature sensor that can be read by the ICH5R chipset on the server board. The sensor is located just to the right of the USB connector looking at the front of the unit.

4.5 RJ-45 COM2 Port and USB Ports

4.5.1 RJ-45 COM2 RS-232 Port

The Front Panel I/O (FPIO) board has provision for an RS-232C port using an RJ-45 connector. This is available for use at the front of the chassis. Grounding EMP_INUSE_L disables the rear COM2 port and enables the front port.

Table 4-4. RJ-45 (RS232-C) Pin-out

Pin #	I/O	Signal Name	Description
1	O	SPB_EMP_RTS_L	Request To Send
2	O	SPB_EMP_DTR_L	Data Terminal Ready
3	O	SPB_EMP_SOUT	Serial Out
4	PWR	GND	GND
5	I	EMP_INUSE_L	In Use
6	I	SPB_EMP_SIN	Serial In
7	I	SPB_EMP_DSR_L	Data Set Ready
8	I	SPB_EMP_CTS_L	Clear To Send

4.5.2 USB Port

The FPIO board has provision for USB 1.1 for use at the front of the chassis. A single vertical stacked connector is used for connections.

Table 4-5. USB Pin-out

Pin #	I/O	Signal Name	Description
B1	PWR	VREG_FP_USBPWR	USB_PWR_2
B2	I/O	USB_DM4_FP	USB_BCK3_L
B3	I/O	USB_DP4_FP	USB_BCK3
B4	GND	VSS (GND)	VSS (GND)

4.6 Connector Information

The following table shows all the connectors on the FPIO system board, the interconnect used for each connector, and the destination for the interconnect. In addition, the first column references the location on the following figure of the connector location.

Table 4-6. FPIO Board Connections

FPIO Board Connections				
Loc	**Ref Des**	**Function**	**Interconnect**	**Connects to**
A	J7A1	Fan Control/Sense/Pwr	Cable from SB	The server board
B	J1,J2,J3,J4	Fan Connectors	Fan connector	40mm & 80mm Fans
C	J8	Front Panel Connector	Cable from SB	The server board
D	J5	USB (2 Channels)	Cable from SB	The server board
E	J9	USB/RS232 Ports (Ext.)	External Conn	External USB/RS232 connections

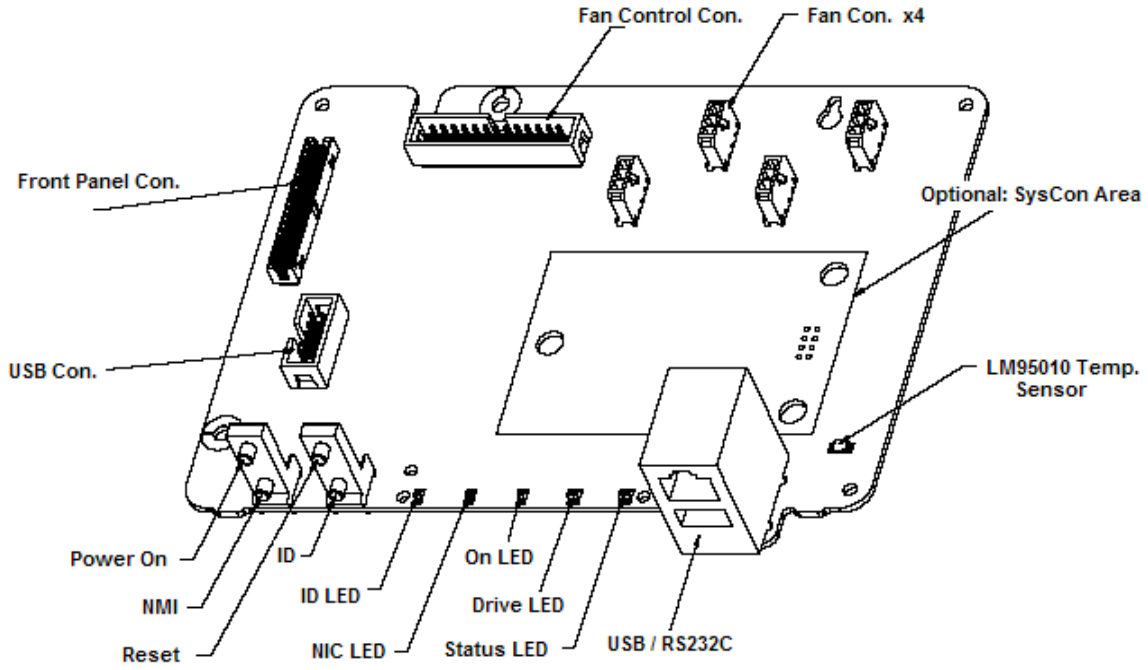


Figure 4-2: FPIO Connector Location

Table 4-7: Connector Housing information

Conn	Function	Intel PN	AML	s/k/l/p*	CNT	HSN
FPIO Board C13071-200						
J7A1	Fan 2x10	201418-976	Foxconn HL16133-D7	y/y/y/y	15u”	94V0
J1 J2 J3 J4	Fan 1x3	C13083-002	Molex 43650-0317 Tyco1445093-3	y/y/y/y y/y/y/y	30u” 30u”	94V0 94V0
J5	USB 2x5	201418-978	Foxconn HL16053-P9	y/y/y/y	15u”	94V0
J8	FP 2x17	744983-005	Foxconn HL54177-D3	y/y/y/y	15u”	94V0
J9	USB/com	680356-003	FXN UB11123-L40	na	30u”	94V0

s/k/l/p* - shrouded/keyed/latching/polarized

The 2x13 fan, the 1x3 fan, and the 2x17 front panel connector pin-outs are shown in the following tables.

4.6.1 FPIO Board Front Panel Connector Pinout

The following table details the pin-out of the front panel connector to the server board.

Table 4-8. Front Panel J8 Connector

Pin	Front Panel Signal	Pin	Front Panel Signal
1	TEMP_PWM_R	2	SPB_DTR_L
3	SPB_DCD_L	4	SPB_RTS_L
5	SPB_CTS_L	6	SPB_SIN
7	SPB_SOUT	8	SPB_DSR_L
9	SPB_EN_L	10	FP_NMI_BTN_L
11	GND	12	LAN_ACT_A_L
13	N/C	14	FP_ID_BTN_L
15	GND	16	FP_RST_BTN_L
17	LAN_ACT_B_L	18	FP_HDD_FLT_LED_R
19	NC	20	FP_PWR_BTN_L
21	Pin Pulled	22	FP_ID_LED_R
23	GND	24	N/C
25	FP_PWR_LED_R	26	P5V_STBY
27	P5V_STBY	28	FP_STATUS_LED2_R
29	N/C	30	FP_STATUS_LED1_R
31	HDD_LED_ACT_R	32	P5V
33	P5V_STBY	34	P5V_STBY

4.6.2 Fan 1x3 Connector Pin-out

The four fans all have the same wire harness and the connector pin-out is shown in the following table.

Table 4-9. Fan 1x3 Connector

Pin	Signal
1	GND
2	Fan Speed Control
3	Fan Tachometer Signal

4.6.3 Fan 2x13 Connector Pin-out

One cable brings the fan speed control voltage to the FPIO board from the server board, and returns the fan tachometer signal from the FPIO board to the server board. This fan 2x13 connector pin-out is shown in the following table.

Table 4-10. Fan 2x13 Connector

Pin	Fan Signal	Pin	Fan Signal
1	BB_LED_FAN4_R	2	BB_LED_FAN2_R
3	BB_LED_FAN3_R	4	BB_LED_FAN1_R
5	ZZ_FANCON8	6	ZZ_FANCON4
7	ZZ_FANCON7	8	ZZ_FANCON3
9	ZZ_FANCON6	10	ZZ_FANCON2
11	ZZ_FANCON5	12	ZZ_FANCON4
13	GND	14	GND
15	GND	16	GND
17	FAN_SPEED_CNTL2	18	FAN_SPEED_CNTL1
19	FAN_SPEED_CNTL2	20	FAN_SPEED_CNTL2
21	BB_LED_FAN7_R	22	BB_LED_FAN5_R
23	BB_LED_FAN8_R	24	BB_LED_FAN6_R
25	NC	26	NC

4.7 Specifications

4.7.1 Electrical Specifications

DC specifications for the front panel board power connectors are summarized in this section excluding disk drive power. All power rails must operate within +/- 5% voltage range.

Table 4-11. Maximum Power Requirements (mA)

12V	5V	3.3V	+5V_STBY
N/A	86(mA)	N/A	184(mA)

4.7.2 Mechanical Specifications

The following figure shows the mechanical specifications of the front panel board. All dimensions are given in inches.

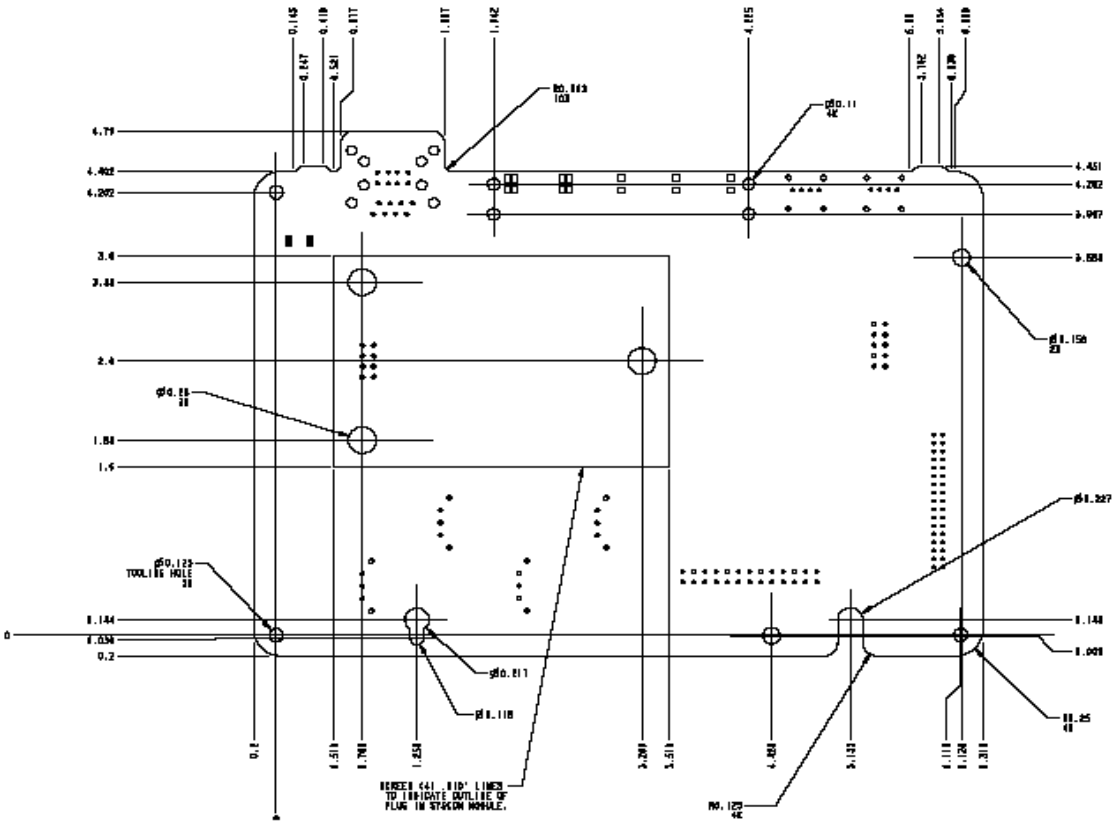


Figure 4-3. Front Panel Board Mechanical Specifications

5. Low Profile/Half-Length PCI-X Riser Board

This chapter describes the design and external interface of the Low Profile/Half-Length PCI-X riser board. Features of the Low Profile/Half-Length PCI-X riser board include:

- Three 3.3 V 64-bit PCI-X slots

5.1 Chapter Structure and Outline

The information contained in this chapter is organized into four sections. The information is presented in a modular format, with numbered headings for each major topic and subtopic. The content of each section is summarized as follows:

Section 5.2: Introduction:
Provides an overview of the Low Profile/Half-Length PCI-X riser board, showing primary components and their relationships, and physical board layout diagrams.

Section 5.3: Functional Description:
Provides a functional description of the Low Profile/Half-Length PCI-X riser board.

Section 5.4: Connector Interface:
Gives signal descriptions and the corresponding electrical parameters for each input and output of a given connector.

Section 5.5: Specifications:
Describes the electrical, environmental and mechanical specifications.

5.2 Introduction

The Low Profile/Half-Length PCI-X riser card supports three 3.3 V 64-bit slots. The bus speed varies from 33MHz to 133MHz depending on the type of PCI adapters configured in the Low Profile/Half-Length PCI-X riser card. This is described in the Intel® Server Board SE7520JR2 Technical Product Specification.

Figure 5-1 is the layout of the Low Profile/Half-Length PCI-X riser board.

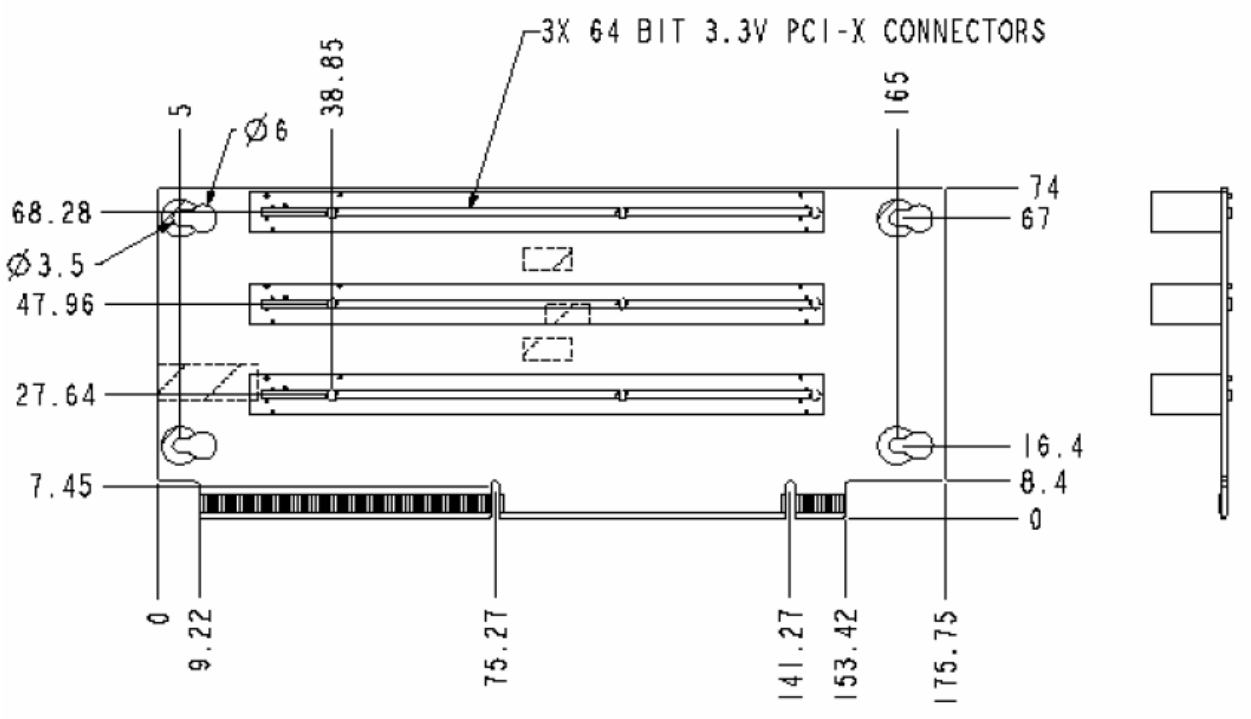


Figure 5-1. Low Profile/Half-Length PCI-X Riser Board Layout

5.3 Functional Description

The Low Profile/Half-Length PCI-X riser card has three 3.3 V 64-bit slots with a maximum bus speed of 133MHz.

IDSELs are device ID 17 for slot 1, device ID 18 for slot 2 and device ID 19 for slot 3.

5.4 Connector Interface

Table 5-1 provides the low profile riser slot pin assignments.

Table 5-1. Low Profile Riser Slot Pin-out

Pin-Side B	PCI Spec Signal	Description	Pin-Side A	PCI Spec Signal	Description
101	-12V		101	RSVD	
100	RSVD		100	+12V	
99	GND		99	RSVD	
98	RSVD		98	+5V	
97	+5V		97	+5V	
96	+5V		96	INTA#	This pin will be connected on the 2U riser to INT_A# of the bottom PCI slot, INT_D# of the middle slot and

Pin-Side B	PCI Spec Signal	Description	Pin-Side A	PCI Spec Signal	Description
					INT_C# of the top slot.
95	INTB#	This pin will be connected on the 2U riser to INT_B# of the bottom PCI slot, INT_A# of the middle slot and INT_D# of the top slot.	95	INTC#	This pin will be used by 1U/2U riser to bring the INT_C# interrupt on the bottom PCI slot down to the baseboard.
94	INTD#	This pin will be used by 1U/2U riser to bring the INT_D# interrupt on the bottom PCI slot down to the baseboard.	94	+5V	
93	+5V		93	GND	
92	GND		92	REQ3#	Highest PCI Slot (SLOT3)
91	CLK3	Highest PCI Slot (SLOT3)	91	GND	
90	GND		90	GNT3#	Highest PCI Slot (SLOT3)
89	CLK2	Middle PCI Slot (SLOT2)	89	+5V	Was GND
88	GND		88	RSVD	
87	REQ2#	Middle PCI Slot (SLOT2)	87	+5V	Was GND
86	GND		86	LECC4	
85	LECC5		85	GND	Was Vio 3.3V or 1.5V
84	GND		84	LECC3	
83	+3.3V		83	GNT2#	
82	LECC2		82	3.3VAUX	3 slots at 375ma
81	GND		81	RST#	
80	CLK1	Lowest PCI slot (SLOT1)	80	+3.3V	Was VIO 3.3V or 1.5V
79	GND		79	GNT1#	Lowest PCI slot (SLOT1)
78	REQ1#	Lowest PCI slot (SLOT1)	78	GND	
77	+3.3V	Was 3.3V or 1.5V	77	PME#	
76	AD[31]		76	AD[30]	
75	AD[29]		75	+3.3V	
74	GND		74	AD[28]	
73	AD[27]		73	AD[26]	
72	AD[25]		72	GND	
71	+3.3V		71	AD[24]	
70	C/BE[3]#		70	RSVD	Lower slot IDSEL=AD17 Middle Slot=AD18, Top slot=AD19
69	AD[23]		69	+3.3V	
68	GND		68	AD[22]	
67	AD[21]		67	AD[20]	
66	AD[19]		66	GND	
65	+3.3V		65	AD[18]	
64	AD[17]		64	AD[16]	
63	C/BE[2]#		63	+3.3V	
62	GND		62	FRAME#	
61	IRDY#		61	GND	

Pin-Side B	PCI Spec Signal	Description	Pin-Side A	PCI Spec Signal	Description
		KEYWAY			KEYWAY
		KEYWAY			KEYWAY
60	+3.3V		60	TRDY#	
59	DEVSEL#		59	GND	
58	PCI-XCAP		58	STOP#	
57	LOCK#		57	+3.3V	
56	PERR#		56	SMBD	Daisy chain to all slots
55	+3.3V		55	SMBCLK	Daisy chain to all slots
54	SERR#		54	GND	
53	+3.3V		53	PAR /ECC0	
52	C/BE[1]#		52	AD[15]	
51	AD[14]		51	+3.3V	
50	GND		50	AD[13]	
49	AD[12]		49	AD[11]	
47	AD[10]		47	GND	
47	M66EN		47	AD[09]	
46	Mode 2		46	C/BE[0]#	
45	GND		45	+3.3V	Was GND
44	AD[08]		44	+3.3V	
43	AD[07]		43	+3.3V	
42	+3.3V		42	AD[06]	
41	AD[05]		41	AD[04]	
40	AD[03]		40	GND	
39	GND		39	AD[02]	
38	AD[01]		38	AD[00]	
37	+3.3V	Was Vio 3.3V or 1.5V	37	+3.3V	Was Vio 3.3V or 1.5V
36	ACK64# /ECC1		36	REQ64# /ECC6	
35	+5V		35	+5V	
34	+5V		34	+5V	
33	RSVD		33	GND	
32	GND		32	C/BE[7]#	
31	C/BE[6]#		31	C/BE[5]#	
30	C/BE4#		30	V (I/O)	3.3V or 1.5V
29	GND		29	PAR64 /ECC7	
28	AD[63]		28	AD[62]	
27	AD[61]		27	GND	
26	V (I/O)	3.3V or 1.5V	26	AD[60]	
25	AD[59]		25	AD[58]	
24	AD[57]		24	GND	
23	GND		23	AD[56]	

Pin-Side B	PCI Spec Signal	Description	Pin-Side A	PCI Spec Signal	Description
22	AD[55]		22	AD[54]	
21	AD[53]		21	V (I/O)	3.3V or 1.5V
20	GND		20	AD[52]	
19	AD[51]		19	AD[50]	
18	AD[49]		18	GND	
17	V (I/O)	3.3V or 1.5V	17	AD[48]	
16	AD[47]		16	AD[46]	
15	AD[45]		15	GND	
14	GND		14	AD[44]	
13	AD[43]		13	AD[42]	
12	AD[41]		12	V (I/O)	3.3V or 1.5V
		KEYWAY			KEYWAY
		KEYWAY			KEYWAY
11	GND		11	AD[40]	
10	AD[39]		10	AD[38]	
9	AD[37]		9	GND	
8	V (I/O)	3.3V or 1.5V	8	AD[36]	
7	AD[35]		7	AD[34]	
6	AD[33]		6	GND	
5	GND		5	AD[32]	
4			4		
3	PRSNT_N	0=Riser Present	3	GND	
2	GND		2		
1	Size	0=1U, 1= 2U	1	GND	

5V = 12 = 12 or 6 amps 3 slots needs 6 amps for 3 10W boards

3.3V= 19 = 19 or 9.5 amps 3 slots needs 9 amps for 3 10W boards

202 pin connector length = 139.45mm=5.49”

5.5 Electrical Specification

The maximum power per slot is 25 W. This maximum power per slot conforms to *PCI Specification 2.2*.

6. Full Height/Full-Length PCI-E Riser Board

This chapter describes the design and external interface of the Full Height/Full-Length PCI-E riser board. Features of the Full Height/Full-Length PCI-E riser board include:

- Two x4 PCI-E slots
- One 3.3 V 64-bit PCI slots

6.1 Chapter Structure and Outline

The information contained in this chapter is organized into four sections. The information is presented in a modular format, with numbered headings for each major topic and subtopic. The content of each section is summarized as follows:

Section 6.2: Introduction:
Provides an overview of the Full Height/Full-Length PCI-X riser board, showing primary components and their relationships, and physical board layout diagrams.

Section 6.3: Functional Description:
Provides a functional description of the Full Height/Full-Length PCI-X riser board.

Section 6.4: Connector Interface:
Gives signal descriptions and the corresponding electrical parameters for each input and output of a given connector.

Section 6.5: Specifications:
Describes the electrical, environmental and mechanical specifications.

6.2 Introduction

The Full Height/Full-Length PCI-E riser card supports two x4 PCI-E slots and one 3.3V 64-bit PCI-X slot. For the PCI-X slot, the bus speed varies from 33MHz to 133MHz depending on the type of PCI adapter configured in the slot. This is described in the Intel® Server Board SE7520JR2 Technical Product Specification.

Figure 6-1 is a drawing of the Full Height/Full-Length PCI-E riser board layout.

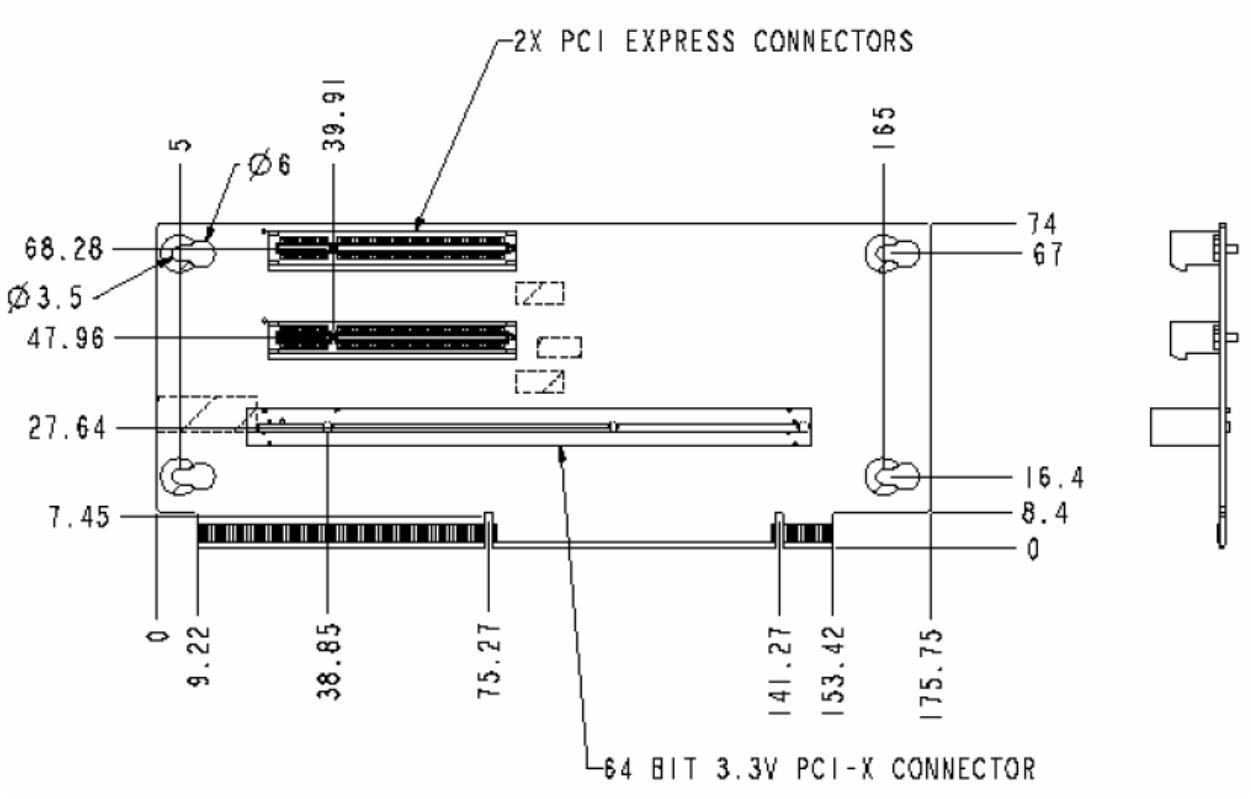


Figure 6-1. Full Height/Full-Length PCI-E Riser Board Layout

6.3 Functional Description

The Full Height/Full-Length PCI-E riser card has two PCI-E slots and one 3.3 V 64-bit PCI-X slot with a maximum bus speed of 133MHz.

IDSELs are device ID 17 for slot 1, device ID 18 for slot 2 and device ID 19 for slot 3.

6.4 Connector Interface

Table 6-1 provides the pin-out for the full height riser slot.

Table 6-1. Full Height Riser Slot Pin-out

Pin-Side B	PCI Spec Signal	Description	Pin-Side A	PCI Spec Signal	Description
140	12V		140	12V	
139	12V		139	12V	
138	Ground		138	GND	
137	-12V		137	3.3VAux	375ma per slot and 3 slots
136	12V		136	Wake#	
135	GND		135	12V	Two slots = 4 amps
134	REFCLK2+	FL-3GIO Slot 2/PXH - DIF5P	134	3.3V	
133	REFCLK2+	FL-3GIO Slot 2/PXH - DIF5N	133	PERST_N	
132	GND		132	GND	1 amp per pin
131	GND		131	REFCLK1+	FL-3GIO Slot 1 – DIF4P
130	HSOp(0)		130	REFCLK1+	FL-3GIO Slot 1 – DIF4N
129	HSOn(0)		129	GND	
128	GND		128	HSIp(0)	
127	GND		127	HSIn(0)	
126	HSOp(1)		126	GND	
125	HSOn(1)		125	GND	
124	GND		124	HSIp(1)	
123	GND		123	HSIn(1)	
122	HSOp(2)		122	GND	
121	HSOn(2)		121	GND	
120	GND		120	HSIp(2)	
119	GND		119	HSIn(2)	
118	HSOp(3)		118	GND	
117	HSOn(3)		117	GND	
116	GND		116	HSIp(3)	
115	GND		115	HSIn(3)	
114	HSOp(4)		114	GND	
113	HSOn(4)		113	GND	
112	GND		112	HSIp(4)	
111	GND		111	HSIn(4)	
110	HSOp(5)		110	GND	
109	HSOn(6)		109	GND	
108	GND		108	HSIp(5)	
107	GND		107	HSIn(5)	

Pin-Side B	PCI Spec Signal	Description	Pin-Side A	PCI Spec Signal	Description
106	HSOp(6)		106	GND	
105	HSOn(6)		105	GND	
104	GND		104	HSIp(6)	
103	GND		103	HSIn(6)	
102	HSOp(7)		102	GND	
101	HSOn(7)		101	GND	
100	GND		100	HSIp(7)	
99	+5V		99	HSIn(7)	
98	INTB#	This pin will be connected on the 2U riser to INT_B# of the bottom PCI slot, INT_A# of the middle slot and INT_D# of the top slot.	98	GND	
97	INTD#	This pin will be used by 1U/2U riser to bring the INT_B# interrupt from the top and INT_C# from the middle PCI slot down to the baseboard.	97	ZCR_PRSNT_L	From TDI of lowest slot only
96	+5V		96	+5V	
95	Reserved	SLOT_ID_FL, not required as the risers are unique.	95	+5V	
94	+5V		94	ZCR_MSKID_L	From TMS of lowest slot only
93	IOP INTA	SCSI Interrupt A to ZCR. This pin will be used by 1U/2U riser to bring the INT_C# interrupt on the bottom PCI slot down to the baseboard	93	+5V	
92	IOP INTB	SCSI Interrupt B to ZCR. This pin will be used by 1U/2U riser to bring the INT_D# interrupt on the bottom PCI slot down to the baseboard	92	INTA#	This pin will be connected on the 2U riser to INT_A# of the bottom PCI slot, INT_D# of the middle slot and INT_C# of the top slot.
91	GND		91	INTC#	This pin will be used by 1U/2U riser to bring the INT_A# interrupt from the top and INT_B# from the middle PCI slot down to the baseboard.
90	CLK3	Highest PCI Slot (SLOT3)	90	GND	
89	GND		89	REQ3#	Highest PCI Slot (SLOT3)
88	CLK2	Middle PCI Slot (SLOT2)	88	GND	
87	GND		87	GNT3#	Highest PCI Slot (SLOT3)
86	REQ2#	Middle PCI Slot (SLOT2)	86	GND	
85	GND		85	RST#	
84	Reserved		84	GND	
83	GND		83	Reserved	
	KEY			KEY	
	KEY	End of x16 PCI-Express connector		KEY	
82	Reserved		82	+5V	Was Vio 3.3V or 1.5V

Pin-Side B	PCI Spec Signal	Description	Pin-Side A	PCI Spec Signal	Description
81	GND		81	Reserved	
80	CLK1	Lowest PCI slot (SLOT1)	80	GND	
79	Ground		79	GNT2#	Middle PCI Slot (SLOT2)
78	REQ1#	Lowest PCI slot (SLOT1)	78	+3.3V	Was Vio 3.3V or 1.5V
77	+3.3V	Was Vio 3.3V or 1.5V	77	GNT1#	Lowest PCI slot (SLOT1)
76	PME2#	active riser only, PME needed per PCI segment, reserved for passive riser	76	Ground	
75	AD[31]		75	PME1#	for passive slots on both passive and active riser
74	AD[29]		74	PME3#	active riser only, PME needed per PCI segment reserved for passive riser
73	Ground		73	AD[30]	AD[31]
72	AD[27]		72	+3.3V	
71	AD[25]		71	AD[28]	
70	+3.3V		70	AD[26]	
69	C/BE[3]#		69	Ground	
68	AD[23]		68	AD[24]	
67	Ground		67	RSVRD	Reserved
66	AD[21]		66	+3.3V	
65	AD[19]		65	AD[22]	
64	+3.3V		64	AD[20]	
63	AD[17]		63	Ground	
62	C/BE[2]#		62	AD[18]	
61	Ground		61	AD[16]	
60	IRDY#		60	+3.3V	
59	+3.3V		59	FRAME#	
58	DEVSEL#		58	Ground	
57	PCI-XCAP		57	TRDY#	
56	LOCK#		56	Ground	
55	PERR#		55	STOP#	
54	+3.3V		54	+3.3V	
53	SERR#		53	SMBD	Daisy chain to all slots
52	+3.3V		52	SMBCLK	Daisy chain to all slots
51	C/BE[1]#		51	Ground	
50	AD[14]		50	PAR	
49	Ground		49	AD[15]	
48	AD[12]		48	+3.3V	
47	AD[10]		47	AD[13]	
46	M66EN		46	AD[11]	
45	Ground		45	Ground	
44	Ground		44	AD[09]	
43	AD[08]		43	C/BE[0]#	
42	AD[07]		42	+3.3V	

Pin-Side B	PCI Spec Signal	Description	Pin-Side A	PCI Spec Signal	Description
41	+3.3V		41	AD[06]	
40	AD[05]		40	AD[04]	
39	AD[03]		39	Ground	
38	Ground		38	AD[02]	
37	AD[01]		37	AD[00]	
36	+3.3V	Was Vio 3.3V or 1.5V	36	+3.3V	Was Vio 3.3V or 1.5V
35	ACK64#		35	REQ64#	
34	+5V		34	+5V	
33	+5V		33	+5V	
32	Reserved		32	+5V	Was gnd
31	Ground		31	C/BE[7]#	
30	C/BE[6]#		30	C/BE[5]#	
29	C/BE[4]#		29	Ground	Was VIO
28	Ground		28	PAR64	
27	AD[63]		27	AD[62]	
26	AD[61]		26	3.3V	Was GND
25	3.3V		25	AD[60]	
24	AD[59]		24	AD[58]	
23	AD[57]		23	Ground	
22	Ground		22	AD[56]	
21	AD[55]		21	AD[54]	
20	AD[53]		20	3.3V	
19	Ground		19	AD[52]	
18	AD[51]		18	AD[50]	
17	AD[49]		17	Ground	
16	3.3V		16	AD[48]	
15	AD[47]		15	AD[46]	
14	AD[45]		14	Ground	
13	Ground		13	AD[44]	
12	AD[43]		12	AD[42]	
KEY		Reversed PCI-Express	KEY		
KEY		Reversed PCI-Express	KEY		
11	AD[41]		11	3.3V	V
10	Ground		10	AD[40]	
9	AD[39]		9	AD[38]	
8	AD[37]		8	Ground	
7	3.3V		7	AD[36]	
6	AD[35]		6	AD[34]	
5	AD[33]		5	Ground	
4	Ground		4	AD[32]	
3	Type1	Type(1:0) (1U)00 = PCI-Express, (1U)01 = PCI (1U)10 = N/A	3	PXH_RST_N	Input to reset the PXH on the active Riser

Pin-Side B	PCI Spec Signal	Description	Pin-Side A	PCI Spec Signal	Description
		(1U)11 = N/A			
2	Type0	(2U)00=2xPCI-Express+PCI (2U)01=3x PCI (2U)10=PXH 3 PCI-X-D (2U)11=No Riser	2	Ground	
1	Size	0=1U, 1 = 2U	1	PXH_PWR OK	Input to indicate to PXH on active riser that baseboard power is OK

6.5 Electrical Specification

The maximum power per slot is 25 W. This maximum power per slot conforms to *PCI Specification 2.2*.

7. AC Power Subsystem

This chapter defines the features and functionality of the AC-input switching power subsystem. The AC power supply will not be NEBS hardened, so NEBS certification of an IP network server configured with an AC power subsystem will not be possible.

7.1 Features

- 600 W output capability in full AC input voltage range
- Power good indication LEDs
- Predictive failure warning
- External cooling fans with multi-speed capability
- Remote sense of 3.3 V, 5 V, and 12 Vdc outputs
- Brown out protection and recovery
- Built-in overloading protection capability
- Onboard field replaceable unit (FRU) information
- I^2C interface for server management functions
- Integral handle for insertion/extraction

7.2 Chapter Structure and Outline

The information contained in this chapter is organized into two sections. The information is presented in a modular format, with numbered headings for each major topic and subtopic. The content of each section is summarized as follows:

Section 7.3: AC-input Power Supply Cage
Provides an overview of the AC-input power cage.

Section 7.4: AC-input Power Supply Module
Provides an overview of the AC-input power supply module.

7.3 AC-input Power Supply Cage

7.3.1 AC-input Power Supply Cage Mechanical Specification

The AC-input power supply cage can support up to two 600W SSI Thin Power Supply (TPS) modules in a 1+1 configuration or a 1+0 configuration. A mechanical drawing for the power supply cage is shown below.

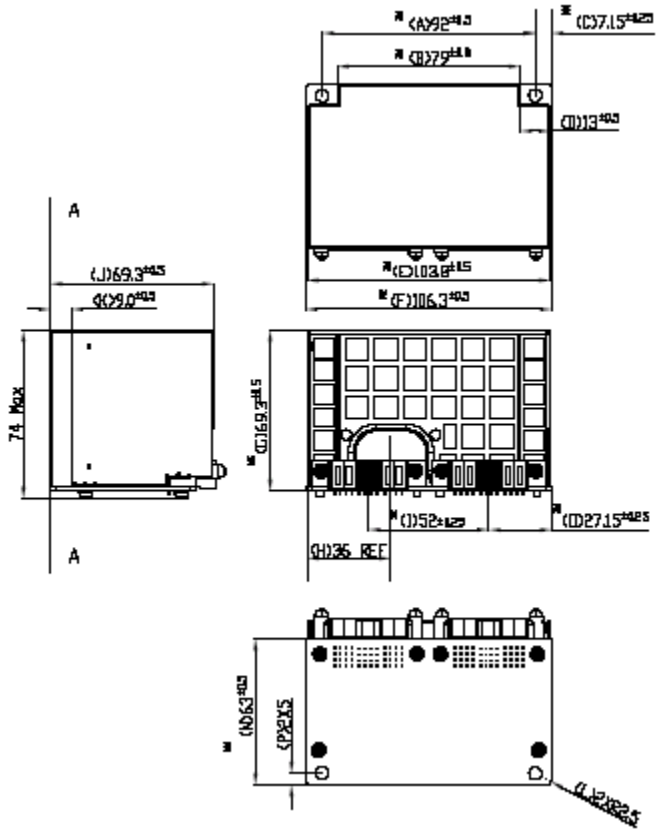
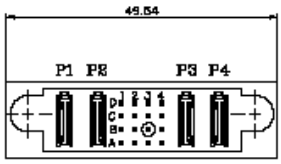


Figure 7-1. Power Supply Cage Mechanical Drawing



OUTPUT CONNECTOR DIAGRAM
B3 IS SHORTENED.

OUTPUT CONNECTOR : FCI 51939-136
PIN ASSIGNMENT:

Signal Pins				
POSITION	1	2	3	4
D	+12VRS	-12V	+5VSB	15VCC
C	PWOK	RS RTN	+5VSB	A0
B	+12VLS	RESERVE	PS KILL	A1
A	PS ON#	SDA	SCL	PS ALERT#
Power Blades				
P1	P2	P3	P4	
+12V	+12V	RTN	RTN	

Figure 7-2. Power Supply Cage Input Connector Drawing and Pin-out

7.3.2 Power Supply Cage Wire Harness

The power distribution board connects to the system via a wire harness. The harness size, connectors, and pin outs are shown below. Listed or recognized component appliance wiring material (AVLV2), VW-1 flame rating, rated 105°C Min, 300Vdc Min shall be used for all output wiring.

Table 7-1. Cable Lengths

From	Length mm	To connector #	No of pins	Description
Backplane cover exit hole	125, turn 90°	P1	2x12	Server board Power Connector
Backplane cover exit hole	320	P2	2x4	Processor Power Connector
Backplane cover exit hole	290	P3	1x5	Power Signal Connector
Backplane cover exit hole	385	P4	1x3	5V Riser Power Connector
Backplane cover exit hole	110	P5	2x3	Hard Drive Interface Board Power Connector

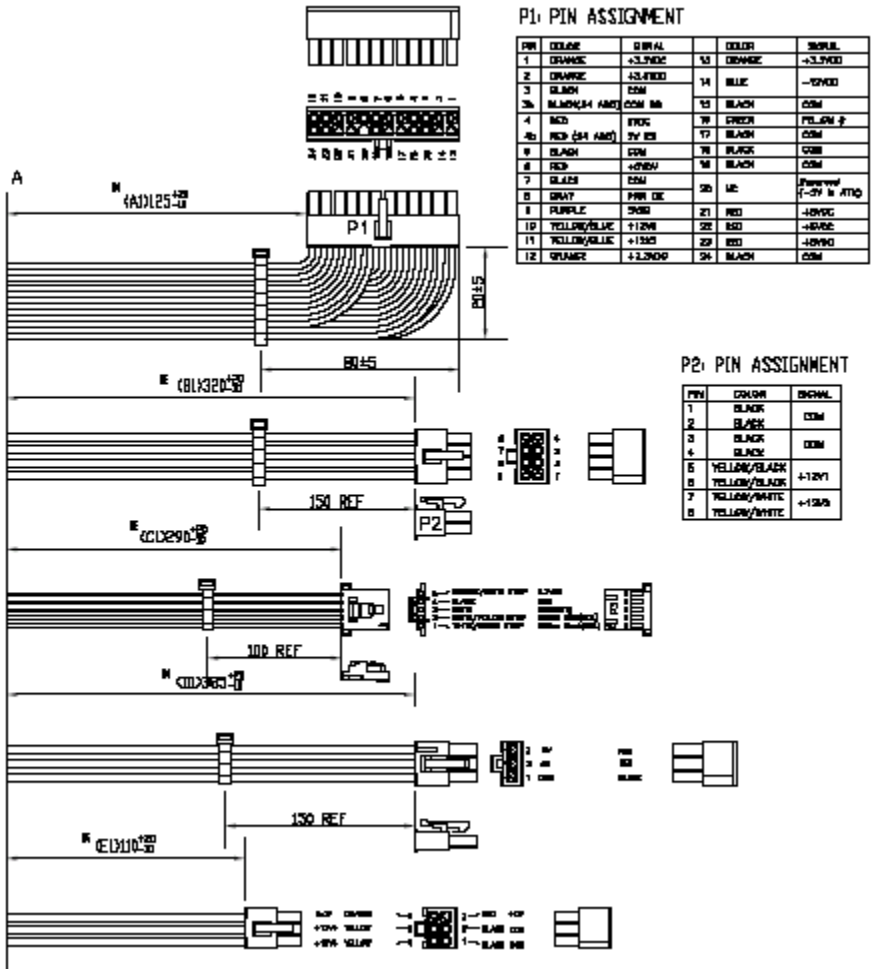


Figure 7-3. Output Wire Harness Detail

7.3.3 P1 Server Board Power Connector

A 24-pin Molex* 39-01-2245 (or equivalent) connector and harness from the power supply cage provides the server board with the required voltages and interface signals. The following table provides the connector pin-out.

Table 7-2. 24-pin Server Board Power Connector Pin-out

PIN	SIGNALS	18 AWG COLOR	PIN	SIGNAL	18 AWG COLORS
1	+3.3 VDC	Orange	12	+3.3 VDC	Orange
2	+3.3 VDC	Orange	13	+3.3 VDC	Orange
3*	COM (GND)	Black	14	-12 VDC	Blue
	COM	Black (24 AWG)	15	COM	Black
4*	5 VDC	Red	16	PS_ON#	Green
	5V RS	Red (24 AWG)	17	COM	Black
5	COM	Black	18	COM	Black
6	+5 VDC	Red	19	COM	Black
7	COM	Black	20	*Reserved (-5V in ATX)*	*NC*
8	PWR OK	Gray	21	+5 VDC	Red
9	5VSB	Purple	22	+5 VDC	Red
10	+12 V3	Yellow/Blue Stripe	23	+5 VDC	Red
11	+12 V3	Yellow/Blue Stripe	24	COM	Black

Note:
* Remote Sense wire double crimped.

7.3.4 P2 Processor Power Connector

An 8-pin Molex 39-01-2085 (or equivalent) connector and harness from the power supply cage provides the server board with the required +12V power required for the processors. The following table provides the connector pin-out.

Table 7-3. P2 Processor Power Connector Pin-out

PIN	SIGNAL	18 AWG COLOR	PIN	SIGNAL	18 AWG COLOR
1	COM	Black	5	+12 V1	Yellow/Black Stripe
2	COM	Black	6	+12 V1	Yellow/Black Stripe
3	COM	Black	7	+12 V2	Yellow/White Stripe
4	COM	Black	8	+12 V2	Yellow/White Stripe

Note:
The 12V remote sense should be connected just before the 240VA current sense resistors on the PDB.

7.3.5 P3 Power Signal Cable

A 5-wire cable with a Molex 50-57-9705 (or equivalent) female housing connector is used to direct power management signals to the server board. The following table shows the pin-out.

Table 7-4. P3 Power Signal Cable Pin-out

Pin	Signal	24 AWG Colors	Description
1	SMBus Clock (SCL)	White/Green Stripe	Serial Clock.
2	SMBus Data (SDL)	White/Yellow Stripe	Serial Data. Information from the power supply.
3	SMBAlert#	White	Indicates power supply is operating beyond its limits and has failed or may fail soon.
4	COM	Black	Return remote sense
5	3.3RS	Orange/White Stripe	3.3V sense

Notes:

- It is recommended to use gold plated signal connector contacts on both the PDB connector and the server board header.
- If the server signal connector is unplugged, the PS/PDB-combo shall not shut down or go into an OVP condition.

7.3.6 P4 5V Riser Power Connector

A 3-wire cable with a Molex Mini-Fit Jr. PN# 39-01-4031 connector is used to provide power to the 5 V riser.

Table 7-5. P4 5V Riser Power Connector Pin-out

Pin	Signal	22 AWG COLOR
1	COM	Black
2	5V	Red
3	5V	Red

7.3.7 P5 Hard Drive Interface Board Power Connector

A 3-wire cable with a Molex Mini-Fit Jr. PN# 39-01-2065 connector is used to provide power to the FPIO system board for system logic power, for peripheral drive power, and for disk drive power.

Table 7-6. P5 Hard Drive Interface Board Power Connector Pin-out

PIN	SIGNAL	18 AWG Colors
1	COM	Black
2	COM	Black
3	5V	Red
4	12V4	Yellow
5	12V4	Yellow
6	3.3V	Orange

7.3.8 Output Current Requirements

This describes the +12V output power requirements from the power distribution board with either one or two ERP700W power supply module(s) plugged into the input of the power distribution board.

Table 7-7. +12V Outputs Load Ratings

	+12V1	+12V2	+12V3	+12V4
MAX Load	16A	16A	16A	16A
MIN Static / Dynamic Load	0.75A	0.75A	0.5A	0.5A
Peak load (12 seconds)	18A	18A	18A	18A
Max Output Power	12V x16A =192W	12V x16A =192W	12V x16A =192W	12V x16A =192W

Notes:
The combined total power limit for ALL outputs is 580W max.
+12V1/2/3/4 combined output limit = 40A / 56A pk max.

The following table defines power and current ratings of the two DC-to-DC converters located on the PDB, each powered from +12V rail. The converters must meet both static and dynamic voltage regulation requirements for the minimum and maximum loading conditions.

Table 7-8. DC/DC Converters Load Ratings

	+12VDC Input DC/DC Converters	
	+3.3V Converter	**+5V Converter**
MAX Load	20A	26A
MIN Static / Dynamic Load	0.5A	0.5A
Max Output Power, see note 1	3.3V x20A =66W	5V x26A =130W

Note:
3.3V / 5V combined power limit: 150W max.

7.3.9 Hot-swapping Power Modules

The AC-input power supply cage is capable of supporting hot-swapping of power supply modules in a 1+1 configuration. Hot-swapping a power supply module is the process of extracting and inserting a power supply module from a functioning system.

7.3.10 Intelligent Cage Functions

The power supply module and power distribution board (PDB) combination shall provide a monitoring interface to the system over a server management bus. Devices should be compatible with both SMBus 2.0 'high power' and I^2C V_{dd} based power and drive. This bus may operate inside the power supply module and PDB at 5V (powered from stand-by voltage) but, looking from the system server management into the power supply module and PDB combination, it shall be compatible with the 3.3V bus. A bi-directional I2C voltage translator IC, such as GTL2002 or similar, may be employed on the PDB. The SMBus pull-ups are located on the server board.

The power distribution board's I2C serial bus will have a dual function: to provide power supply module and PDB monitoring features and to convey the stored FRU data in the power supply module and PDB EEPROM.

7.3.11 FRU Data

The power supply cage contains a 2 KB EEPROM device that contains FRU data for the cage according to the IPMI spec. Each separate output is given a different number for identification purposes.

7.4 AC-input Power Supply Module

7.4.1 AC-input Power Supply Module Mechanical Specification

The AC-input power system supports one 600W SSI Thin Power Supply (TPS) module for a non-redundant configuration, or two in a 1+1 redundant configuration.

7.4.1.1 Power Supply Module Mechanical Drawing

The power supply module contains one 40mm fan. However, a fan in the AC-input power supply cage provides cooling to the module(s). The module provides a handle to assist in insertion and extraction and can be inserted and extracted without the assistance of tools.

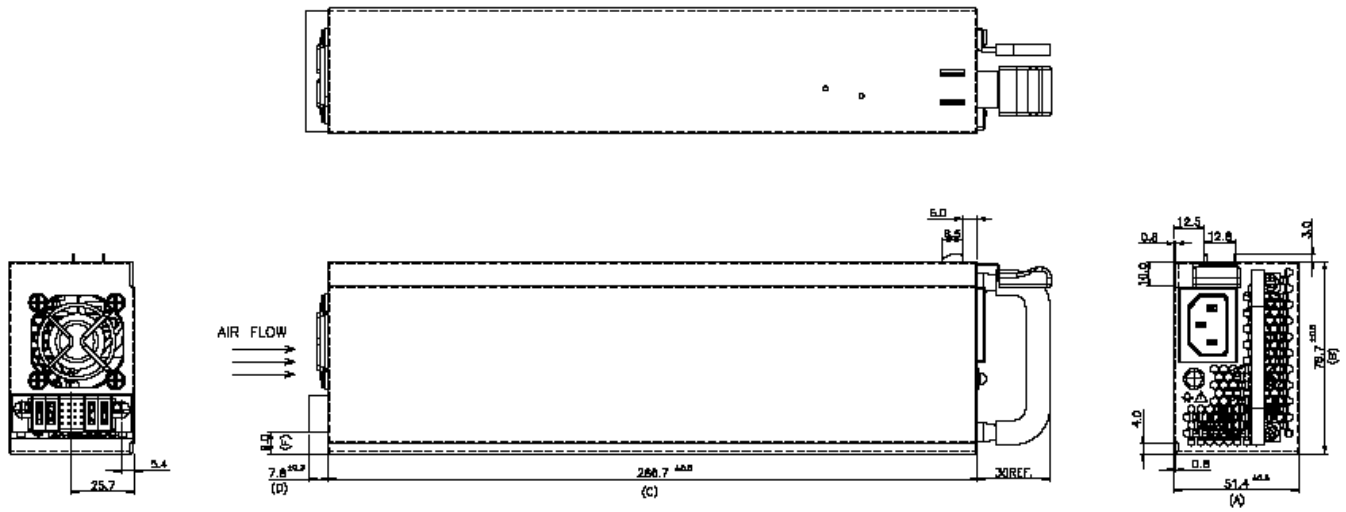
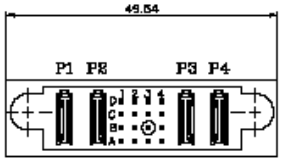


Figure 7-4. Power Supply Module Mechanical Drawing

7.4.2 Power Supply Module to Cage Interconnect

The power supply provides a pluggable terminal block, which mates to a connector located at the PDB. This is a blind mating type connector that connects the power supply's output voltages and signals.

The power supply shall be provided with a reliable protective earth ground. All secondary circuits shall be connected to protective earth ground. Resistance of the ground returns to chassis shall not exceed 1.0 mΩ. This path may be used to carry DC current.



OUTPUT CONNECTOR DIAGRAM
B3 IS SHORTENED.

OUTPUT CONNECTOR : FCI 51939-136
PIN ASSIGNMENT:

Signal Pins				
POSITION	1	2	3	4
D	+12VRS	−12V	+5VSB	15VCC
C	PWOK	RS_RTN	+5VSB	A0
B	+12VLS	RESERVE	PS_KILL	A1
A	PS_ON#	SDA	SCL	PS_ALERT#
Power Blades				
P1	P2	P3	P4	
+12V	+12V	RTN	RTN	

Figure 7-5. Power Supply Module Output Connector and Pin-out Drawing

7.4.3 Output Current Requirements

The power supply module provides three main outputs; +12V, -12V, and 5V standby, along with the 15VBIAS voltage. Two DC-to-DC converters located in the cage provide the 3.3V and 5V rails from the 12V provided by the power supply module.

The combined maximum output power of all outputs is 600 W (680 W peak). Each output has a maximum and minimum current rating as shown in the following table.

Table 7-9. Power Supply Module 600W Load Ratings

	+12V	+5Vsb	-12V
MAX Load	49.0A	2.0A	0.5A
MIN DYNAMIC Load	2.5A	0.1A	0A
MIN STATIC Load	0.5A	0.1A	0A
PEAK Load (12 seconds min)	56.0A	2.5A	N/A
Max Output Power (continuous), see note 1	12V x 49A = 588W max	5V x 2A = 10W max	-12V x 0.5A = 6W max
Peak Output Power (for 10s min), see note 2	12V x 56A = 672W pk	5V x 2.5A = 12.5W pk	N/A

Notes:

1. At max load the 12V output voltage is allowed to sag to –4%, which is 11.52V; so the actual max power will then be: 11.52V x 49A = 564.5 W, and the same applies for 5VSB: 4.80Vx2A=9.6W; so total max continuous Power = 564.5+9.6=574.1W .
2. At peak load the 12V output voltage is allowed to sag to –4%, which is 11.52V; so the actual peak power will then be: 11.52V x 56A = 645W; and the same applies to 5VSB: 4.80Vx2.5A=12W. The total peak power = 657 W pk.

7.4.4 Power Supply Module LED Indicator

The power supply module provides a single external bi-color LED to indicate the status of the power supply. When AC is applied to the power supply module and standby voltages are available, the LED will blink green.

The LED will be solid on green when all the power outputs are available.

The LED will be solid on amber when the power supply has failed - shutdown due to over current or shutdown due to over temperature. Refer to the following table for conditions of the LED.

Table 7-10. LED Indicators

Power Supply Condition	Bi-color LED
No AC power to all power supplies	OFF
No AC power to this PSU only (for 1+1 configuration) or Power supply **critical event** causing a shutdown: failure, fuse blown (1+1 only), OCP(12V), OVP(12V), Fan Failed	AMBER
Power supply **warning events** where the power supply **continues to operate**: high temp, high power/high current, slow fan.	1Hz Blink AMBER
AC present / Only 5Vsb on (PS Off)	1Hz Blink GREEN
Output ON and OK	GREEN
No AC power to all power supplies	OFF

7.4.5 Air Flow

The power supply shall incorporate **one 40mm fan** for self cooling and also used for partial system cooling. The fans will provide no less than **10 CFM** airflow through the power supply when installed in the system and operating at maximum fan speed. The cooling air will enter the power module from the PDB side (pre-heated air from the system). Variable fans speed is based on output load and ambient temperature. Under standby mode, the fans must run minimum RPM.

7.4.6 Thermal Protection

The power supply incorporates thermal protection that causes a shut down if airflow through the power supply is insufficient. Thermal protection activates shutdown before the temperature of any power supply component reaches the maximum rated temperature. This shutdown takes place prior to over-temperature induced damage to the power supply.

8. Regulatory Specifications

The IP Network Server meets the specifications and regulations for safety and EMC defined in this chapter.

8.1 Safety Compliance

USA/Canada	UL 60950, 3rd Edition/CSA 22.2, No. 60950-0, 3rd Edition
Europe	Low Voltage Directive, 73/23/EEC TUV/GS to EN60950 2nd Edition with Amendments, A1 = A2 + A3 + A4
International	CB Certificate and Report to IEC 950, 3rd Edition including EMKO-TSE (74-SEC) 207/94 and all international deviations

8.2 Electromagnetic Compatibility

USA	FCC 47 CFR Parts 2 and 15, Verified Class A Limit
Canada	IC ICES-003 Class A Limit
Europe	EMC Directive, 89/336/EEC EN55022, Class A Limit, Radiated & Conducted Emissions EN55024 Immunity Characteristics for ITE EN61000-4-2 ESD Immunity (level 2 contact discharge, level 3 air discharge) EN61000-4-3 Radiated Immunity (level 2) EN61000-4-4 Electrical Fast Transient (level 2) EN61000-4-5 Surge EN61000-4-6 Conducted RF EN61000-4-8 Power Frequency Magnetic Fields EN61000-4-11 Voltage Fluctuations and Short Interrupts EN61000-3-2 Harmonic Currents EN61000-3-3 Voltage Flicker
Australia/New Zealand	AS/NZS 3548, Class A Limit
Japan	VCCI Class A ITE (CISPR 22, Class A Limit) IEC 1000-3-2; Harmonic Currents
Taiwan	BSMI Approval, CNS 13438, Class A
Korea	RRL Approval, Class A
China	CCC Approval
Russia	Gost Approval
International	CISPR 22, Class A Limit

8.3 CE Mark

The CE marking on this product indicates that it is in compliance with the European Union's EMC Directive 89/336/EEC, and Low Voltage Directive, 73/23/EEC.

Appendix A: Glossary

This appendix contains important acronyms and terms used in the preceding chapters.

Term	Definition
A, Amp	Ampere
A/µs	Amps per microsecond
AC	Alternating current
ACPI	Advanced Configuration and Power Interface
ANSI	American National Standards Institute
APIC	Advanced Programmable Interrupt Controller
ASIC	Application specific integrated circuit
AWG	American wire gauge
BIOS	Basic input/output system
BMC	Bus management controller
Bridge	Circuitry that connects one computer bus to another
Byte	8-bit quantity
C	Centigrade
CE	Community European
CFM	Cubic feet per minute
CISPR	International Special Committee on Radio Interference
CSA	Canadian Standards Organization
CTS	Clear to send
DAT	Digital audio tape
dB	Decibel
dBA	Acoustic decibel
DC	Direct current
DIMM	Dual inline memory module
DMI	Desktop management interface
DOS	Disk operating system
DRAM	Dynamic random access memory
DSR	Data set ready
DTR	Data terminal ready
DWORD	Double word - 32-bit quantity
ECC	Error checking and correcting
EEPROM	Electrically erasable programmable read-only memory
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
EMP	Emergency management port
EN	European Standard (Norme Européenne or Europäische Norm)
EPS	External product specification
ESCD	Extended system configuration data
ESD	Electrostatic discharge
ESR	Equivalent series resistance
F	Fahrenheit

Term	Definition
FCC	Federal Communications Commission
FFC	Flexible flat connector
Flash ROM	EEPROM
FPC	Front panel controller
FRB	Fault resilient booting
FRU	Field replaceable unit
G	Acceleration in gravity units, 1G = 980665 m/s^2
GB	Gigabyte - 1024 MB
GND	Ground
GPIO	General purpose input/output
Grms	Root mean square of acceleration in gravity units
GUI	Graphical user interface
HDD	Hard disk drive
HPIB	Hot-plug indicator board
HSC	Hot-swap controller
Hz	Hertz – 1 cycle/second
I/O	Input/output
I^2C*	Inter-integrated circuit bus
ICMB	Intelligent Chassis Management Bus
IDE	Integrated drive electronics
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IFLASH	Utility to update Flash EEPROM
IMB	Intelligent management bus
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Initiative
IRQ	Interrupt request line
ITE	Information technology equipment
ITP	In-target probe
JAE	Japan Aviation Electronics
KB	Kilobyte - 1024 bytes
kV	Killivolt – 1,000 volts
L2	Second-level cache
LAN	Local area network
LED	Light-emitting diode
LVDS	Low voltage differential SCSI
mA	Milliamp
MB	Megabyte - 1024 KB
MEC	Memory expansion card
mm	Millimeter
MPS	Multiprocessor specification
MTTR	Mean time to repair
mΩ	Milliohm
NEMKO	Norges Elektriske Materiellkontroll (Norwegian Board of Testing and Approval of Electrical Equipment)

Term	Definition
NIC	Network interface card
NMI	Nonmaskable interrupt
NWPA	NetWare* Peripheral Architecture
ODI	Open data-link interface
OEM	Original equipment manufacturer
OPROM	Option ROM (expansion BIOS for a peripheral)
OS	Operating system
OTP	Over-temperature protection
OVP	Over-voltage protection
PC-100	Collection of specifications for 100 MHz memory modules
PCB	Printed circuit board
PCI	Peripheral component interconnect
PHP	PCI hot-plug
PID	Programmable interrupt device
PIRQ	PCI interrupt request line
PMM	POST memory manager
PnP	Plug and play
POST	Power-on Self Test
PSU	Power supply unit
PVC	Polyvinyl chloride
PWM	Pulse width modulation
RAS	Reliability, availability, and serviceability
RIA	Ring indicator
RPM	Revolutions per minute
RTS	Request to send
SAF-TE	SCSI Accessed Fault-Tolerant Enclosures
SCA	Single connector attachment
SCL	Serial clock
SCSI	Small Computer Systems Interface
SDR	Sensor data records
SDRAM	Synchronous dynamic RAM
SEC	Single edge connector
SEL	System event log
SELV	Safety extra low voltage
SEMKO	Sverge Elektriske Materiellkontroll (Swedish Board of Testing and Approval of Electrical Equipment)
SGRAM	Synchronous graphics RAM
SM	Server management
SMBIOS	System management BIOS
SMBus	Subset of I^2C bus/protocol (developed by Intel)
SMI	System management interrupt
SMM	Server management mode
SMP	Symmetric multiprocessing
SMRAM	System management RAM
SMS	Server management software

Term	Definition
SPD	Serial presence detect
SSI	Server system infrastructure
TUV	Technischer Uberwachungs-Verein (A safety testing laboratory with headquarters in Germany)
UL	Underwriters Laboratories, Inc.
USB	Universal Serial Bus
UV	Under-voltage
V	Volt
VA	Volt-amps (volts multiplied by amps)
Vac	Volts alternating current
VCCI	Voluntary Control Council for Interference
Vdc	Volts direct current
VDE	Verband Deutscher Electrotechniker (German Institute of Electrical Engineers)
VGA	Video graphics array
VRM	Voltage regulator module
VSB	Voltage standby
W	Watt
WfM	Wired for Management
Word	A 16-bit quantity
Ω	Ohm
μF	Microfarad
μs	Microsecond

Appendix B: Reference Documents

Refer to the following documents for additional information:

ACPI

- *Advanced Configuration And Power Interface Specification*, Revision 1.0b, http://www.teleport.com/~acpi/.

Boot

- *BIOS Boot Specification*, Version 1.01, http://www.ptltd.com/techs/specs.html.
- *El Torito CD-ROM Boot Specification*, Version1.0, http://www.ptltd.com/techs/specs.html.

DMI

- *Desktop Management Interface (DMI) Specification*, Version 2.0s, Desktop Management Task Force, Inc., http://www.dmtf.org/spec/dmis.html.

ESCD

- *Extended System Configuration Data Specification*, Version 1.02a, http://www.microsoft.com/hwdev/respec/PNPSPECS.HTM.

Ethernet

- *Intel 82559 Fast Ethernet Multifunction PCI/Cardbus Controller Datasheet*, Intel Corporation, http://developer.intel.com/design/network/datashts/738259.htm.

Flash

- *Intel 5 VOLT FlashFile™ Memory (28F008SA x8) Datasheet*, December 1998, Intel Corporation, Number 290429-008, http://developer.intel.com/design/flcomp/datashts/290429.htm.

I_2O

- *Intelligent Input/Output (I_2O) Architecture Specification*, Revision 1.0, I_2O Special Interest Group, http://www.Intelligent-IO.com

MPS

- *MultiProcessor Specification*, Version 1.4, Intel Corporation, http://www-techdoc.intel.com/design/intarch/manuals/242016.htm.

PC133 SDRAM

- *PC SDRAM Registered DIMM Specification*, Revision 1.2, Intel Corporation, http://developer.intel.com/technology/memory/.

- *PC SDRAM Specification*, Revision 1.63, Intel Corporation, http://developer.intel.com/technology/memory/.
- *PC SDRAM Serial Presence Detect (SPD) Specification*, Revision 1.2A, Intel Corporation, http://developer.intel.com/technology/memory/.

PCI

- *PCI Bus Power Management Interface Specification*, Revision 1.1, PCI Special Interest Group, http://www.pcisig.com/.
- *PCI Local Bus Specification*, Revision 2.1, PCI Special Interest Group, http://www.pcisig.com/.
- *PCI Hot-plug Specification*, Revision 1.0, PCI Special Interest Group, http://www.pcisig.com/.
- *PCI Hot-plug Application and Design*, Alan Goodrum, ISBN 0-929392-60-4.
- *Compaq PCI Hot-Plug Megacell Specification.*

Phoenix* BIOS

- *Phoenix BIOS 6.0 Users Manual*, Phoenix Technologies Ltd.

PID

- *Programmable Interrupt Device External Product Specification*, Revision 1.1, Intel Corporation, Document number OR4-680777.

Plug and Play

- *Plug and Play BIOS Specification*, Version 1.0a, http://www.microsoft.com/hwdev/respec/PNPSPECS.HTM.
- *Clarification to Plug and Play BIOS Specification*, Version 1.0a, http://www.microsoft.com/hwdev/respec/PNPSPECS.HTM.
- *Plug and Play ISA Specification*, Version 1.0a, http://www.microsoft.com/hwdev/respec/PNPSPECS.HTM.
- *Clarification to Plug and Play ISA Specification*, Version 1.0a, http://www.microsoft.com/hwdev/respec/PNPSPECS.HTM.

PMM

- *POST Memory Manager Specification*, Version 1.01, http://www.ptltd.com/techs/specs.html.

Power Supply

- *Intel® Carrier Grade Server TIGI2U AC Power Supply Cage Specification*, Revision 1.0, Intel Corporation.

- *Intel® Carrier Grade Server TIGI2U AC Power Supply Module Specification*, Revision 1.0, Intel Corporation.

Regulatory

- *CISPR 22: Limits and Methods of Measurement of Radio Interference Characteristics of Information Technology Equipment*, 2nd Edition.
- *CFR 47: Federal Communications Commission (FCC) Compliance with the Class A Limits for Computing Devices (FCC Mark)*, Part 2 & 15.
- *ANSI C63.4: American National Standard for Methods of Measurement of Radio-Noise Emissions from Low Voltage Electronic Equipment in the Range of 9kHz to 40GHz for EMI Testing*, 1992.
- *CISPR 24: Information Technology Equipment - Immunity Characteristics Limits and Methods of Measurement*, 1st Edition.
- *ICES-003: Canadian Radio Interference Regulations for Digital Apparatus*.
- *EN 61000-3-2: Electromagnetic Compatibility (EMC) Part 3: Limits - Section 2: Limits for Harmonic Current Emissions.*
- *JEIDA MITI Guideline for Suppression of High Harmonics in Appliances and General-Use Equipment*.

Server Management

- *Emergency Management Port v1.0 Interface External Product Specification*, Revision 0.83, Intel Corporation.
- *Intelligent Platform Management Interface (IPMI) Specification*, Version 1.0, Revision 1.1, Intel Corporation, http://developer.intel.com/design/servers/ipmi/spec.htm.

SMBIOS

- *System Management BIOS Reference Specification*, Version 2.3, http://www.ptltd.com/techs/specs.html.

Super I/O

- *National PC97317 SuperI/O Plug and Play Compatible Chip with ACPI-Compliant Controller/Extender*, http://www.national.com/pf/PC/PC97317.html.

USB

- *Universal Serial Bus Specification*, Revision 1.0, http://www.usb.org/developers.

VGA

- *ATI RAGE IIC Technical Reference Manual*.

Wired for Management

- *Wired for Management (WfM) Baseline Specifications*, Version 2.0, Intel Corporation, http://developer.intel.com/ial/wfm/wfmspecs.htm.

Windows

- *Hardware Design Guide for Microsoft Windows NT Server*, Version 2.0, http://www.microsoft.com/HWDEV/serverdg.htm.

Miscellaneous

- *Intel Environmental Standards Handbook,* June 1999, Intel Document No. 662394-04.
- *VRM 8.3 DC-DC Converter Specification.*
- VRM 8.4 DC-DC Converter Specification.