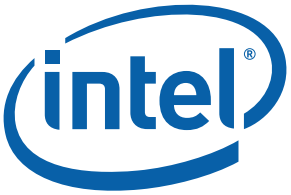


Intel® Server Board S5000PHB

Technical Product Specification

April 2008

Rev. 1.2

Order Number: D70057-005

Contents

Figures

Tables

Revision History

Revision	Date	Doc ID	Description
1.2	April 2008	D70057-005	Edited processor information to include Quad-Core Intel® Xeon® processors 5400 series Removed SysCon information. Added Intel Z-U130 Solid State Drive. Minor grammar and formatting changes.
1.1	Jul 2007	D70057-004	Globally corrected product model number. Updated block diagrams in “Functional Architecture” to include NIC port numbers. Updated TIGW1U block diagram in “Functional Architecture” to include Telco alarms. Added LV4128 to supported processor matrix in “Functional Architecture”. Added section on MAC address definition for Ethernet ports to “Functional Architecture”. Updated DIMM numbers in SMBus block diagram in “Platform Management”. Corrected description and illustration of POST code diagnostic LED order in “Light Guided Diagnostics” and “POST Codes”. Added information on early POST codes, beep codes, and on-screen error messages to “POST Codes”.
1.0	Feb 2007	D70057-003	Removed unsupported sensors from table in Appendix B.
0.9	Feb 2007	D70057-002	Added NSW1U-Bypass configuration. Replaced single block diagram with three updated configuration-specific diagrams. Updated component layout figure. Added information on serial port B configuration jumper and port A header. Added sensor table to Appendix B.
0.8	Sep 2006	D70057-001	Initial release of document.

1 Introduction

This Technical Product Specification (TPS) provides board-specific information detailing the features, functionality, and high level architecture of the Intel® Server Board S5000PHB. Users should see the *Intel® S5000 Server Board Family Datasheet* for more detail on board sub-systems, including chipset, BIOS, and system management software.

Design level information for specific sub-systems can be obtained by ordering the External Product Specifications (EPS) or External Design Specifications (EDS) for a given sub-system. EPS and EDS documents are not publicly available and must be ordered through your local Intel representative.

1.1 Document Outline

This document is divided into the following chapters:

- Chapter 1, “Introduction”
- Chapter 2, “Product Overview”
- Chapter 3, “Functional Architecture”
- Chapter 4, “Platform Management”
- Chapter 5, “Connector / Header Locations and Pin-outs”
- Chapter 6, “Jumper Block Settings”
- Chapter 7, “Light Guided Diagnostics”
- Chapter 8, “Power and Environmental Specifications”
- Chapter 9, “Regulatory and Certification Information”
- Appendix A, “Integration and Usage Tips”
- Appendix B, “Sensor Tables”
- Appendix C, “POST Codes”
- Appendix D, “Glossary”
- Appendix E, “Reference Documents”

1.2 Server Board Use Disclaimer

Intel® server boards support add-in peripherals and contain high-density VLSI and power delivery components that need adequate airflow to cool. Intel ensures through its own chassis development and testing that when Intel server building blocks are used together, the fully integrated system will meet the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of air flow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible if components fail or the server board does not operate correctly when used outside any of their published operating or non-operating limits.

2 Product Overview

The Intel® Server Board S5000PHB is a monolithic printed circuit board with features that support the high-density 1U IP network server and carrier grade server markets.

2.1 Intel® Server Board S5000PHB SKU Availability

In this document, the name S5000PHB describes the family of boards that is available under a common product name. The core features for each board are common, but each board has the following distinctions:

Server Board Product Code	Feature Distinctions	Server System Where Used
TMWBSBRD01W	Dual CPU sockets for Dual-Core Intel® Xeon® processors 5100 series, SAS connector, two dual-port Ethernet controllers and 2 dual NIC connectors, Telco alarm connector	Intel® Carrier Grade Server TIGW1U
TMRBSBRD01W	Dual CPU sockets for Quad-Core Intel® Xeon® processors 5400 series, SAS connector, two dual-port Ethernet controllers and 2 dual NIC connectors, Telco alarm connector	Intel® Carrier Grade Server TIGW1U
NSWBSBRDR01W	Single CPU socket for Dual-Core Intel® Xeon® processors 5100 series, SATA, two dual-port Ethernet controllers and two dual NIC rear connectors	Intel® IP Network Server NSW1U rear NIC (NSW1U-RNIC) or bypass (NSW1U-Bypass)
NSRBSBRDR01W	Single CPU socket for Quad-Core Intel® Xeon® processors 5400 series, SATA, two dual-port Ethernet controllers and two dual NIC rear connectors	Intel® IP Network Server NSW1U rear NIC (NSW1U-RNIC) or bypass (NSW1U-Bypass)
NSWBSBRDF01W	Single CPU socket for Dual-Core Intel® Xeon® processors 5100 series, SATA	Intel® IP Network Server NSW1U front NIC (NSW1U-FNIC)

Throughout this document, all references to the Server Board S5000PHB refer to all server board SKUs unless specifically noted otherwise. Your specific board may or may not have all the features described based on the listed board differences.

2.2 Server Board S5000PHB Feature Set

Table 1. Server Board S5000PHB Features

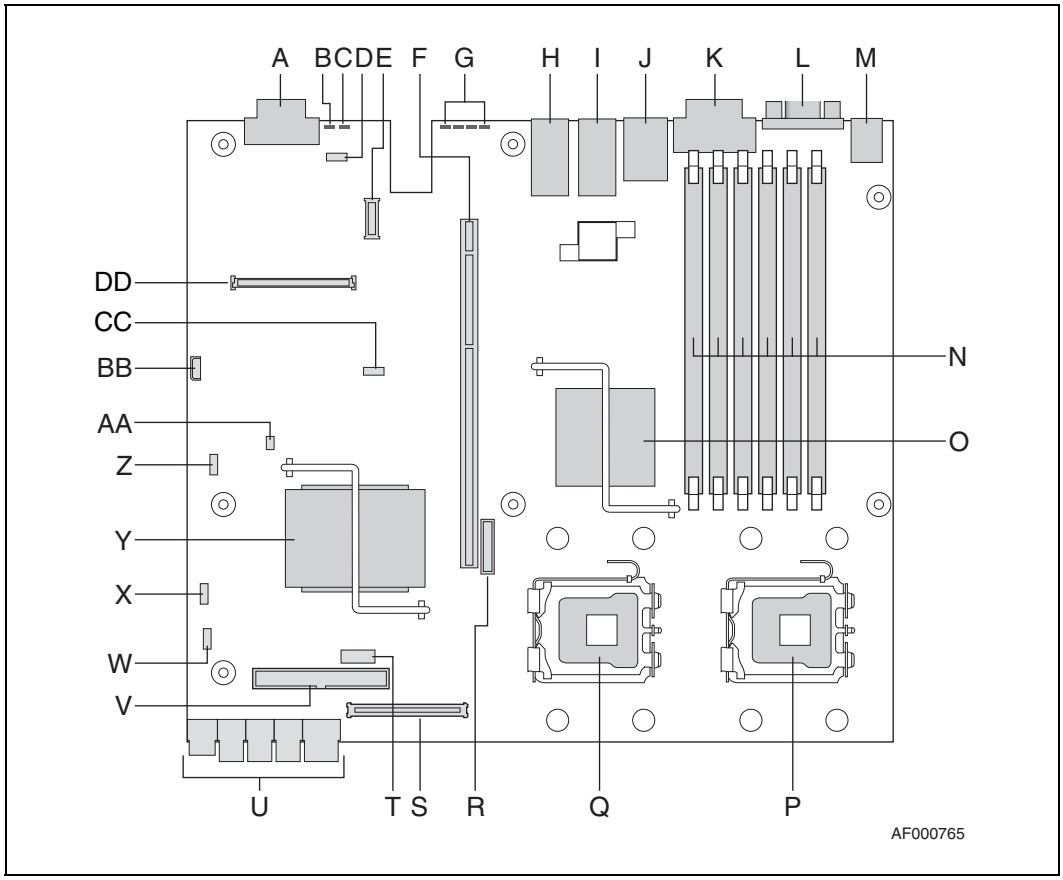
Feature	Description
Processors	771-pin LGA sockets supporting one (any NSW1U) or two (any TIGW1U) Dual-Core Intel® Xeon® processors 5100 series, with system bus speeds of 1066 MHz or 1333 MHz, or one (NSW1U-RNC, NSW1U-Bypass) or two (any TIGW1U) Quad-Core Intel® Xeon® processors 5400 series, with system bus speeds of 1066 MHz or 1333 MHz.
Memory	Six DIMM slots supporting fully buffered DIMM technology (FBDIMM) memory. 240-pin DDR2-533 and DDR2-677 FBDIMMs can be used.
Chipset	Intel® 5000 Chipset Family, which includes the following components: • Intel® 5000P Memory Controller Hub • Intel® ESB2-E I/O Controller
On-board Connectors and Headers	External connections: • Stacked PS/2 ports for keyboard and mouse • Video connector • RJ45 Serial B port connector • Two USB 2.0 Ports • Four RJ45 connectors for 10/100/1000 Mbps Ethernet connections (except NSW1U-F) • One SAS connector with optional RAID support (TIGW1U only) • DB-15 Telco Alarms connector (TIGW1U only) Internal connectors/headers: • Serial A port header • ASMI connector to support optional Intel® Remote Management Module 2 • GCM3 connector to support the optional Intel® Remote Management Module 2 • 140-pin front panel flex connector • Power distribution board (PDB) connector
Add-in PCI, PCI-X*, PCI Express* Cards	PCI super slot supporting low-profile PCI-X* or PCIe* riser cards to accept single full-height, full-length PCI, PCI-X, or PCI Express adapter cards.
On-board Video	ATI* RN50 video controller with 16 Mbytes of DDR SDRAM
LAN (except NSW1U-F)	• Two 10/100/1000 Intel® 82563EB ports supporting Intel® I/O Acceleration Technology • Two 10/100/1000 Intel® 82571EB ports supporting Intel® I/O Acceleration Technology
System Management	Support for Intel® System Management Software

2.3 Server Board Layout

2.3.1 Connector and Component Locations

Figure 1 shows the board layout of the Server Board S5000PHB. Each connector and major component is identified by a letter, and a description is given in the table below the figure.

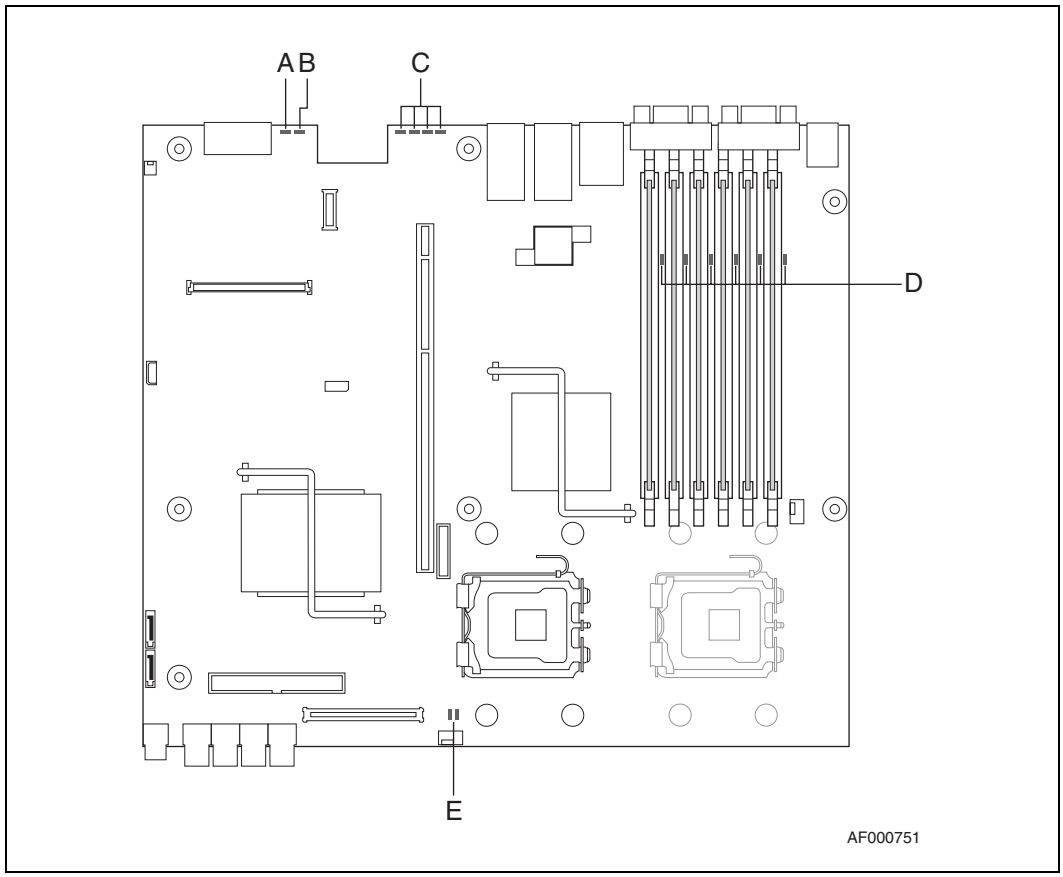
Figure 1. Server Board S5000PHB Components and Connector Location Diagram



Item	Description	Item	Description
A	SAS Connector (TIGW1U only)	P	CPU #2 connector (TIGW1U only)
B	System Identification LED (blue)	Q	CPU #1 connector
C	System Status LED (green/amber)	R	Battery
D	Serial Port B DSR/DCD jumper (J2A2)	S	Flex connector to front panel board
E	GCM Connector	T	Serial Port A header
F	PCI Express/PCI-X riser card slot	U	Main power connector
G	POST Code diagnostic LEDs	V	PATA (IDE) connector
H	Dual-port LAN connector (not on NSW1U-F)	W	Password Clear jumper (J1H2)
I	Dual-port LAN Connector (not on NSW1U-F)	X	BIOS Bank Select jumper (J1G1)
J	Dual USB 2.0/RJ45 serial port B connector	Y	Intel® ESB2-E I/O Controller Hub
K	Telco alarms connector (TIGW1U only)	Z	CMOS Clear jumper (J1F1)
L	Video connector	AA	BMC Force Update jumper (J1E3)
M	PS/2 keyboard and mouse connector	BB	3-Pin IPMB header
N	FBDIMM sockets	CC	Processor select jumper
O	Intel® 500P Memory Controller Hub	DD	Intel® Remote Management Module 2 connector

2.3.2 Light Guided Diagnostic LED Locations

Figure 2. Light Guided Diagnostic LED Locations



Item	Description	Item	Description
A	System Identification LED – blue	D	DIMM Fault LEDs
B	System Status LED – green / amber	E	CPU Fault LEDs
C	POST Code diagnostic LEDs		

2.3.3 Server Board Mechanical Drawings

Figure 3. Hole and Component Locations

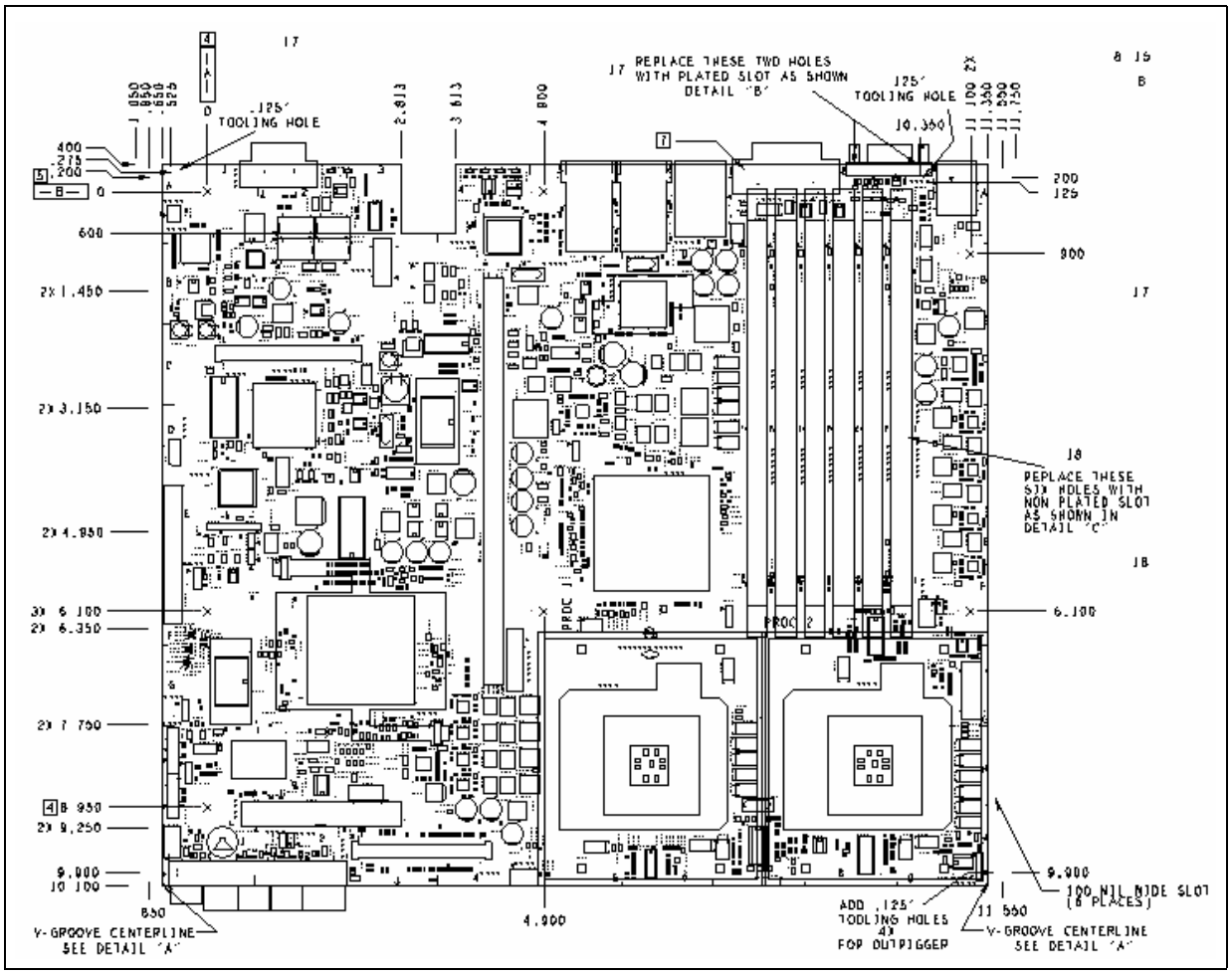


Figure 4. Restricted Areas on Primary Side

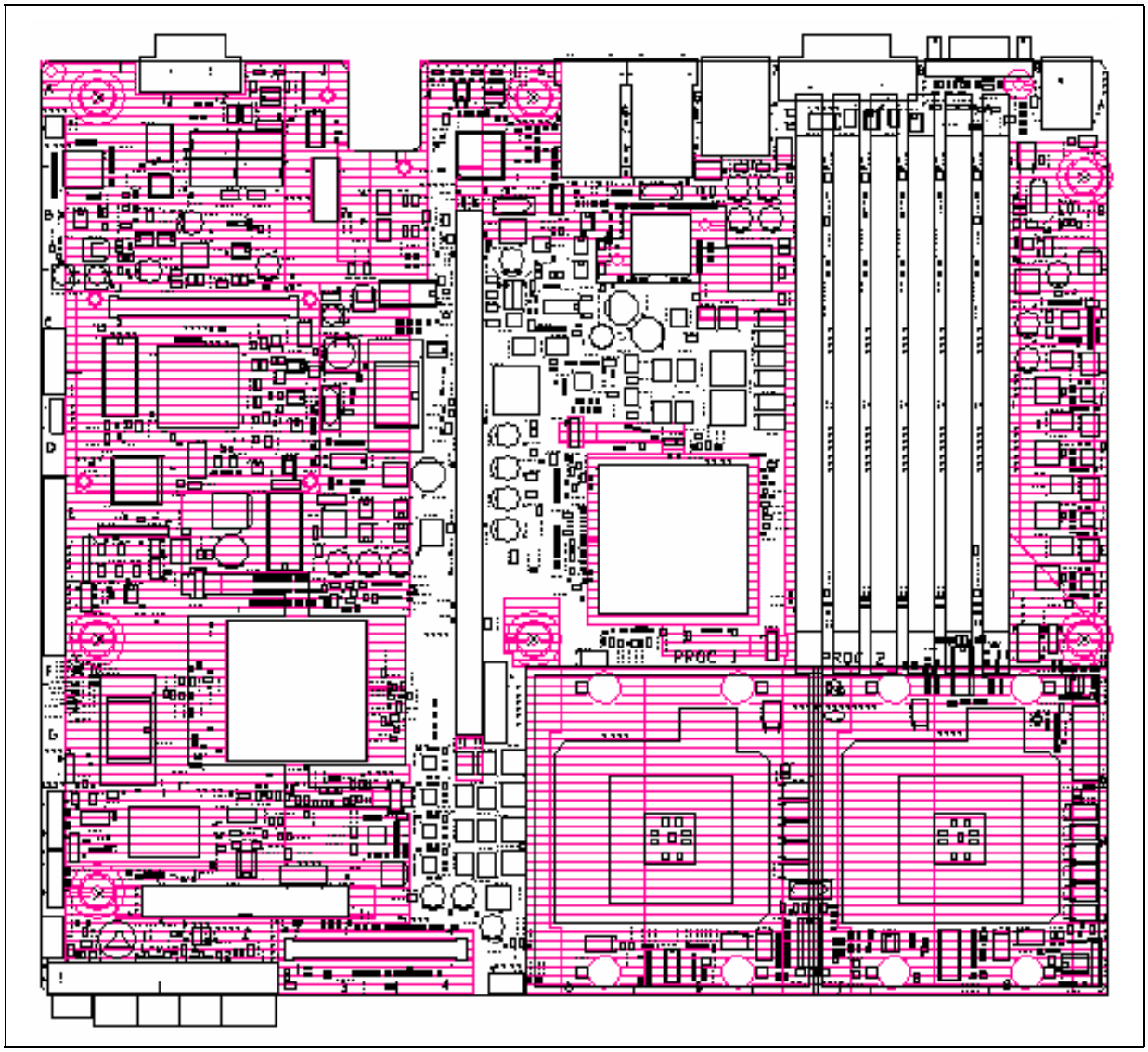
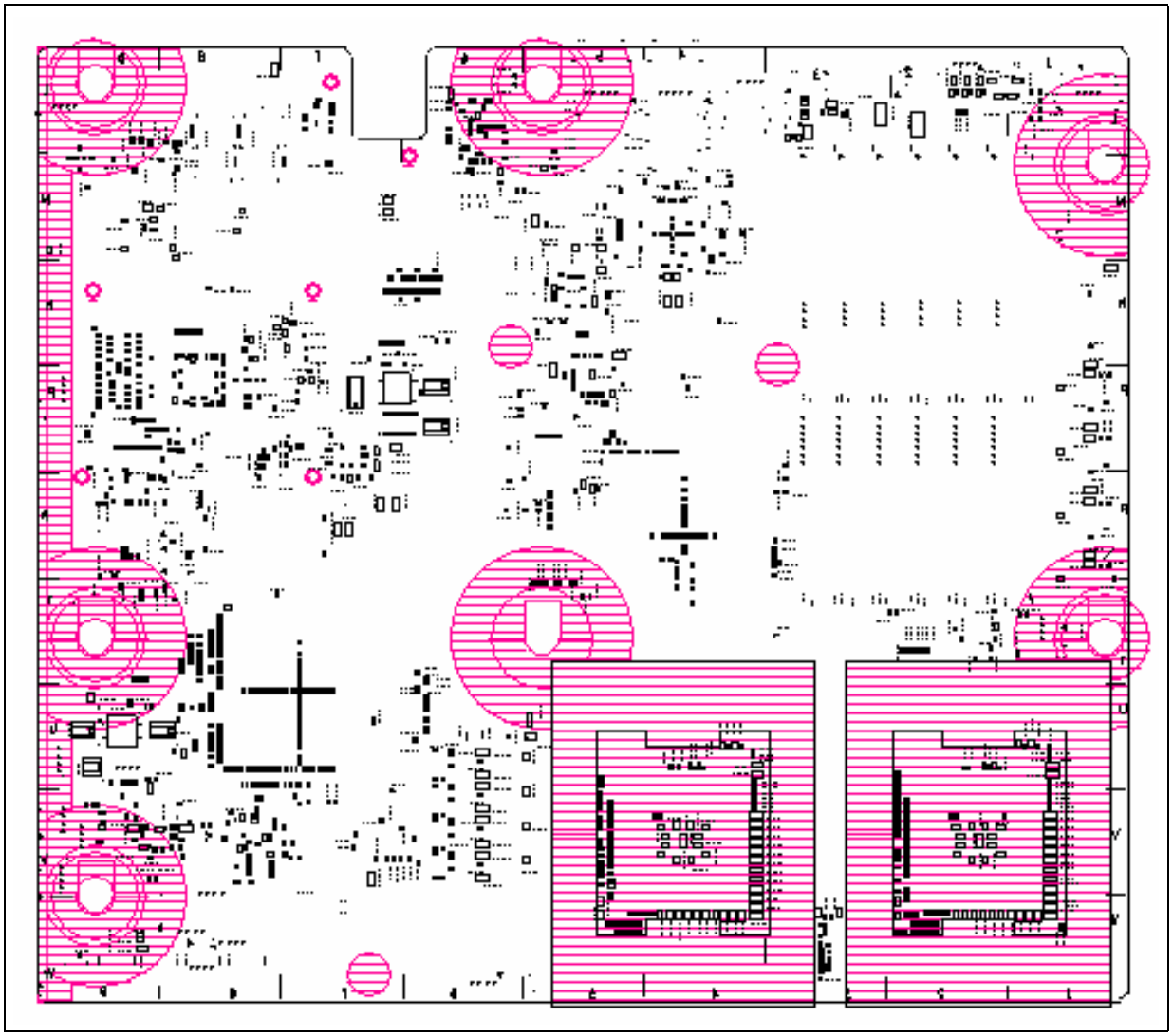


Figure 5. Restricted Areas on Secondary Side



3 Functional Architecture

The architecture and design of the Intel® Server Board S5000PHB is based on the Intel® 5000P Chipset. The chipset is designed for systems that use the Dual-Core Intel® Xeon® processor 5100 series with system bus speed of 1066 MHz or 1333 MHz, or the Quad-Core Intel® Xeon® processor 5400 series with system bus speed of 1066 MHz or 1333 MHz.

The chipset contains two main components:

- The 5000P Memory Controller Hub (MCH) for the host bridge
- The ESB2-E I/O controller hub for the I/O subsystem

This chapter provides a high-level description of the functionality associated with each chipset component and the architectural blocks that make up this server board. For more detail of the functionality for each of the chipset components and each of the functional architecture blocks, see the *Intel® S5000 Series Chipset Server Board Family Datasheet*.

3.1 Block Diagrams

This section provides block diagrams of the three different configurations of the Intel® Server Board S5000PHB.

Figure 6 shows the block diagram of the dual-processor server board configuration, as used in the Intel® Carrier Grade Server TIGW1U.

Figure 7 shows the block diagram of the single-processor server board configuration with on-board NICs, as used in the rear NIC and NIC bypass configurations of the Intel® Network Server NSW1U.

Figure 8 shows the block diagram of the single-processor server board configuration without on-board NICs, as used in the front NIC configuration of the Intel® Network Server NSW1U.

Figure 6. Functional Block Diagram, TIGW1U Configuration

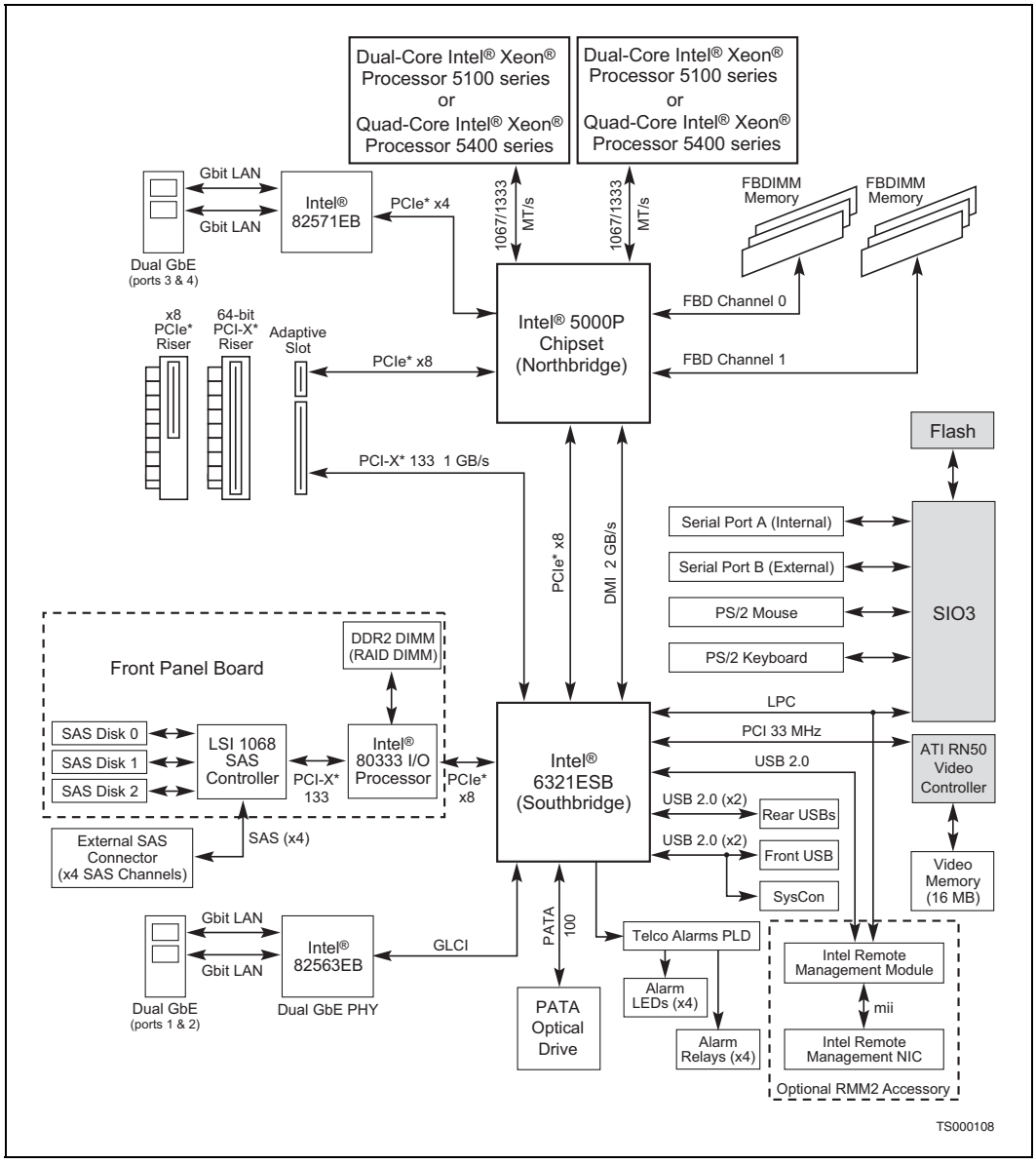


Figure 7. Functional Block Diagram, NSW1U-R and NSW1U-B Configurations

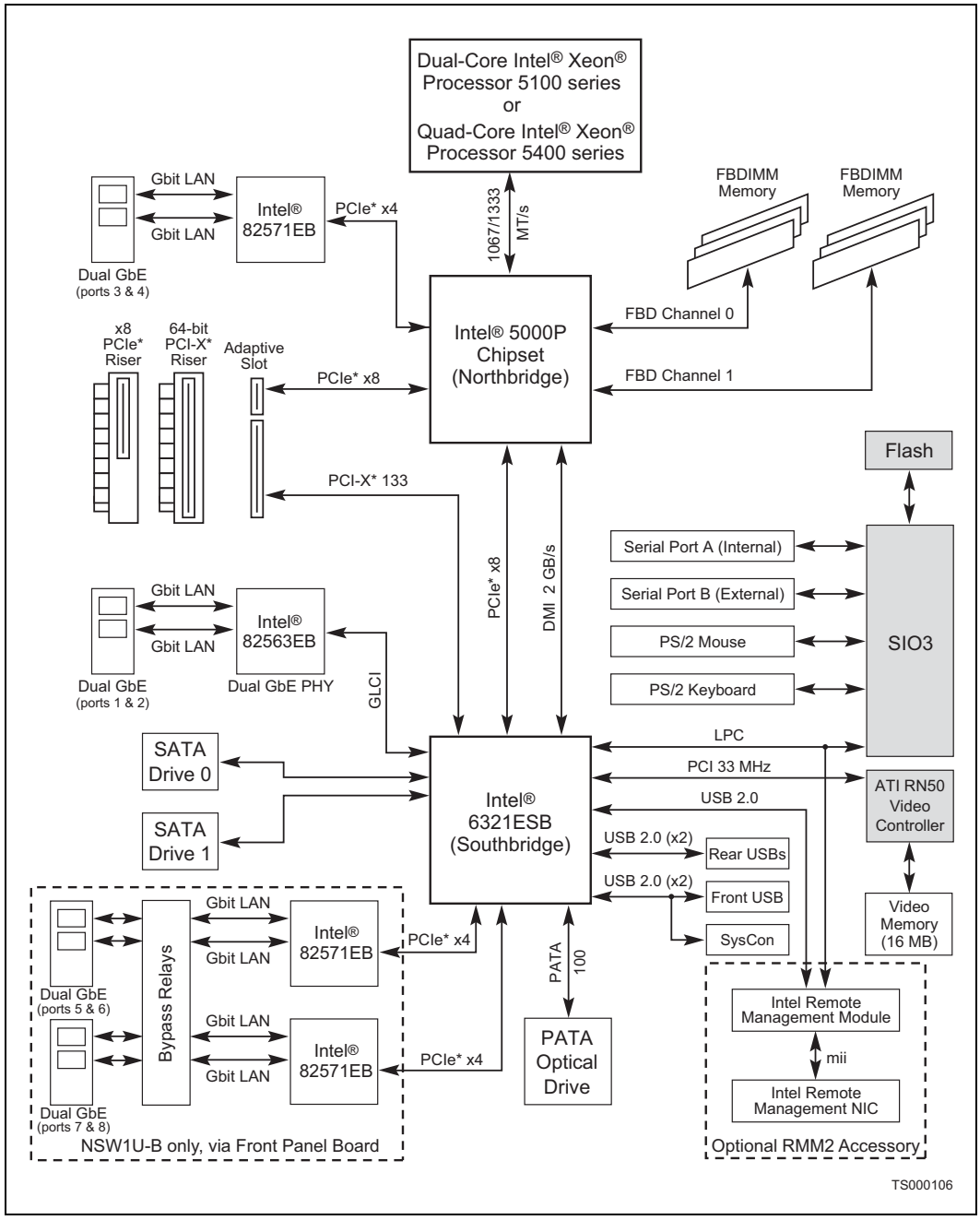
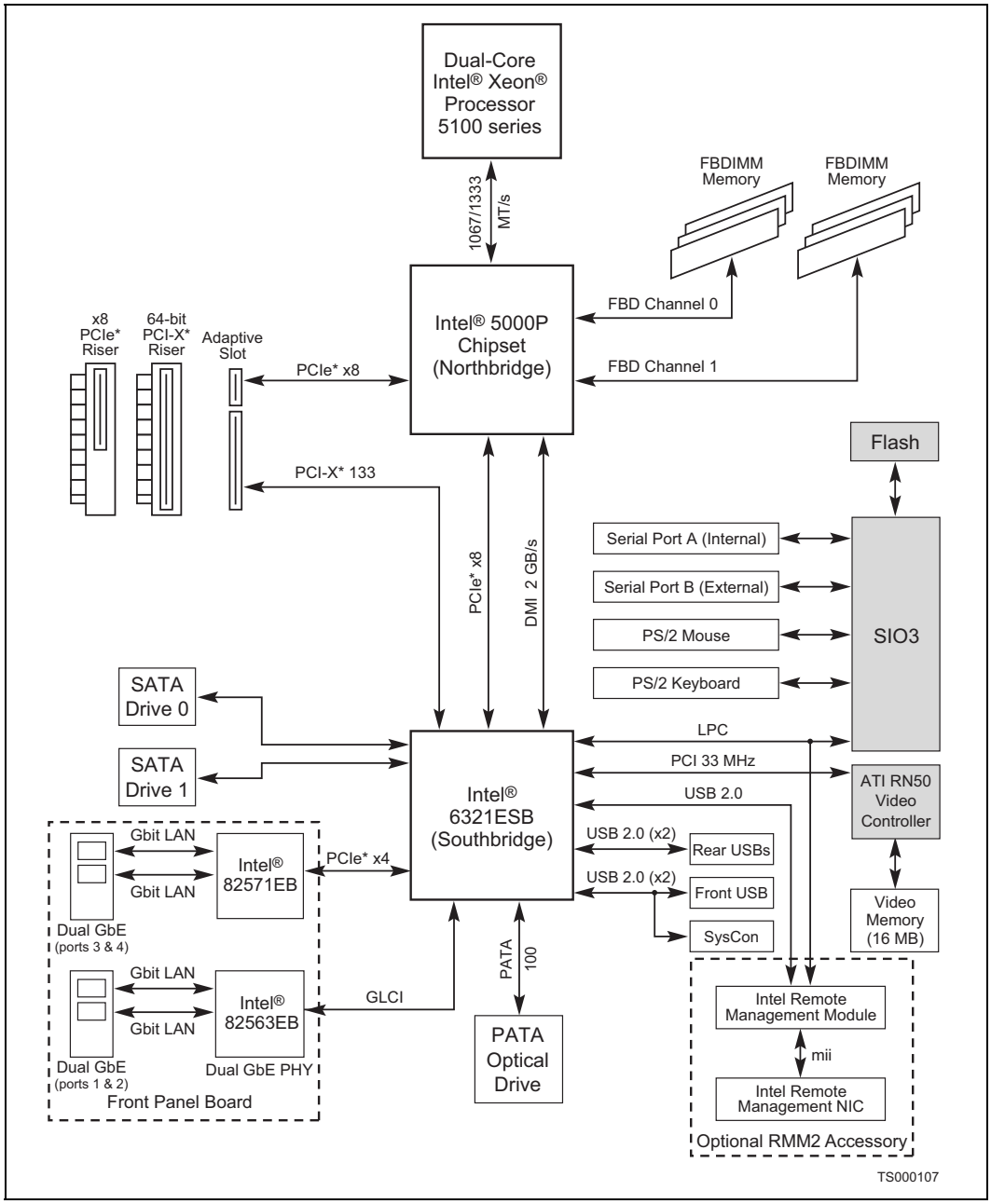


Figure 8. Functional Block Diagram, NSW1U-F Configuration



3.2 Intel® 5000P Memory Controller Hub (MCH)

The Intel® 5000P Memory Controller Hub (MCH) is a 1432-pin FCBGA package that includes the following core platform functions:

- System bus interface for the processor sub-system
- Memory controller
- PCI Express* ports including the Enterprise South Bridge Interface
- FBD thermal management
- SMBus interface

This section provides a high-level overview of some of these core functions as they pertain to this server board. Additional information is in the *Intel® S5000 Server Board Family Datasheet* and the *Intel® 5000P Memory Controller Hub External Design Specification* (restricted document).

3.2.1 System Bus Interface

The MCH is configured for symmetric multi-processing across two independent front side bus interfaces that connect to the Dual-Core Intel® Xeon® processors 5100 series, or to the Quad-Core Intel® Xeon® processors 5400 series. Each front side bus on the MCH uses a 64-bit wide, 1066 MHz or 1333 MHz data bus. The 1333 MHz data bus is capable of transferring data at up to 10.66 GB/s. The MCH supports a 36-bit wide address bus, capable of addressing up to 64 GB of memory. The MCH is the priority agent for both front side bus interfaces, and is optimized for one processor on each bus.

3.2.2 Processor Support

The server board supports one (TIGW1U) or two (all NSW1U) Dual-Core Intel® Xeon® processors 5100 series, with system bus speeds of 1066 MHz or 1333 MHz and core frequencies from 1.60 to 3.00 GHz, or one (TIGW1U) or two (NSW1U RNIC or Bypass) Quad-Core Intel® Xeon® processors 5400 series, with system bus speeds of 1066 MHz or 1333 MHz and core frequencies of 2.3 or 2.83 GHz. Previous generations of the Intel Xeon processor are not supported on this server board. See the Configuration Guide for your specific server system for a list of supported processors:

- For the Intel® Carrier Grade Server TIGW1U, see http://www.intel.com/support/telecom/computeboards/tigw1u/sb/CS-026555.htm
- For the Intel® IP Network Server NSW1U, see http://www.intel.com/support/telecom/computeboards/nsw1u/sb/CS-025497.htm

3.2.2.1 Processor Population Rules

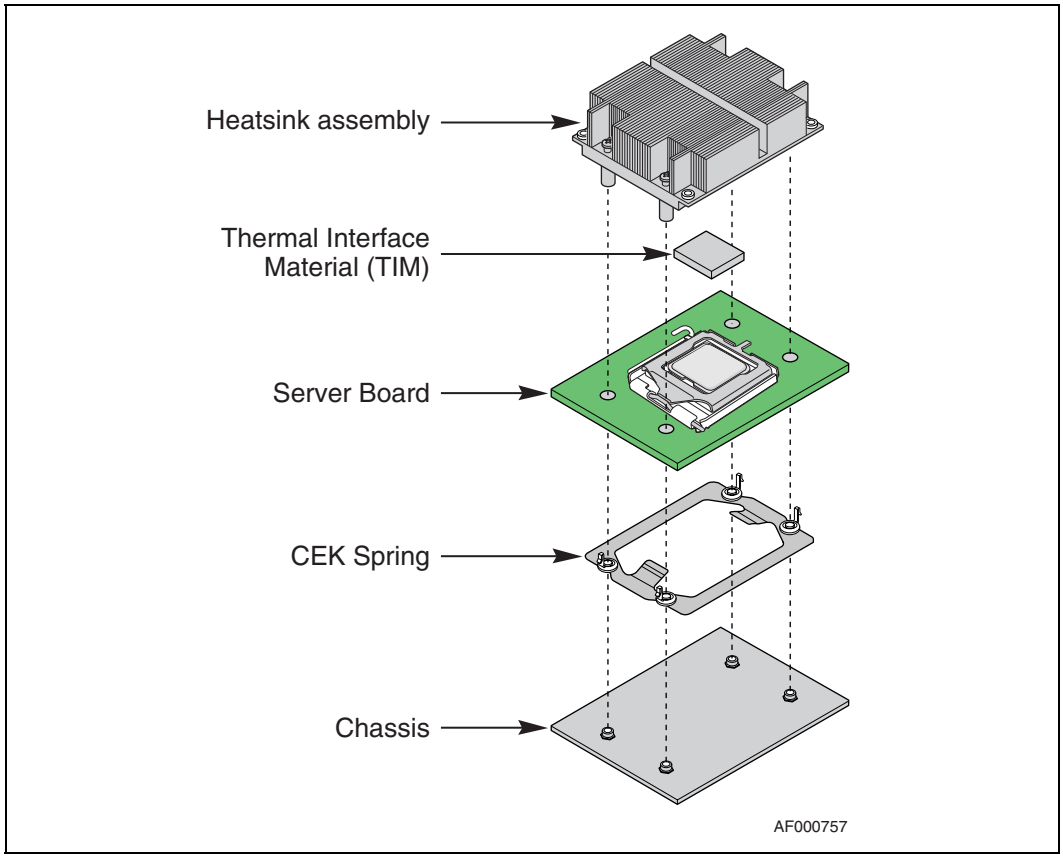
When two processors are installed, both must be of identical revision, core voltage, and bus/core speed. When only one processor is installed, it must be in the socket labeled CPU1. The other socket must be empty. No terminator is required in the second processor socket when using a single-processor configuration.

3.2.2.2 Common Enabling Kit (CEK) Design Support

The server board complies with the Intel® Common Enabling Kit (CEK) processor mounting and heat sink retention solution. The server board ships with a CEK spring snapped onto the underside of the server board beneath each processor socket. The heat sink attaches to the CEK, over the top of the processor and the thermal interface material (TIM). See the figure below for the stacking order of the chassis, CEK spring, server board, TIM, and heat sink.

The CEK spring is removable, allowing for the use of heat sink retention solutions other than the Intel CEK.

Figure 9. CEK Processor Mounting



3.2.3 Memory Sub-system

The MCH masters two fully buffered DIMM (FBD) memory channels. FBD memory utilizes a narrow, high speed, frame-oriented interface referred to as a channel. On the server board, the two channels are routed to six DIMM slots and are capable of supporting registered DDR2-533 and DDR2-667 FBDIMM memory (stacked or unstacked). Peak theoretical memory data bandwidth is 6.4 GB/s with DDR2-533 or 8.0 GB/s with DDR2-667.

To boot the system, the system BIOS on the server board uses a dedicated I^2C bus to retrieve DIMM information needed to program the MCH memory registers. Table 2 provides the I^2C addresses for each DIMM slot.

Table 2. I^2C Addresses for Memory Module SMB

Device	Address
DIMM A1	0xA0
DIMM A2	0xA2
DIMM A3	0xA4

Table 2. I^2C Addresses for Memory Module SMB

Device	Address
DIMM B1	0xA0
DIMM B2	0xA2
DIMM B3	0xA4

3.2.3.1 Memory RASUM Features

The MCH supports several memory RASUM (Reliability, Availability, Serviceability, Usability, and Manageability) features. These features include the Intel® x4 Single Device Data Correction (x4 SDDC) for memory error detection and correction, Memory Scrubbing, Retry on Correctable Errors, memory Built-In Self Test (BIST), and DIMM Sparing. Memory Mirroring is not supported on the S5000PHB. See the *Intel® S5000 Server Board Family Datasheet* for more information describing these features.

3.2.3.2 Supported Memory

The server board supports up to six DDR2-533 or DDR2-667 Fully Buffered DIMMs (FBD memory). Table 3 and Table 4 show the maximum memory configurations supported using the specified memory technology.

Table 3. Maximum 6 DIMM System Memory Configuration – x8 Single Rank

DRAM Technology x8 Single Rank	Maximum Capacity
256 Mb	1.5 GB
512 Mb	3 GB
1024 Mb	6 GB
2048 Mb	12 GB

Table 4. Maximum 6 DIMM System Memory Configuration – x4 Dual Rank

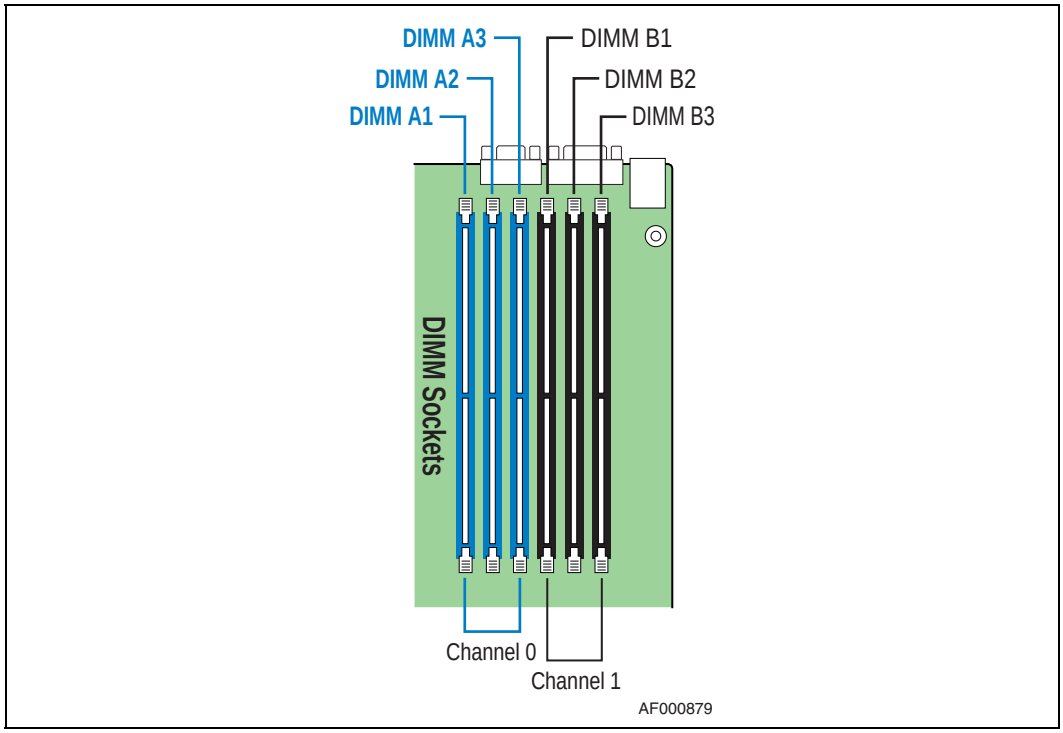
DRAM Technology x4 Dual Rank	Maximum Capacity
256 Mb	6 GB
512 Mb	12 GB
1024 Mb	24 GB

Note: DDR2 DIMMs that are not fully buffered are NOT supported on this server board. See the Intel® Server Board S5000PHB *Tested Memory List* for a list of supported memory for this server board.

3.2.3.3 DIMM Population Rules and Supported DIMM Configurations

Figure 10 identifies the positions of the six DIMM slots.

Figure 10. Server Board S5000PHB DIMM Slots



DIMM pairs are populated in the following DIMM slot order: A1 and B1, A2 and B2, A3 and B3. DIMMs within a given pair must be identical with respect to size, speed, and organization. However, DIMM capacities can be different between different DIMM pairs. For example, a valid mixed DIMM configuration may have 512 MB DIMMs installed in DIMM slots A1 and B1, and 1 GB DIMMs installed in DIMM slots A2 and B2. Operation with a single DIMM is supported with the DIMM installed in slot A1, but populating in pairs is recommended.

Supported DIMM configurations are shown in Table 5.

Table 5. FBD DIMM Population Options

Channel 0			Channel 1			Sparing Possible
DIMM A1	DIMM A2	DIMM A3	DIMM B1	DIMM B2	DIMM B3	
Populated						No
Populated			Populated			No
Populated	Populated		Populated	Populated		Yes
Populated	Populated	Populated	Populated	Populated	Populated	No

3.2.3.3.1 Sparing Mode Memory Configuration

The MCH provides memory sparing capabilities. Sparing is a RASUM feature that involves configuring a DIMM to be placed in reserve so it can be use to replace a DIMM that fails. The Memory Sparing configuration is subject to the following rules:

- DIMM slots A1 and B1 must be populated by FBDIMMs that are identical in organization, size, and speed.

- DIMM slots A2 and B2 must be populated by FBDIMMs that are identical in organization, size, and speed.
- The pair of FBDIMMs in DIMM slots A1 and B1 need not be identical in organization, size, and speed to the pair of modules in DIMM slots A2 and B2.
- Sparing must be enabled in the BIOS setup so that the BIOS will configure Rank Sparing Mode.
- The larger of the pairs {A1, B1} and {A2, B2} is the spare pair unit; the smaller pair is the active pair.

3.3 ESB2-E I/O Controller

The ESB2-E is a multi-function device that provides four distinct functions: an I/O controller, a PCI-X* bridge, a gigabit Ethernet (GbE) controller, and a baseboard management controller (BMC). Each function within the ESB2-E has its own set of configuration registers. Once configured, each appears to the system as a distinct hardware controller.

A primary role of the ESB2-E is to provide the gateway to all PC-compatible I/O devices and features. The server board uses the following ESB2-E features:

- PCI-X* bus interface
- Six-channel SATA interface w/SATA busy LED control
- Dual GbE MAC
- Baseboard Management Controller (BMC)
- Single ATA interface, with Ultra DMA 100 capability
- Universal Serial Bus (USB) 2.0 interface
- Removable media drives
- LPC bus interface
- PC-compatible timer/counter and DMA controllers
- APIC and 8259 interrupt controller
- Power management
- System RTC
- General purpose I/O

This section describes the function of most of the listed features as they pertain to this server board. For more detailed information, see the *Intel® S5000 Server Board Family Datasheet or the Intel® Enterprise South Bridge-2 External Design Specification* (restricted document).

3.3.1 PCI Sub-System

The primary I/O buses for the server board are PCI, PCI-X*, and PCI Express* (PCIe*), with six independent PCI bus segments. The PCI buses comply with the *PCI Local Bus Specification*, Revision 2.3. Table 6 lists the characteristics of the PCI bus segments. Details about each bus segment follow the table.

Table 6. PCI Bus Segment Characteristics

PCI Bus Segment	Voltage	Width	Speed/ Bandwidth	Type	On-board Device Support
PCI32 ESB2-E	3.3V	32 bits	33 MHz	PCI	Used internally for video controller
PXA ESB2-E	3.3V/5.0V	64 bits	133 MHz	PCI-X	Passive riser slot (one slot)
PE1, PE2 ESB2-E PCIe	3.3V	x8	20 Gbps	PCIe	To front panel via flex connector
PE4 BNB PCIe	3.3V	x4	10 Gbps	PCIe	Intel® 82571EB LAN (except NSW1U-F)
PE6, PE7 BNB PCIe	3.3V	x8	20 Gbps	PCIe	Passive riser slot (one slot)

3.3.1.1 PCI32: 32-bit, 33-MHz PCI Subsystem

All 32-bit, 33-MHz PCI I/O is directed through the ESB2-E ICH6. The 32-bit, 33-MHz PCI segment created by the ESB2-E ICH6 is known as the PCI32 segment. The PCI32 segment supports the ATI* RN50 2D graphics accelerator as a video controller.

3.3.1.2 PXA: 64-bit, 133MHz PCI Subsystem

One 64-bit PCI-X bus segment is directed through the ESB2-E ICH6. This PCI-X segment, PXA, supports one slot on an optional passive riser card.

3.3.1.3 PE1, PE2: Two x4 PCI Express Bus Segments

Two x4 PCI Express bus segments are directed through the ESB2-E. These PCI Express segments support either a Ethernet Front Panel (EFP) board (NSW1U servers only) or an SAS Front Panel (SFP) board (TIGW1U server only).

3.3.1.4 PE4: One x4 PCI Express Bus Segment

One x4 PCI Express bus segment is directed through the ESB2-E. This PCI Express segment, PE4, supports one Intel® 82571EB LAN controller on all products except NSW1U-F.

3.3.1.5 PE6, PE7: Two x4 PCI Express Bus Segments

Two x4 PCI Express bus segments are directed through the MCH. These PCI Express segments, PE6 and PE7, support one x8 PCI Express link to the passive riser slot.

3.3.1.6 PCI Riser Slot

The server board provides one riser slot capable of supporting a single-slot PCI-X passive riser card or a single-slot PCIe passive riser card.

3.3.2 Parallel ATA (PATA) Support

The integrated IDE controller of the ESB2-E ICH6 provides one IDE channel. It redefines signals on the IDE cable to allow both host and target throttling of data and transfer rates of up to 100 MB/s. For this server board, the IDE channel was designed to provide optical drive support to the platform. The BIOS initializes and supports ATAPI devices such as LS-120/240, CD-ROM, CD-RW, and DVD. The IDE channel is accessed

through a single, high-density, 44-pin connector which provides both power and I/O signals. The ATA channel can be configured and enabled or disabled by accessing the BIOS Setup Utility during POST.

3.3.3 USB 2.0 Support

The USB controller functionality that is integrated into the ESB2-E provides the server board with the interface for up to eight USB 2.0 ports. The Server Board S5000PHB uses five of these USB 2.0 ports as follows:

- Two external USB connectors are located on the back edge of the server board.
- Two USB ports are routed through the flex connector to the front panel board. The front panel board typically makes one of these ports available externally and uses one to support an optional Intel® Z-U130 Value Solid State Drive.
- One USB port is dedicated to the ASMI connector for the optional Intel® Remote Management Module 2.

3.4 Video Support

The server board provides an ATI* RN50 PCI graphics accelerator, along with 16 MB of DDR video SRAM and support circuitry for an embedded VGA video sub-system. The ATI RN50 chip contains a VGA video controller, clock generator, 2D engine, and RAMDAC in a 359-pin BGA. One 4M x 16-bit x 4 bank DDR SRAM chip provides 16 MB of video memory.

The VGA sub-system supports a wide number of combinations of resolution, color depths, and refresh rate for both CRT and LCD monitors.

Video is accessed using a standard 15-pin VGA connector found on the back edge of the server board. Hot plugging the video while the system is running is supported.

On-board video can be disabled through the BIOS Setup Utility or when an add-in video card is installed. The system BIOS also provides the option for dual video operation when an add-in video card is configured in the system.

3.4.1 Video Modes

The ATI RN50 chip supports all standard IBM* VGA modes. Table 7 shows the 2D modes supported for both CRT and LCD.

Table 7. Supported Video Modes

Resolution	Refresh Rate (Hz)	Color Depth (bpp)		
		166 MHz Mem Clk	200 MHz Mem Clk	250 MHz Mem Clk
640 x 480	60, 72, 75, 85, 90, 100, 120, 160, 200	8/16/32	8/16/32	8/16/32
800 x 600	60, 70, 72, 75, 85, 90, 100	8/16/32	8/16/32	8/16/32
	160	8/16	8/16/32	8/16/32
	200	8/16	8/16	8/16/32

Table 7. Supported Video Modes

Resolution	Refresh Rate (Hz)	Color Depth (bpp)		
		166 MHz Mem Clk	200 MHz Mem Clk	250 MHz Mem Clk
1024 x 768	60, 70, 72, 75, 85	8/16/32	8/16/32	8/16/32
	90, 100	8/16	8/16/32	8/16/32
	120	8/16	8/16	8/16/32
	140, 150, 160	8/16	8/16	8/16
	200	8	8/16	8/16
1152 x 864	43, 47, 60	8/16/32	8/16/32	8/16/32
	70, 75, 80	8/16	8/16/32	8/16/32
	85, 100	8/16	8/16	8/16/32
	120	8/16	8/16	8/16
	150, 160	8	8/16	8/16
1280 x 1024	60	8/16	8/16/32	8/16/32
	70, 74, 75	8/16	8/16	8/16/32
	85, 90, 100	8/16	8/16	8/16
	120	8	8/16	8/16
1600 x 1200	52	8/16	8/16	8/16/32
	58, 60, 66	8/16	8/16	8/16
	75	8	8/16	8/16

3.4.2 Video Memory Interface

The memory controller sub-system of the RN50 arbitrates requests from the direct memory interface, the VGA graphics controller, the drawing co-processor, the display controller, the video scalar, and the hardware cursor. Requests are serviced in a manner that ensures display integrity and maximum CPU/co-processor drawing performance.

The server board supports a 16 Mbyte (4 MB ×16 bits × 4 banks) DDR SDRAM device for video memory.

3.4.3 Dual Video

The BIOS supports single and dual video modes. Single video mode is enabled by default.

- In single video mode (Dual Monitor Video = Disabled), the on-board video controller is disabled when an add-in video card is detected.
- In dual video mode (On-board Video = Enabled, Dual Monitor Video = Enabled), the on-board video controller is enabled and will be the primary video device. The external video card will be allocated resources and is considered the secondary video device.

BIOS Setup provides user options to configure the feature as follows.

Table 8. BIOS Video Options

Feature	Options	Description
On-board Video	**Enabled** Disabled	
Dual Monitor Video	Enabled **Disabled**	This feature is unavailable and displayed as shaded if the On-board Video feature is set to “Disabled”

3.5 Network Interface Controller (NIC)

Network interface support is provided from the built-in dual GbE MAC features of the ESB2 in conjunction with the Intel® 82563EB compact Physical Layer Transceiver (PHY) and, separately, the Intel® 82571EB. Together, they provide the server board with support for four LAN ports. Both devices are capable of transmitting and receiving data at rates of 1000 Mbps, 100 Mbps, or 10 Mbps on each port.

The 82563EB device is based upon proven PHY technology integrated into Intel gigabit Ethernet controllers. The physical layer circuitry provides a standard IEEE 802.3 Ethernet interface for 1000Base-T, 100Base-T, and 10Base-T applications (802.3, 802.3u, and 802.3ab).

The 82571EB Dual Gigabit Ethernet Controller connects to the ESB2 by means of a x4 PCI Express (PCIe) link, and provides both Media Access Controller (MAC) and physical layer (PHY) functionality.

Each network interface controller (NIC) drives two LEDs located on each network interface connector. The green link/activity LED (to the left of the connector) indicates network connection when on, and transmit/receive activity when blinking. The bi-color speed LED (to the right of the connector) indicates 1000-Mbps operation when amber, 100-Mbps operation when green, and 10-Mbps operation when off. Table 9 provides summarizes the LED indications.

Table 9. NIC Status LED Indications

LED Color	LED State	NIC State
Green (Left)	On	Network connection present but inactive
	Blinking	Transmit/receive activity
Green/Amber (Right)	Off	10 Mbps speed
	Amber	100 Mbps speed
	Green	1000 Mbps speed

3.5.1 I/O Acceleration Technology

Intel® I/O Acceleration Technology (I/OAT) moves network data more efficiently through Intel® Xeon® processor-based servers for improved application responsiveness across diverse operating systems and virtualized environments. I/OAT improves network application responsiveness by unleashing the power of Intel Xeon processors through more efficient network data movement and reduced system overhead. Intel multi-port network adapters with Intel I/OAT provide high-performance I/O for server consolidation and virtualization through stateless network acceleration that seamlessly scales across multiple ports and virtual machines. I/OAT provides safe and flexible network acceleration through tight integration into popular Operating Systems and Virtual Machine Monitors, avoiding the support risks of third-party network stacks and preserving existing network requirements such as teaming and failover.

3.5.2 MAC Address Definition

Each Server Board S5000PHB has a block of consecutive MAC addresses assigned to it at the factory. The quantity of addresses assigned depends on the configuration of the server board. The Bypass version of the IP Network Server NSW1U is assigned ten MAC addresses, and the other server board configurations are assigned six MAC addresses.

The base address assigned during the manufacturing process is indicated with a white MAC address sticker placed on the board. The sticker displays the MAC address in both bar code and alphanumeric formats. The printed MAC address is assigned to NIC 1. NIC 2 is assigned a MAC address equal to the NIC 1 address +1. Both NICs are associated with the 82563EB PHY device.

The next two MAC addresses (offsets +2 and +3 relative to the printed address) are assigned to the baseboard management controller (BMC) embedded in the ESB-2. These MAC addresses are used by the BMC's embedded network stack to enable IPMI remote management over LAN and are not accessible to operating system network drivers. These BMC LAN channels use the same physical RJ45 connectors as NIC1 and NIC2 of the operating system, but must have their own unique IP addresses configured and used by the ESB2. (For tools to configure the ESB2 LAN channels, see http://ipmiutil.sourceforge.net/).

The next two addresses (offsets +4 and +5) are assigned to NIC 3 and NIC 4, which are implemented using a 82571EB Dual Gigabit Ethernet Controller.

The Server Board S5000PHB configuration for the Bypass version of the IP Network Server NSW1U is assigned an additional block of four MAC addresses (offsets +6 through +9) for the four NICs that are implemented on a unique Ethernet front panel (EFP) board assembly that includes two 82571EB Dual Gigabit Ethernet Controllers.

3.6 Super I/O Device

Legacy I/O support is provided by using a National Semiconductor* PC87427 Super I/O device. This chip contains all of the necessary circuitry to support the following functions:

- GPIOs
- Two serial ports (A & B)
- Keyboard and mouse support
- Wake up control
- System health support

3.6.1 Serial Ports

The server board provides two serial ports: an external RJ45 connector for serial port B, and an internal DH10 serial header for serial port A.

3.6.1.1 Serial Port B

The rear Serial B port is a fully functional serial port that can support any standard serial device. An RJ45 connector is used for this serial port to allow direct connection to serial port concentrators, which typically use RJ45 connectors and are widely used in the high-density server market. For server applications that use a serial concentrator to access the system management features of the server board, a standard 8-pin CAT-5 cable from the serial concentrator is plugged directly into the rear RJ45 serial port.

Various serial port concentrators may require either the DCD (Data Carrier Detect) or DSR (Data Signal Ready) signal on Pin 7 of the RJ45 connector. To accommodate both types of concentrators, the rear Serial B port connector can be configured using an on-board jumper (J2A2) to support either of these signals. The default configuration connects the DSR signal for compatibility with Cisco* serial concentrators. See Section 6.2, "Serial B Port Configuration Jumper" on page 51, for details on how to configure the port to support the DCD signal for use with standard modems or serial concentrators that do not use the Cisco convention.

For server applications that require a DB9 serial connector, an 8-pin RJ45-to-DB9 adapter must be used. The following table provides the pin-out required for the adapter to provide RS-232 support. 8-pin RJ45-to-DB9 DCD, DSR, and EMP-Modem adapters are available from Intel in the Serial Port Accessory Kit, product code: AXXRJ45DB9.

Table 10. Serial B Port RJ45 Connector Pin-Out and DB9 Adapter Pin Assignments

RJ45 Pin No.	Signal	Description	DB9 Pin No.
1	RTS	Request to Send	7
2	DTR	Data Terminal Ready	4
3	TD	Transmitted Data	3
4	SGND	Signal Ground	5
5	RI	Ring Indicator	9
6	RD	Received Data	2
7	DCD/DSR	Data Carrier Detect -or- Data Signal Ready (default)†	1 or 6 ††
8	CTS	Clear To Send	8

† The signal on RJ45 Pin 7 is configured by jumper J2A2 on the Server Board S5000PHB. It may be either DSR (the default configuration for Cisco compatibility) or DCD.

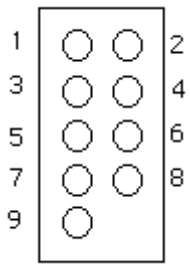
†† The wiring of the RJ45-to-DB9 adapter should match the requirements of the external serial device used and the configuration of the RJ45 pin-out. One of two pin-out configurations is used, depending on whether the serial device requires a DSR or DCD signal.

The Serial B port signals are also available on the front-panel flex connector.

3.6.1.2 Serial Port A

The Serial A port is an optional port accessed through an internal 9-pin DH-10 header. A standard DH10-to-DB9 cable can be used to direct the Serial A port to the rear of a chassis. The Serial A interface follows the standard RS-232 pin-out as defined in the Table 11.

Table 11. Serial A Header Pin Assignments

Header Pin No.	Signal Name	Serial Port A Header Pin-Out
1	DCD	
2	DSR	
3	RX	
4	RTS	
5	TX	
6	CTS	
7	DTR	
8	RI	
9	GND	

Note: When using the Serial A port header, you must use a cable with a mating connector that does not have a keying tab on the side of the connector body. Such a tab mechanically interferes with the housing of the PATA (IDE) connector, and prevents the cable from being seated properly.

3.6.2 Floppy Disk Controller

The server board does not support a floppy disk controller interface, but the system BIOS recognizes USB floppy devices.

3.6.3 Keyboard and Mouse Support

Dual, stacked PS/2 ports on the back edge of the server board provide keyboard and mouse support. Either port can support a mouse or keyboard. Neither port supports hot plugging.

3.6.4 Wake-up Control

The super I/O contains functionality that allows various events to power-on and power-off the system.

3.6.5 System Health Support

The SIO3 provides an interface via GPIOs for BIOS and server management firmware to activate the diagnostic LEDs, the FRU fault indicator LEDs for processors, FBDIMMs, and fans, and the system status LED. See Section 2.3 for the location of the LEDs on the server board except for the fan LEDs. For the fan LED locations, see the technical product specification for your particular server system.

The SIO3 also provides PWM fan control to the system fans, monitors tach and presence signals for the system fans, and monitors baseboard and front panel temperature.

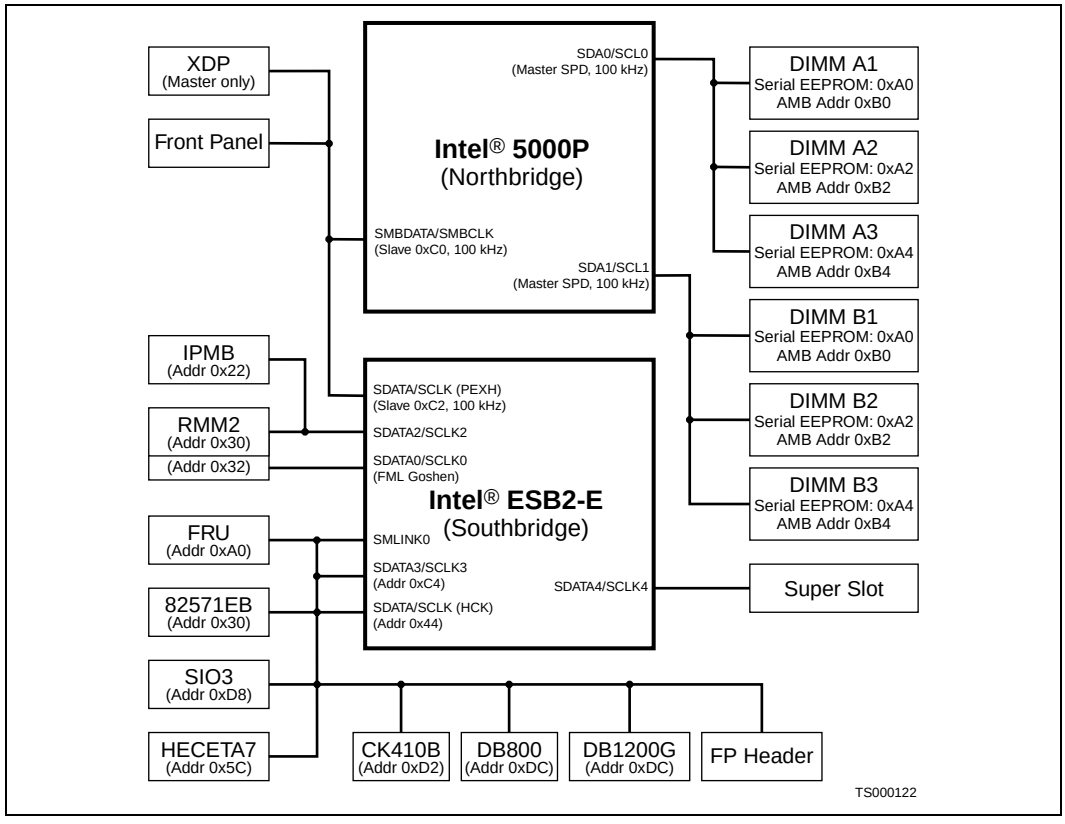
4 Platform Management

The platform management sub-system on the Intel® Server Board S5000PHB is based on the integrated baseboard management controller (BMC) features of the ESB2-E. The on-board platform management subsystem consists of communication buses, sensors, system BIOS, and server management firmware. Figure 11 provides an overview of the Server Management Bus (SMBUS) architecture used on this server board.

See Appendix B, "Sensor Tables" for on-board sensor data.

For more detailed platform management information, see the *Intel® S5000 Server Board Family Datasheet*.

Figure 11. SMBUS Block Diagram



5 Connector / Header Locations and Pin-outs

5.1 Board Connector Information

This chapter provides information about the connectors, headers, and jumpers on the Intel® Server Board S5000PHB. Table 12 lists the connector types available on the board and the corresponding reference designators printed on the silkscreen.

Table 12. Board Connectors, Headers, and Jumpers

Connector	Qty	Reference Designator(s)	Connector Type	Pin Count
Power Distribution Board	1	J1J3	Main and Auxiliary Power	16
CPU	2	U5G1, U8G1	CPU Sockets	771
Main Memory	6	J7B1, J7B2, J8B1, J8B2, J8B3, J9B1	DIMM Sockets	240
Riser Superslot	1	J4B1	Card Edge	280
Front Panel Flex Connector	1	J4J1	Shrouded Header	140
ASMI	1	J3C1	Mezzanine	120
GCM3	1	J3B1	Mezzanine	30
IDE	1	J2J1	Shrouded Header	44
Battery	1	XBT4G1	Battery Holder	3
Keyboard / Mouse	1	J9A1	External, PS/2, stacked	12
Rear USB / Serial Port B	1	J6A1	External, stacked	16
Serial Port A	1	J3H2	Header (internal)	9
Video connector	1	J8A1	External, D-Sub	15
LAN connector 10 / 100 / 1000	2	JA6A1, JA5A1	External LAN connector with built-in magnetic	38
IPMB	1	J1D1	Header	3
System Recovery Setting Jumpers	3	J1H2, J1G1, J1F1, J1E3	Jumper	3
Processor Select Jumper Caution: Pins 2-3 should never be jumpered. The system will not function correctly if these pins are jumpered.	1	J3E2	Jumper	3
Telco Alarms	1	J8A2	External, D-Sub	15
SAS Connector	1	J2A1	External	25

5.2 Power Connectors

The main (and only) power supply connection is made through the power distribution board via connector J1J3. This connector provides I^2C monitoring of the power supply along with the +12V, -12V, 5V, 3.3V, 5V standby, and sense lines. Table 13 defines the connector pin-out.

Table 13. Power Connector Pin-out (J1J3)

Pin	Signal	Pin	Signal
1	PS_PWRGD	9	5V Standby
2	PS_ON_N	10	5V Standby
3	-12V	11	5V Sense
4	SMB_SCL	12	5V Standby
5	SMB_SDA	Blade	12V
6	SMB_ALRT	Blade	5V
7	GND_SENSE	Blade	3.3V
8	3.3V Sense	Blade	GND

5.3 System Management Headers

5.3.1 Remote Management Module 2 Connector

A 120-pin ASMI Connector (J3C1) is included for sole support of the optional Intel® Remote Management Module 2. There is no support for third-party ASMI cards.

Note: This connector is not compatible for use with Intel® Server Management Module Professional Edition (Product Code AXXIMMPRO) or the Intel® Server Management Module Advanced Edition (Product Code AXXIMMADV).

Table 14. ASMI Connector Pin Assignments (J3C1) (Sheet 1 of 3)

Pin	Signal Name	Pin	Signal Name
1	Reserved - NC	2	GND
3	ESB_PLT_RST_G1_N	4	Reserved - NC
5	GND	6	Reserved - NC
7	Reserved - NC	8	GND
9	Reserved - NC	10	GND
11	GND	12	Reserved - NC
13	GND	14	IRQ_SERIAL_R
15	USB_ESB_P7P	16	GND
17	USB_ESB_P7N	18	GND
19	GND	20	Reserved - NC
21	P3V3	22	Reserved - NC
23	LPC_LAD<0>	24	GND
25	LPC_LAD<1>	26	LPC_FRAME_N
27	P3V3	28	LPC_LAD<2>
29	LPC_LCLK	30	LPC_LAD<3>

Table 14. ASMI Connector Pin Assignments (J3C1) (Sheet 2 of 3)

Pin	Signal Name	Pin	Signal Name
31	P3V3	32	P3V3
33	SMB_1_3V3SB_MS_DAT	34	SMB_IPMB_3V3SB_DAT
35	SMB_1_3V3SB_SL_DAT	36	SMB_IPMB_3V3SB_CLK
37	SMB_1_3V3SB_MS_CLK	38	SMB_0_3V3SB_MS_CLK
39	SMB_1_3V3SB_INT	40	SMB_0_3V3SB_INT
41	P3V3_AUX	42	SMB_0_3V3SB_MS_DAT
43	SPB_IMM_DSR_N	44	SMB_0_3V3SB_SL_DAT
45	SPB_IMM_RTS_N	46	P3V3_AUX
47	SPB_IMM_CTS_N	48	FM_IMM_PRESENT_N
49	SPB_IMM_DCD_N	50	SPB_IMM_DTR_N
51	SPB_RI_N	52	SPB_IMM_SIN
53	SPB_IMM_SOUT	54	P3V3_AUX
55	P3V3_AUX	56	V_LCDDATA7
57	V_LCDCNTL3	56	V_LCDDATA6
59	P3V3_AUX	60	V_LCDDATA5
61	Reserved - NC	62	V_LCDDATA4
63	Reserved - NC	64	V_LCDDATA3
65	GND	66	V_LCDCNTL1
67	V_LCDCNTL0	68	GND
69	Reserved - NC	70	V_LCDDATA15
71	GND	72	V_LCDDATA714
73	V_LCDDATA23	74	V_LCDDATA13
75	V_LCDDATA22	76	V_LCDDATA12
77	V_LCDDATA21	78	V_LCDDATA11
79	V_LCDDATA20	80	GND
81	V_LCDDATA19	82	V_LCDCNTL2
83	GND	84	V_DVO_DDC_SDA
85	FM_MAN_LAN_TYPE1	86	V_DVO_DDC_SCL
87	FM_MAN_LAN_TYPE1	88	RST_PS_PWRGD
89	Reserved - NC	90	Reserved - NC
91	Reserved - NC	92	Reserved - NC
93	MII_MDC_RMII_SPARE	94	Reserved - NC
95	MII_COL_RMIIB_RXER	96	GND
97	GND	98	MII_CRS_RMIIB_CRS
99	MII_TXER_RMIIB_TXEN	100	MII_TXCLK_RMIIB_RXCLK
101	MII_MDIO_RMIIB_PRESENT	102	GND
103	GND	104	MII_TXD3_RMIIB_TXD1
105	MII_RXD3_RMIIB_RXD1	106	MII_TXD2_RMIIB_TXD0
107	MII_RXD2_RMIIB_RXD0	108	GND
109	GND	110	MII_TXD1_RMIIA_TXD1

Table 14. ASMI Connector Pin Assignments (J3C1) (Sheet 3 of 3)

Pin	Signal Name	Pin	Signal Name
111	MII_RXD1_RMIIA_RXD1	112	MII_TXD0_RMIIA_TXD0
113	MII_RXD0_RMIIA_RXD0	114	GND
115	GND	116	MII_TXEN_RMIIA_TXEN
117	MII_RXCLK	118	MII_RXER_RMIIA_TXER
119	MII_RXDV_RMIIA_CRS	120	GND

5.3.2 IPMB Header

Table 15. IPMB Header Pin Assignments (J1D1)

Pin	Signal Name	Description
1	SMB_IPMB_5VSB_DAT	BMC IMB 5V Standby Data Line
2	GND	
3	SMB_IPMB_5VSB_CLK	BMC IMB 5V Standby Clock Line

5.4 Riser Superslot

The server board has one superslot (J4B1) utilizing Intel® Adaptive Slot Technology. It is capable of supporting single-slot passive riser cards that support either PCI-X* or PCI Express* full-height / full-length adapter cards. Table 17 shows the pin-out for the superslot.

Table 16. Low-profile Riser Slot Pin Assignments (J4B1) (Sheet 1 of 5)

Pin	Signal	Pin	Signal
A1	PWRGD_SYS_BUF	B1	12V
A2	12V	B2	12V
A3	12V	B3	12V
A4	GND	B4	GND
A5	NC	B5	SMBCLK
A6	NC	B6	SMBDATA
A7	NC	B7	GND
A8	NC	B8	3.3V
A9	3.3V	B9	NC
A10	3.3V	B10	3.3V STANDBY
A11	PE_RST_N	B11	PE_WAKE_N
A12	GND	B12	NC
A13	CLK_100M_P	B13	GND
A14	CLK_100M_N	B14	PCIE6_TX0_P
A15	GND	B15	PCIE6_TX0_N
A16	PCIE6_RX0_P	B16	GND
A17	PCIE6_RX0_N	B17	NC

Table 16. Low-profile Riser Slot Pin Assignments (J4B1) (Sheet 2 of 5)

Pin	Signal	Pin	Signal
A18	GND	B18	GND
A19	NC	B19	PCIE6_TX1_P
A20	GND	B20	PCIE6_TX1_N
A21	PCIE6_RX1_P	B21	GND
A22	PCIE6_RX1_N	B22	GND
A23	GND	B23	PCIE6_TX2_P
A24	GND	B24	PCIE6_TX2_N
A25	PCIE6_RX2_P	B25	GND
A26	PCIE6_RX2_N	B26	GND
A27	GND	B27	PCIE6_TX3_P
A28	GND	B28	PCIE6_TX3_N
A29	PCIE6_RX3_P	B29	GND
A30	PCIE6_RX3_N	B30	NC
A31	GND	B31	NC
A32	NC	B32	GND
A33	NC	B33	PCIE7_TX0_P
A34	GND	B34	PCIE7_TX0_N
A35	PCIE7_RX0_P	B35	GND
A36	PCIE7_RX0_N	B36	GND
A37	GND	B37	PCIE7_TX1_P
A38	GND	B38	PCIE7_TX1_N
A39	PCIE7_RX1_P	B39	GND
A40	PCIE7_RX1_N	B40	GND
A41	GND	B41	PCIE7_TX2_P
A42	GND	B42	PCIE7_TX2_N
A43	PCIE7_RX2_P	B43	GND
A44	PCIE7_RX2_N	B44	GND
A45	GND	B45	PCIE7_TX3_P
A46	GND	B46	PCIE7_TX3_N
A47	PCIE7_RX3_P	B47	GND
A48	PCIE7_RX3_N	B48	NC
A49	GND	B49	GND
A50	12V	B50	-12V
A51	PCIX_IRQ_N[1]	B51	5V
A52	5V	B52	PCIX_IRQ_N[3]
A53	5V	B53	5V
A54	5V	B54	5V
A55	PCIX_IRQ_N[2]	B55	PCIX_IRQ_N[0]
A56	5V	B56	GND
A57	PCIX_REQ_N[2]	B57	NC

Table 16. Low-profile Riser Slot Pin Assignments (J4B1) (Sheet 3 of 5)

Pin	Signal	Pin	Signal
A58	GND	B58	GND
A59	PCIX_GNT_N[2]	B59	NC
A60	GND	B60	GND
A61	PCIX_RST_N	B61	PCIX_REQ_N[1]
A62	5V	B62	GND
A63	NC	B63	GND
A64	GND	B64	PCIX_CLK
A65	PCIX_GNT_N[1]	B65	GND
A66	3.3V	B66	PCIX_REQ_N[0]
A67	PCIX_GNT_N[0]	B67	3.3V
A68	GND	B68	PCIX_PME_N[2]
A69	PCIX_PME_N[1]	B69	PCIX_AD[31]
A70	PCIX_PME_N[3]	B70	PCIX_AD[29]
A71	PCIX_AD[30]	B71	GND
A72	3.3V	B72	PCIX_AD[27]
A73	PCIX_AD[28]	B73	PCIX_AD[25]
A74	PCIX_AD[26]	B74	3.3V
A75	GND	B75	PCIX_CBE_N[3]
A76	PCIX_AD[24]	B76	PCIX_AD[23]
A77	PCIX_AD[22]	B77	GND
A78	3.3V	B78	PCIX_AD[21]
A79	PCIX_AD[20]	B79	PCIX_AD[19]
A80	PCIX_AD[18]	B80	3.3V
A81	GND	B81	PCIX_AD[17]
A82	PCIX_AD[16]	B82	PCIX_CBE_N[2]
A83	PCIXCAP	B83	GND
A84	3.3V	B84	PCIX_IRDY_N
A85	PCIX_FRAME_N	B85	3.3V
A86	GND	B86	PCIX_DEVSEL_N
A87	PCIX_TRDY_N	B87	GND
A88	GND	B88	PCIX_LOCK_N
A89	PCIX_STOP_N	B89	PCIX_PERR_N
A90	3.3V	B90	3.3V
A91	PCIX_SERR_N	B91	3.3V
A92	GND	B92	PCIX_CBE_N[1]
A93	PCIX_PAR	B93	PCIX_AD[14]
A94	PCIX_AD[15]	B94	GND
A95	3.3V	B95	PCIX_AD[12]
A96	PCIX_AD[13]	B96	PCIX_AD[10]
A97	PCIX_AD[11]	B97	PCIX_M66EN

Table 16. Low-profile Riser Slot Pin Assignments (J4B1) (Sheet 4 of 5)

Pin	Signal	Pin	Signal
A98	GND	B98	GND
A99	PCIX_AD[9]	B99	GND
A100	PCIX_CBE_N[0]	B100	PCIX_AD[8]
A101	3.3V	B101	PCIX_AD[7]
A102	PCIX_AD[6]	B102	3.3V
A103	PCIX_AD[4]	B103	PCIX_AD[5]
A104	GND	B104	PCIX_AD[3]
A105	PCIX_AD[2]	B105	GND
A106	PCIX_AD[0]	B106	PCIX_AD[1]
A107	3.3V	B107	3.3V
A108	PCIX_REQ64	B108	PCIX_ACK64
A109	5V	B109	5V
A110	5V	B110	5V
A111	PCIX_CBE_N[7]	B111	GND
A112	PCIX_CBE_N[5]	B112	PCIX_CBE_N[6]
A113	GND	B113	PCIX_CBE_N[4]
A114	PCIX_PAR64	B114	GND
A115	PCIX_AD[62]	B115	PCIX_AD[63]
A116	3.3V	B116	PCIX_AD[61]
A117	PCIX_AD[60]	B117	3.3V
A118	PCIX_AD[58]	B118	PCIX_AD[59]
A119	GND	B119	PCIX_AD[57]
A120	PCIX_AD[56]	B120	GND
A121	PCIX_AD[54]	B121	PCIX_AD[55]
A122	GND	B122	PCIX_AD[53]
A123	PCIX_AD[52]	B123	GND
A124	PCIX_AD[50]	B124	PCIX_AD[51]
A125	GND	B125	PCIX_AD[49]
A126	PCIX_AD[48]	B126	3.3V
A127	PCIX_AD[46]	B127	PCIX_AD[47]
A128	GND	B128	PCIX_AD[45]
A129	PCIX_AD[44]	B129	GND
A130	PCIX_AD[42]	B130	PCIX_AD[43]
A131	3.3V	B131	PCIX_AD[41]
A132	PCIX_AD[40]	B132	GND
A133	PCIX_AD[38]	B133	PCIX_AD[39]
A134	GND	B134	PCIX_AD[37]
A135	PCIX_AD[36]	B135	3.3V
A136	PCIX_AD[34]	B136	PCIX_AD[35]
A137	GND	B137	PCIX_AD[33]

Table 16. Low-profile Riser Slot Pin Assignments (J4B1) (Sheet 5 of 5)

Pin	Signal	Pin	Signal
A138	PCIX_AD[32]	B138	GND
A139	GND	B139	RISER_TYPE1
A140	RISER_TYPE2	B140	RISER_TYPE0

5.5 Front Panel Flex Connector

The server board provides a 140-pin high-density front panel flex connector (J4J1) to route control panel, midplane, and backplane signals from the server board to the front panel board. Two general types of front panels are available for use with the Server Board S5000PHB: an Ethernet Front Panel (EFP) for use with NSW1U servers and a SAS front panel (SFP) for use with the TIGW1U server. Table 17 provides the pin-out for this connector.

Table 17. 140-Pin Front Panel Flex Connector Pin Assignments (J4J1) (Sheet 1 of 3)

Pin #	Signal Name	Pin #	Signal Name
1	FLEX_PRES2	2	USB_P3P
3	SMB_CLK	4	USB_P3N
5	SMB_DATA	6	GND
7	OC_N[3]	8	CLK_100M_PCIE_P
9	GND	10	CLK_100M_PCIE_N
11	PCIE2_TX3_N	12	NC
13	PCIE2_TX3_P	14	GND
15	DU_HD_LED	16	PCIE2_RX3_N
17	GND	18	PCIE2_RX3_P
19	PCIE2_TX2_N	20	DU_LED4
21	PCIE2_TX2_P	22	GND
23	DU_LED2	24	PCIE2_RX2_N
25	GND	26	PCIE2_RX2_P
27	PCIE2_TX1_N	28	TELCO_LED_SELECT
29	PCIE2_TX1_P	30	GND
31	DU_LED3	32	PCIE2_RX1_N
33	GND	34	PCIE2_RX1_P
35	PCIE2_TX0_N	36	PWR_ENABLE
37	PCIE2_TX0_P	38	GND
39	FP_PWR_GOOD	40	PCIE2_RX0_N
41	GND	42	PCIE2_RX0_P
43	PCIE1_TX3_N	44	NIC_ACT_LED_N
45	PCIE1_TX3_P	46	GND
47	PWR_LED_N	48	PCIE1_RX3_N
49	GND	50	PCIE1_RX3_P
51	PCIE1_TX2_N	52	NMI_BTN_N
†	Marked signals are only used in TIGW1U systems.		

Table 17. 140-Pin Front Panel Flex Connector Pin Assignments (J4J1) (Sheet 2 of 3)

Pin #	Signal Name	Pin #	Signal Name
53	PCIE1_TX2_P	54	GND
55	PWR_BTN_N	56	PCIE1_RX2_N
57	GND	58	PCIE1_RX2_P
59	PCIE1_TX1_N	60	RST_BTN_N
61	PCIE1_TX1_P	62	GND
63	ID_BTN_N	64	PCIE1_RX1_N
65	GND	66	PCIE1_RX1_P
67	PCIE1_TX0_N	68	ID_LED_BUF_N
69	PCIE1_TX0_P	70	GND
71	TEMP_SENSOR	72	PCIE1_RX0_N
73	GND	74	PCIE1_RX0_P
75	USB_P2N	76	GND
77	USB_P2P	78	GND
79	GND	80	USB_OC_N[2]
81	FAN1_TACH	82	FAN2_TACH
83	FAN3_TACH	84	FAN4_TACH
85	FAN5_TACH	86	FAN6_TACH
87	FAN7_TACH	88	FAN8_TACH
89	FAN9_TACH	90	FAN_CPU1_PWM
91	FAN_PWM	92	FAN_CPU2_PWM
93	GND	94	GND
95	DTR2_N	96	EMP_INUSE_L
97	RTS2_N	98	SOUT2
99	SIN2	100	CTS2_N
101	DSR2_N	102	DCD2_N
103	GND	104	GND
105	SAS_RX7_P †	106	SYS_RESET_N †
107	SAS_RX7_N †	108	GND †
109	RAID_MODE_R †	110	SAS_TX7_N †
111	GND †	112	SAS_TX7_P †
113	SAS_RX6_P †	114	IBUTTON_PRES_N †
115	SAS_RX6_N †	116	GND †
117	SMB_SERIAL_CLK1 †	118	SAS_TX6_N †
119	GND †	120	SAS_TX6_P †
121	SAS_TX4_P †	122	FAULT_LED_SHIFT_OUT †
123	SAS_TX4_N †	124	GND †
125	RSM_RST_N †	126	SAS_RX4_N †
127	GND †	128	SAS_RX4_P †
129	SAS_RX5_P †	130	SAS_RAID_SPKR †
†	Marked signals are only used in TIGW1U systems.		

Table 17. 140-Pin Front Panel Flex Connector Pin Assignments (J4J1) (Sheet 3 of 3)

Pin #	Signal Name	Pin #	Signal Name
131	SAS_RX5_N †	132	GND †
133	SAS_DISABLE_N †	134	SAS_TX5_N †
135	GND †	136	SAS_TX5_P †
137	P3V3_STBY	138	GND
139	P3V3_STBY	140	GND
†	Marked signals are only used in TIGW1U systems.		

5.6 I/O Connector Pinout Definitions

5.6.1 VGA Connector

Table 18 details the pin-out definition of the VGA connector (J6A1).

Table 18. VGA Connector Pin Assignments (J8A1)

Pin	Signal Name	Description
1	V_IO_R_CONN	Red (analog color signal R)
2	V_IO_G_CONN	Green (analog color signal G)
3	V_IO_B_CONN	Blue (analog color signal B)
4	TP_VID_CONN_B4	No connection
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	TP_VID_CONN_B9	No Connection
10	GND	Ground
11	TP_VID_CONN_B11	No connection
12	V_IO_DDCDAT	DDCDAT
13	V_IO_HSYNC_CONN	HSYNC (horizontal sync)
14	V_IO_VSYNC_CONN	VSYNC (vertical sync)
15	V_IO_DDCCLK	DDCCLK

5.6.2 NIC Connectors

The server board provides two dual-RJ45 NIC connectors (except for the server board variant used in the NSW1U-F server) oriented side-by-side on the back edge of the board (JA6A1, JA5A1). The pin-out for each connector is identical and is defined in Table 19.

Table 19. Dual-RJ-45 10/100/1000 NIC Connector Pin Assignments (JA6A1, JA5A1)

Pin	Signal	Pin	Signal
1	NC	2	LAN_B_MDI3N
3	LAN_B_MDI2P	4	1.8V
5	LAN_B_MDI1N	6	LAN_B_MDI0P
7	1.8V	8	LAN_B_MDI3P
9	1.8V	10	LAN_B_MDI2N
11	LAN_B_MDI1P	12	1.8V
13	LAN_B_MDI0N	14	1.8V
15	LAN_A_MDI0P	16	LAN_A_MDI1N
17	1.8V	18	1.8V
19	LAN_A_MDI3N	20	GND
21	LAN_A_MDI0N	22	1.8V
23	LAN_A_MDI1P	24	LAN_A_MDI2N
25	1.8V	26	LAN_A_MDI3P
27	LINKA_LINKUP	28	LINKA_ACT_N
29	LINKA_100	30	LINKA_1000
31	LINKB_LINKUP	32	LINKB_ACT_N
33	LINKB_100	34	LINKB_1000
35	GND	36	GND
37	GND	38	GND

5.6.3 IDE Connector

The server board includes an IDE connector to access the single IDE channel from the ESB2 I/O controller hub. The design intent for this connector is to provide IDE support for a single slim-line optical drive, such as CD-ROM or DVD. The pin-out for this connector is defined in Table 20.

Table 20. 40-pin IDE Connector Pin Assignments (J2J1) (Sheet 1 of 2)

Pin	Signal	Pin	Signal
1	PLT_RST_N	2	GND
3	PDD[7]	4	PDD[8]
5	PDD[6]	6	PDD[9]
7	PDD[5]	8	PDD[10]
9	PDD[4]	10	PDD[11]
11	PDD[3]	12	PDD[12]
13	PDD[2]	14	PDD[13]
15	PDD[1]	16	PDD[14]
17	PDD[0]	18	PDD[15]
19	GND	20	NC
21	PDDREQ	22	GND
23	PDIOW_N	24	GND

Table 20. 40-pin IDE Connector Pin Assignments (J2J1) (Sheet 2 of 2)

Pin	Signal	Pin	Signal
25	PDIOR_N	26	GND
27	PIORDY	28	GND
29	PDDACK_N	30	GND
31	IRQ14	32	NC
33	PDA1	34	IDE_PRI_CBLSNS
35	PDA0	36	PDA2
37	PDCS1_N	38	PDCS3_N
39	IDE_LED_N	40	GND

5.6.4 GCM3 Connector

The server board provides an internal 30-pin mezzanine style connector (J1B2) to accommodate a proprietary form factor GCM3 Ethernet connector module. Table 21 details the pin-out of the GCM3 connector.

Table 21. 30-pin GCM3 Module Connector Pin Assignments (J3B1)

Pin	Signal	Pin	Signal
1	LAN_TYPE2	2	MII_MDC
3	LAN_TYPE1	4	MII_COL
5	GND	6	GND
7	MII_TXCLK	8	MII_TXER
9	MII_CRS	10	MII_MDIO
11	GND	12	GND
13	MII_TXD2	14	MII_RXD3
15	MII_TXD1	16	MII_RXD2
17	GND	18	GND
19	MII_TXD3	20	MII_RXD1
21	MII_TXD0	22	MII_RXD0
23	GND	24	GND
25	MII_TXEN	26	MII_RXCLK
27	P3V3_AUX	28	P3V3_AUX
29	MII_RXER	30	MII_RXDV

5.6.5 SAS Connector

The server board variant used in the TIGW1U server provides one SAS connector. This port (J2A1) provides RAID support. The pin configuration for this connector is defined in Table 22.

Table 22. SAS Connector Pin Assignments (J2A1)

Pin	Signal	Pin	Signal
S1	SAS_RX4_P	S2	SAS_RX4_N
S3	SAS_RX5_P	S4	SAS_RX5_N
S5	SAS_RX6_P	S6	SAS_RX6_N
S7	SAS_RX7_P	S8	SAS_RX7_N
S9	SAS_TX7_N	S10	SAS_TX7_P
S11	SAS_TX6_N	S12	SAS_TX6_P
S13	SAS_TX5_N	S14	SAS_TX5_P
S15	SAS_TX4_N	S16	SAS_TX4_P
G1	GND	G2	GND
G3	GND	G4	GND
G5	GND	G6	GND
G7	GND	G8	GND
G9	GND		

5.6.6 Serial Port Connectors

The server board provides one external RJ45 Serial ‘B’ port (J6A1) and one internal 9-pin Serial ‘A’ port header (J3H2). Table 23 and Table 24 define the pin-outs for each.

Table 23. External RJ-45 Serial ‘B’ Port Pin Assignments (J6A1)

Pin	Signal Name	Description
1	SPB_RTS	RTS (Request To Send)
2	SPB_DTR	DTR (Data Terminal Ready)
3	SPB_OUT_N	TXD (Transmit Data)
4	GND	Ground
5	SPB_RI	RI (Ring Indicate)
6	SPB_SIN_N	RXD (Receive Data)
7	SPB_DSR_DCD -OR- SPB_DSR_DSR †	DCD (Data Carrier Detect) [default] -OR- DSR (Data Set Ready) †
8	SPB_CTS	CTS (Clear To Send)
†	The signal on Pin 7 of the rear Serial B connector is configurable using jumper J2A2. The default setting is compatible with Cisco serial concentrators; the alternate configuration is compatible with standard modems.	

Table 24. Internal 9-pin Serial ‘A’ Header Pin Assignments (J3H2) (Sheet 1 of 2)

Pin	Signal Name	Description
1	SPA_DCD	DCD (Data Carrier Detect)
2	SPA_DSR	DSR (Data Set Ready)
3	SPA_SIN_L	RXD (Receive Data)

Table 24. Internal 9-pin Serial 'A' Header Pin Assignments (J3H2) (Sheet 2 of 2)

Pin	Signal Name	Description
4	SPA_RTS	RTS (Request To Send)
5	SPA_SOUT_N	TXD (Transmit Data)
6	SPA_CTS	CTS (Clear To Send)
7	SPA_DTR	DTR (Data Terminal Ready)
8	SPA_RI	RI (Ring Indicate)
9	GND	Ground

Note: When using the Serial A header, you must use a cable with a mating connector that does not have a keying tab on the connector body. Such a tab mechanically interferes with the housing of the PATA (IDE) connector and prevents the cable from being seated properly.

5.6.7 Keyboard and Mouse Connector

A stacked dual PS/2 port connector (J9A1) supports both a keyboard and a mouse. Both connectors have the same pin-out and can be used interchangeably for either keyboard or mouse. Table 25 details the pin-out of the PS/2 connectors.

Table 25. Stacked PS/2 Keyboard and Mouse Port Assignments (J9A1)

Pin	Signal Name	Description
1	KB_DATA_F	Keyboard Data
2	TP_PS2_2	Test point – keyboard
3	GND	Ground
4	P5V_KB_F	Keyboard / mouse power
5	KB_CLK_F	Keyboard Clock
6	TP_PS2_6	Test point – keyboard / mouse
7	MS_DAT_F	Mouse Data
8	TP_PS2_8	Test point – keyboard / mouse
9	GND	Ground
10	P5V_KB_F	Keyboard / mouse power
11	MS_CLK_F	Mouse Clock
12	TP_PS2_12	Test point – keyboard / mouse
13	GND	Ground
14	GND	Ground
15	GND	Ground
16	GND	Ground
17	GND	Ground

5.6.8 USB Connector

Table 26 details the pin-out of the external dual-USB connector (J6A1) found on the back edge of the server board. The connector is a combination device that includes two USB ports and an RJ45 serial port in the same connector housing. The two USB connectors have the same pin-out as detailed in the table.

Table 26. External USB Connector Pin Assignments (J6A1)

Pin	Signal Name	Description
1	USB_OC#_FB_1	USB_PWR
2	USB_P#N_FB_2	DATAL0 (Differential data line paired with DATAH0)
3	USB_P#N_FB_2	DATAH0 (Differential data line paired with DATAL0)
4	GND	Ground

5.6.9 Telco Alarms Connector

The version of the Server Board S5000PHB that is used in the Carrier Grade Server TIGW1U provides a Telco Alarms connector. Telco Alarms is a notification mechanism that provides error, warning, or status alarms when specific system events occur. The server board provides a DB15 rear-alarms connector for the alarms. The pin-out for this connector is in Table 27.

Table 27. Optional Telco Alarms Connector Pin Assignments (J8A2)

Pin	Signal	Pin	Signal
1	MINOR_RST_POS	2	MINOR_RST_NEG
3	MAJOR_RST_POS	4	MAJOR_RST_NEG
5	CRITICAL_NO	6	CRITICAL_NC
7	CRITICAL_COMM	8	MINOR_NO
9	MINOR_NC	10	MINOR_COMM
11	MAJOR_NO	12	MAJOR_NC
13	MAJOR_COMM	14	PWR_NO
15	PWR_COMM		

6 Jumper Block Settings

The Intel® Server Board S5000PHB has several 2-pin and 3-pin jumper blocks that can be used to configure, protect, or recover specific features of the server board. Pin 1 on each jumper block is denoted by a "•" or "▼" symbol. See Figure 1, "Server Board S5000PHB Components and Connector Location Diagram" on page 12 for jumper block locations.

6.1 Jumper Blocks

Table 28. Jumpers

Jumper Name	Pins	What happens at system reset...
J1E3: BMC Force Update jumper	**No Jumper**	BMC Firmware Force Update Mode – Disabled (Default)
	Jumper	BMC Firmware Force Update Mode – Enabled
J1H2: Password Clear jumper	**1-2**	These pins should have a jumper in place for normal system operation. (Default)
	2-3	If these pins are jumpered, administrator and user passwords will be cleared on the next reset. These pins should **not** be jumpered for normal operation.
J1G1: Bank Select jumper	1-2	Force to lower flash bank during boot-up
	2-3	Normal operation/use primary flash bank (Default)
J1F1: CMOS Clear jumper	**1-2**	These pins should have a jumper in place for normal system operation. (Default)
	2-3	If these pins are jumpered, the CMOS settings will be cleared on the next reset. These pins should **not** be jumpered for normal operation
J3E2: Processor Select jumper	**1-2**	If these pins are jumpered, the system is configured for a Dual-Core Intel® Xeon® processors 5100 series. (Default) Caution: Pins 2-3 should never be jumpered. The system will not function correctly if these pins are jumpered.
	No Jumper	If no pins are jumpered, the system is configured for a Quad-Core Intel® Xeon® processors 5300 series.
Note: **Bold** entry in "Pins" column indicates default configuration.		

6.1.1 CMOS Clear and Password Reset Procedures

The CMOS Clear and Password Reset recovery features achieve the desired operation with minimal system down time. The procedure is identical for these two features, but has changed from previous generation Intel server boards. The following steps outline the procedure for both operations.

1. Power the server down and remove the power cable. (Standby power is present on the server board when power is turned off but still connected.)
2. Open the server.

3. Move the jumper from the default operating position (Pins 1-2) to the Reset/Clear position (Pins 2-3) on the appropriate jumper (J1F1 for CMOS Clear or J1H2 for Password Reset).
4. Wait 5 seconds.
5. Move the jumper back to the default position (Pins 1-2).
6. Close the server chassis.
7. Reconnect the power source and power up the server.
8. Password and/or CMOS is now cleared and can be reset by going into BIOS setup.

6.1.2 BMC Force Update Procedure

When performing a standard BMC firmware update procedure, the update utility places the BMC into update mode, allowing the firmware to load safely onto the flash device. If the BMC firmware update process fails because the BMC was not the proper update state, the server board provides a BMC Force Update jumper to force the BMC into the update state. The following procedure should be followed if the standard BMC firmware update process fails.

1. Power down the server and remove the power cable. (Standby power is present on the server board when power is turned off but still connected.)
2. Open the server.
3. Place a jumper on the J1E3 header.
4. Close the server.
5. Reconnect the power source and power up the server.
6. Perform the BMC firmware update procedure as documented in README.TXT file that is included in the given BMC Firmware Update package.
7. After successful completion of the firmware update process, the firmware update utility may generate an error stating that the BMC is still in update mode.
8. Power down the server and remove the power cable.
9. Open the server.
10. Remove jumper from J1E3.
11. Close the server.
12. Reconnect power source and power up the server.

Note: Normal BMC functionality is disabled when the Force BMC Update jumper is populated. The server should never be run with the BMC Force Update jumper populated and should only be used if the standard firmware update process fails. This header should remain unpopulated when the server is running normally.

6.1.3 BIOS Select Jumper

The jumper block at J1G1 is used to select which BIOS image the system will boot. Pin 1 on the jumper is identified with a "▼". This jumper should only be moved if you wish to force the BIOS to boot to the secondary bank, which may hold a different version of BIOS.

The rolling BIOS feature of the server board will automatically alternate the Boot BIOS to the secondary bank in the event the BIOS image in the primary bank is corrupted and cannot boot for any reason.

6.2 Serial B Port Configuration Jumper

The rear of the Server Board S5000PHB provides an RJ45 connector for the Serial B port, which is intended for direct connection to serial devices such as serial port concentrators using a standard Cat. 5 cable. But various serial devices which use RJ45 connectors differ in what signal they require on Pin 7. For example, standard modems typically require the DSR signal, while many serial concentrators (including models from Cisco) require the DCD signal. Jumper J2A2 allows the serial port to be configured to provide either of these two signals as described in Table 29

Table 29. Serial B Port Configuration Jumper

Jumper Name	Pins	Description of Configuration
J2A2: Serial Port	**1-2**	DCD (Data Carrier Detect) signal routed to Pin 7 of rear RJ45 Serial B port connector. This configuration provides compatibility with Cisco serial concentrators. (Default)
	2-3	DSR (Data Set Ready) signal routed to Pin 7 of rear RJ45 Serial B port connectors. This configuration provides compatibility with standard modems.
Note: **Bold** entry in "Pins" column indicates default configuration.		

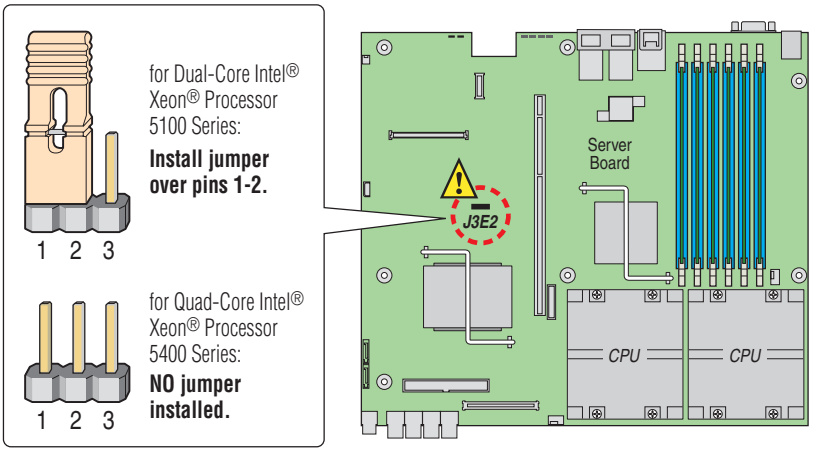
6.3 Processor Select Jumper

The server board is pre-configured for the Dual-Core Intel® Xeon® processor 5100 series, but the following server system product codes support both the Dual-Core Intel® Xeon® processor 5100 series and the Quad-Core Intel® Xeon® processor 5400 series. These product codes have an "R in the third position.

- NSRA0201W: Intel® IP Network Server NSW1U, rear NIC port, AC
- NSRD0201W: Intel® IP Network Server NSW1U, rear NIC port, DC
- NSRA0401W: Intel® IP Network Server NSW1U, bypass, AC
- TMRA0201W: Intel® Carrier Grade Server TIGW1U. AC
- TMRD0201W: Intel® Carrier Grade Server TIGW1U. DC

If you have a product with one of these product codes and you want to use a Quad-Core Intel® Xeon® processor 5400 series, you must remove the jumper from pins 1-2 on the processor select jumper. This jumper is located at position J3E2 on the server board. See the following figure.

CAUTION: Jumper J3E2 must be configured to match your installed processor or your system will not boot properly.



Regardless of the processor model you install, you must use BIOS version R0085 or later with any server that has one of the above product codes:

Caution: If your server has one of the above product codes, then configuring it with a BIOS version lower than R0085 will cause system instabilities and your system may not boot.

7 Light Guided Diagnostics

The Intel® Server Board S5000PHB has on-board diagnostic LEDs to assist in troubleshooting board-level issues. This section shows where each LED is located and provides a high-level usage description. For a more detailed description, see the *Intel® S5000 Server Board Family Datasheet*.

7.1 System ID LED and System Status LED

The server board provides LEDs for both System ID and System Status. These two LEDs are labeled “B” and “C”, respectively in Figure 2, “Light Guided Diagnostic LED Locations ” on page 13.

The blue System ID LED can be illuminated using either of two mechanisms:

- When the System ID button on the system control panel is pressed, the ID LED displays a solid blue color until the button is pressed again.
- When the appropriate IPMI Chassis Identify hex value is issued, the ID LED either blinks blue for 15 seconds and then turns off or blinks indefinitely until the appropriate IPMI Chassis Identify hex value is issued to turn it off.

The bi-color System Status LED operates as follows:

Table 30. System Status LED Decoder

System Status LED Indication		Status
Green	On [1]	Standby power on, system ready, or operating normally
	Blinking [1,2]	Degraded operation; see Section 7.1.3
Amber	On	Critical or non-recoverable condition; see Section 7.1.1
	Blinking [2]	Non-critical condition; see Section 7.1.2
Off	Off	Main and standby power off

Notes:
1. The amber status indication takes precedence over the green indication. When the amber LED is on or blinking, the green LED indications are suppressed.
2. Blink rate is ~1 Hz with at 50% duty cycle.

The following sub-sections define the system status conditions that are monitored and reported by the System Status LED when the server board is integrated into a supported Intel server chassis and is configured with the appropriate sensor data records (SDRs). Operation of the LED may differ if the server board is integrated into a custom chassis for which the appropriate SDRs are not written.

7.1.1 System Status LED – Monitored Critical Conditions

A critical condition is any critical or non-recoverable threshold crossing associated with the following events:

- Temperature, voltage, or fan critical threshold crossing.

- Power subsystem failure. The BMC asserts this failure whenever it detects a power control fault (e.g., the BMC detects that the system power remains ON even though the BMC has de-asserted the signal to turn off power to the system).
- A hot-swap backplane uses the Set Fault Indication command to indicate when one or more of the drive fault status LEDs is asserted on the hot-swap backplane.
- The system cannot power up due to incorrectly installed processor(s), or processor incompatibility.
- The satellite controller sends a critical or non-recoverable state, via the Set Fault Indication command to the BMC.
- Critical event logging errors, including: System Memory Uncorrectable ECC error, and fatal/uncorrectable bus errors such as PCI SERR and PERR.

7.1.2 System Status LED – Monitored Non-Critical Conditions

A non-critical condition is a threshold crossing associated with the following events:

- Temperature, voltage, or fan non-critical threshold crossing
- Chassis intrusion
- The satellite controller sending a non-critical state, via the Set Fault Indication command, to the BMC.
- Set Fault Indication command from system BIOS. The BIOS may use the Set Fault Indication command to indicate additional non-critical status such as a system memory or CPU configuration changes.

7.1.3 System Status LED – Monitored Degraded Conditions

A degraded condition is associated with the following events:

- Non-redundant power supply operation. This applies only when the BMC is configured for a redundant power subsystem.
- One or more processors are disabled by fault resilient booting (FRB) or by the BIOS.
- The BIOS has disabled or mapped out some of the system memory.

7.2 DIMM Fault LEDs

The server board provides a memory fault LED for each DIMM slot. The DIMM fault LED is illuminated when the System BIOS disables the specified DIMM after it reaches a specified number of failures or specific critical DIMM failures are detected. See the *Intel® S5000 Server Board Family Datasheet* for more details. These LEDs (six in all) are labeled “D” in Figure 2, “Light Guided Diagnostic LED Locations ” on page 13.

7.3 Processor Fault LED

The server board provides a Processor Fault LED for each processor. The location of these co-located LEDs is designated by the letter “E” in Figure 2, “Light Guided Diagnostic LED Locations ” on page 13. The LED labeled DS5J1 in the PCB silkscreen is associated with CPU1 while LED DS4J1 is associated with CPU2.

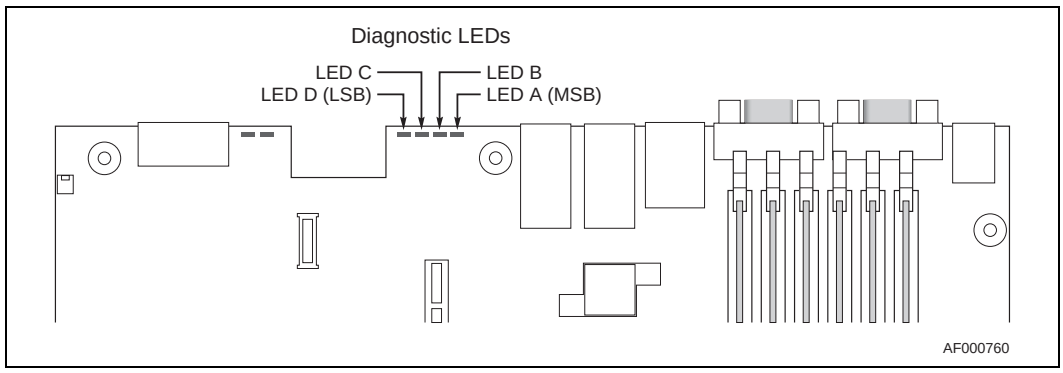
7.4 POST Code Diagnostic LEDs

During the system boot process, the BIOS executes platform configuration processes, each of which is assigned a specific hex POST code number. As each configuration routine is started, the BIOS displays the corresponding POST code to the POST Code

Diagnostic LEDs found on the back edge of the server board. If the system hangs during the POST process, the Diagnostic LEDs can be used to identify the last POST process to be executed to aid in troubleshooting. See Appendix C, "POST Codes" for a complete description of how these LEDs are read, and for a list of all supported POST codes.

The POST code LEDs are located next to the rear-panel LAN connectors. Table 31 can be used to decode the LED display to ascertain a given POST code. The most significant bit is represented by LED A, which is the POST LED farthest from the LAN connectors. The least significant bit is represented by LED D, which is located closest to the LAN connectors. Refer to Figure 12 for the LED layout.

Figure 12. POST Code Diagnostic LED Location



POST codes consist of one byte of data, and each LED simultaneously represents one bit from the most significant nibble and one bit from the least significant nibble. To be specific, LED A indicates bits 7 and 3, LED B indicates bits 6 and 2, LED C indicates bits 5 and 1, and LED D indicates bits 4 and 0. The various LED indications map to the bit values in each nibble as shown in Table 31.

Table 31. POST Code Decoder

LED Indication	MS Nibble Bit Value	LS Nibble Bit Value
Amber	1	1
Red	1	0
Green	0	1
Off	0	0

Consider the example of POST code ACh. The most significant nibble (bit seven to bit four) equals 1010b and the least significant nibble (bit three to bit zero) equals 1100b. LED A must therefore represent a 1 for bit seven and a 1 for bit three, LED B a 0 for bit six and a 1 for bit two, LED C a 1 for bit five and a 0 for bit one, and LED D a 0 for bit four and a 0 for bit zero. As shown in Table 32, this POST code is displayed as the LED sequence of amber (LED A), green (LED B), red (LED C), and off (LED D).

Table 32. POST Code Decoding Example

	LED A	LED B	LED C	LED D	
Display	Amber	Green	Red	Off	
MS Nibble Bit Value	1	0	1	0	= Ah
LS Nibble Bit Value	1	1	0	0	= Ch

8 Power and Environmental Specifications

8.1 Intel® Server Board S5000PHB Design Specifications

Operation of the Intel® Server Board S5000PHB at conditions beyond those shown in the following table may cause permanent system damage. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 33. Server Board Design Specifications

Operating Temperature	5º C to 50º C † (32º F to 131º F)
Non-Operating Temperature	-40º C to 70º C (-40º F to 158º F)
DC Voltage	±5% of all nominal voltages
Shock (Unpackaged)	Trapezoidal, 50 G, 170 inches/sec
Shock (Packaged) (40 lbs to < 80 lbs)	24 inches
Vibration (Unpackaged)	5 Hz to 500 Hz, 3.13 G RMS random
† Chassis design must provide proper airflow to avoid exceeding the processor maximum case temperature.	

Disclaimer Note: Intel® server boards support add-in peripherals and contain high-density VLSI and power delivery components that need adequate airflow to cool. Intel ensures through its own chassis development and testing that when Intel server building blocks are used together, the fully integrated system will meet the intended thermal requirements of these components. It is the responsibility of the system integrator who chooses not to use Intel-developed server building blocks to consult vendor datasheets and operating parameters to determine the amount of air flow required for their specific application and environmental conditions. Intel Corporation cannot be held responsible, if components fail or the server board does not operate correctly when used outside any of their published operating or non-operating limits.

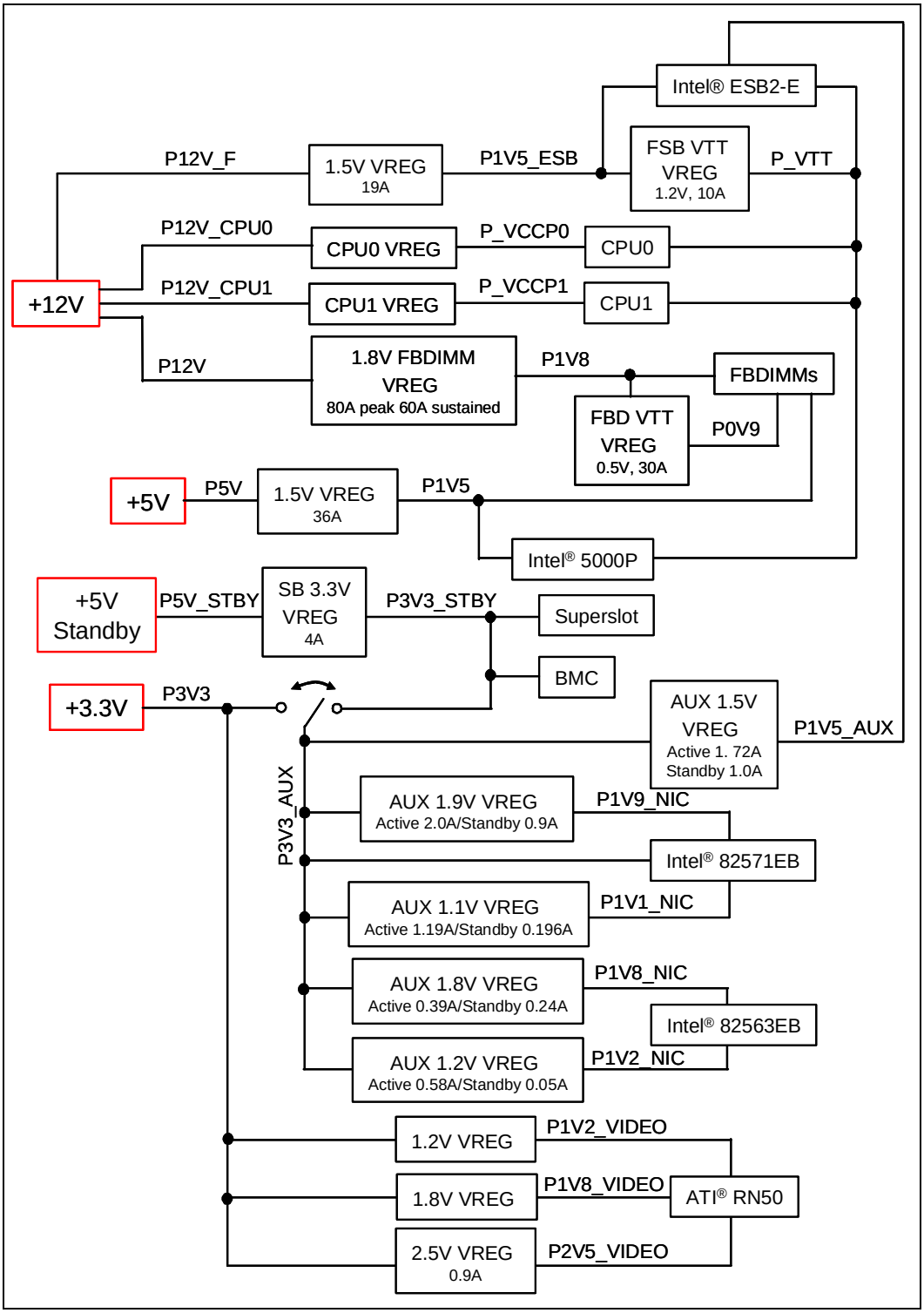
8.2 Intel® Server Board S5000PHB Power Specifications

This section provides power supply design guidelines for a system using the Intel® Server Board S5000PHB. Much of the information is drawn directly from the power supply and power distribution board design specifications for the Intel® Network Server NSW1U or Carrier Grade Server TIGW1U systems. As such, much of this information is also in the Technical Product Specification documents for those products. The information is provided here is for reference only since use of an Intel® Network Server NSW1U or Carrier Grade Server TIGW1U chassis will ensure that all of these specifications, including voltage and current specifications and power supply on/off sequencing characteristics, are met.

8.2.1 Power Distribution

The following diagram shows the power distribution implemented on this server board.

Figure 13. Intel® Server Board S5000PHB Power Distribution Block Diagram



8.2.2 Processor Power Support

The Server Board S5000PHB supports the Thermal Design Point (TDP) guideline for Dual-Core Intel® Xeon® processors 5100 series and Quad-Core Intel® Xeon® processors 5400 series. The Flexible Motherboard (FMB) Guidelines have been followed to help determine the suggested thermal and current design values for anticipating future processor needs.

The *Dual-Core Intel® Xeon® Processor 5100 Series Datasheet* and the *Dual-Core Intel® Xeon® Processor 5400 Series Datasheet* contain detailed information on the TDP guidelines and actual power and thermal specifications for the specific processor models supported by the Server Board S5000PHB.

See the

8.2.3 Output Power / Currents

The following table defines power and current ratings for the 450 W power supplies used in Intel IP Network Server NSW1U and Intel Carrier-Grade Network Server TIG1U systems. The power supply must meet both static and dynamic voltage regulation requirements for the minimum loading conditions.

Table 34. 450 W Load Ratings

Rail	Consumption
3.3V	10.11 W
5V	6.38 W
5V Standby	1.49 W
12V	15.2 W
-12V	119 mW
1.5V (Northbridge)	18.27 W
1.5V	19.8 W
1.8V	38.4 W
0.9V	1.56 W
Vtt	11.41 W
3.3V Standby	1.89 W
3.3V Auxiliary	371 mW
Vccp0	80 W
Vccp1	80 W
1.5V Auxiliary	1.55 W
1.5V (Southbridge)	4.64 W
1.1V	1.52 W
1.8V (LAN)	910 mW
1.2V (LAN)	580 mW
1.9V	390 mW
1.2V (VID)	1.34 W
2.5V (VID)	482 mW
1.8V (VID)	350 mW
Note: Maximum continuous total DC power will not exceed 450 W.	

8.2.4 Turn-On No-Load Operation

At power-on, the system presents a no-load condition to the power supply. In this no-load state the voltage regulation limits for the 3.3 V and 5 V are relaxed to ±10% and the limits for the +12 V rails are relaxed to +10/-8%. When operating loads are applied, the voltages regulate to normal limits.

Table 35. No-Load Operating Range

Voltage Rail	Minimum Continuous	Maximum Continuous	Peak
+3.3V	0 A	7 A	
+5V	0 A	5 A	
+12V1	0 A	5 A	7 A
+12V2	0 A	5 A	7 A
+12V3	0 A	6 A	
+12V4	0 A	5 A	
-12V	0 A	0.5 A	
+5VSB	0.1 A	3.0 A	3.5 A

8.2.5 Grounding

The grounds of the pins of the power supply output connector provide the power return path. The output connector ground pins must be connected to safety ground (power supply enclosure). This grounding should be well designed to ensure passing the maximum allowed Common Mode Noise levels.

The power supply must be provided with a reliable protective earth ground. All secondary circuits must be connected to protective earth ground. Resistance of the ground returns to chassis must not exceed 1.0 mΩ. This path may be used to carry DC current.

8.2.6 Standby Outputs

The 5 VSB output must be present when a power input greater than the power supply turn-on voltage is applied.

8.2.7 Remote Sense

The power supply uses remote sense to regulate out drops in the system for the +3.3 V and +5 V outputs, and the power supply has remote sense returns (ReturnS) to regulate out ground drops for these output voltages. The +12 V, –12 V, and 5 VSB outputs only use remote sense referenced to the ReturnS signal. The remote sense input impedance to the power supply must be greater than 200Ω on 3.3VS and 5VS; this is the value of the resistor connecting the remote sense to the output voltage internal to the power supply. Remote sense must be able to regulate out a minimum of a 200 mV drop on the +3.3 V output. The remote sense return (ReturnS) must be able to regulate out a minimum of a 200 mV drop in the power ground return. The current in any remote sense line is less than 5 mA to prevent voltage sensing errors. The power supply must operate within specification over the full range of voltage drops from the power supply's output connector to the remote sense points.

8.2.8 Voltage Regulation

The power supply output voltages must stay within the following voltage limits when operating at steady state and dynamic loading conditions. These limits include the peak-peak ripple/noise.

Table 36. Voltage Regulation Limits

Output	Tolerance	MIN	NOM	MAX	Units
+3.3 V	±5%	+3.14	+3.30	+3.46	V_{rms}
+5 V	±5%	+4.75	+5.00	+5.25	V_{rms}
+12 V1, +12 V2, +12 V3, +12 V4	±5%	+11.40	+12.00	+12.60	V_{rms}
–12 V	+9/–5%	–10.80	–12.00	–13.20	V_{rms}
+5 VSB	±5%	+4.75	+5.00	+5.25	V_{rms}

8.2.9 Dynamic Loading

The output voltages must remain within limits for the step loading and capacitive loading specified in the table below. The load transient repetition rate must be tested between 50 Hz and 5 kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The Δ step load may occur anywhere within the MIN load to the MAX load conditions.

Table 37. Transient Load Requirements

Output	Δ Step Load Size (See note 2)	Load Slew Rate	Test capacitive Load
+3.3 V	5.0 A	0.25 A/µsec	250 µF
+5 V	6.0 A	0.25 A/µsec	400 µF
+12 V1, +12 V2, +12 V3, +12 V4	28.0 A	0.25 A/µsec	2200 µF [1,2]
+5VSB	0.5 A	0.25 A/µsec	20 µF

Notes:
1. Step loads on each 12V output may happen simultaneously.
2. The +12V should be tested with 2200 µF evenly split between the four +12V rails.

8.2.10 Capacitive Loading

The power supply must be stable and meet all requirements with the following capacitive loading ranges.

Table 38. Capacitive Loading Conditions

Output	MIN	MAX
+3.3 V	250 µF	6,800 µF
+5 V	400 µF	4,700 µF
+12 V1, +12 V2, +12 V3, +12 V4	500 µF each	11,000 µF each
-12 V	1 µF	350 µF
+5 VSB	20 µF	350 µF

8.2.11 Closed-Loop Stability

The power supply must be unconditionally stable under all line/load/transient load conditions including capacitive load ranges. A minimum of 45° phase margin and -10dB gain margin is required. Closed-loop stability must be ensured at the maximum and minimum loads as applicable.

8.2.12 Common Mode Noise

The common mode noise on any output must not exceed 350 mV p-p over the frequency band of 10 Hz to 30 MHz.

The common mode noise measurement is made across a 100Ω resistor between each of the DC outputs, including ground, at the DC power connector and chassis ground (power subsystem enclosure). The test set-up should use an FET probe.

8.2.13 Ripple and Noise

The maximum allowed ripple/noise output of the power supply is defined in the following table. This is measured over a bandwidth of 0 Hz to 20 MHz at the power supply output connectors. A 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor is placed at the point of measurement.

Table 39. Ripple and Noise

+3.3 V	+5 V	+12 V1 / +12 V2 / +12 V3 / +12 V4	-12 V	+5 VSB
50 mV p-p	50 mV p-p	120 mV p-p	120 mV p-p	50 mV p-p

8.2.14 Soft Starting

The power supply must contain a control circuit which provides a monotonic soft start for its outputs without overstress of the AC line or any power supply components at any specified AC line or load conditions. There is no requirement for rise time on the 5 V standby, but the turn on/off must be monotonic.

8.2.15 Timing Requirements

The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 5 to 70 ms, except for 5VSB, which is allowed to rise within 1.0 to 25 ms. All outputs must rise monotonically. Each output voltage must reach regulation within 50 ms (T_{vout_on}) of all other voltages during turn on of the power supply. Each output voltage must fall out of regulation within 400 ms (T_{vout_off}) of all other voltages during turn off. The following diagrams show the timing requirements for the power supply being turned on and off via the AC input with PSON held low, and the PSON signal with the AC input applied.

Table 40. Output Voltage Timing

Item	Description	MIN	MAX	Units
T_{vout_rise}	Output voltage rise time from each main output.	5.0 *	70 *	ms
T_{vout_on}	All main outputs must be within regulation of each other within this time.		50	ms
T_{vout_off}	All main outputs must leave regulation within this time.		400	ms
Note: * The 5VSB output voltage rise time shall be from 1.0 ms to 25.0 ms				

Figure 14. Output Voltage Timing

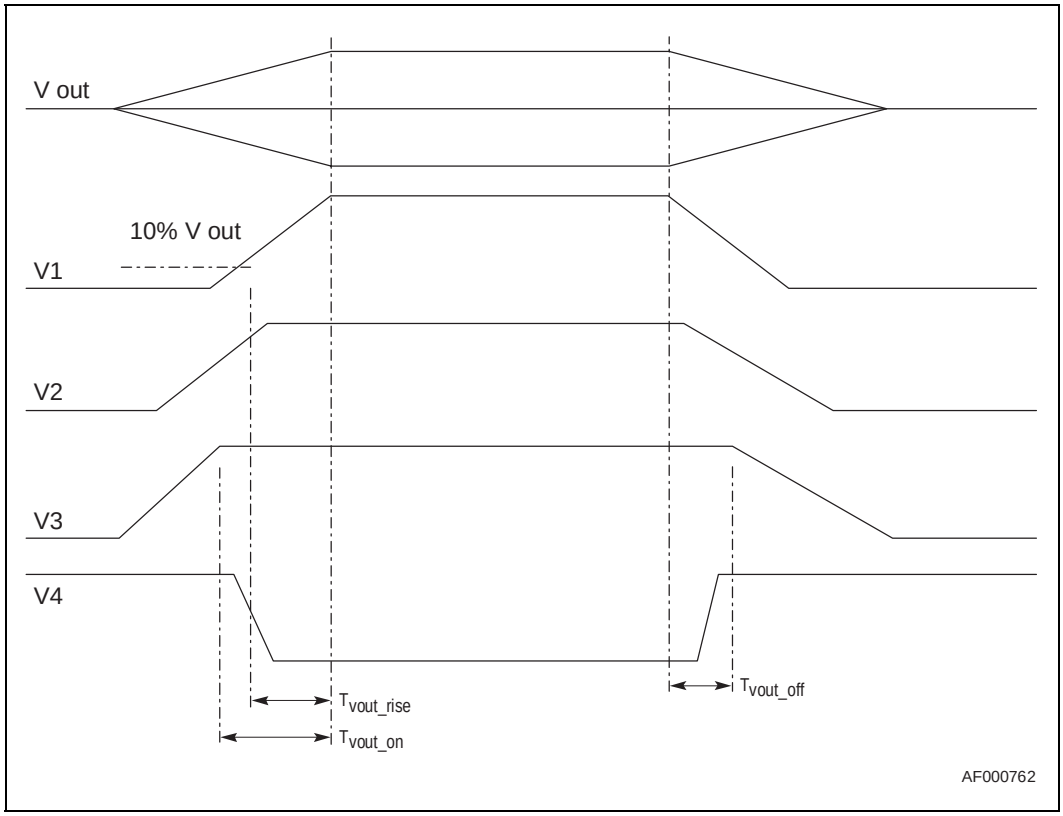
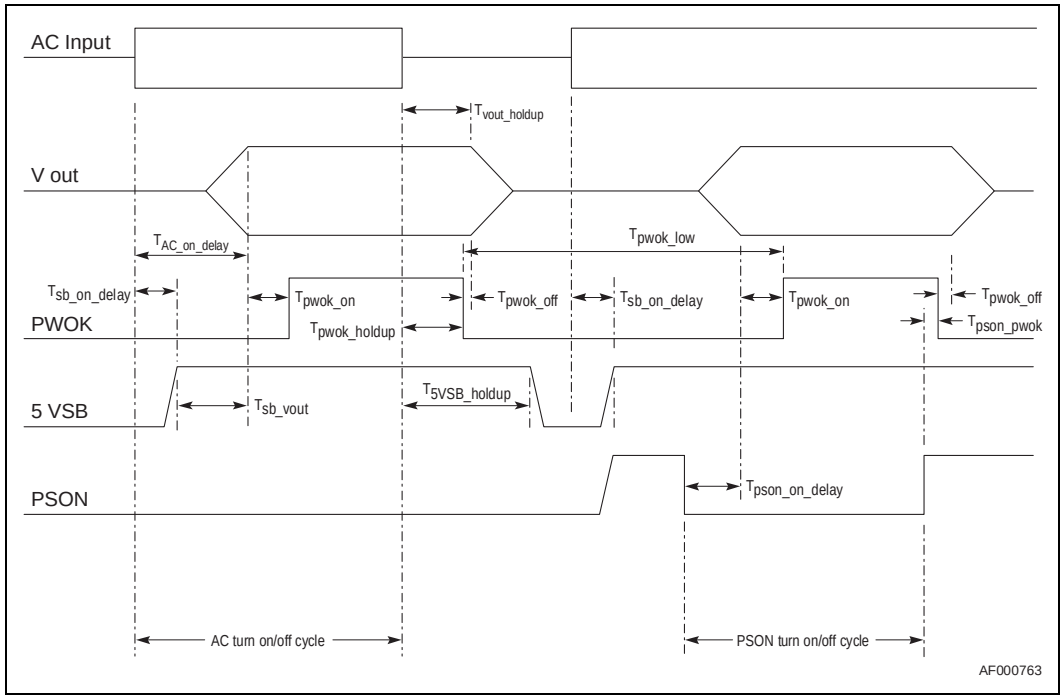


Table 41. Turn On/Off Timing

Item	Description	MIN	MAX	UNITS
$T_{sb\_on\_delay}$	Delay from AC being applied to 5VSB being within regulation.		1500	ms
$T_{ac\_on\_delay}$	Delay from AC being applied to all output voltages being within regulation.		2500	ms
T_{vout_holdup}	Time all output voltages stay within regulation after loss of AC. Measured at 60% of maximum load.	21		ms
T_{pwok_holdup}	Delay from loss of AC to de-assertion of PWOK. Measured at 60% of maximum load.	20		ms
$T_{pson\_on\_delay}$	Delay from PSON# active to output voltages within regulation limits.	5	400	ms
T_{pson_pwok}	Delay from PSON# adjective to PWOK being de-asserted.		50	ms
T_{pwok_on}	Delay from output voltages within regulation limits to PWOK asserted at turn on.	100	500	ms
T_{pwok_off}	Delay from PWOK de-asserted to output voltages (3.3V, 5V, 12V, -12V) dropping out of regulation limits.	1		ms
T_{pwok_low}	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal.	100		ms
T_{sb_vout}	Delay from 5VSB being in regulation to O/As being in regulation at AC turn on.	50	1000	ms
T_{5VSB_holdup}	Time the 5VSB output voltage stays within regulation after loss of AC.	70		ms

Figure 15. Turn On/Off Timing (Power Supply Signals)



8.2.16 Residual Voltage Immunity in Standby Mode

The power supply must be immune to any residual voltage placed on its outputs (typically a leakage voltage through the system from standby output) up to 500 mV. There must be no additional heat generated, nor stress of any internal components with this voltage applied to any individual output, and all outputs simultaneously. It also should not trip the power supply protection circuits during turn on.

Residual voltage at the power supply outputs for a no-load condition must not exceed 100 mV when AC voltage is applied and the PSON# signal is de-asserted.

9 Regulatory and Certification Information

WARNING

To ensure regulatory compliance, you must adhere to the assembly instructions in this guide to ensure and maintain compliance with existing product certifications and approvals. Use only the described, regulated components specified in this guide. Use of other products/components will void the UL listing and other regulatory approvals of the product and will most likely result in noncompliance with product regulations in the region(s) in which the product is sold.

To help ensure EMC compliance with your local regional rules and regulations, before computer integration, make sure that the chassis, power supply, and other modules have passed EMC testing using a server board with a microprocessor from the same family (or higher) and operating at the same (or higher) speed as the microprocessor used on this server board. The final configuration of your end system product may require additional EMC compliance testing. For more information please contact your local Intel Representative.

This is an FCC Class A device. Integration of it into a Class B chassis does not result in a Class B device.

9.1 Product Regulatory Compliance

Intended Application – This product was evaluated as Information Technology Equipment (ITE), which may be installed in offices, schools, computer rooms, and similar commercial type locations. The suitability of this product for other product categories and environments (such as: medical, industrial, residential, alarm systems, test equipment, etc.), other than an ITE application, may require further evaluation. This is an FCC Class A device. Integration of it into a Class B chassis does not result in a Class B device.

9.1.1 Product Safety Compliance

- UL60950 – CSA 60950(USA / Canada)
- EN60950 (Europe)
- IEC60950 (International)
- CB Certificate and Report, IEC60950 (report to include all country national deviations)
- CE - Low Voltage Directive 73/23/EEE (Europe)

9.1.2 Product EMC Compliance – Class A Compliance

Note: Compliance to the following Class A EMC requirements has been verified when installed in the Intel® IP Network Server NSW1U chassis.

- FCC /ICES-003 - Emissions (USA/Canada) Verification
- CISPR 22 – Emissions (International)

- EN55022 - Emissions (Europe)
- EN55024 - Immunity (Europe)
- CE – EMC Directive 89/336/EEC (Europe)
- VCCI Emissions (Japan)
- BSMI CNS13438 Emissions (Taiwan)
- GOST R 29216-91 Emissions - Listed on one System License (Russia)
- GOST R 50628-95 Immunity – Listed on one System License (Russia)
- RRL MIC Notice No. 1997-41 (EMC) and 1997-42 (EMI) (Korea)

9.1.3 Certifications / Registrations / Declarations

- UL Certification or NRTL (US/Canada)
- CE Declaration of Conformity (CENELEC Europe)

9.2 Product Regulatory Compliance Markings

The Intel Server Baseboard bears the following regulatory marks.

Regulatory Compliance	Country	Marking
UL Mark	USA/Canada	
CE Mark	Europe	

Appendix A: Integration and Usage Tips

- When adding or removing components or peripherals from the Intel® Server Board S5000PHB, input power must be removed from the server. With input power connected to the server, 5 V standby is still present on the server board even though the server is powered off.
- Processors must be installed in order. CPU 1, which is located near the center of the front edge of the server board, must be populated to operate the system.
- On the back edge of the server board are four diagnostic LEDs which display a sequence of red, green, or amber POST codes during the boot process. If the server board hangs during POST, the LEDs will display the last POST event run before the hang.
- Only fully-buffered DIMMs (FBDIMMs) are supported on this server board. For a list of supported memory for this server board, see the *Intel® Server Board S5000PHB Tested Memory List*.
- For a list of Intel-supported operating systems, add-in cards, and peripherals for this server board, see the *Intel® Server Board S5000PHB Tested Hardware and OS List.*
- Only Dual-Core Intel® Xeon® processors 5100 series or Quad-Core Intel® Xeon® processors 5400 series with system bus speeds of 1066 MHz and 1333 MHz are supported on this server board. Previous generation Intel Xeon processors are not supported.
- For the tested memory list, see http://www.intel.com/support/telecom/computeboards/nsw1u/sb/CS-024511.htm
- For the tested hardware and operating system list, see http://www.intel.com/support/telecom/computeboards/nsw1u/sb/CS-023702.htm

Appendix B: Sensor Tables

This appendix lists the sensor identification numbers and information regarding the sensor type, name, supported thresholds, assertion and de-assertion events, and a brief description of the sensor purpose. See the *Intelligent Platform Management Interface Specification, Version 1.5*, for sensor and event/reading-type table information.

- **Sensor Type**
  Sensor Type references the values enumerated in the *Sensor Type Codes* table in the IPMI specification. It provides the context in which to interpret the sensor, such as the physical entity or characteristic that is represented by this sensor.
- **Event / Reading Type**
  Event/Reading Type references values from the *Event/Reading Type Code Ranges* and *Generic Event/Reading Type Codes* tables in the *IPMI specification*. Note that digital sensors are a specific type of discrete sensor that have only two states.
- **Event Offset / Triggers**
  Event Thresholds are “supported event generating thresholds” for threshold types of sensors:
  - **[u,l][nr,c,nc]**: upper nonrecoverable, upper critical, upper noncritical, lower nonrecoverable, lower critical, lower noncritical
  - **uc, lc**: upper critical, lower critical

  Event Triggers are “supported event generating offsets” for discrete type sensors. The offsets can be found in the “Generic Event/Reading Type Codes” or “Sensor Type Codes” tables in the IPMI specification, depending on whether the sensor event/reading type is generic or a sensor specific response.
- **Criticality / System Status**
  Classifies the severity and nature of the condition associated with the sensor. Also indicates the contribution the sensor makes to the system status LED indication.
- **Assertion / De-assertion Enables**
  Assertion and de-assertion indicators reveal the type of events the sensor can generate:
  - As: Assertions
  - De: De-assertion
- **Readable Value / Offsets**
  - Readable Value indicates the type of value returned for threshold and other non-discrete type sensors.
  - Readable Offsets indicate the offsets for discrete sensors that are readable via the Get Sensor Reading command. Unless otherwise indicated, all event triggers are readable; i.e., Readable Offsets consists of the reading type offsets that do not generate events.

- **Event Data**
  This is the data that is included in an event message generated by the associated sensor. For threshold-based sensors, the following abbreviations are used:
  - R: Reading value
  - T: Threshold value
- **Sensor Rearm**
  Indicates the type of rearm supported by the sensor. (Rearm is a request for the event status of a sensor to be rechecked and updated upon a transition between good and bad states. The following abbreviations are used:
  - A: Automatic sensor rearm
  - M: Manual sensor rearm
  - I: Sensor rearm by init agent
- **Standby Operation**
  Indicates sensors that operate on standby power. These sensors may be accessed or will generate events when the main (system) power is turned off, but the server power is still connected to the power source so that +5V standby power is present.

Table 42. BMC Sensors and Events (Sheet 1 of 7)

Sensor No.	Sensor Name[3]	Sensor Type	Event/ Reading Type	Event Offset Triggers	Criticality/ System Status	Assert/ Deassert	Readable Value/ Offset	Event Data	Rearm	Stand-by
01h	Power Unit Status	Power Unit 09h	Sensor Specific 6Fh	Power down Power cycle A/C lost	OK	As & De	–	Trig Offset	A,I	X
				Soft power control failure Power unit failure	Fatal					
02h	Power Unit Redundancy[4]	Power Unit 09h	Generic 0Bh	Fully Redundant	OK	As & De	–	Trig Offset	A	X
				Redundancy Lost	Degraded					
				Redundancy degraded	Degraded					
				Non-red: suff res from redund	Degraded					
				Non-red: suff from insuff	Degraded					
				Non-red: insufficient	Fatal					
				Redun degrade from fully redun	Degraded					
				Redun degrade from non-redundant	Degraded					
03h	Watchdog	Watchdog 2 23h	Sensor Specific 6Fh	Timer expired, status only Hard reset Power down Power cycle Timer interrupt	OK	As	–	Trig Offset	A,I	X
04h	Platform Security Violation	Platform Security Violation Attempt 06h	Sensor Specific 6Fh	Secure mode violation attempt Out-of-band access password violation	OK	As & De	–	Trig Offset	A,I	X

Notes:

1. Not supported except for ESB2 embedded NICs
2. For system with redundant cooling capability, the contribution to system status is determined by the Fan Redundancy sensor.
3. Actual sensor name strings in SDR may vary from the names in this table, according to platform-specific usage.
4. Sensor only present on systems that have applicable redundancy (for instance, fan or power supply).
5. The BMC does not provide a direct contribution to overall system status due to the DIMM sensors. BIOS determines contribution depending on failure scenario and uses the Set Fault Indication command to provide this information to the BMC.
6. Error logging for this sensor is due to port-mortem memory error scan after an SMI Timeout has occurred. Contribution to system status is determined by the SMI Timeout sensor.

Table 42. BMC Sensors and Events (Sheet 2 of 7)

Sensor No.	Sensor Name[3]	Sensor Type	Event/ Reading Type	Event Offset Triggers	Criticality/ System Status	Assert/ Deassert	Readable Value/ Offset	Event Data	Rearm	Stand-by
07h	FP Diag Interrupt (NMI)	Critical Interrupt 13h	Sensor Specific 6Fh	Front panel NMI / diagnostic interrupt Bus uncorrectable error	OK	As	–	Trig Offset	A,I	–
09h	System Event Log	Event Logging Disabled 10h	Sensor Specific 6Fh	Log area reset / cleared	OK	As	–	Trig Offset	A,I	X
0Ah	Session Audit	Session Audit 2Ah	Sensor Specific 6Fh	00h – Session activation 01h – Session deactivation	OK		–	As defined by IPMI	A,I	X
0Bh	System Event ('System Event')	System Event 12h	Sensor Specific 6Fh	00 – System reconfigured 04 – PEF action	OK	As	–	Trig Offset	A,I	X
10h	BB +1.2V Vtt	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-Fatal	As & De	Analog	R, T	A,I	–
11h	BB+1.8V NIC Core	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-Fatal	As & De	Analog	R, T	A,I	X
12h	BB +1.5V AUX	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-Fatal	As & De	Analog	R, T	A,I	–
13h	BB +1.5V	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-Fatal	As & De	Analog	R, T	A,I	–
14h	BB +1.8V	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-Fatal	As & De	Analog	R, T	A,I	–
15h	BB +3.3V	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-Fatal	As & De	Analog	R, T	A,I	–
16h	BB +3.3V STB	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-Fatal	As & De	Analog	R, T	A,I	X
17h	BB +1.5V ESB	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-Fatal	As & De	Analog	R, T	A,I	X
18h	BB +5V	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-Fatal	As & De	Analog	R, T	A,I	–

Notes:

1. Not supported except for ESB2 embedded NICs
2. For system with redundant cooling capability, the contribution to system status is determined by the Fan Redundancy sensor.
3. Actual sensor name strings in SDR may vary from the names in this table, according to platform-specific usage.
4. Sensor only present on systems that have applicable redundancy (for instance, fan or power supply).
5. The BMC does not provide a direct contribution to overall system status due to the DIMM sensors. BIOS determines contribution depending on failure scenario and uses the Set Fault Indication command to provide this information to the BMC.
6. Error logging for this sensor is due to port-mortem memory error scan after an SMI Timeout has occurred. Contribution to system status is determined by the SMI Timeout sensor.

Table 42. BMC Sensors and Events (Sheet 3 of 7)

Sensor No.	Sensor Name[3]	Sensor Type	Event/ Reading Type	Event Offset Triggers	Criticality/ System Status	Assert/ Deassert	Readable Value/ Offset	Event Data	Rearm	Stand-by
19h	BB +1.2V NIC	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-Fatal	As & De	Analog	R, T	A,I	–
1Ah	BB +12V AUX	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-Fatal	As & De	Analog	R, T	A,I	–
1Bh	BB 0.9V	Voltage 02h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-Fatal	As & De	Analog	R, T	A,I	–
1Eh	BB Vbat	Battery 29h	Sensor Specific 6Fh	01h Battery failed	Degraded	As & De	–	R, T	A,I	X
30h	BB Temp	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-Fatal	As & De	Analog	R, T	A,I	X
31h	Reserved for OEM use	-	-	-	-	-	-	-	-	-
32h	Front Panel Temp	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-Fatal	As & De	Analog	R, T	A,I	X
50h – 58h	Tach Fan Sensors	Fan 04h	Threshold 01h	[l] [c,nc]	nc = Degraded c = Non-fatal[2]	As & De	Analog	R, T	M,I	–
70h	Power Supply Status[4] 1	Power Supply 08h	Sensor Specific 6Fh	Presence	OK	As & De	–	Trig Offset	A	X
				Failure	Degraded					
				Predictive fail	Degraded					
				A/C lost	Degraded					
				Configuration error	OK					
71h	Power Supply Status[4] 2	Power Supply 08h	Sensor Specific 6Fh	Presence	OK	As & De	–	Trig Offset	A	X
				Failure	Degraded					
				Predictive fail	Degraded					
				A/C lost	Degraded					
				Configuration error	OK					

Notes:

1. Not supported except for ESB2 embedded NICs
2. For system with redundant cooling capability, the contribution to system status is determined by the Fan Redundancy sensor.
3. Actual sensor name strings in SDR may vary from the names in this table, according to platform-specific usage.
4. Sensor only present on systems that have applicable redundancy (for instance, fan or power supply).
5. The BMC does not provide a direct contribution to overall system status due to the DIMM sensors. BIOS determines contribution depending on failure scenario and uses the Set Fault Indication command to provide this information to the BMC.
6. Error logging for this sensor is due to port-mortem memory error scan after an SMI Timeout has occurred. Contribution to system status is determined by the SMI Timeout sensor.

Table 42. BMC Sensors and Events (Sheet 4 of 7)

Sensor No.	Sensor Name[3]	Sensor Type	Event / Reading Type	Event Offset Triggers	Criticality / System Status	Assert / Deassert	Readable Value / Offset	Event Data	Rearm	Stand-by
78h	Power Nozzle Power Supply 1	Current 03h	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-Fatal	As & De	Analog	R, T	A,I	–
79h	Power Nozzle Power Supply 2	Current 03h	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-Fatal	As & De	Analog	R, T	A,I	–
7Ah	Power Gauge V1 rail (+12v) Power Supply 1	Current 03h	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-Fatal	As & De	Analog	R, T	A,I	–
7Bh	Power Gauge V1 rail (+12v) Power Supply 2	Current 03h	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-Fatal	As & De	Analog	R, T	A,I	–
7Ch	Power Gauge (aggregate power) Power Supply 1	Other Units 0Bh	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-Fatal	As & De	Analog	R, T	A,I	–
7Dh	Power Gauge (aggregate power) Power Supply 2	Other Units 0Bh	Threshold 01h	[u] [c,nc]	nc = Degraded c = Non-Fatal	As & De	Analog	R, T	A,I	–
82h	System ACPI Power State	System ACPI Power State 22h	Sensor Specific 6Fh	S0 / G0 S1 S3 S4 S5 / G2 G3 mechanical off	OK	As	–	Trig Offset	A,I	X
84h	Button	Button 14h	Sensor Specific 6Fh	Power button Reset button	OK	As	–	Trig Offset	A,I	X
85h	SMI Timeout	SMI Timeout F3h	Digital Discrete 03h	01h – State asserted	Fatal	As & De	–	Trig Offset	A,I	–
87h	NMI Signal State	OEM C0h	Digital Discrete 03h	01h – State asserted	OK	–	01h	–	A,I	–
88h	SMI Signal State	OEM C0h	Digital Discrete 03h	01h – State asserted	OK	–	01h	–	A,I	–

Notes:

1. Not supported except for ESB2 embedded NICs
2. For system with redundant cooling capability, the contribution to system status is determined by the Fan Redundancy sensor.
3. Actual sensor name strings in SDR may vary from the names in this table, according to platform-specific usage.
4. Sensor only present on systems that have applicable redundancy (for instance, fan or power supply).
5. The BMC does not provide a direct contribution to overall system status due to the DIMM sensors. BIOS determines contribution depending on failure scenario and uses the Set Fault Indication command to provide this information to the BMC.
6. Error logging for this sensor is due to port-mortem memory error scan after an SMI Timeout has occurred. Contribution to system status is determined by the SMI Timeout sensor.

Table 42. BMC Sensors and Events (Sheet 5 of 7)

Sensor No.	Sensor Name[3]	Sensor Type	Event/ Reading Type	Event Offset Triggers	Criticality/ System Status	Assert/ Deassert	Readable Value/ Offset	Event Data	Rearm	Stand-by
90h	Proc 1 Status	Processor 07h	Sensor Specific 6Fh	IERR	Fatal	As & De	–	Trig Offset	M	X
				Thermal trip	Fatal					
				Config error	Fatal					
				Presence	OK					
				Disabled	Degraded					
91h	Proc 2 Status	Processor 07h	Sensor Specific 6Fh	IERR	Fatal	As & De	–	Trig Offset	M	X
				Thermal trip	Fatal					
				Config error	Fatal					
				Presence	OK					
				Disabled	Degraded					
98h	Proc 1 Temp	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-Fatal	As & De	Analog	R, T	A,I	–
99h	P1 Therm Margin	Temperature 01h	Threshold 01h	-	-	-	-	-	A,I	–
9Ah	Proc 2 Temp	Temperature 01h	Threshold 01h	[u,l] [c,nc]	nc = Degraded c = Non-Fatal	As & De	Analog	R, T	A,I	–
9Bh	P2 Therm Margin	Temperature 01h	Threshold 01h	-	-	-	-	-	A,I	–
A0h - ADh	PCIe Link Sensors	Critical Interrupt 13F	Sensor Specific 6Fh	Bus correctable error	Degraded	As	–	See the BIOS EPS	A,I	–
				Bus uncorrectable error	Non-Fatal					
C0h	P1 Therm Ctrl %	Temperature 01h	Threshold 01h	[u] [c]	Non-Fatal	As & De	Analog	Trig Offset	A,I	–
C1h	P2 Therm Ctrl %	Temperature 01h	Threshold 01h	[u] [c]	Non-Fatal	As & De	Analog	Trig Offset	A,I	–

Notes:

1. Not supported except for ESB2 embedded NICs
2. For system with redundant cooling capability, the contribution to system status is determined by the Fan Redundancy sensor.
3. Actual sensor name strings in SDR may vary from the names in this table, according to platform-specific usage.
4. Sensor only present on systems that have applicable redundancy (for instance, fan or power supply).
5. The BMC does not provide a direct contribution to overall system status due to the DIMM sensors. BIOS determines contribution depending on failure scenario and uses the Set Fault Indication command to provide this information to the BMC.
6. Error logging for this sensor is due to port-mortem memory error scan after an SMI Timeout has occurred. Contribution to system status is determined by the SMI Timeout sensor.

Table 42. BMC Sensors and Events (Sheet 6 of 7)

Sensor No.	Sensor Name[3]	Sensor Type	Event / Reading Type	Event Offset Triggers	Criticality / System Status	Assert / Deassert	Readable Value / Offset	Event Data	Rearm	Stand-by
C8h	Proc 1 VRD Hot	Temperature 01h	Digital Discrete 05h	01h – Limit exceeded	Non-Fatal	As & De	–	Trig Offset	A,I	–
C9h	Proc 2 VRD Hot	Temperature 01h	Digital Discrete 05h	01h – Limit exceeded	Non-Fatal	As & De	–	Trig Offset	A,I	–
D0h	Proc 1 Vcc	Voltage 02h	Threshold 01h	-	-	-	-	-	-	–
D1h	Proc 2 Vcc	Voltage 02h	Threshold 01h	-	-	-	-	-	-	–
D2h	Proc 1 Vcc Out-of-Range	Voltage 02h	Digital Discrete 05h	01h – Limit exceeded	Non-Fatal	As & De	Discrete	R, T	A,I	–
D3h	Proc 2 Vcc Out-of-Range	Voltage 02h	Digital Discrete 05h	01h – Limit exceeded	Non-Fatal	As & De	Discrete	R, T	A,I	–
D8h	CPU Population Error	Processor 07h	Generic 03h	01h –- State asserted	Fatal	As & De	–	R, T	A	–
E0h – E5h	DIMM 1- 8	Slot Connector 21h	Sensor Specific 6Fh	Fault status asserted	Situation dependent[5]	As & De	–	Trig Offset	A	–
				Device installed	OK					
				Disabled	Situation dependent[5]					
				Sparing	OK					
ECh - EDh	Memory Error A - B	Memory 0Ch	Sensor Specific 6Fh	Uncorrectable ECC	OK[6]	As & De	–	Trig Offset	A	–
F0h	B0 DIMM Sparing Enabled	Entity Presence 25h	Sensor Specific 6Fh	Entity present	OK	As	–	Trig Offset	A	–

Notes:

1. Not supported except for ESB2 embedded NICs
2. For system with redundant cooling capability, the contribution to system status is determined by the Fan Redundancy sensor.
3. Actual sensor name strings in SDR may vary from the names in this table, according to platform-specific usage.
4. Sensor only present on systems that have applicable redundancy (for instance, fan or power supply).
5. The BMC does not provide a direct contribution to overall system status due to the DIMM sensors. BIOS determines contribution depending on failure scenario and uses the Set Fault Indication command to provide this information to the BMC.
6. Error logging for this sensor is due to port-mortem memory error scan after an SMI Timeout has occurred. Contribution to system status is determined by the SMI Timeout sensor.

Table 42. BMC Sensors and Events (Sheet 7 of 7)

Sensor No.	Sensor Name[3]	Sensor Type	Event/ Reading Type	Event Offset Triggers	Criticality/ System Status	Assert/ Deassert	Readable Value/ Offset	Event Data	Rearm	Stand-by
F1h	B0 DIMM Sparing Redundancy	Memory 0Ch	Discrete 0Bh	Fully redundant	OK	As	–	Trig Offset	A	–
				Non-red: suff res from redund	Degraded					
				Non-red: suff res from insuff res	Degraded					
				Non-red: Insuff res	Fatal					

Notes:
1. Not supported except for ESB2 embedded NICs
2. For system with redundant cooling capability, the contribution to system status is determined by the Fan Redundancy sensor.
3. Actual sensor name strings in SDR may vary from the names in this table, according to platform-specific usage.
4. Sensor only present on systems that have applicable redundancy (for instance, fan or power supply).
5. The BMC does not provide a direct contribution to overall system status due to the DIMM sensors. BIOS determines contribution depending on failure scenario and uses the Set Fault Indication command to provide this information to the BMC.
6. Error logging for this sensor is due to port-mortem memory error scan after an SMI Timeout has occurred. Contribution to system status is determined by the SMI Timeout sensor.

Appendix C: POST Codes

C.1 Diagnostic LED POST Code Decoder

During the system boot process, the BIOS executes platform configuration processes, each of which is assigned a specific hexadecimal POST code number. As each configuration routine is started, the BIOS displays the POST code to the POST Code Diagnostic LEDs on the back edge of the server board. To assist in troubleshooting a system hang during the POST process, the Diagnostic LEDs can be used to identify the last attempted POST process.

Each POST code is represented by the combination of colors displayed by four LED devices. Each device can display three colors: green, red, and amber (which results from the red and green LEDs being illuminated simultaneously). The POST codes are divided into an upper nibble and a lower nibble. Each bit set in the upper nibble is represented by a red LED and each bit set in the lower nibble is represented by a green LED. If a given bit is set in both the upper and lower nibbles, then both red and green LEDs are lit, resulting in amber. If a bit is clear in both nibbles, the LED is off.

In the below example, the BIOS sends a value of ACh to the diagnostic LED decoder. The LEDs are decoded as follows:

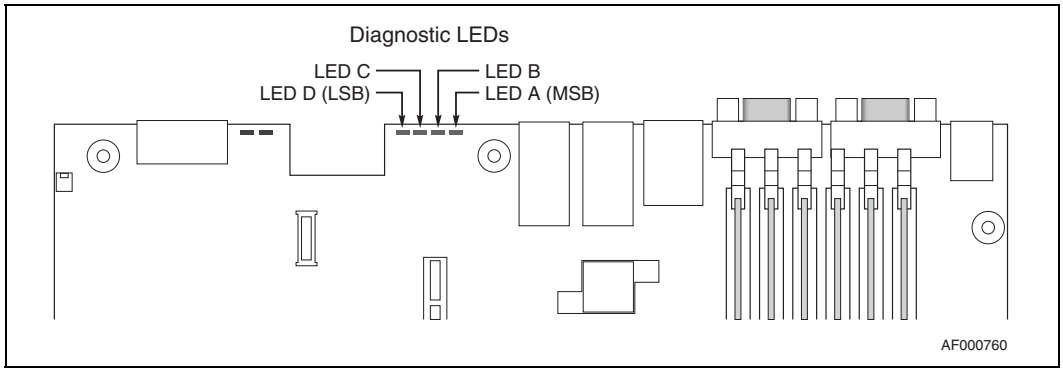
- Red bits = 1010b = Ah
- Green bits = 1100b = Ch

Since the red bits correspond to the upper nibble and the green bits correspond to the lower nibble, the two are superimposed to yield ACh.

Table 43. POST Progress Code LED Example

Hex Value	LEDs							
	MSB (8h)		(4h)		(2h)		LSB (1h)	
	Red	Green	Red	Green	Red	Green	Red	Green
A0h	On (1)		Off (0)		On (1)		Off (0)	
0Ch		On (1)		On (1)		Off (0)		Off (0)
ACh (result)	Amber		Green		Red		Off	

Figure 16. Diagnostic LED Placement Diagram



C.2 Codes Used in Early POST

When the server is powered up, the BIOS performs memory tests before proceeding to the main POST routine. If errors are encountered during this early POST phase, the BIOS displays POST codes in the range from E0h to EFh, which are used for reporting other system errors during the later POST.

Error conditions that may occur during the early POST phase and the corresponding BIOS behavior include the following:

- If no memory is available, the BIOS displays POST code E1h (LED display Red, Red, Red, Green) and halts the system.
- If the BIOS cannot electrically identify – and thus communicate with – the AMB on an installed FBDIMM, the BIOS eventually times out and reports POST code E4h (LED display Red, Amber, Red, Off). This condition is usually indicative of hardware failure in the serial channel on which the AMBs sit.
- If an FBDIMM or a set of FBDIMMs on the same FBD memory channel (row) fails Memory IBIST, or Memory Link Training, the BIOS displays POST code E6h (LED display Red, Amber, Amber, Off). If all of the memory fails IBIST, the system acts as if no memory is available and displays E1h.
- If the BIOS detects an FBDIMM with bad or corrupted SPD data, it displays POST code EBh (LED display Amber, Red, Amber, Green) and halts the system.
- If an FBDIMM has no SPD information at all, the BIOS treats that FBDIMM slot as if no FBDIMM is present on it. If this is the only FBDIMM installed in the system, the BIOS halts the system with POST code E1h (no memory detected) displayed.

C.3 Standard POST Codes

Table 44 lists the hex codes, LED displays, and descriptions of the codes that are sequentially displayed by the BIOS during POST. If the POST fails to complete, the displayed code indicates the specific test that was executing when the failure occurred.

Table 44. Diagnostic LED POST Code Decoder (Sheet 1 of 3)

Checkpoint	G=Green, R=Red, A=Amber				Description
	MSB			LSB	
Host Processor					
10h	Off	Off	Off	R	Power-on initialization of the host processor (bootstrap processor)
11h	Off	Off	Off	A	Host processor cache initialization (including AP)
12h	Off	Off	G	R	Starting application processor initialization
13h	Off	Off	G	A	SMM initialization
Chipset					
21h	Off	Off	R	G	Initializing a chipset component
Memory					
22h	Off	Off	A	Off	Reading configuration data from memory (SPD on DIMM)
23h	Off	Off	A	G	Detecting presence of memory
24h	Off	G	R	Off	Programming timing parameters in the memory controller
25h	Off	G	R	G	Configuring memory parameters in the memory controller
26h	Off	G	A	Off	Optimizing memory controller settings
27h	Off	G	A	G	Initializing memory, such as ECC init
28h	G	Off	R	Off	Testing memory
PCI Bus					
50h	Off	R	Off	R	Enumerating PCI busses
51h	Off	R	Off	A	Allocating resources to PCI busses
52h	Off	R	G	R	Hot Plug PCI controller initialization
53h	Off	R	G	A	Reserved for PCI bus
54h	Off	A	Off	R	Reserved for PCI bus
55h	Off	A	Off	A	Reserved for PCI bus
56h	Off	A	G	R	Reserved for PCI bus
57h	Off	A	G	A	Reserved for PCI bus
USB					
58h	G	R	Off	R	Resetting USB bus
59h	G	R	Off	A	Reserved for USB devices
ATA / ATAPI / SATA					
5Ah	G	R	G	R	Resetting PATA / SATA bus and all devices
5Bh	G	R	G	A	Reserved for ATA
SMBUS					
5Ch	G	A	Off	R	Resetting SMBUS
5Dh	G	A	Off	A	Reserved for SMBUS
Local Console					
70h	Off	R	R	R	Resetting the video controller (VGA)
71h	Off	R	R	A	Disabling the video controller (VGA)

Table 44. Diagnostic LED POST Code Decoder (Sheet 2 of 3)

Checkpoint	G=Green, R=Red, A=Amber				Description
	MSB			LSB	
72h	Off	R	A	R	Enabling the video controller (VGA)
Remote Console					
78h	G	R	R	R	Resetting the console controller
79h	G	R	R	A	Disabling the console controller
7Ah	G	R	A	R	Enabling the console controller
Keyboard (PS2 or USB)					
90h	R	Off	Off	R	Resetting the keyboard
91h	R	Off	Off	A	Disabling the keyboard
92h	R	Off	G	R	Detecting the presence of the keyboard
93h	R	Off	G	A	Enabling the keyboard
94h	R	G	Off	R	Clearing keyboard input buffer
95h	R	G	Off	A	Instructing keyboard controller to run Self Test (PS/2 only)
Mouse (PS2 or USB)					
98h	A	Off	Off	R	Resetting the mouse
99h	A	Off	Off	A	Detecting the mouse
9Ah	A	Off	G	R	Detecting the presence of mouse
9Bh	A	Off	G	A	Enabling the mouse
Fixed Media					
B0h	R	Off	R	R	Resetting fixed media device
B1h	R	Off	R	A	Disabling fixed media device
B2h	R	Off	A	R	Detecting presence of a fixed media device (IDE hard drive detection, etc.)
B3h	R	Off	A	A	Enabling / configuring a fixed media device
Removable Media					
B8h	A	Off	R	R	Resetting removable media device
B9h	A	Off	R	A	Disabling removable media device
BAh	A	Off	A	R	Detecting presence of a removable media device (IDE CD-ROM detection, etc.)
BCh	A	G	R	R	Enabling / configuring a removable media device
Boot Device Selection					
D0h	R	R	Off	R	Trying boot device selection
D1h	R	R	Off	A	Trying boot device selection
D2h	R	R	G	R	Trying boot device selection
D3h	R	R	G	A	Trying boot device selection
D4h	R	A	Off	R	Trying boot device selection
D5h	R	A	Off	A	Trying boot device selection
D6h	R	A	G	R	Trying boot device selection
D7h	R	A	G	A	Trying boot device selection
D8h	A	R	Off	R	Trying boot device selection

Table 44. Diagnostic LED POST Code Decoder (Sheet 3 of 3)

Checkpoint	G=Green, R=Red, A=Amber				Description
	MSB			LSB	
D9h	A	R	Off	A	Trying boot device selection
DAh	A	R	G	R	Trying boot device selection
DBh	A	R	G	A	Trying boot device selection
DCh	A	A	Off	R	Trying boot device selection
DEh	A	A	G	R	Trying boot device selection
DFh	A	A	G	A	Trying boot device selection
Pre-EFI Initialization (PEI) Core					
E0h	R	R	R	Off	Started dispatching early initialization modules (PEIM)
E2h	R	R	A	Off	Initial memory found, configured, and installed correctly
E1h	R	R	R	G	Reserved for initialization module use (PEIM)
E3h	R	R	A	G	Reserved for initialization module use (PEIM)
Driver Execution Environment (DXE) Core					
E4h	R	A	R	Off	Entered EFI driver execution phase (DXE)
E5h	R	A	R	G	Started dispatching drivers
E6h	R	A	A	Off	Started connecting drivers
DXE Drivers					
E7h	R	A	A	G	Waiting for user input
E8h	A	R	R	Off	Checking password
E9h	A	R	R	G	Entering BIOS setup
EAh	A	R	A	Off	Flash Update
EEh	A	A	A	Off	Calling Int 19. One beep unless silent boot is enabled
EFh	A	A	A	G	Unrecoverable boot failure / S3 resume failure
Runtime Phase / EFI Operating System Boot					
F4h	R	A	R	R	Entering sleep state
F5h	R	A	R	A	Exiting sleep state
F8h	A	R	R	R	Operating system has requested EFI to close boot services (ExitBootServices( ) has been called)
F9h	A	R	R	A	Operating system has switched to virtual address mode (SetVirtualAddressMap( ) has been called)
FAh	A	R	A	R	Operating system has requested the system to reset (ResetSystem( ) has been called)
Pre-EFI Initialization Module (PEIM) / Recovery					
30h	Off	Off	R	R	Crisis recovery has been initiated because of a user request
31h	Off	Off	R	A	Crisis recovery has been initiated by software (corrupt flash)
34h	Off	G	R	R	Loading crisis recovery capsule
35h	Off	G	R	A	Handing off control to the crisis recovery capsule
3Fh	G	G	A	A	Unable to complete crisis recovery

C.4 POST Error Beep Codes

Table 45 lists POST error beep codes. Prior to system video initialization, BIOS uses these beep codes to inform users on error conditions. The beep code is followed by a user-visible code on the POST Diagnostic LEDs.

Table 45. POST Error Beep Codes

Beeps	Error Message	Description
3	Memory error	System halted because of a fatal error related to the memory was detected.
6	BIOS rolling back error	The system has detected a corrupted BIOS in the flash part, and is rolling back to the last good BIOS.

The BMC may generate beep codes upon detection of failure conditions. Beep codes are sounded each time the problem is discovered, such as on each power-up attempt, but are not sounded continuously.

Codes that are common across all Intel® server boards and systems that use the Intel® S5000 chipset are listed in Table 46. Each digit in the code is represented by a sequence of beeps whose count is equal to the digit.

Table 46. BMC Beep Codes

Code	Reason for Beep	Associated Sensors	Supported?
1-5-2-1	CPU: Empty slot / population error – Processor slot 1 is not populated	CPU Population Error	Yes
1-5-2-2	CPU: No processors (terminators only)	N/A	No
1-5-2-3	CPU: Configuration error (e.g., VID mismatch)	N/A	No
1-5-2-4	CPU: Configuration error (e.g., BSEL mismatch)	N/A	No
1-5-4-2	Power fault: DC power unexpectedly lost (power good dropout)	Power Unit – power unit failure offset	Yes
1-5-4-3	Chipset control failure	N/A	No
1-5-4-4	Power control fault	Power Unit – soft power control failure offset	Yes

C.5 POST Error Messages

Whenever possible, the BIOS outputs the current boot progress codes on the video screen. Progress codes are 32-bit values plus optional data. The 32-bit numbers include class, subclass, and operation information. The class and subclass fields point to the type of hardware that is being initialized. The operation field represents the specific initialization activity. Based on the data bit availability to display progress codes, a progress code can be customized to fit the data width. The higher the data bit, the higher the granularity of information that can be sent on the progress port. The progress codes may be reported by the system BIOS or option ROMs.

The Response section in the following table is divided into two types:

- Pause: The message is displayed in the Error Manager screen, an error is logged to the SEL, and user input is required to continue. The user can take immediate corrective action or choose to continue booting.
- Halt: The message is displayed in the Error Manager screen, an error is logged to the SEL, and the system cannot boot unless the error is resolved. The user needs to replace the faulty part and restart the system.

Table 47. POST Error Message Codes

Error Code	Error Message	Response
004C	Keyboard / interface error	Pause
0012	CMOS date / time not set	Pause
5220	Configuration cleared by jumper	Pause
5221	Passwords cleared by jumper	Pause
5223	Configuration default loaded	Pause
0048	Password check failed	Halt
0141	PCI resource conflict	Pause
0146	Insufficient memory to shadow PCI ROM	Pause
8110	Processor 01 internal error (IERR) on last boot	Pause
8111	Processor 02 internal error (IERR) on last boot	Pause
8120	Processor 01 thermal trip error on last boot	Pause
8121	Processor 02 thermal trip error on last boot	Pause
8130	Processor 01 disabled	Pause
8131	Processor 02 disabled	Pause
8160	Processor 01 unable to apply BIOS update	Pause
8161	Processor 02 unable to apply BIOS update	Pause
8190	Watchdog timer failed on last boot	Pause
8198	Operating system boot watchdog timer expired on last boot	Pause
0192	L3 cache size mismatch	Halt
0194	CPUID, processor family are different	Halt
0195	Front side bus mismatch	Pause
0197	Processor speeds mismatched	Pause
8300	Baseboard management controller failed self-test	Pause
8306	Front panel controller locked	Pause
8305	Hot swap controller failed	Pause
84F2	Baseboard management controller failed to respond	Pause
84F3	Baseboard management controller in update mode	Pause
84F4	Sensor data record empty	Pause
84FF	System event log full	Pause
8500	Memory Component could not be configured in the selected RAS mode	Pause
8520	DIMM_A1 failed Self Test (BIST)	Pause
8521	DIMM_A2 failed Self Test (BIST)	Pause
8522	DIMM_A3 failed Self Test (BIST)	Pause
8524	DIMM_B1 failed Self Test (BIST)	Pause
8525	DIMM_B2 failed Self Test (BIST)	Pause
8526	DIMM_B3 failed Self Test (BIST)	Pause
8540	Memory Component lost redundancy during the last boot	Pause
8580	DIMM_A1 Correctable ECC error encountered	Pause
8581	DIMM_A2 Correctable ECC error encountered	Pause
8582	DIMM_A3 Correctable ECC error encountered	Pause

Table 47. POST Error Message Codes

Error Code	Error Message	Response
8584	DIMM_B1 Correctable ECC error encountered	Pause
8585	DIMM_B2 Correctable ECC error encountered	Pause
8586	DIMM_B3 Correctable ECC error encountered	Pause
8600	Primary and secondary BIOS IDs do not match	Pause
8601	Override jumper is set to force boot from lower alternate BIOS bank of flash ROM	Pause
8602	WatchDog timer expired (secondary BIOS may be bad)	Pause
8603	Secondary BIOS checksum fail	Pause

Appendix D Glossary

This appendix contains important terms used in the preceding chapters.

Term	Definition
ACPI	Advanced Configuration and Power Interface
AP	Application Processor
APIC	Advanced Programmable Interrupt Control
ASIC	Application Specific Integrated Circuit
ASMI	Advanced Server Management Interface
BIOS	Basic Input/Output System
BIST	Built-In Self Test
BMC	Baseboard Management Controller
Bridge	Circuitry connecting one computer bus to another, allowing an agent on one to access the other
BSP	Bootstrap Processor
byte	8-bit quantity
CBC	Chassis Bridge Controller (A microcontroller connected to one or more other CBCs; together they bridge the IPMB buses of multiple chassis.)
CEK	Common Enabling Kit
CHAP	Challenge Handshake Authentication Protocol
CMOS	In terms of this specification, this describes the PC-AT compatible region of battery-backed 128 bytes of memory, which normally resides on the server board.
DPC	Direct Platform Control
EEPROM	Electrically Erasable Programmable Read-Only Memory
EFP	Ethernet Front Panel
EHCI	Enhanced Host Controller Interface
EMP	Emergency Management Port
EPS	External Product Specification
ESB2	Enterprise South Bridge 2
FBD	Fully Buffered DIMM
FMB	Flexible Mother Board
FRB	Fault Resilient Booting
FRU	Field Replaceable Unit
FSB	Front Side Bus
GB or Gbyte	Gigabyte (=1024 Mbytes)
GbE	Gigabit (1 billion bit/second) Ethernet
GPIO	General Purpose I/O

Term	Definition
GTL	Gunning Transceiver Logic
HSC	Hot-Swap Controller
Hz	Hertz (1 cycle/second)
I^2C	Inter-Integrated Circuit Bus
IA	Intel® Architecture
IBF	Input Buffer
ICH	I/O Controller Hub
ICMB	Intelligent Chassis Management Bus
IERR	Internal Error
IFB	I/O and Firmware Bridge
INTR	Interrupt
IP	Internet Protocol
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
IR	Infrared
ITP	In-Target Probe
KB or Kbyte	Kilobyte (=1024 bytes)
kbps	Kilobits (1000 bits) per second
KCS	Keyboard Controller Style
LAN	Local Area Network
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LPC	Low Pin Count
LUN	Logical Unit Number
MAC	Media Access Control
MB or Mbyte	Megabyte (=1024 Kbytes)
MCH	Memory Controller Hub
MD2	Message Digest 2 – Hashing Algorithm
MD5	Message Digest 5 – Hashing Algorithm – Higher Security
ms	Milliseconds
MTTR	Memory Type Range Register
Mux	Multiplexor
NIC	Network Interface Controller
NMI	Nonmaskable Interrupt
OBF	Output Buffer
OEM	Original Equipment Manufacturer
Ohm (Ω)	Fundamental unit of electrical resistance
PDB	Power Distribution Board
PEF	Platform Event Filtering
PEP	Platform Event Paging
PIA	Platform Information Area (this feature configures the firmware for the platform hardware)

Term	Definition
PLD	Programmable Logic Device
PMI	Platform Management Interrupt
POST	Power-On Self Test
PSMI	Power Supply Management Interface
PWM	Pulse-Width Modulation
RAID	Redundant Array of Inexpensive (or Independent) Drives
RAM	Random Access Memory
RASUM	Reliability, Availability, Serviceability, Usability, and Manageability
RISC	Reduced Instruction Set Computing
ROM	Read Only Memory
RTC	Real-Time Clock (Component of ICH peripheral chip on the server board)
SAS	Serial Attached SCSI
SDR	Sensor Data Record
SCSI	Small Computer System Interface
SEEPROM	Serial Electrically Erasable Programmable Read-Only Memory
SEL	System Event Log
SFP	SAS Front Panel
SIO	Server Input/Output
SMI	Server Management Interrupt (SMI is the highest priority nonmaskable interrupt)
SMM	Server Management Mode
SMS	Server Management Software
SNMP	Simple Network Management Protocol
TBD	To Be Determined
TIM	Thermal Interface Material
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UHCI	Universal Host Controller Interface
UTC	Universal time coordinare
VID	Voltage Identification
VRD	Voltage Regulator Down
ZIF	Zero Insertion Force

Appendix E: Reference Documents

See the following documents for additional information:

- Intel® S5000 Server Board Family Datasheet
  http://www.intel.com/support/motherboards/server/sb/cs-022620.htm
- Dual-Core Intel® Xeon® Processor 5100 Series Datasheet
  http://www.intel.com/design/xeon/datashts/313355.htm
- Dual-Core Intel® Xeon® Processor 5100 Series Thermal/Mechanical Design Guidelines
  http://www.intel.com/design/xeon/guides/313357.htm
- Quad-Core Intel® Xeon® Processor 5400 Series Datasheet
  http://download.intel.com/design/xeon/datashts/318589.pdf
- Dual-Core Intel® Xeon® Processor 5400 Series Thermal/Mechanical Design Guidelines
  http://download.intel.com/design/xeon/guides/318611.pdf
- Intel® S5000 Server Board Family BIOS Core External Product Specification (restricted document)
- Intel® S5000 Server Board Family BMC Core External Product Specification (restricted document)
- Intel® 5000P Memory Controller Hub External Design Specification (restricted document)
- Intel® Enterprise South Bridge-2 (ESB2) External Design Specification (restricted document)
- Intel® Carrier Grade Server TIGW1U Configuration Guide
  http://www.intel.com/support/telecom/computeboards/tigw1u/sb/CS-026555.htm
- Intel® IP Network Server NSW1U, Configuration Guide
  http://www.intel.com/support/telecom/computeboards/nsw1u/sb/CS-025497.htm