

CPU to PCI Write Buffer

When enabled, allows data and address access to the internal buffer of 82C576MV so the processor can be released from waiting state. The options are: Enabled (Default), Disabled.

PCI Master Write Buffer

When enabled, allows PCI write operation by informing the CPU of pending data from the PCI device. The processor is released from the waiting state by a signal from the master card. The options are: Enabled (Default), Disabled.

PCI Master Prefetch

When enabled, allows the data and address to be saved in the internal buffer of 82C576MV to reduce the master drive access time. The options are: Enabled (Default), Disabled.

PCI Master Burst Read

When enabled, allows the PCI master drive to burst read data from the system, instead of the normal speed (32 bits at a time). It increases the data transfer from PCI to the system. The options are: Enabled (Default), Disabled.

PCI Master Burst Write

When enabled, allows the PCI master drive to burst write data to the system, instead of the normal speed (32 bits at a time). It increases the data transfer from PCI to the system. The options are: Enabled (Default), Disabled.

PCI Dynamic Decoding

When enabled, allows the PCI IDE controller to automatically decode the next 1KB codes that come after a PCI cycle. It will improve the system performance. The options are: Enabled (Default), Disabled.

PCI Dynamic Bursting

When enabled, allows the processor to execute the "Burst write" function during a PCI cycle. The options are: Enabled (Default), Disabled.

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PCI Byte Merge

When enabled, allows the PCI cycle to send data out only after the internal buffer of 82C576MV is filled up completely. If you are using Trident 9440 PCI VGA card (VC-910), AVANCE ALG 2301 PCI VGA card or KELVIN 64-PCI (Cirrus 5434) PCI VGA card, keep this feature disabled. The options are: Disabled (Default), Enabled

Local Memory Detect Point

If set at Fast, the PCI access to the same 1KB address in memory will be reduced one PCI cycle. If you are using the Adaptec PCI SCSI Card AHA-2940/45, please set at "Medium". The options are: Fast (Default), Medium.

PCI Burst

When enabled, it will improve the data transfer on PCI Buses. Disable it during trouble-shooting. The options are: Disabled, Enabled (Default).

PCI Master 0 WS Write

When enabled, allows zero wait state cycle delay when the PCI master drive writes data to DRAM. The options are: Enabled (Default), Disabled.

Interrupt Assignments of PCI Slots

SLOT	INT OF SLOT	INT OF VR82C576
A	A	A
	B	B
	C	C
	D	D
B	A	B
	B	C
	C	D
	D	A
C	A	C
	B	D
	C	A
	D	B

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