NP430HX Motherboard Specification Update

Release Date: April 1997

Order Number 281828-004

The NP430HX Motherboard may contain design defects or errors known as errata. Characterized errata that may cause the NP430HX Motherboard's behavior to deviate from published specifications are documented in this specification update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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REVISION HISTORY

Date of Revision	Version	Description
August 1996	-001	This document is the first Specification Update for the Intel NP430HX motherboard.
October 1996	-002	Added Erratum 3, Specification Clarification 1, Documentation Changes 1-8.
December 1996	-003	Added Errata 4-5 and Specification Clarification 2.
April 1997	-004	Added Errata 6-9 and PBA/BIOS Table. Moved Specification Clarification 1 to Erratum 10. Updated Specification Clarification 2 and Documentation Change 4.

PREFACE

This document is an update to the specifications contained in the *NP430HX Motherboard Technical Product Specification* (Order Number 281816). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Refer to the *Pentium® Processor Specification Update* (Order Number 242480) for specification updates concerning the Pentium® processor. Items contained in the *Pentium® Processor Specification Update* that either do not apply to the NP430HX motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

Refer to the *82430HX PCIset Specification Update* (Order Number 297652) for specification updates concerning the 82430HX PCIset. Items contained in the *82430HX PCIset Specification Update* that either do not apply to the NP430HX motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any PCIset errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

Refer to the *82371SB PIIX3 Specification Update* (Order Number 297658) for specification updates concerning the 82371SB PIIX3. Items contained in the *82371SB PIIX3 Specification Update* that either do not apply to the NP430HX motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any PCIset errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Characterized errata may cause the NP430HX motherboard's behavior to deviate from published specifications. Hardware and software designed to be used with any given Printed Board Assembly (PBA) and BIOS revision level must assume that all errata documented for that PBA and BIOS revision are present on all motherboards.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Update for NP430HX Motherboards

GENERAL INFORMATION

Basic NP430HX Motherboard Identification Information

PBA Revision	AA Revision	82430HX PCIset Stepping	BIOS Revision	Notes
657908-400	657909-404	A1	1.00.01.DE0	1, 2, 3, 4, 5

NOTES:

1. The PBA number is found on a small label on the component side of the board.
2. The 82430HX PCIset kit used on this PBA revision consists of two different components as follows:

Device	Stepping	S-Spec Numbers
82439HX	A1	SU087
82371SB	B0	SU093

3. The following errata contained in the *82430HX PCIset Specification Update* (Order Number 297652) either do not apply to the NP430HX motherboard or have been worked around in this PBA and/or BIOS revision: 2-3. All other errata associated with the PCIset apply to this PBA revision. For specific details of any erratum please refer to the *82430HX PCIset Specification Update*.
4. The following errata contained in the *82371SB PIIX3 Specification Update* (Order Number 297658) either do not apply to the NP430HX motherboard or have been worked around in this PBA and/or BIOS revision: 1-7. All other errata associated with the PCIset apply to this PBA revision. For specific details of any erratum please refer to the *82371SB PIIX3 Specification Update*.
5. The following errata contained in Part I of the *Pentium® Processor Specification Update* (Order Number 242480) either do not apply to the NP430HX motherboard or have been worked around in this PBA and/or BIOS revision: 5, 7, 9-11, 13-14, 16-17, 29, 31, 34, 36-37, 39, 40, 46, 48-50, 58, 60-64, 66-67, 69, 71, all DP errata, all AP errata, all TCP errata. All other errata in Part I may apply to this revision level of the motherboard, depending on the stepping of the processor or the specific software that is being executed. Also, some of these errata apply only to motherboards being used in an application development environment. For specific details of any erratum please refer to the *Pentium® Processor Specification Update.*

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the NP430HX motherboard. Intel intends to fix some of the errata in a future revision of the motherboard, and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future revision of the motherboard or BIOS.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This erratum is either new or modified from the previous version of the document.

		ERRATA
1	Fix	ECC non-detection of single/double bit errors on partial memory writes
2	Fix	PCI Delayed Transactions are not supported
3	Fix	System BIOS does not recognize bootable USB devices
4	Fix	BIOS does not support no-emulation mode for CD-ROM boot
5	Fix	CMOS checksum may be lost if power is cycled during boot
6	Fix	IDE operating modes misrepresented in BIOS Setup Program
7	Fixed	Resource conflict with onboard ATI video
8	NoFix	Video capture card may hang system due to improper TRST# signal
9	Fix	Slave on secondary IDE channel is not disabled
10	NoFix	Cannot meet FCC Class B requirements using unshielded USB cable
NO.	**PLANS**	**SPECIFICATION CLARIFICATIONS**
1	Doc	Replaced by Specification Change 1
2	Doc	Bus mastering may not be available using the third PCI slot
NO.	**PLANS**	**DOCUMENTATION CHANGES**
1	Doc	Revision of Section 1.2, “Motherboard Manufacturing Options”
2	Doc	Revision of Motherboard Features descriptions
3	Doc	Addition of OverDrive® processor and Pentium® Processor with MMX™ technology support
4	Doc	Revision of Section 1.5.2, “Second Level Cache”
5	Doc	Addition of ATI 264GT 3-D Graphics Subsystem
6	Doc	Revision of Section 1.9, “Audio Subsystem”
7	Doc	Revision of Figure 5, “Board Connectors”
8	Doc	Revision of Section 1.12.4, “Fan Connectors - J9K1, J9K2”

The errata described in this specification update apply to combinations of PBA revision and BIOS revision as shown in the table below. Descriptions of the individual errata referred to by number in the table below are found in the ERRATA section of this document.

PBA Revision	BIOS Revision	Errata That Apply
657908-400	1.00.01.DE0	1-10

NOTE:

‡ This combination of BIOS revision and PBA revision has not undergone regression testing. Use of a PBA with down-revision BIOS is an untested combination and is undertaken at the user's risk.

ERRATA

1. ECC Non-detection of Single/Double Bit Errors on Partial Memory Writes

PROBLEM: When the 82439HX TXC performs a partial write to main memory (data less than a 64-bit quadword) in ECC mode, single bit errors are corrected but not logged. Double bit errors are not detected or logged.

IMPLICATION: Normally, the controller is able to buffer writes and group them into quadwords. In all these cases where 64 bits are written to memory at a time, both single and double bit errors will be signaled to the operating system. Single bit errors will be corrected using the information contained in the checkbits that are stored with the data in memory. Double bit errors cannot be corrected by the memory controller, but the operating system can warn the user that the error has occurred.

If the controller must perform a partial write, a read-merge-write cycle will occur so that the proper checkbits can be regenerated across the entire 64 bits to be written into DRAM. If erroneous data is read during this cycle, the following will occur:

For single bit errors, the error will be corrected based on the memory checkbits. The corrected data will be written back to memory, but the error will not be flagged to the system, so the user will not receive information from the error log that could be useful in isolating a failing memory module.

For double-bit errors, no error will be detected or signaled to the operating system. The erroneous data will be rewritten to memory and a set of regenerated checkbits will be rewritten at the same time, marking the erroneous data as correct.

WORKAROUND: None. However, for ECC systems that require only single bit error protection, the A1 stepping of the 430HX PCIset does provide this level of reliability.

STATUS: This erratum will be fixed in a future PBA revision.

2. PCI Delayed Transactions Are Not Supported

PROBLEM: An erratum to the A1 stepping of the 82371SB PCI ISA IDE Xcelerator (PIIX3) requires that the option for Delayed Transactions be turned off by the BIOS.

IMPLICATION: System level performance and compatibility are not affected by turning off delayed transactions. The system will be PCI 2.1 compatible and will support all PCI 2.1 compliant cards.

WORKAROUND: None.

STATUS: This erratum will be fixed in a future PBA revision.

3. System BIOS Does Not Recognize Bootable USB Devices

PROBLEM: The system BIOS does not recognize a USB keyboard or mouse during a system boot. A USB keyboard or mouse is not recognized until an operating system that supports USB is loaded.

IMPLICATION: 1. The user is not able to use a USB keyboard to enter the BIOS Setup or to respond to error messages that are displayed before an operating system with USB support is loaded.
2. The user is not able to use a USB keyboard or mouse with any operating system that does not have USB support.

WORKAROUND: Use a standard PS/2* style keyboard and mouse in any configuration where input is required before an operating system with USB support is loaded.

STATUS: This erratum will be fixed in a future BIOS revision.

4. BIOS Does Not Support No-Emulation Mode for CD-ROM Boot

PROBLEM: The system BIOS does not support booting from an "El Torito" bootable CD-ROM using the no-emulation mode format.

IMPLICATION: Booting from a CD-ROM using no emulation mode is not supported. For example, Microsoft Windows* NT* version 4.0 uses no-emulation mode for its boot CD-ROM.

WORKAROUND: Boot the computer from a floppy or hard disk, then install or run the program from the CD-ROM.

STATUS: This erratum will be fixed in a future BIOS revision.

5. CMOS Checksum May Be Lost If Power Is Cycled During Boot

PROBLEM: If the computer power is turned off during a short portion of the boot process, the CMOS checksum byte is not updated. The next time the computer is turned on, the message "CMOS Checksum Invalid" will be displayed.

IMPLICATION: When the message is displayed, the correct checksum has already been recalculated and stored. No user action is required to recover from the error. If the additional message:

> Date and Time Not Set
> Press <F1> for Setup, <Esc> to Boot

is displayed, the user must reset the current date and time using the BIOS Setup program.

WORKAROUND: None.

STATUS: This erratum will be fixed in a future BIOS revision.

6. IDE Operating Modes Misrepresented in BIOS Setup Program

PROBLEM: The BIOS Setup program does not appropriately make the changes entered in the Translation Mode Configuration screen. Changes are made according to sequential drive number instead of the fields specified for IDE Drives.

IMPLICATION: Changes made in the Translation Mode Configuration screen are applied sequentially using the drive numbers as identified by the FDISK utility. For example, changes for the Primary Master drive are applied to drive 1, the Primary Slave is applied to drive 2, and so on. With no drives or one drive attached to the primary connector, changes made to the Primary Master or Primary Slave drives may be applied to drives located in the secondary header.

WORKAROUND: None.

STATUS: This erratum will be fixed in a future BIOS revision.

7. Resource Conflict with Onboard ATI Video

PROBLEM: The system may fail to initialize a 3COM 3C595 bus mastering network card when configured as a Windows* NT* 3.51 server or workstation. Windows NT reports that there is a conflict with the resources of the 3COM 3C595 network card and the onboard ATI* video.

IMPLICATION: The resource conflict will not allow the server to logon to the domain controller. Attaching to the network as a workstation may be intermittent.

WORKAROUND: None.

STATUS: This erratum was fixed with revision 3.0 of the ATI Mach 64 drivers for Windows NT 3.51 available at http:\\www.intel.com.

8. Video Capture Card May Hang System Due to Improper TRST# Signal

PROBLEM: If a PCI add-in card that implements boundary scan is installed, the computer may not boot. In accordance with the PCI 2.1 specification, the add-in card expects the TRST# signal to be pulled down if JTAG is not supported by the motherboard. The motherboard does not implement JTAG boundary scan and does not pull the TRST# signal down.

IMPLICATION: The computer may not boot if a PCI card that implements JTAG boundary scan is inserted.

WORKAROUND: None. PCI add-in cards that implement JTAG boundary scan are not compatible with this motherboard.

STATUS: This erratum will not be fixed.

9. Slave on Secondary IDE Channel is not Disabled

PROBLEM: If the IDE Device Configuration option in BIOS Setup is set to disable the secondary IDE slave device, it will not be disabled in the following configuration:

- ATAPI device attached as master to the secondary IDE connector.
- ATAPI device attached as slave to the secondary IDE connector.

IMPLICATION: In the above configuration, any ATAPI device attached as a secondary slave will remain enabled even if the BIOS setting for the secondary slave is set to disabled.

WORKAROUND: None.

STATUS: This erratum will be fixed in a future BIOS revision.

10. Cannot Meet FCC Class B Requirements using Unshielded USB Cable

PROBLEM: The motherboard will generate excessive electromagnetic radiation on unshielded USB cables, even if no device or a low speed (sub-channel) USB device is attached to the cable.

IMPLICATION: Systems based on this motherboard will not meet FCC Part 15 Class B requirements when unshielded USB cable is used. Although this condition is a violation of the USB v1.0 specification, it is not believed to have any effect on normal USB device operation.

WORKAROUND: Use USB devices with shielded cable that meet the requirements for high speed (fully-rated) USB devices.

STATUS: This erratum will not be fixed.

SPECIFICATION CLARIFICATIONS

The Specification Clarifications listed in this section apply to the *NP430HX Technical Product Specification* (Order Number 281816). All Specification Clarifications will be incorporated into a future version of that specification.

1. Replaced by Erratum 10

2. Bus Mastering May Not Be Available Using The Third PCI Slot

The following note will be added as part of Section 1.12.11, Add-in Board Expansion Connectors:

The shared PCI slot (J4C1) does not support bus mastering if both the onboard LAN adapter and onboard video controller are enabled.

DOCUMENTATION CHANGES

The Documentation Changes listed in this section apply to the NP430HX *Motherboard Technical Product Specification* (Order Number 281816). All Documentation Changes will be incorporated into a future version of the appropriate NP430HX motherboard documentation.

1. Revision of Section 1.2, Motherboard Manufacturing Options

This section will be replaced in its entirety as follows:

Option One:

- 256 KB Pipeline Burst SRAM soldered onto the motherboard for L2 cache
- Full Duplex integrated audio using Yamaha OPL3-SA integrated CODEC/FM synthesizer
- ATI -VT graphics subsystem with 1 MB of 60 ns SGRAM
- 10/100 Mbps LAN
- Universal serial bus (USB) connectors
- "Soft-off," (motherboard can turn off system power through software control)

Option Two:

- 512 KB Pipeline Burst SRAM soldered onto the motherboard for L2 cache
- Full Duplex integrated audio using Yamaha OPL3-SA integrated CODEC/FM synthesizer
- ATI -GT graphics subsystem with 2 MB of 60 ns SGRAM
- 10/100 Mbps LAN
- Universal serial bus (USB) connectors
- "Soft-off," (motherboard can turn off system power through software control)

2. Revision of Motherboard Features Descriptions

In Figure 1, Motherboard Features, the following changes will be made to the descriptions:

B Optional Yamaha OPL3-SA FM synthesizer to Yamaha OPL3-SA synthesizer

E Optional ATI 264 VT graphics controller to ATI 264 VT or ATI 264 GT graphics controller

H Optional Dual stacked USB connectors to Dual stacked USB connectors

M Optional SGRAM devices to SGRAM devices

N Optional 82557 LAN controller to 82557 LAN controller

O Optional 83840 device to 83840 device

3. Addition of OverDrive® Processor and Pentium® Processor With MMX™ Technology Support

In section 1.4, the first paragraph will be replaced in its entirety as follows:

The NP430HX motherboard is designed to operate with 3.3 volt Pentium ® processors. An onboard linear voltage regulator circuit provides the required 3.3 volts from the 5.0 volt tap of the power supply. An on-board jumper enables use of OverDrive ® processors and Pentium processors with MMX ™ technology. All Pentium processors (those running internally at 75, 90, 100, 120, 133, 150, 166, and 200 MHz) are supported.

4. Revision of Section 1.5.2, Second Level Cache

This section will be replaced in its entirety as follows:

The Pentium processor's internal cache can be complemented by a second-level (L2) cache using high-performance pipelined burst SRAMs with GWE (Global Write Enabled). A factory option on the NP430HX motherboards is an onboard 256 KB or 512 KB direct-mapped, write-back L2 cache. The L2 cache is implemented with two pipeline burst SRAM devices that take advantage of the Global Write Enable pin. An 8Kb x 8 external Tag SRAM provides caching support for up to 256 KB cache memory. A 32Kb x 8 external Tag SRAM provides caching support for up to 512 KB cache memory. There are no upgrade options for the second-level cache. Both Tag SRAM components provide caching support for the first 64 MB of main memory.

5. Addition of ATI 264GT 3-D Graphics Subsystem

The following will be inserted as Section 1.9 Graphics Subsystem (ATI 264GT 3-D Graphics Controller). All following sections will be renumbered accordingly.

GRAPHICS SUBSYSTEM (ATI-264GT 3-D GRAPHICS CONTROLLER)

The ATI-GT 3-D graphics controller is a highly integrated, 208 pin, VLSI multimedia graphics and video controller that integrates the following features:

- The controller is housed in a 208-pin PQFP package.
- The controller implements video acceleration and 3-D rendering.
- The controller supports 3-D rendering with as little as 1MB of SGRAM graphic memory.
- The controller is able to function as a PCI bus master.
- The controller supports connection to Plug and Play monitors with both DDC1 (Data Display Channel 1) and DDC2B capability. This allows changing of the monitor resolutions and color options without rebooting the computer.

GRAPHICS UPGRADE OPTIONS

The NP430HX motherboard has several headers that support expansion of the graphic subsystem. The LBP VESA feature connector supports connection to devices such as ATI MPEG and TV products.

Two video memory upgrade connectors support connection to video memory upgrade modules from ATI. These upgrade modules allow upgrading the total video memory from the standard 1 MB (or 2 MB) of onboard SGRAM, to either 2 MB or 4 MB of total video memory.

RESOLUTIONS SUPPORTED

Table 1 lists the available video resolutions using the video controller and a standard 1 MB of SGRAM video memory. The controller supports 3-D rendering with as little as 1 MB of SGRAM graphic memory. The video memory can be upgraded to a maximum of 4 MB of video memory using plug-in daughterboards. Refer to the video controller data sheet for the video resolutions available with more than 1MB of video memory.

Table 1. Supported Video Resolutions

Resolution	Supported with 1 MB SGRAM	Refresh Rate (Hz)
640 x 480 x 256 colors	Yes	100
640 x 480 x 64K colors	Yes	100
640 x 480 x 16.7M colors	Yes	100
800 x 600 x 256 colors	Yes	100
800 x 600 x 64K colors	Yes	100
800 x 600 x 16.7M colors	No	100
1024 x 768 x 256 colors	Yes	100
1024 x 768 x 64K colors	No	100
1152 x 864 x 256 colors	Yes	80
1152 x 864 x 64K colors	No	80
1280 x 1024 x 16 colors	Yes	75
1280x 1024 x 256 colors	No	75

GRAPHICS DRIVERS AND UTILITIES

Common graphics drivers and utilities for DOS, Windows* 3.1x, Windows 95, and other operating systems, as well as a variety of applications (such as AutoCAD) are available for the NP430HX motherboard. Contact your vendor for a list of available drivers. The Windows 3.1x and Windows 95 drivers include the ATI WinSwitch utility that allows users to change screen resolution without rebooting Windows, and the ATI DeskTop that supports panning and scrolling across a virtual workspace of up to 2048 x 1536.

Drivers for some operating systems such as OS/2* are native to the operating systems. Drivers for SCO and Interactive UNIX* should be obtained from the respective UNIX vendor. Although Windows 95 installs native drivers for the onboard video, these drivers are not optimized, so you should obtain and install the accelerated drivers available through your vendor.

6. Revision of Section 1.9, Audio Subsystem

The first paragraph, first sentence will be replaced in its entirety as follows:

The NP430HX motherboard features a 16-bit stereo audio subsystem based upon the Yamaha OPL3-SA FM synthesizer.

7. Revision of Figure 5, Board Connectors

Connectors number J9K1/J9K2 (Fan Connectors) will be changed as follows:

Pin 1 will be changed to Pin 3. Pin 3 will be changed to Pin 1. Pin 2 will remain unchanged.

8. Revision of Section 1.12.4, Fan Connectors - J9K1, J9K2

Fan Connectors - J9K1, J9K2 will be replaced in its entirety as follows:

FAN CONNECTORS - J9K1, J9K2

Pin	Signal Name
1	Sense tachometer
2	+ 12 V
3	Ground