Performance/AU Motherboard Specification Update

Release Date: September 1996

Order Number: 281807-004

The Performance/AU Motherboard may contain design defects or errors known as errata. Characterized errata that may cause the Performance/AU Motherboard's behavior to deviate from published specifications are documented in this specification update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 7641
Mt. Prospect, IL 60056-7641

or call in North America 1-800-879-4683, Europe 44-0-1793-431-155, France 44-0-1793- 421-777,

Germany 44-0-1793-421-333, other Countries 708-296-9333

CONTENTS

REVISION HISTORY

Date of Revision	Version	Description
April 1996	-001	This document is the first Specification Update for the Intel Performance/AU motherboard.
May 1996	-002	Added Specification Changes 1-2, Modified Errata to reflect items fixed since the last revision.
June 1996	-003	Added Errata 11-12.
September 1996	-004	Added Erratum 13.

PREFACE

This document is an update to the specifications contained in the *Performance/AU Motherboard Technical Product Specification* (Order Number 281802). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Refer to the *Pentium® Pro Processor Specification Update* (Order Number 242689) for specification updates concerning the Pentium Pro processor. Items contained in the *Pentium® Pro Processor Specification Update* that either do not apply to the Performance/AU motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

Refer to the *Intel 82450KX/GX PCIset Specification Update* (Order Number 243109) for specification updates concerning the Intel 450KX/GX PCIset. Any PCIset errata from that document which apply to this motherboard revision level and that have not been worked around are noted in this document.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Characterized errata may cause the Performance/AU motherboard's behavior to deviate from published specifications. Hardware and software designed to be used with any given Printed Board Assembly (PBA) and BIOS revision level must assume that all errata documented for that PBA and BIOS revision level are present on all motherboards.

Specification Update for Performance/AU Motherboards

GENERAL INFORMATION

Basic Performance/AU Motherboard Identification Information

PBA Revision	82450KX Stepping	CPU Stepping/ S-Spec	Fab Revision	BIOS Revision	Notes
633784-604	A-2 kit	B-0/SY002	D	1.00.03.CG0	1, 2, 3
633784-605	A-2 kit	B-0/SY011	D	1.00.03.CG0	2, 3
633784-605	A-2 kit	C-0/SY010	D	1.00.03.CG0	2, 4
633784-606	A-2 kit	B-0/SY011	D	1.00.03.CG0	2, 3
633784-606	A-2 kit	C-0/SY010	D	1.00.03.CG0	2, 4
633784-703	B-0 kit	C-0/SY010	E	1.00.05.CG0	4, 5
633784-704	B-0 kit	C-0/SY010	E	1.00.06.CG0	4, 5

NOTES:

1. The Pentium® Pro processor VID pins are not supported on the S-Spec SY002 devices and, therefore, jumper J29 is installed on this PBA revision of the motherboard.
2. The Intel 450KX PCIset kit used on this PBA revision consists of four different components as follows:

Device	Stepping	S-Spec Numbers		
82451KX (MIC)	A-1	SU025	**OR**	SU039
82452KX (DP)	A-1	SU026		SU040
82453KX (DC)	A-2	SU027		SU041
82454KX (PB)	A-2	SU028		SU042

3. The following errata are contained in the *Pentium® Pro Processor Specification Update* (Order Number 242689*)* for the B-0 stepping of the processor and either do not apply to the Performance/AU motherboard or have been worked around in this PBA and/or BIOS revision: 1, 4, 5, 8-10, 12-15, 17-18, 20, 23, 25-28, 30-33, 35-39, 41-43, 45, 47-48, 50 and 1-6AP. All other errata associated with the B-0 stepping of the processor apply to this PBA revision.
4. The following errata are contained in the *Pentium® Pro Processor Specification Update* (Order Number 242689*)* for the C-0 stepping of the processor and either do not apply to the Performance/AU motherboard or have been worked around in this PBA and/or BIOS revision: 1, 4, 8, 10, 14-15, 20, 23, 26-28, 30-33, 36-39, 41-43, 45, 47-48, 50 and 1-6AP. All other errata associated with the C-0 stepping of the processor apply to this PBA revision.
5. The Intel 450KX PCIset used on this PBA revision consists of four different components as follows:

Device	Stepping	S-Spec Numbers
82451KX (MIC)	A-1	SU025 or SU039

Device	Stepping	S-Spec Numbers
82452KX (DP)	A-3	SU061
82453KX (DC)	A-4	SU062
82454KX (PB)	A-4	SU064

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the Performance/AU motherboard. Intel intends to fix some of the errata in a future revision of the motherboard, and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future revision of the motherboard or BIOS.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This erratum is either new or modified from the previous version of the document.

NO.	PLANS	ERRATA
1	Fixed	PCI bus masters that issue 0-length memory write cycles may result in invalid data
2	Fixed	Bus mastering IDE hard drive controller feature not present
3	NoFix	S/W applications dependent on deturbo may fail
4	Fix	Booting from certain CD-ROM drives may cause system to hang
5	Fixed	64-bit PCI bus master adapters not supported
6	Fixed	System BIOS always initializes ISA Plug-and-Play adapters
7	Fixed	Diagnostic software may fail during IDE hard drive test
8	Fixed	Certain PCI adapter combinations may cause system to hang
9	Fixed	FLASH logo area feature is not supported
10	Fixed	Ctrl-Alt-Del after initial power-on may cause system to hang
11	Fixed	BIOS SETUP does not recognize February 29, 2000 as a valid date
12	Fixed	System BIOS does not recognize certain dates as valid
13	Fixed	PCI video adapter cards fail on secondary or tertiary PCI bus
No.	**PLANS**	**SPECIFICATION CHANGES**
1	Doc	Corrections to the signal names of PCI connectors
2	Doc	Change to the signal name of speaker connector
NO.	**PLANS**	**SPECIFICATION CLARIFICATIONS**
1	Doc	Memory map cacheability
2	Doc	Enhanced Parallel Port (EPP) v1.7 support
3	Doc	IRQ 12 BIOS limitation
4	Doc	Corrections to the “Real Time Clock” settings
5	Doc	Populating SIMM banks

NO.	PLANS	DOCUMENTATION CHANGES
1	Doc	Each memory bank provides a 72-bit wide data path (not 64-bit), page 5, third paragraph
2	Doc	ECC protection for memory data only
3	Doc	Corrections to front panel connection drawing
4	Doc	CPU voltage override jumper
5	Doc	Corrections to memory map description
6	Doc	Bit #0, #3, & #4 entries in table D-2 (page 17) should reference table B-1 (page 14)
7	Doc	IDE Translation Mode section should reference “Standard CHS” instead of “CHS”, page 26, second paragraph
8	Doc	IRQ section of Plug-and-Play Configuration screen “on-bd” reference should actually read as “onboard”
9	Doc	PCI connector signal names
10	Doc	Using the BIOS upgrade utility

ERRATA

1. PCI Bus Masters That Issue 0-Length Memory Write Cycles May Result in Invalid Data

PROBLEM: PCI bus master adapters that issue 0-length write cycles to memory may cause data corruption due to known errata in the A-2 stepping of the 82454KX PCI Bridge component. A 0-length write cycle is defined as a PCI transaction from a bus mastering agent into system memory in which none of the byte enabled bits are asserted.

IMPLICATION: A PCI bus mastering adapter that issues 0-length write cycles may result in memory data corruption and unreliable system behavior.

WORKAROUND: None identified. However, no PCI adapters are currently known to issue 0-length write cycles. The Intel 82371FB PCI-ISA Xcelerator component DOES issue 0-length write cycles (see Erratum Number 2).

STATUS: This erratum was fixed in PBA revision 633784-703.

2. Bus Mastering IDE Hard Drive Controller Feature Not Present

PROBLEM: The bus mastering IDE function of the Intel 82371FB PCI-ISA Xcelerator (PIIX) is not supported due to known errata in the A-2 stepping of the 82454KX PCI Bridge component (see Erratum Number 1) involving 0-length write cycles.

IMPLICATION: Bus mastering IDE drivers that are available for various operating systems should not be used with the on-board PIIX device as they may result in memory data corruption and unreliable system behavior.

WORKAROUND: PCI bus mastering SCSI or IDE add-in cards can be used as long as they do not issue 0-length write cycles.

STATUS: This erratum was fixed in PBA revision 633784-703

3. S/W Applications Dependent on Deturbo May Fail

PROBLEM: The DeTurbo option in BIOS SETUP only disables cache and does not slow the processor clock speed due to errata in the A-2 stepping of the 82454KX PCI Bridge component.

IMPLICATION: Older software applications that rely on DeTurbo capability to slow the processor clock speed may not function as expected.

WORKAROUND: None identified.

STATUS: There are no plans to fix this erratum.

4. Booting From Certain CD-ROM Drives May Cause System to Hang

PROBLEM: A system BIOS problem prevents either a Mitsumi FX-400 or NEC CDR-271 IDE CD-ROM drive from successfully booting a CD-ROM media as a hard drive image.

IMPLICATION: BIOS SETUP allows the user to indicate whether an IDE CD-ROM device should be recognized as a system boot device. When the system attempts to boot from a CD-ROM device during

startup and a bootable CD-ROM ("El Torito" format) is present, the user can select from a menu whether to boot the CD-ROM as either a hard (Drive C:) or floppy (Drive A:) image. If the floppy drive option is selected, the system will hang.

WORKAROUND: This problem is only known to affect the Mitsumi FX-400 and NEC CDR-271 CD-ROM drives. If the hard drive option is selected during startup, the system will boot normally.

STATUS: This erratum will be fixed in a future BIOS revision.

5. Multiple 64-bit PCI Bus Master Adapters May Cause Invalid Transactions

PROBLEM: The PCI signal REQ64# is bussed between the 32-bit PCI expansion slots and is pulled up with a single resistor on the Performance/AU motherboard. According to version 2.1 of the PCI specification, the REQ64# signal should not be bussed and should have individual pull-up resistors for each PCI slot.

IMPLICATION: It is possible for a 64-bit PCI bus master adapter to attempt a 64-bit DMA transaction to another 64-bit PCI adapter, resulting in an invalid transaction since only a 32-bit PCI data path is present.

WORKAROUND: None identified. However, the PCI specification indicates that 64-bit PCI adapters may determine at reset whether a 32- or 64-bit data path is present. This erratum does not apply to configurations in which only a single 64-bit PCI adapter is installed.

STATUS: This erratum was fixed in PBA revision 633784-703.

6. System BIOS Always Initializes ISA Plug-and-Play Adapters

PROBLEM: If the "Use ICU" and "Windows* 95" options are selected in the BIOS Plug-and-Play SETUP screen, any ISA Plug-and-Play adapters that are installed will always be initialized by the system BIOS during startup.

IMPLICATION: The desired behavior for the BIOS under Windows 95 is to not initialize ISA Plug-and-Play adapters so that the operating system can assign and initialize all non-boot device resources during startup. It is possible that ISA Plug-and-Play adapter resources could be assigned resources by the BIOS that are in conflict with other non-boot adapter devices. In such a scenario, Windows 95 might be unable to successfully resolve the resource conflicts thereby preventing initialization of the other devices.

WORKAROUND: If a resource conflict exists between ISA Plug-and-Play adapter resources and other non-boot devices, the ISA Plug-and-Play device(s) can be disabled using the Windows 95 Device Manager feature. When Windows 95 is shutdown and the system is rebooted, the BIOS will then not initialize the ISA Plug-and-Play adapter(s), as expected, and Windows 95 will proceed to assign resources to all non-boot devices.

STATUS: This erratum was fixed in BIOS revision 1.00.05.CG0.

7. Diagnostic Software May Fail During IDE Hard Drive Test

PROBLEM: The INT13 BIOS services that are used to invoke IDE hard drive diagnostics (functions 13 and 14) contain a timing loop that may not allow enough time for the drive diagnostics to successfully complete.

IMPLICATION: Software utilities (e.g. QA Plus) that use the INT13 functions for IDE hard drive diagnostic purposes may receive a timeout error from the BIOS falsely indicating a drive malfunction. In fact, the drive is operating normally in all respects and simply requires a longer time interval to complete its self-test routines.

WORKAROUND: None identified. However, this is only known to affect diagnostic applications and does not occur with all IDE hard drives.

STATUS: This erratum was fixed in BIOS revision 1.00.05.CG0.

8. Certain PCI Adapter Combinations May Cause System to Hang

PROBLEM: The system BIOS improperly masks the PCI ROM size field of some PCI adapters (e.g. IBM Auto LAN Streamer PCI Adapter) during startup, which may result in an insufficient amount of ROM shadow memory being reserved for that adapter. Specifically, the BIOS fails to mask the unused high-order bit of the ROM size field, so adapter cards that return this unused bit as a zero will work as expected.

IMPLICATION: If a PCI adapter is not assigned sufficient ROM shadow memory, then another PCI adapter that also contains ROM and is subsequently detected by the system BIOS may have ROM shadow memory assigned that overlaps the actual shadow memory region for the earlier-detected PCI adapter. This condition will cause both adapters to respond to the same PCI memory address(es), resulting in a PCI bus lockup and system hang.

WORKAROUND: The majority of PCI adapters return unused bits in the PCI ROM size field as zero, so this problem scenario is relatively rare. However, if the overlapping ROM shadow memory condition exists as described above and only one of the installed PCI adapters is affected, it may be possible to resolve the conflict by swapping the PCI slots in which the affected PCI adapters are installed. For example, with a IBM Auto LAN Streamer PCI Adapter and another PCI adapter installed in a system, it would be desirable for the IBM adapter to be installed in a PCI slot that is scanned after the other PCI adapter during BIOS initialization. The rightmost PCI slot is scanned first by the BIOS during POST.

STATUS: This erratum was fixed in BIOS revision 1.00.05.CG0

9. FLASH Logo Area Feature is Not Supported

PROBLEM: The 8-Kbyte FLASH logo area is not accessed following completion of the BIOS POST.

IMPLICATION: A custom logo that has been programmed into the FLASH logo area using the FLASH logo utility available from Intel will not be displayed during the boot process, as expected.

WORKAROUND: None identified.

STATUS: This erratum was fixed in BIOS revision 1.00.05.CG0

10. Ctrl-Alt-Del After Initial Power-On May Cause System to Hang

PROBLEM: The CMOS shutdown byte (location 0Fh) is not cleared by the system BIOS following power-on. During the motherboard manufacturing test process, a non-zero value is written to the shutdown byte that can cause the system BIOS to initiate a shutdown sequence at startup.

IMPLICATION: If a Ctrl-Alt-Del (warm reboot) is initiated after the very first system power-on and following a “Insert bootable media” message (no boot device detected), the system may hang.

WORKAROUND: Ensure that a bootable disk is present before powering on the system for the very first time. This scenario can only occur prior to the first system boot cycle.

STATUS: This erratum was fixed in BIOS revision 1.00.05.CG0

11. BIOS SETUP Does Not Recognize February 29, 2000 As a Valid Date

PROBLEM: The BIOS Setup program will not allow the system date to be set to Feb 29, 2000.

IMPLICATION: Any program that uses the system time and date stamps to determine when to perform some activity will not perform that scheduled activity. Date and time stamps for files created on these dates will be incorrect.

WORKAROUND: If the system BIOS has not been upgraded, the system date will have to be reset to the correct date on March 1, 2000.

STATUS: This erratum was fixed in BIOS revision 1.00.06.CG0.

12. System BIOS Does not Recognize Certain Dates As Valid

PROBLEM: If the motherboard is powered on or reset with the system date set to October 20-31 or December 20-31, the system BIOS will report "CMOS Time and Date Not Set" and the system date will be reset to Jan 01, 1990 during Power On Self Test (POST). If the user resets the system to the correct date and reboots, the system BIOS reports the same error message and again resets the date to Jan 01, 1990.

IMPLICATION: Any program that uses the system time and date stamps to determine when to perform some activity will not perform that scheduled activity. Date and time stamps for files created on these dates will be incorrect.

WORKAROUND: None.

STATUS: This erratum was fixed in BIOS revision 1.00.06.CG0.

13. PCI Video Adapter Cards Fail on Secondary or Tertiary PCI Bus

PROBLEM: A PCI video card that is placed on the secondary side of a PCI-to-PCI bridge fails at power up. Symptoms may be either a system freeze or missing video.

IMPLICATION: The user will need to install any video card on the primary side of a PCI-to-PCI bridge.

WORKAROUND: Install a video card in an on-board PCI slot, which is always on the primary side of any PCI-to-PCI bridge.

STATUS: This erratum was fixed in BIOS revision 1.00.07.CG0.

SPECIFICATION CHANGES

1. Corrections to the Signal Names of PCI Connectors

On Page 23 of the Performance/AU Motherboard Technical Product Specification, the table referring to PCI signal names will be changed as follows:

Pin	New signal name	Old Signal Name
A1	TRST#	GND
A3	TMS	No Connect
A4	TDI	No Connect
A26	IDSEL	AD22
B2	TCK	No Connect
B4	TDO	No Connect
B9	Prsnt1#	No Connect
B11	Prsnt2#	No Connect

2. Change to the Signal Name of Speaker Connector

On page 18 of the Performance/AU Motherboard Technical Product Specification, the table referring to signals on the speaker header will be changed as follows:

Pin 23 is changed to GND from +5V. This change applies only to PBAs based on Fab E of the Performance/AU motherboard.

SPECIFICATION CLARIFICATIONS

1. Corrections to Memory Map Description

Page 15 of the *Performance/AU Motherboard Technical Product Specification* will be modified to reflect the memory regions that are cacheable vs. non-cacheable. Conventional and extended conventional memory (0 to 640-Kbytes) are cacheable. The memory range E0000h - EFFFFh is not cacheable. The range F0000h - FFFFFh is cacheable and write-protected. ROM memory on PCI adapters in the range C0000h - DFFFFh is cacheable, shadowed, and write-protected. ROM memory on ISA adapters is shadowed only. ROM shadow memory within the range C8000h - DFFFFh can be disabled using the ISA Shared Memory Size and Base Address options in BIOS SETUP.

2. Enhanced Parallel Port (EPP) v1.7 Support

References to EPP support on pages 7 and 29 will be modified to reflect the fact that the BIOS initializes the parallel port of the PC87306B Super I/O controller for EPP mode v1.7 when the EPP option is selected via BIOS SETUP.

3. IRQ 12 BIOS Limitation

A note will be added to the *IRQ 3, 4, 5, 7, 9, 10, 11, 12* section on page 31 (Appendix H) to reflect the fact that IRQ 12 cannot be set as the only IRQ "available" for PCI devices - one other IRQ must also be set as "available".

4. Corrections to the "Real Time Clock" Settings

On page 7 of the Performance/AU Motherboard Technical Product Specification in the section "PC87306B Super I/O Controller", "Integrated Real Time clock accurate within +/- 13 minutes/year" will be changed to read "Integrated Real Time clock accurate within +/- 13 minutes/year at 25ºC and 5 volts when the system is continuously powered on."

5. Populating SIMM Banks

The section System Memory (page 5) includes the recommendation, "Optimum performance will be achieved when both banks are populated." When only two SIMM sockets (single bank) are populated the system BIOS will set memory interleave to 1:1. An erratum in the A2 stepping of the 82450KX PCIset prevents inbound write posting from being enabled in 1:1 memory interleaved configurations. A system that makes extensive use of ISA devices that require a high sustained data transfer rate, such as network interface cards, or multiple high bandwidth PCI I/O devices may see lowered I/O performance. When the second SIMM bank is populated, the BIOS will set memory interleaving to 2:1 and enable inbound write posting. For guidelines on configuring the Performance/AU system, please consult the *Pentium® Pro Processor Desktop/Workstation Guide*, available on the World Wide Web at http://pentium.intel.com/procs/support/ppro/82450.htm. For configuration guidelines for network server systems, please consult the *Pentium® Pro Processor Network Server Configuration Guide*, available at http://pentium.intel.com/procs/support/ppro/pproserv.htm.

DOCUMENTATION CHANGES

The Documentation Changes listed in this section apply to the *Performance/AU Motherboard Technical Product Specification* (Order Number 242933-001). All Documentation Changes will be incorporated into a future version of the appropriate Performance/AU motherboard documentation.

1. Refer to Summary Table of Changes

2. ECC Protection for Memory Data Only

Page 6 incorrectly states that ECC protection is provided for Pentium ® Pro processor control signals. The 82454KX PCI Bridge only provides ECC protection for memory data (single-bit correction/double-bit detection).

3. Corrections to Front Panel Connection Drawing

Pages 10 and 19 display a drawing of the front panel connections with incorrect header labels. The header labeled as “Power LED” should actually show no label and the header labeled as “Sleep LED” should be labeled as “Power LED”. Also, the header references to “Sleep Driver” and “Sleep Req” should be deleted.

4. CPU Voltage Override Jumper

Page 14 incorrectly states that the CPU voltage override jumper J29 disables the Pentium Pro processor voltage ID (VID) detection circuitry. Installation of this jumper actually forces the proper VID when versions of the Pentium Pro processor are present that do not support the VID pins. If the processor supports the VID pins, then jumper J29 must be removed in order to supply the proper voltage to the processor.

5. Corrections to Memory Map Description

Page 15 (third paragraph) states that bus cycles are generated when the 512 KB Base Memory option is selected in SETUP and accesses are performed to the 512 to 638-Kbyte memory range. This sentence will be changed to read that ISA bus cycles are performed for accesses to this memory range when the 512 KB option is selected.

The fourth paragraph will be changed to reflect the fact that accesses to the A000h - BFFFh memory range generate either PCI or ISA bus cycles, depending on where the graphics adapter resides. Also, this memory range is not cacheable.

Also, the memory map table (Table C-1) incorrectly indicates the size for the E0000h - E9FFFh memory range as 32-Kbytes instead of the actual 40-Kbytes.

6-8. Refer to Summary Table of Changes

9. PCI Connector Signal Names

Page 23 (Appendix G) should reference the following PCI connector pins as follows:

Pin	Signal Name
A6	PCI INTA#
A7	PCI INTC#
B7	PCI INTB#
B8	PCI INTD#

10. Using the BIOS Upgrade Utility

The first paragraph under the heading *Using The Upgrade Utility* on Page 35 (Appendix K) should read as follows:

If the utility is obtained from the BBS, UNZIP the archive and follow the instructions to create a BIOS upgrade diskette. Reboot the system with the upgrade diskette in the bootable floppy drive, and follow the menu-driven program.