Premiere/PCI

Baby-AT Board & Expandable Desktop
Technical Product Summary

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281604-002

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Table of Contents

Introduction

The Premiere/PCI Expandable Desktop is a state-of-the-art platform delivering the latest Pentium™ microprocessor and I/O technology on an industry-standard Baby-AT form factor motherboard. It is ideal for demanding desktop applications requiring the maximum in I/O expansion flexibility.

A 60 MHz or 66 MHz Pentium microprocessor is complemented by a 256 KB second level write-back cache to provide workstation- level computing performance. A Pentium OverDrive™ socket provides access to future performance enhancements, and SIMM sockets support up to 128 MB of system memory.

The Premiere/PCI Baby-AT motherboard offers outstanding I/O capabilities. Three PCI local bus slots provide a high bandwidth data path for data-intensive functions such as graphics and disk I/O. Integrated peripherals include the RZ1000, which provides a PCI local bus primary IDE interface, as well as the SMC 37C665 Super I/O component, which provides floppy and secondary IDE drive interfaces, two FIFO serial ports and an ECP-capable parallel port. Five ISA slots complete the I/O mix.

STANDARD BABY-AT FORM FACTOR

The Premiere/PCI Baby-AT motherboard conforms to the industry standard Baby-AT form factor. It meets the specifications for maximum board size, board mounting locations, expansion slot placement, and keyboard connector location. In addition to complying to the standard, the Premiere/PCI Baby-AT provides three slots which will accommodate PCI expansion cards.

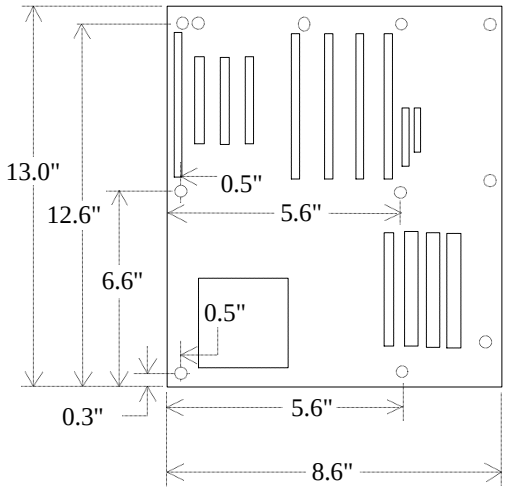
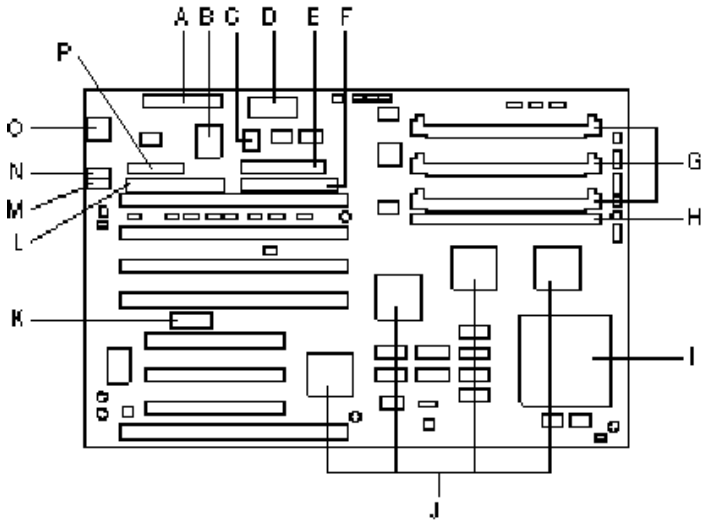


Figure 1. Premiere/PCI Baby-AT Motherboard dimensions.

Board Level Features



A. Power supply connectors
B. Super I/O controller
C. Flash EEPROM containing the BIOS
D. Real-time clock, CMOS RAM, and integral battery
E. Floppy diskette drive connector
F. IDE Connector on ISA bus
G. Angled (low profile) SIMM connectors
H. Vertical SIMM connector
I. Pentium microprocessor
J. Mercury chip set
K. Auxiliary (3.3 v) PCI power connector
L. Parallel connector
M. COM2 (RS232) connector
N. COM1 (RS232) connector
O. Keyboard connector
P. IDE Connector on PCI local bus

Figure 2. Premiere/PCI Baby-AT Motherboard components

CPU

The Premiere/PCI Baby-AT motherboard is designed to operate with either a 60 MHz or 66 MHz Pentium microprocessor. This processor is compatible with the 8086, 80286, i386™ and i486™ CPUs. It supports both read and write burst mode bus cycles, and includes an on-chip 16 KB cache which is split into 8 KB code and 8 KB data caches employing a write-back policy. The Pentium processor also integrates an advanced numeric coprocessor which significantly increases the speed of floating point operations, while maintaining compatibility with i486™DX math coprocessors and complying with ANSI/IEEE standard 754-1985.

Premiere/PCI Baby-AT motherboards equipped with 66 MHz Pentium processors have a voltage control circuit that regulates Vcc to the CPU and frequency synthesizer. The voltage regulation accomodates a variety of Intel CPUs and increases the overall robustness and reliability of the motherboard. Boards without the voltage regulator circuitry cannot reliably use 66 MHz Pentium processors.

The motherboard contains two mounting holes which allow a dedicated fan to be located directly in front of the CPU socket. A 12 volt connector suitable for a CPU fan is located close to the mounting holes.

PERFORMANCE UPGRADE

A 273-pin Type 4 Zero Insertion Force socket provides users with a performance upgrade path using Pentium OverDrive processors. The OverDrive processor being developed for use in this socket will provide performance beyond that delivered by the Pentium microprocessor.

SECOND LEVEL CACHE

The Pentium processor's internal cache is complemented with a 256 KB direct mapped, write-thru second level cache implemented with eight 32Kx8, 15 ns SRAM devices. Tag and control logic is contained in the 82434LX PCMC core chip.

SYSTEM MEMORY

The Premiere/PCI motherboard provides four 72-pin SIMM sites for memory expansion. The sockets support 256K x 36 (1 MB), 512K x 36 (2 MB), 1M x 36 (4 MB), 2M x 36 (8 MB), 4M x 36 (16 MB), and 8M x 36 (32 MB) SIMM modules. Minimum memory size is 2 MB and maximum memory size, using four 8M x 36 SIMM modules, is 128 MB. Memory timing requires 70 ns fast page devices. Parity generation/checking is provided for each byte. Non-parity 32 bit SIMMs also may be used, in which case the parity generation/checking circuitry is automatically disabled.

The four sockets are arranged as Bank A and Bank B, with each bank consisting of two sockets and providing a 64-bit wide data path and 8 parity bits. Both SIMMs in a bank must be of the same memory size and type, although Banks A and B may have different types of memory installed. Bank A only, Bank B only, or both banks may be populated. There are no jumper settings required for the memory size, which is automatically detected by the system BIOS. Tin-lead SIMMs should be used when adding DRAM.

The memory array is controlled by the Intel 82434LX PCMC and data buffering is provided by two Intel 82433LX Local Bus Extension devices.

EXPANSION SLOTS

Up to seven expansion slots may be populated on the Premiere/PCI Baby-AT motherboard. Expansion cards are oriented perpendicular to the motherboard.

There are five ISA bus expansion connectors and three PCI expansion connectors. One slot is shared by connectors that will accommodate either an ISA or a PCI expansion card, but not both at the same time. All three PCI expansion slots accept PCI master cards to fully support the PCI specification.

The motherboard design limits the length of add-in cards in some slots. The height of the CPU heat sink limits the use of the two PCI connectors at J10C1 and J10C2 to less than full-length devices. The length of cards installed in the ISA connector at J10F1 may be limited if a SIMM is installed in the vertical SIMM socket (J3F1). And the location of the serial port header may limit the type of card that can be installed in the ISA connector at J10G1.

PCI 3.3 VOLT CAPABILITIES

To maintain strict compliance with the PCI specification, the motherboard provides a connector which can be used to route 3.3 volt power to the PCI slots. The connector may be used with a separate 3.3 volt power supply or with a custom designed voltage converter.

PERIPHERAL COMPONENT INTERCONNECT (PCI) CHIP SET

The Intel Mercury chip set consists of one 82434LX PCI/Cache/Memory Controller (PCMC), two 82433LX Local Bus eXtension (LBX) devices, and one 82378IB System I/O (SIO) bridge chip. The Mercury chip set provides the following functions:

- CPU reset control
- CPU L1 cache control
- CPU burst mode control
- CPU interface control
- Integrated second level write-back cache controller with tag comparator
- Fast Page-mode DRAM controller
- Burst memory read/write control logic
- Data bus conversion to PCI
- Parity generation/detection to memory
- AT-BUS direction control
- Chip select for keyboard controller and RTC
- Speaker control
- NMI logic
- Floating-point coprocessor interface
- Keyboard reset, gate A20 emulation logic
- DMA controller
- Interrupt controller
- Counters/Timers

82434LX PCI/CACHE/MEMORY CONTROLLER (PCMC)

The 82434LX provides all control signals necessary to drive a second level cache and the DRAM array, including multiplexed address signals. It also controls system access to memory and generates snoop controls to maintain cache coherency.

82433LX LOCAL BUS EXTENSION (LBX)

There are two 82433LX components which provide data bus buffering and dual port buffering to the memory array. Controlled by the 82434LX, the 82433LX devices add one load each to the PCI bus and perform all the necessary byte and word swapping. The devices include memory and I/O write buffers.

82378IB SYSTEM I/O (SIO)

The 82378IB integrates seven 32-bit DMA channels, five 16-bit timer/counters, two eight-channel interrupt controllers, NMI logic, ISA refresh address generation, and PCI/ISA bus arbitration circuitry together onto the same device.

Detailed information on the chip set is available in the Intel 82430 PCISet data sheet.

RZ1000 PCI IDE INTERFACE

The Premiere/PCI Baby-AT motherboard offers two IDE channels: one on the PCI local bus and one on the ISA bus. PCI-based IDE provides performance much improved over the traditional ISA-based IDE.

PCI TO IDE INTERFACE CIRCUIT

An onboard PCI to IDE interface is provided by the PCTech RZ1000 component and a specially-tuned system BIOS, which is fully compatible with existing IDE software. The RZ1000 provides a 32-bit buffered interface to two IDE drives, allowing these drives to be accessed at full PCI bandwidth. The component also supports Enhanced IDE Mode 3 timing, allowing the drive to transfer data at its full bandwidth. The system BIOS provides transparent access to these features, as well as support for Logical Block Addressing (LBA) which allows the use of drives larger than 528 MB. The PCI IDE interface functions as the primary interface using Interrupt 14. A sdecondary IDE interface (IRQ15) is provided by the SMC 37C665 I/O controller.

IDE PHYSICAL INTERFACE

The PCI IDE physical interface consists of a dedicated 40-pin header connector (J11F1). A separate 40-pin connector is dedicated to the SMC 37C655 IDE interface. When the on-board IDE controllers are enabled, the RZ1000 is the primary interface and the ISA IDE controller is the secondary interface.

SMC 37C665 SUPER I/O CONTROLLER

Control for the integrated serial ports, parallel port, floppy drive and IDE hard drive interface is incorporated into a single component, the SMC FDC37C665. This component provides:

- Two NS16C552-compatible UARTs with send/receive 16 byte FIFO
- Multi-mode bi-directional parallel port
  - Standard mode; IBM* and Centronics compatible
  - Enhanced Parallel Port (EPP) with BIOS/Driver support
  - High Speed mode; Extended Capabilities Port (ECP) compatible
- Industry standard floppy controller with 16 byte data FIFO (2.88 MB floppy support)
- IDE hard disk decode and chip select

Header pins located near the back of the board allow cabling to use these interfaces. The serial ports can be enabled as COM1 and COM2, or disabled. The parallel port can be configured via the Setup program as LPT1 or disabled, and can be set as bi-directional or output only when enabled. The IDE interface supports standard, Type B, and Type F DMA.

KEYBOARD INTERFACE

An Intel 8742 surface mount microcontroller contains the Phoenix Technologies-compatible keyboard/mouse controller code. An AT-style keyboard connector is located on the back panel side of the motherboard. The 5V line on this connector is protected with a PolySwitch* circuit which acts much like a self-healing fuse, re-establishing the connection after an over-current condition is removed. While this device eliminates the possibility of having to replace a fuse, care should be taken to turn off the system power before installing or removing a keyboard.

The 8742 microcontroller code supports Power-On/Reset (POR) password protection. The POR password is set via the Setup program. The keyboard controller also provides for the following "hot key" sequences:

- CTRL-ALT-DEL: System software reset. This sequence performs a software reset of the system by jumping to the beginning of the BIOS code and running the POST operation.
- CTRL-ALT+ and CTRL-ALT-: Turbo mode selection. CTRL-ALT- sets the system for de-turbo mode (emulation of an 8 MHz 80286 CPU) and CTRL-ALT+ sets the system for turbo mode (normal operation at 60 MHz). Changing the Turbo mode may be prohibited by an operating system or application software. For example, the CPU speed cannot be changed with the hot keys when the CPU is in Protected Mode.

DALLAS DS12887 REAL TIME CLOCK, CMOS RAM AND BATTERY

The Real Time Clock (RTC) is implemented using a Dallas DS12887 device. The DS12887 is accurate to within 13 minutes/year and requires no external support (the battery and oscillator are integrated into the device). The internal battery has an estimated lifetime of ten years.

The RTC can be set via the BIOS SETUP Program. CMOS memory supports the standard 128-byte battery-backed RAM, fourteen bytes for clock and control registers, and 114 bytes of general purpose non-volatile CMOS RAM. All CMOS RAM is reserved for BIOS use. The CMOS RAM can be set to specific values or cleared to the system default values using the BIOS SETUP program. Also, the CMOS RAM values can be cleared to the system defaults by using a hardware jumper. Appendix B lists jumper configurations.

SYSTEM BIOS

The Premiere/PCI Baby-AT motherboard uses an American Megatrends Incorporated (AMI) ROM BIOS, which is stored in Flash EEPROM and easily upgraded using a floppy disk-based program. BIOS upgrades will be available for download from the Intel bulletin board system. In addition to the AMIBIOS, the Flash EEPROM also contains the Setup utility, Power-On Self Tests (POST), update recovery code, and the PCI auto-configuration utility. This motherboard supports system BIOS shadowing, allowing the BIOS to execute from 32-bit on-board write-protected DRAM.

The BIOS displays a sign-on message during POST identifying the type of BIOS and a five-digit revision code. First production units will display a revision code of 1.00.01.AF2 As BIOS updates occur, the revision number will increase to 1.00.02.AF2, and so on.

Information on BIOS functions can be found in the IBM PS/2 and Personal Computer BIOS Technical Reference published by IBM, and the ISA and EISA Hi-Flex AMIBIOS Technical Reference published by AMI. Both manuals are available at most technical bookstores.

FLASH IMPLEMENTATION

The Intel 28F001BXT 1 Mb FLASH component is organized as 128K x 8 (128 KB). The Flash device is divided into five areas, as described in Table 1.

System Address		*FLASH Memory Area*
F0000H	FFFFFH	64 KB Main BIOS
EE000H	EFFFFH	8 KB Boot Block (Not FLASH erasable)
ED000H	EDFFFH	4 KB OEM LOGO Area
E8000H	ECFFFH	20 KB System BIOS Reserved
E0000H	E7FFFH	32 KB Not Used

Table 1. Flash Memory Organization

The FLASH device resides in system memory in two 64 KB segments starting at E0000H, and can be mapped two different ways, depending on the mode of operation. In *Normal Mode,* address line A16 is inverted, setting the E000H and F000H segments so that the BIOS is organized as shown in the system address column above. *Recovery mode* removes the inversion on address line A16, swapping the E000H and F000H segments so that the 8 KB boot block resides at FE000H where the CPU expects the bootstrap loader to exist. This mode is only necessary in the unlikely event that a BIOS upgrade procedure is interrupted, causing the BIOS area to be left in an unusable state. For information on recovering the BIOS in the event of a catastrophic failure, refer to Appendix E.

BIOS UPGRADES

Flash memory makes distributing BIOS upgrades easy. A new version of the BIOS can be installed from a diskette. BIOS upgrades will be available for download from the bulletin board system.

The disk-based Flash upgrade utility (FMUP.EXE) has three options for BIOS upgrades:

- The Flash BIOS can be updated from a file on a disk;
- The current BIOS code can be copied from the Flash EEPROM to a disk file as a backup in the event that an upgrade cannot be successfully completed; or
- The BIOS in the Flash device can be compared with a disk file to ensure the system has the correct BIOS version.

The upgrade utility ensures the upgrade BIOS matches the target system to prevent accidentally installing a BIOS for a different type of system. Security to prevent unauthorized changes to the BIOS is provided via a write-protect jumper. The default setting is to allow BIOS upgrades. A recovery jumper is provided to allow recovery in the unlikely event of an unsuccessful BIOS upgrade. The jumper forces the ROM decode to access an 8 KB block of write protected recovery code in the Flash device.

SETUP UTILITY

The ROM-based Setup utility allows the configuration to be modified without opening the system for most basic changes. The Premiere/PCI Baby-AT motherboard also incorporates many new capabilities into the Flash EEPROM, including:

- Auto configuration of IDE hard disks (manual selection of the drive type is no longer required).
- Support for two IDE disk interfaces (primary and secondary) providing access to 4 IDE devices (when a second IDE controller is added on the PCI or ISA bus).
- An option allowing the user to assign a block of addresses below the 1 MB boundary as non-shadowed, non-cached. This area is primarily used for expansion card ROM which causes timing problems when shadowed and cached.
- ISA interrupts IRQ9, IRQ10 and IRQ11 may be assigned to add-in card ISA adapters, thereby informing the PCI configuration utility which interrupts not to use.

The Setup utility is accessible only during the Power-On Self Test (POST) by pressing the <DEL> or <F1> key after the POST memory test has begun and before boot begins. A prompt may be enabled that informs users to press the <F1> key to access Setup. A motherboard jumper can be set to prevent user access to Setup for security purposes. Setup options are detailed in Appendix C.

PCI AUTO-CONFIGURATION CAPABILITY

The PCI auto-configuration utility operates in conjunction with the system Setup utility to allow the insertion and removal of PCI cards to the system without user intervention. When the system is turned on after adding a PCI add-in card, the BIOS automatically configures interrupts, I/O space, and other parameters. The user does not have to configure jumpers or worry about potential resource conflicts. Because PCI cards use the same interrupt resources as ISA cards, the user must specify the interrupts used by ISA add-in cards in the Setup utility. The PCI Auto-Configuration function complies with version 2.0G of the PCI BIOS specification.

SECURITY FEATURES

BIOS Password

A BIOS password feature provides security during the boot process. A password can be entered using the Setup utility and must be re-entered prior to disk boot each time the system is reset. To enable, disable, or change the password, refer to the Setup program options in Appendix C.

If the password is forgotten, it can be cleared by turning off the system and setting the "password clear" jumper to the clear position.

Setup Enable Jumper

A baseboard jumper controls access to the BIOS Setup utility. By setting jumper to the disable position, the user is prevented from accessing the Setup utility at any time.

CONNECTORS

FRONT PANEL CONNECTIONS

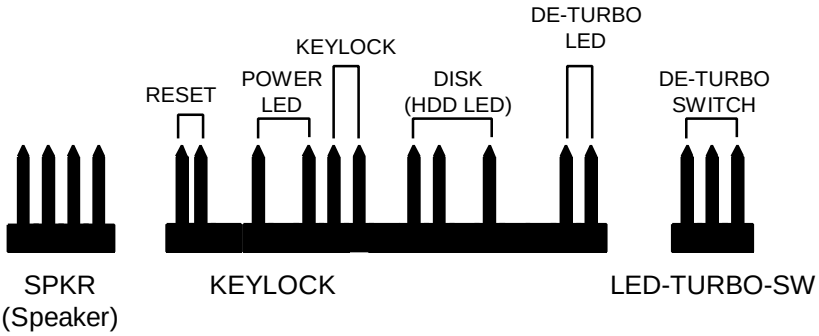


Figure 3: Front Panel Connectors

Figure 3 shows connectors provided on the motherboard for various functions. See Appendix I for the pin assignments.

The external speaker provides error beep code information during the Power-On Self Test if the system cannot use the video interface. See Appendix D - AMIBIOS Error Messages and Beep Codes for more information about error beep codes.

BACK PANEL CONNECTIONS

The Premiere/PCI Baby-AT includes an AT-style keyboard connector integrated on the back panel side of the motherboard.

I/O CONNECTIONS

The motherboard contains stake pin header connections for cabling the serial, parallel, floppy, and IDE interfaces. Figure 4 shows the locations of these connectors, orientation of pin 1 on each, the numbering of each connector, and for IDE and Floppy, the missing key pin.

Fast Fan is the default connection and provides 12V power for operating the fan. For slower and quieter fan operation (less cooling), the Slow Fan connector provides 10V power.

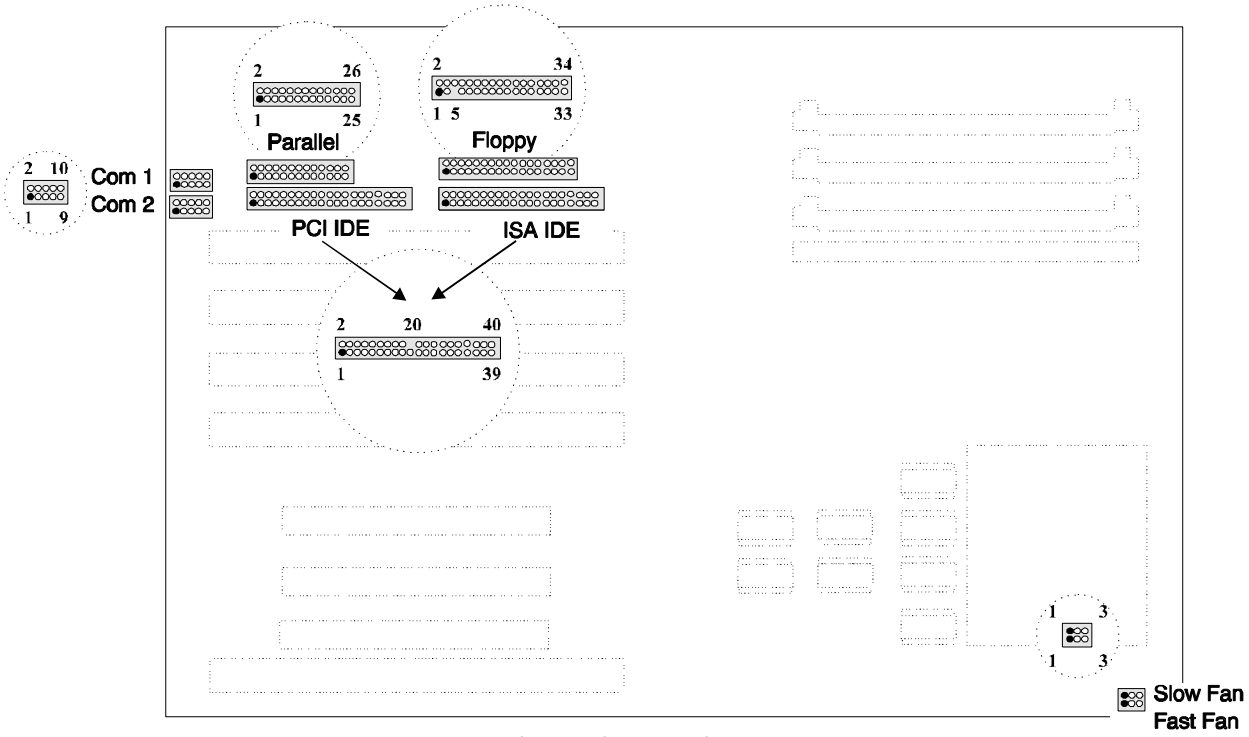


Figure 4. I/O Connections

System Level Features

CHASSIS

The Premiere/PCI Expandable Desktop easily provides the expandability required for most traditional PC applications – seven peripheral bays, seven expansion slots, an ample 200 watt power supply and an additional fan located at the front left side of the chassis to help keep the system cool. The user can access five of the peripheral bays from the front of the chassis. The Premiere/PCI Expandable Desktop also meets stringent environmental requirements.

PERIPHERAL BAYS

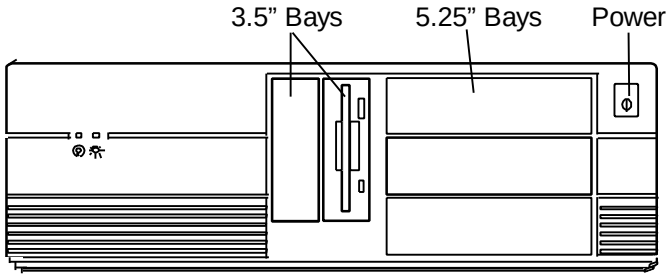


Figure 5: Premiere/PCI Expandable Desktop Front Panel

Seven expansion bays are available for peripherals and other add-in devices. These include three 5¼" half-height bays and two 3½" one-inch bays that are accessible from the front panel. Two internal 3½" peripheral bays are located above the power supply.

FAN

The Premiere/PCI Expandable Desktop has two fans to keep the system cool. One fan within the power supply provides 28 cfm of air movement. The second fan, located behind the card guide, provides 26 cfm across the add-in cards and the CPU. The second fan receives 12 Vdc directly from the baseboard at stake pin location J1D1.

EXPANSION SLOTS

The Premiere/PCI Expandable Desktop has seven expansion card slots, as shown in Figure 6. Several of the slots are intended for use with less than full-length cards. One ISA slot is limited in length by the 3½" peripheral bay carrier, one ISA card slot is limited in length by the left-most SIMM socket, two ISA card slots are full length, two PCI slots are limited in length by the CPU heatsink, and one is a full length shared slot, accepting either an ISA or a PCI expansion card.

FRONT PANEL

The Premiere/PCI Expandable Desktop front panel consists of a power switch, a power-on LED and a hard disk access LED. Five peripheral bays also can be accessed from the front panel, as shown in Figure 5.

BACK PANEL

The back panel consists of access panels for the expansion slots (one location is unused), two DB9 RS-232 serial ports, a bi-directional parallel port, an AT-style keyboard connector, a 115/230 voltage switch, a power supply input, an auxiliary power output and the power supply fan. Punch-out locations also are provided for adding a second parallel port and a SCSI-2 connector.

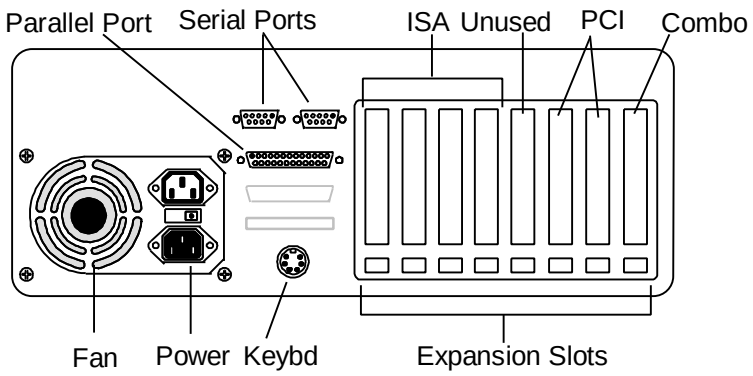


Figure 6. Premiere/PCI Expandable Desktop Back Panel.

POWER SUPPLY

The Premiere/PCI Expandable Desktop integrates a 200 watt switchable power supply for all onboard resources, add-in cards, and peripherals. The Astec Corp. model SA201-3440 supports operating settings at 100-120 VAC (5 Amps AC) or 200-240 VAC (3 Amps AC). The input voltage is selected using a switch on the back of the system.

AC POWER INPUT SPECIFICATIONS

Input frequency 50/60 Hz	
AC Voltage	*Current*
90-135	5.0 A
180-265	3.0 A

Table 2. Power Supply Input Specifications.

DC OUTPUT SPECIFICATIONS

DC Voltage	*Max. Continuous Current*	*Peak Current 15 Seconds*	*Minimum Current Load*
+5V	22.0A	-	3.0A
-5V	0.5A	-	0A
+12V	8.0A	9.0 A	0A
-12V	0.5A	-	0A

Table 3. Power Supply DC Output Specifications.

POWER CONSUMPTION

Table 4 lists the current used by system resources in a configuration which includes 8 MB of DRAM. Table 5 lists the typical power consumed by the same configuration. This information is preliminary and is provided only as a guide for calculating approximate total system power usage with additional resources added.

CURRENT

DC Voltage	*Max. Continuous Current*	*Peak Current 15 Seconds*	*Minimum Current Load*
+5V	18.5A	18.5	2.5A
-5V	0.9A	0.9A	0A
+12V	4.6A	9.5A	0.5A
-12V	0.5A	0.5A	0A

Table 4. Premiere/PCI Expandable Desktop Current Requirements (Preliminary)

WATTS

Resource	*Typical Power*
Premiere/PCI Expandable Desktop baseboard, 8 MB , 256 KB cache	50 watts
Teac 3½" Floppy drive	1.7 watts

Table 5. Current Use by System Resources (Preliminary)

FLOPPY DRIVE

The Premiere/PCI Expandable Desktop integrates a 3½" Teac Floppy drive Model FD-235HF into the right 3½" bay. This is the same proven floppy disk drive that has been used on many previous Intel systems.

SPEAKER

The standard system ships with an external speaker installed. The user may enable/disable the device using the Setup utility or program the speaker via port 61H. The speaker provides error beep code information during POST if the system cannot use the video interface. The Premierec/PCI Expandable Desktop product guide (order # 616545) contains detailed beep and error code information.

CHASSIS COLOR

The chassis color is beige. The bottom and back of the chassis are not painted.

Premiere/PCI OmniRACK Chassis

The Premiere/PCI Baby-AT motherboard also is available in Intel's OmniRACK rackmountable chassis. OmniRACK can be used in an industry-standard REA 19-inch equipment rack or as an embedded microcomputer. Premiere/PCI OmniRACK offers a 230 watt power supply with temperature-controlled internal cooling fans. The system contains four peripheral bays (two 5¼" x 1.6", one 3½" x 1.6", and one 3½" x 1") housed in a removable drive cage. For more information on the OmniRack chassis, see the OmniRACK Technical Product Summary, available from Intel Literature or the bulletin board system.

The order code for the Premiere/PCI OmniRACK product is ORP605P8.

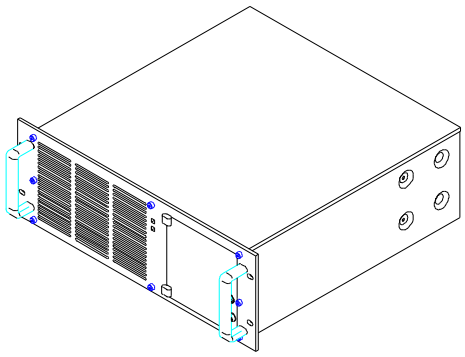


Figure 7. OmniRACK Chassis with access door closed

Appendix A - User-Installable Upgrades

SYSTEM MEMORY

Table A-1 shows the possible memory combinations. The Premiere/PCI Baby-AT motherboard supports both parity and non-parity SIMMs, but they cannot be mixed within the same memory bank. SIMM requirements are 70ns, Fast Page Mode, with tin-lead connectors.

SIMM 1,2 (Bank 0) SIMM Type (Amount)	*SIMM 3,4 (Bank 1) SIMM Type (Amount)*	*Total System Memory*
256K X 36 (1 MB)	Empty	2 MB
256K X 36 (1 MB)	256K X 36 (1 MB)	4 MB
256K X 36 (1 MB)	512K X 36 (2 MB)	6 MB
256K X 36 (1 MB)	1M X 36 (4 MB)	10 MB
256K X 36 (1 MB)	2M X 36 (8 MB)	18 MB
256K X 36 (1 MB)	4M X 36 (16 MB)	34 MB
256K X 36 (1 MB)	8M X 36 (32 MB)	66 MB
512K X 36 (2 MB)	Empty	4 MB
512K X 36 (2 MB)	256K X 36 (1 MB)	6 MB
512K X 36 (2 MB)	512K X 36 (2 MB)	8 MB
512K X 36 (2 MB)	1M X 36 (4 MB)	12 MB
512K X 36 (2 MB)	2M X 36 (8 MB)	20 MB
512K X 36 (2 MB)	4M X 36 (16 MB)	36 MB
512K X 36 (2 MB)	8M X 36 (32 MB)	68 MB
1M X 36 (4 MB)	Empty	8 MB
1M X 36 (4 MB)	256K X 36 (1 MB)	10 MB
1M X 36 (4 MB)	512K X 36 (2 MB)	12 MB
1M X 36 (4 MB)	1M X 36 (4 MB)	16 MB
1M X 36 (4 MB)	2M X 36 (8 MB)	24 MB
1M X 36 (4 MB)	4M X 36 (16 MB)	40 MB
1M X 36 (4 MB)	8M X 36 (32 MB)	72 MB
2M X 36 (8 MB)	Empty	16 MB
2M X 36 (8 MB)	256K X 36 (1 MB)	18 MB
2M X 36 (8 MB)	512K X 36 (2 MB)	20 MB
2M X 36 (8 MB)	1M X 36 (4 MB)	24 MB
2M X 36 (8 MB)	2M X 36 (8 MB)	32 MB
2M X 36 (8 MB)	4M X 36 (16 MB)	48 MB
2M X 36 (8 MB)	8M X 36 (32 MB)	80 MB
4M X 36 (16 MB)	Empty	32 MB
4M X 36 (16 MB)	256K X 36 (1 MB)	34 MB
4M X 36 (16 MB)	512K X 36 (2 MB)	36 MB
4M X 36 (16 MB)	1M X 36 (4 MB)	40 MB
4M X 36 (16 MB)	2M X 36 (8 MB)	48 MB
4M X 36 (16 MB)	4M X 36 (16 MB)	64 MB
4M X 36 (16 MB)	8M X 36 (32 MB)	96 MB
8M X 36 (32 MB)	Empty	64 MB
8M X 36 (32 MB)	256K X 36 (1 MB)	66 MB
8M X 36 (32 MB)	512K X 36 (2 MB)	68 MB
8M X 36 (32 MB)	1M X 36 (4 MB)	72 MB
8M X 36 (32 MB)	2M X 36 (8 MB)	80 MB
8M X 36 (32 MB)	4M X 36 (16 MB)	96 MB
8M X 36 (32 MB)	8M X 36 (32 MB)	128 MB

Table A-1. Possible SIMM Memory Combinations

Appendix B - Jumpers

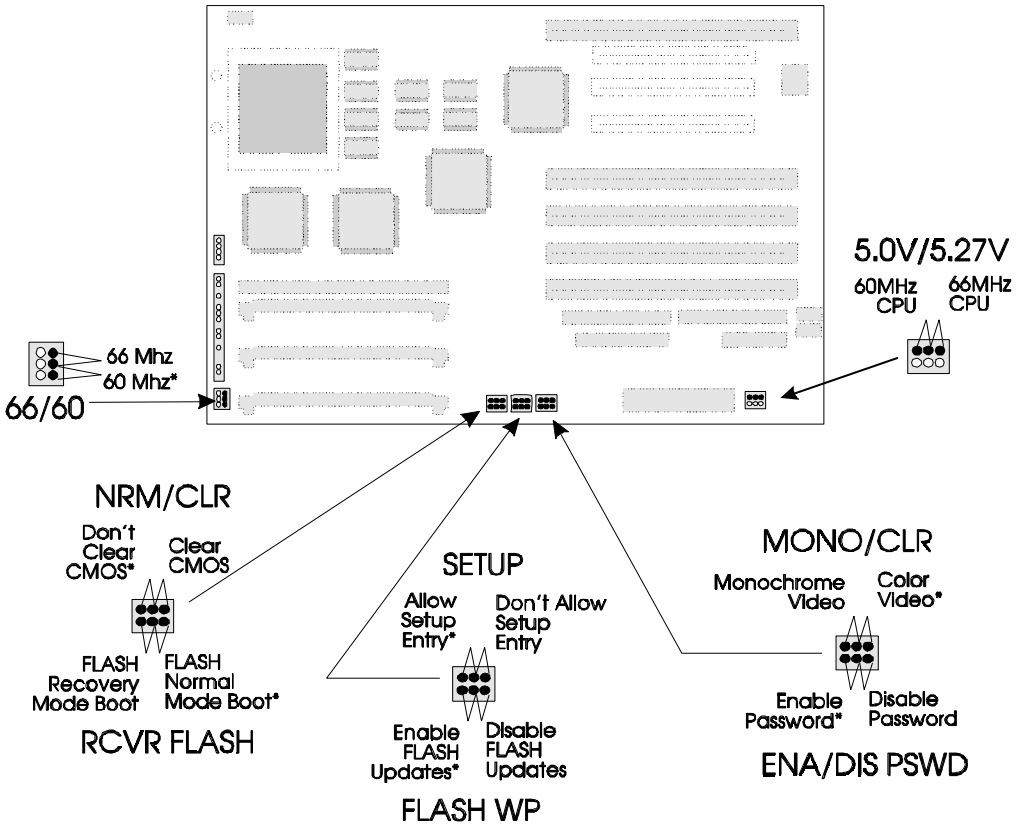


Figure B-1. Jumper locations and settings (*denotes default setting)

66/60

This jumper is set at the factory for the appropriate CPU clock frequency and may not be changed by the user. If changed from the factory setting, improper operation may result.

FLASH RECOVERY (RCVR FLASH)

Allows recovery if the system FLASH update process results in corrupted EPROM.

CLEAR CMOS (NRM/CLR)

Allows CMOS settings to be reset to default values.

SETUP ENABLE (SETUP)

Allows access to CMOS Setup Utility to be disabled.

FLASH WRITE PROTECT (FLASH WP)

Allows reprogramming of FLASH EPROM to be disabled.

COLOR/MONO (MONO/CLR)

Chooses Monochrome or Color video mode at boot.

PASSWORD CLEAR (ENA/DIS PSWD)

Allows system password to be cleared.

VOLTAGE CONTROL (5.0V/5.27V)

Set at the factory to regulates CPU voltage at 5.0V for 60 MHz Pentium processor or 5.27V for 66 MHz Pentium processor. Improper operation may result if the factory setting is changed.

Appendix C - AMIBIOS Setup

ENTERING THE SETUP PROGRAM

Press and hold the <DEL> or <F1> key during the power-up sequence. Figure C-1 shows the first screen.

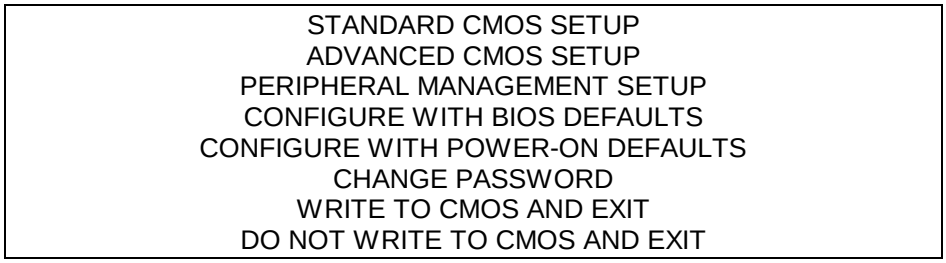


Figure C-1. Opening Screen on Entering Setup Program

OVERVIEW OF SELECTIONS

STANDARD CMOS SETUP

Allows the user to modify basic options for the PC, such as time, date, floppies, hard drives and keyboard.

ADVANCED CMOS SETUP

Allows the user to modify more advanced features, including enabling or disabling parity checking, cache, numlock, shadowing, IDE DMA transfer modes, ISA interrupts, and ISA linear frame buffer.

PERIPHERAL MANAGEMENT SETUP

Allows the user to modify the peripheral options associated with the SMC37C665 I/O controller, including serial and parallel port addresses.

CONFIGURE WITH BIOS DEFAULTS

Reloads CMOS with default values from the ROM table.

CONFIGURE WITH POWER-ON DEFAULTS

Reloads CMOS with power-up values.

CHANGE PASSWORD

Allows the user to specify a password that will be needed to enter the Setup program or boot DOS. Once the password is specified, it can be changed, deleted or disabled using this utility. To delete or disable the password function, simply enter a carriage return instead of a new password. If the password is forgotten, a jumper on the board can be moved to clear the password (see Appendix B – Jumpers).

WRITE TO CMOS AND EXIT

Saves the configuration and any changes made to CMOS.

DO NOT WRITE TO CMOS AND EXIT

Allows the user to exit the setup utility without saving any configuration changes to CMOS.

STANDARD CMOS SETUP

DATE	Specify the current date
TIME	Specify the current time
Floppy Drive A:	If present, select the size and type
Floppy Drive B:	If present, select the size and type
Drive C: Type	There are three choices for configuring an IDE hard drive: • Auto Configure; the BIOS will automatically sense the hard drive in the system and configure it appropriately • User Type 1; allows the user to explicitly configure the hard drive in the event the hard drive in the system does not support the identify drive command needed to support auto-configuration • User Type 2; Same as user type 1
Drive D: Type	Support for multiple IDE drives. Same options as Drive C:
Drive E: Type	Support for multiple IDE drives. Same options as Drive C:
Drive F: Type	Support for multiple IDE drives. Same options as Drive C:
Drive C: Time-out	Time-out specification for the IDE auto-configuration. If the drive does not auto-configure in this amount of time, there will be an error message. Default is 5 seconds. Choices are 0, 5, 15, and 31 seconds.
Drive D: Time-out	Same as the Drive C: Time-out description
Drive E: Time-out	Same as the Drive C: Time-out description
Drive F: Time-out	Same as the Drive C: Time-out description (note: to decrease the time required for boot-up, set all unused drives to o)
Keyboard	Installed or Not Installed. Default is Installed.
Base Memory	Reports the amount of base memory. There are no options.
Extended Memory	Reports the amount of extended memory. There are no options.

ADVANCED CMOS SETUP

Typematic Rate Programming	Enabled or Disabled. Default is disabled. When enabled, the following two typematic options are valid.
Typematic Rate Delay (msec.)	250, 500, 750 or 1000 millisecond delay. Default is 500. Determines how long it takes for the auto-repeat function to start when a person is holding down a key on the keyboard.
Typematic Rate (Chars/sec)	6, 30, 24, 20, 15, 12, 10 or 8 characters/second. Default is 15. Determines the speed at which characters repeat when you hold down a key on the keyboard. The higher the number, the faster the repeat.
Press <F1> Message Display	Enabled or Disabled. Default is enabled. The message "Hit <F1> to Enter Setup" appears on the screen during the power up sequence.
System Boot Up Num Lock	On or Off. Default is off, reflecting the state of the "Num Lock" keyboard feature when the system boots.
System Boot Up Sequence	Drive A: before C:, Drive C: before A:, or Drive C: Only. Default is to check Drive A: before C: for an operating system, which allows the user to boot from a floppy if necessary.
System Boot Up CPU Speed	High or Low. Default is High. If high is selected, boot up will occur at full speed. If low is selected, the board is put into de-turbo mode, which results in slower operation.
Cache Memory	Enabled or Disabled. Default is enabled. Both the L1 and L2 cache are enabled or disabled by this selection.
Network Password Checking	Enabled or Disabled. Default is disabled. If enabled, the system will complete the entire boot-up process, but the keyboard will remain locked until the password sequence is typed.
ISA Linear Frame Buffer	Disabled, 1 MB, 2 MB, or 4 MB. Default is disabled. The linear frame buffer is primarily for ISA video cards. If enabled, improvement may be noted in performance of ISA video cards using the linear frame buffer. It also provides a means to access memory located on the ISA bus immediately below 16MB.

ADVANCED CMOS SETUP (CONTINUED)

Set Linear Frame Address to	When you enable the ISA linear frame buffer, this entry is displayed automatically. When you disable the linear frame buffer, this entry becomes N/A.
Disable Shadow Memory Size	Enabled or Disabled. Default is disabled. This selection is tied to the next selection "Disable Shadow Memory Base". If the shadow memory base is set to either C0000H or D0000H, then you can select a shadow memory size of either 16, 32, 48, or 64 KBytes.
Disable Shadow Memory Base	This selection allows the user to alter where the non-shadowed memory is located. The choices are either in the C0000H or D0000H range. There are several options within each range. For example, within the C0000H range you can choose C0000H, C4000H, C8000H, or CC000H. This setting effects the previous menu selection. Once you have made your selection in this menu your choices in the previous menu "Disable Shadow Memory Size" may be altered. The maximum size of the shadow memory is 64KB. You can only achieve 64kB if you specify the Shadow Memory Base to be at C0000H or D0000H. As you select the other shadow memory base options, you will notice that the shadow memory size begins to get smaller.
Base Memory Size	640/512. Default is 640KB. Provides a means to disable on-bd DRAM to access memory locations from 80000-9FFFFH on the ISA bus.
IDE DMA Transfer Mode	Default is disabled. When enabled, the user can choose from 3 different types of IDE DMA transfers: Standard (compatible), Type B, or Type F. Type F is the fastest DMA transfer mode.
IDE Multiple Sector Mode	Default is disabled and this selection is tied to the previous selection (IDE DMA Transfer Mode). When enabled, choices are 1, 2, 4, 8, 16, 32, or 64 sectors per burst (S/B). This setting programs the IDE DMA cycles to transfer multiple sectors per burst. A setting of 64 S/B assures the maximum burst size supported by the drive that is installed in the system.
Enhanced ISA Timing	Enabled or Disabled. Default is disabled. When enabled, the ISA bus will run at 10 MHz. This results in faster system performance if the ISA agents in the system can tolerate 10 MHz (instead of the standard 8 MHz).
IDE LBA Translations	Enabled or Disabled. Default is disabled. When enabled, supports Logical Block Addressing to allow full utilization of drives larger than 528 MB.
ISA IRQ 9	Free or Used. If an ISA agent in the system uses this interrupt, it must be specified here as used. The PCI auto-configuration code checks this entry and may attempt to use the interrupt is it is free.
ISA IRQ 10	Free or Used. If an ISA agent in the system uses this interrupt, it must be specified here as used. The PCI auto-configuration code checks this entry and may attempt to use the interrupt is it is free.
ISA IRQ 11	Free or Used. If an ISA agent in the system uses this interrupt, it must be specified here as used. The PCI auto-configuration code checks this entry and may attempt to use the interrupt is it is free.

PERIPHERAL MANAGEMENT SETUP

Programming option	Auto or Manual. Default is Auto, meaning that the peripherals controlled by the SMC665 I/O component are automatically configured during power up. If Auto is selected, the following menu options have no effect. If Manual is selected, settings must be entered for all of the following peripherals.
On-Board Floppy Drive	Enabled or disabled.
On-Board IDE drive	Enabled or disabled.
First Serial Port Address	Disabled, 2E8H, 3E8H, 2F8H, or 3F8H. The address is automatically set in auto programming mode, although this entry will show "disabled"
Second Serial Port Address	Disabled, 2E8H, 3E8H, 2F8H, or 3F8H. The address is automatically set in auto programming mode, although this entry will show "disabled"
Parallel Port Address	Disabled, 278H, 378H, or 3BCH. The address is automatically set in auto programming mode, although this entry will show "disabled"
Parallel Port Mode	Normal or Extended. Default is normal. Extended enables the port for bi-directional operation.

Appendix D - AMIBIOS Error messages and Beep Codes

Errors can occur during POST (Power On Self Test) which is performed every time the system is powered on. Fatal errors, which prevent the system to continue the boot process, are communicated through a series of audible beeps. Other errors are displayed in the following format:

ERROR *Message Line 1*

ERROR *Message Line 2*

For most displayed error messages, there is only one message. If a second message appears, it is "RUN SETUP". If this message occurs, press <F1> to run AMIBIOS Setup.

BEEP CODES

Beeps	*Error Message*	*Description*
1	Refresh Failure	The memory refresh circuitry on the motherboard is faulty.
2	Parity Error	Parity error in the first 64 KB of memory.
3	Base 64 KB Memory Failure	Memory failure in the first 64 KB.
4	Timer Not Operational	Memory failure in the first 64 KB of memory, or Timer 1 on the motherboard is not functioning.
5	Processor Error	The CPU on the motherboard generated an error.
6	8042 - Gate A20 Failure	The keyboard controller (8042) may be bad. The BIOS cannot switch to protected mode.
7	Processor Exception Interrupt Error	The CPU generated an exception interrupt.
8	Display Memory Read/Write Error	The system video adapter is either missing or its memory is faulty. This is not a fatal error.
9	ROM Checksum Error	ROM checksum value does not match the value encoded in BIOS.
10	CMOS Shutdown Register Rd/Wrt Error	The shutdown register for CMOS RAM failed.
11	Cache Error / External Cache Bad	The external cache is faulty.

ERROR MESSAGES

Error Message	*Explanation*
8042 Gate - A20 Error	Gate A20 on the keyboard controller (8042) is not working. Replace the 8042.
Address Line Short!	Error in the address decoding circuitry on the motherboard.
Cache Memory Bad, Do Not Enable Cache!	Cache memory is defective. Replace it.
CH-2 Timer Error	Most AT systems include two timers. There is an error in timer 2.
CMOS Battery State Low	CMOS RAM is powered by a battery. The battery power is low. Replace the battery.
CMOS Checksum Failure	After CMOS RAM values are saved, a checksum value is generated for error checking. The previous value is different from the current value. Run AMIBIOS Setup.
CMOS System Options Not Set	The values stored in CMOS RAM are either corrupt or nonexistent. Run Setup.
CMOS Display Type Mismatch	The video type in CMOS RAM does not match the type detected by the BIOS. Run AMIBIOS Setup.
CMOS Memory Size Mismatch	The amount of memory on the motherboard is different than the amount in CMOS RAM. Run AMIBIOS Setup.

ERROR MESSAGES (CONT.)

CMOS Time and Date Not Set	Run Standard CMOS Setup to set the date and time in CMOS RAM.
Diskette Boot Failure	The boot disk in floppy drive A: is corrupt. It cannot be used to boot the system. Use another boot disk and follow the screen instructions.
Display Switch Not Proper	Some systems require a video switch on the motherboard be set to either color or monochrome. Turn the system off, set the switch, then power on.
DMA Error	Error in the DMA controller.
DMA #1 Error	Error in the first DMA channel.
DMA #2 Error	Error in the second DMA channel.
FDD Controller Failure	The BIOS cannot communicate with the floppy disk drive controller. Check all appropriate connections after the system is powered down.
HDD Controller Failure	The BIOS cannot communicate with the hard disk drive controller. Check all appropriate connections after the system is powered down.
INTR #1 Error	Interrupt channel 1 failed POST.
INTR #2 Error	Interrupt channel 2 failed POST.
Invalid Boot Diskette	The BIOS can read the disk in floppy drive A:, but cannot boot the system. Use another boot disk.
Keyboard Is Locked...Unlock It	The keyboard lock on the system is engaged. The system must be unlocked to continue.
Keyboard Error	There is a timing problem with the keyboard. Set the *Keyboard* option in Standard CMOS Setup to *Not Installed* to skip the keyboard POST routines.
KB/Interface Error	There is an error in the keyboard connector.
Off Board Parity Error	Parity error in memory installed in an expansion slot. The format is: OFF BOARD PARITY ERROR ADDR (HEX) = (XXXX) *XXXX* is the hex address where the error occurred.
On Board Parity Error	Parity error in motherboard memory. The format is: OFF BOARD PARITY ERROR ADDR (HEX) = (XXXX) *XXXX* is the hex address where the error occurred.
Parity Error ????	Parity error in system memory at an unknown address.

ISA NMI MESSAGES

ISA NMI Message	*Explanation*
Memory Parity Error at *xxxxx*	Memory failed. If the memory location can be determined, it is displayed as *xxxxx*. If not, the message is *Memory Parity Error ????*.
I/O Card Parity Error at *xxxxx*	An expansion card failed. If the address can be determined, it is displayed as *xxxxx*. If not, the message is *I/O Card Parity Error ????*.
DMA Bus Time-out	A device has driven the bus signal for more than 7.8 microseconds.

Appendix E - BIOS Upgrades and Recovery

The Premiere/PCI Baby-AT motherboard incorporates the AMIBIOS in a Flash memory component. Flash BIOS allows easy upgrades without the need to replace an EPROM. The upgrade utility fits on a floppy diskette and provides the capability to save, verify, and update the system BIOS. The upgrade utility can be run from a hard drive or a network drive, but no memory managers can be installed during upgrades.

The latest upgrade utility and BIOS code are available in the *BIOS* section of the Intel bulletin board.

USING THE FLASH UPGRADE UTILITY

If the utility is obtained from the bulletin board, UNZIP the archive and copy the files to a bootable MS-DOS 3.3, 4.01, 5.0, or 6.0 diskette. Reboot the system with the upgrade diskette in the bootable floppy drive and follow the directions in the easy to use menu-driven program.

RECOVERY MODE

In the unlikely event that a FLASH upgrade is interrupted catastrophically, it is possible the BIOS may be left in an unusable state. Recovering from this condition requires the following steps (be sure a power supply and speaker have been attached to the board, and a floppy drive is connected as drive A:):

1. Change Flash Recovery jumper (RCVR FLASH) to the recovery mode position.
2. Install the bootable upgrade diskette into drive A:
3. Reboot the system.
4. Because of the small amount of code available in the non-erasable boot block area, no video is available to direct the procedure. The procedure can be monitored by listening to the speaker and looking at the floppy drive LED. When the system beeps and the floppy drive LED is lit, the system is copying the recovery code into the FLASH device. As soon as the drive LED goes off, the recovery is complete.
5. Turn the system off.
6. Change the "FLASH RECOVERY" jumper back to the default position.
7. Leave the upgrade floppy in drive A: and turn the system on.
8. Continue with the original upgrade.

Appendix F- Memory Map

Address Range (Deci-	*Address Range (hex)*	*Size*	*Description*
1024K-131072K	100000-8000000	130048K	Extended Memory
960K-1023K	F0000-FFFFF	64K	AMI System BIOS
952K-959K	EE000-EFFFF	8K	FLASH Boot Block (Available as HIMEM)
948K-951K	ED000-EDFFF	4K	Logo reserved
928K-947K	E8000-ECFFF	20K	BIOS RESERVED
640K-927K	A0000-E7FFF	288K	Available HI DOS Memory (open to the ISA & PCI bus)
639K	9FC00-9FFFF	1K	Extended BIOS Data (moveable by QEMM, 386MAX)
512K-638K	80000-9FBFF	127K	Extended conventional
0K-511K	00000-7FFFF	512K	Conventional

Table F-1. Premiere/PCI Baby-AT motherboard Memory Map

Appendix G - I/O Map

Address (hex)	*Size(Dec)*	*Description*
0000 - 000F	16 bytes	SIO - DMA 1
0020 - 0021	2 bytes	SIO - Interrupt Controller 1
0040 - 0043	4 bytes	SIO - Timer 1
0048 - 004B	4 bytes	SIO - Timer 2
0060	1 byte	Keyboard Controller Data Byte
0061	1 byte	SIO - NMI, speaker control
0064	1 byte	Kbd Controller, CMD/STAT Byte
0070, bit 7	1 bit	SIO - Enable NMI
0070, bits 6:0	7 bits	SIO - Real Time Clock, Address
0071	1 byte	SIO - Real Time Clock, Data
0073	1 byte	Reserved - Brd. Config.
0075	1 byte	Reserved - Brd. Config.,RD only
0078	1 byte	SIO - BIOS Timer
0080 - 008F	16 bytes	SIO - DMA Page Register
00A0 - 00A1	2 bytes	SIO - Interrupt Controller 2
00C0 - 00DE	31 bytes	SIO - DMA 2
00F0	1 bytes	Reset Numeric Error
0170 - 0177	8 bytes	Secondary IDE Channel

Address (hex)	*Size(Dec)*	*Description*
01F0 - 01F7	8 bytes	Primary IDE Channel
0278 - 027B	4 bytes	Parallel Port 2
02F8 - 02FF	8 bytes	On-Board Serial Port 2
0376	1 byte	Secondary IDE Chan Cmd Port
0377	1 byte	Secondary IDE Chan Stat Port
0378 - 037F	8 bytes	Parallel Port 1
03BC - 03BF	4 bytes	Parallel Port x
03E8 - 03EF	8 bytes	Serial Port 3
03F0 - 03F5	6 bytes	Floppy Channel 1
03F6	1 bytes	Primary IDE Channel Cmnd Port
03F7 (Write)	1 byte	Floppy Channel 1 Command
03F7, bit 7	1 bit	Floppy Disk Change Channel 1
03F7, bits 6:0	7 bits	Primary IDE Channel Status Port
03F8 - 03FF	8 bytes	On-Board Serial Port 1
0CF8	1 byte	PCI Configuration Space Enable
0CF9	1 byte	Deturbo Mode Enable
C000 - C0FF	256 byte	82434LX Config. Registers *
C200 - C2FF	256 byte	82378IB Config. Registers *

Table G-1. Premiere/PCI Baby-AT I/O Address Map
* Only accessible after PCI configuration space is enabled.

Appendix H - Interrupts & DMA Channels

IRQ	*System Resource*
NMI	Parity Error
0	Reserved, Interval Timer
1	Reserved, Keyboard buffer full
2	Reserved, Cascade interrupt from slave PIC
3	Serial Port 2
4	Serial Port 1
5	Parallel Port 2
6	Floppy
7	Parallel Port 1
8	Real Time Clock
9	User available
10	User available
11	User available
12	PS/2 Mouse Port, User available on AT style bds
13	Reserved, Math coprocessor
14	Primary IDE if enabled, else available to user
15	Secondary IDE if enabled, else available to user

Table H-1. Premiere/PCI Baby-AT Interrupts

DMA	*Data Width*	*System Resource*
0	8- or 16-bits	Open
1	8- or 16-bits	Open - Normally used for LAN
2	8- or 16-bits	Floppy
3	8- or 16-bits	Parallel Port
4		Reserved - Cascade channel
5	16-bits	Open
6	16-bits	Open
7	16-bits	IDE

Table H-2. Premiere/PCI Baby-AT DMA Map

Appendix I - Connectors

AT STYLE KEYBOARD PORT

Pi	*Signal Name*
1	Clock
2	Data
3	No Connect
4	Ground
5	Vcc (fused)

PRIMARY POWER

Pin	*Name*	*Function*
1	PWRGD	Power Good
2	+5 V	+ 5 volts Vcc
3	+12 V	+ 12 volts
4	-12 V	- 12 volts
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	-5 V	-5 volts
10	+5 V	+ 5 volts Vcc
11	+5 V	+ 5 volts Vcc
12	+5 V	+ 5 volts Vcc

AUXILIARY (3.3V) POWER

Pin	*Name*	*Function*
1	GND	Ground
2	GND	Ground
3	GND	Ground
4	+3.3 V	+ 3.3 volts
5	+3.3V	+ 3.3 volts
6	+3.3 V	+ 3.3 volts

SPEAKER CONNECTOR

Pin	*Signal Name*
1	SPKR_DAT
2	Key
3	No Connect
4	+5V Vcc

RESET CONNECTOR

Pin	*Signal Name*
1	RESET
2	Ground

KEY LOCK/POWER LED

Pin	*Signal Name*
1	LED_PWR
2	Key
3	Ground
4	KEY LOCK
5	Ground

HARD DRIVE LED (DISK)

Pin	*Signal Name*
1	PULL_UP_330
2	HD ACTIVE-
3	Key
4	PULL_UP_330

TURBO LED

Pin	*Signal Name*
1	PULL_UP_330
2	LED_TURBO-

TURBO SWITCH

Pin	*Signal Name*
1	TURBO
2	Ground
3	No Connect

12V FAST FAN POWER

Pin	*Signal Name*
1	Ground
2	+12 V (polyfused)
3	Ground

10V SLOW FAN POWER

Pin	*Signal Name*
1	Ground
2	+10 V (polyfused)
3	Ground

SERIAL PORTS

Pin	*Signal Name*
1	DCD
2	DSR
3	Serial In - (SIN)
4	RTS
5	Serial Out - (SOUT)
6	CTS
7	DTR
8	RI
9	GND
10	N.C.

IDE CONNECTOR

Signal Name	*Pin*	*Pin*	*Signal Name*
Reset IDE	1	2	Ground
Host Data 7	3	4	Host Data 8
Host Data 6	5	6	Host Data 9
Host Data 5	7	8	Host Data 10
Host Data 4	9	10	Host Data 11
Host Data 3	11	12	Host Data 12
Host Data 2	13	14	Host Data 13
Host Data 1	15	16	Host Data 14
Host Data 0	17	18	Host Data 15
Ground	19	20	Key
DRQ3	21	22	Ground
I/O Write-	23	24	Ground
I/O Read-	25	26	Ground
IOCHRDY	27	28	BALE
DACK3-	29	30	Ground
IRQ14	31	32	IOCS16-
Addr 1	33	34	Ground
Addr 0	35	36	Addr 2
Chip Select 0-	37	38	Chip Select 1-
Activity	39	40	Ground

FLOPPY CONNECTOR

Signal Name	*Pin*	*Pin*	*Signal Name*
Ground	1	2	FDHDIN
Ground	3	4	Reserved
Key	5	6	FDEDIN
Ground	7	8	Index-
Ground	9	10	Motor Enable A-
Ground	11	12	Drive Select B-
Ground	13	14	Drive Select A-
Ground	15	16	Motor Enable B-
Ground	17	18	DIR-
Ground	19	20	STEP-
Ground	21	22	Write Data-
Ground	23	24	Write Gate-
Ground	25	26	Track 00-
Ground	27	28	Write Protect-
Ground	29	30	Read Data-
Ground	31	32	Side 1 Select-
Ground	33	34	Diskette

PARALLEL PORT CONNECTOR

Signal Name	*Pin*	*Pin*	*Signal Name*
STROBE-	1	2	AUTO FEED-
Data Bit 0	3	4	ERROR-
Data Bit 1	5	6	INIT-
Data Bit 2	7	8	SLCT IN-
Data Bit 3	9	10	Ground
Data Bit 4	11	12	Ground
Data Bit 5	13	14	Ground
Data Bit 6	15	16	Ground
Data Bit 7	17	18	Ground
ACJ-	19	20	Ground
BUSY	21	22	Ground
PE (Paper End)	23	24	Ground
SLCT	2	26	N.C.

ISA CONNECTORS

Signal Name	*Pin*	*Pin*	*Signal Name*
GND	B1	A1	IOCHK-
RSTDRV	B2	A2	SD7
Vcc	B3	A3	SD6
IRQ9	B4	A4	SD5
-5V	B5	A5	SD4
DRQ2	B6	A6	SD3
-12V	B7	A7	SD2
0WS-	B8	A8	SD1
+12V	B9	A9	SD0
GND	B10	A10	IOCHRDY
SMEMW-	B11	A11	AEN
SMEMR-	B12	A12	SA19
IOW-	B13	A13	SA18
IOR-	B14	A14	SA17
DACK3-	B15	A15	SA16
DRQ3	B16	A16	SA15
DACK1-	B17	A17	SA14
DRQ1	B18	A18	SA13
REFRESH-	B19	A19	SA12
SYSCLK	B20	A20	SA11
IRQ7	B21	A21	SA10
IRQ6	B22	A22	SA9
IRQ5	B23	A23	SA8
IRQ4	B24	A24	SA7
IRQ3	B25	A25	SA6
DACK2-	B26	A26	SA5
TC	B27	A27	SA4
BALE	B28	A28	SA3
Vcc	B29	A29	SA2
OSC	B30	A30	SA1
GND	B31	A31	SA0
	KEY	KEY	
MEMCS16-	D1	C1	SBHE-
IOCS16-	D2	C2	LA23
IRQ10	D3	C3	LA22
IRQ11	D4	C4	LA21
IRQ12	D5	C5	LA20
IRQ15	D6	C6	LA19
IRQ14	D7	C7	LA18
DACK0-	D8	C8	LA17
DRQ0	D9	C9	MEMR-
DACK5-	D10	C10	MEMW-
DRQ5	D11	C11	SD8
DACK6-	D12	C12	SD9
DRQ6	D13	C13	SD10
DACK7-	D14	C14	SD11
DRQ7	D15	C15	SD12
Vcc	D16	C16	SD13
Master-	D17	C17	SD14
GND	D18	C18	SD15

PCI CONNECTORS (J10B1, J10C1, J10C2)

Signal Name	*Pin*	*Pin*	*Signal Name*
GND	A1	B1	-12V
+12V	A2	B2	No Connect
No Connect	A3	B3	GND
No Connect	A4	B4	No Connect
Vcc	A5	B5	Vcc
PCIINT3-	A6	B6	Vcc
PCIINT1-	A7	B7	PCIINT2-
Vcc	A8	B8	PCIINT4-
Reserved	A9	B9	No Connect
Vcc	A10	B10	Reserved
Reserved	A11	B11	No Connect
GND	A12	B12	GND
GND	A13	B13	GND
Reserved	A14	B14	Reserved
SPCIRST-	A15	B15	GND
Vcc	A16	B16	PCLKE
AGNT-	A17	B17	GND
GND	A18	B18	REQA-
Reserved	A19	B19	Vcc
AD30	A20	B20	AD31
3.3V	A21	B21	AD29
AD28	A22	B22	GND
AD26	A23	B23	AD27
GND	A24	B24	AD25
AD24	A25	B25	3.3V
AD22 (IDSEL)	A26	B26	CBE3-
3.3V	A27	B27	AD23
AD22	A28	B28	GND
AD20	A29	B29	AD21
GND	A30	B30	AD19
AD18	A31	B31	3.3V

Signal Name	*Pin*	*Pin*	*Signal Name*
AD16	A32	B32	AD17
3.3V	A33	B33	CBE2-
FRAME-	A34	B34	GND
GND	A35	B35	IRDY-
TRDY-	A36	B36	3.3V
GND	A37	B37	DEVSEL-
STOP-	A38	B38	GND
3.3V	A39	B39	PLOCK-
SDONE	A40	B40	PERR-
SBO-	A41	B41	3.3V
GND	A42	B42	SERR-
PAR	A43	B43	3.3V
AD15	A44	B44	CBE1-
3.3V	A45	B45	AD14
AD13	A46	B46	GND
AD11	A47	B47	AD12
GND	A48	B48	AD10
AD9	A49	B49	GND
KEY	A50	B50	KEY
KEY	A51	B51	KEY
CBEO-	A52	B52	AD8
3.3V	A53	B53	AD7
AD6	A54	B54	3.3V
AD4	A55	B55	AD5
GND	A56	B56	AD3
AD2	A57	B57	GND
AD0	A58	B58	AD1
Vcc	A59	B59	Vcc
SREQ64-	A60	B60	SACK64-
Vcc	A61	B61	Vcc
Vcc	A62	B62	Vcc

Appendix J - Environmental Standards

Parameter	*Condition*	*Specification*
Temperature		
	Non-Operating	-40°C to +70°C
	Operating	+0°C to +55°C
Humidity		
	Non-Operating	92% Relative Humidity max. @ 36°C
	Operating	80% Relative Humidity max. @ 36°C
Altitude		
	Non-Operating	50,000 feet (15,240 meters)
	Operating	10,000 feet (3048 meters)
ESD		
	1.0kV	No Errors
	2.5kV	No Errors
	5.0kV	5% Soft Errors, 0% Hard Errors, No physical damage
	7.5kV	10% Soft Errors, 0% Hard Errors, No physical damage
	10.0kV	25% Soft Errors, 5% Hard Errors, No physical damage
	12.5kV	50% Soft, 10% Hard, No physical damage
	15.0kV	100% Soft, 25% Hard, No physical damage
	25.0kV	100% Soft, 100% Hard, No physical damage
Shock	Non-Operating	30.0G, 11ms, 1/2 sine

Table J-1. Environmental Standards

Appendix K - Reliability Data

The Mean-Time-Between-Failures (MTBF) data is calculated from predicted data @ 55C.

Premiere/PCI Baby-AT baseboard TBD (Testing in progress)

Appendix L - Early Product Features

Early units of the Premiere/PCI Baby-AT motherboard and Expandable Desktop (code named "Batman"), included several features that differ from those described in this Technical Product Summary. Among them:

BOARD LEVEL FEATURES

CPU

The original motherboard supported only 60 MHz Pentium processors and did not include the voltage regulation circuitry.

REAL TIME CLOCK

The Dallas DS12887 was socketed and could be replaced by the user, if necessary.

IDE

PCI IDE was not integrated on the original Premiere/PCI product. Instead, a PCI IDE paddle card was used in PCI slot 3 (J10C2, the PCI slot closest to the 3.3V connector) and made use of some of the reserved pins on the PCI interface, as listed in the following table:

Signal Name	*Pin*	*Pin*	*Signal Name*
GND	A1	B1	-12V
+12V	A2	B2	STCK (for IDE)
No Connect	A3	B3	GND
STDI	A4	B4	STD0 (for IDE)
Vcc	A5	B5	Vcc
PCIINT3-	A6	B6	Vcc
PCIINT1-	A7	B7	PCIINT2-
Vcc	A8	B8	PCIINT4-
SRSVD1 (for IDE)	A9	B9	No Connect
Vcc	A10	B10	SRSVD2 (for IDE)
SRSVD3 (for IDE)	A11	B11	No Connect
GND	A12	B12	GND
GND	A13	B13	GND
SRSVD4 (for IDE)	A14	B14	SRSVD5 (for IDE)
SPCIRST-	A15	B15	GND
Vcc	A16	B16	PCLKE
AGNT-	A17	B17	GND
GND	A18	B18	REQA-
SRSVD6 (for IDE)	A19	B19	Vcc
AD30	A20	B20	AD31
3.3V	A21	B21	AD29
AD28	A22	B22	GND
AD26	A23	B23	AD27
GND	A24	B24	AD25
AD24	A25	B25	3.3V
AD22 (IDSEL)	A26	B26	CBE3-
3.3V	A27	B27	AD23
AD22	A28	B28	GND
AD20	A29	B29	AD21
GND	A30	B30	AD19
AD18	A31	B31	3.3V

Signal Name	*Pin*	*Pin*	*Signal Name*
AD16	A32	B32	AD17
3.3V	A33	B33	CBE2-
FRAME-	A34	B34	GND
GND	A35	B35	IRDY-
TRDY-	A36	B36	3.3V
GND	A37	B37	DEVSEL-
STOP-	A38	B38	GND
3.3V	A39	B39	PLOCK-
SDONE	A40	B40	PERR-
SBO-	A41	B41	3.3V
GND	A42	B42	SERR-
PAR	A43	B43	3.3V
AD15	A44	B44	CBE1-
3.3V	A45	B45	AD14
AD13	A46	B46	GND
AD11	A47	B47	AD12
GND	A48	B48	AD10
AD9	A49	B49	GND
KEY	A50	B50	KEY
KEY	A51	B51	KEY
CBEO-	A52	B52	AD8
3.3V	A53	B53	AD7
AD6	A54	B54	3.3V
AD4	A55	B55	AD5
GND	A56	B56	AD3
AD2	A57	B57	GND
AD0	A58	B58	AD1
Vcc	A59	B59	Vcc
SREQ64-	A60	B60	SACK64-
Vcc	A61	B61	Vcc
Vcc	A62	B62	Vcc

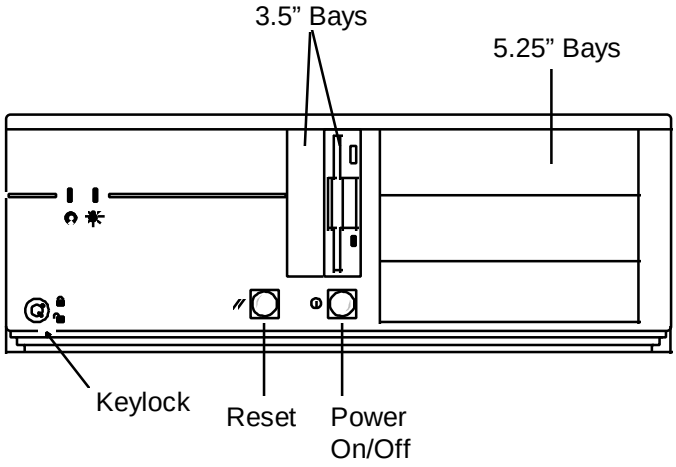
FAN

The Fast Fan/Slow Fan option was not available on the earlier product and there is no jumper.

SYSTEM LEVEL FEATURES

CHASSIS

A different chassis and front bezel was used for the early Premiere/PCI Expandable Desktop. This chassis supported only the five peripheral bays accessible from the front panel.



SYSTEM KEY LOCK

The earlier version of the chassis included a system keylock. When engaged, the key lock prevents keyboard input. Each system was provided with a set of two identical keys.

RESET SWITCH

The earlier chassis included a reset switch on the front panel.

BACK PANEL

The original product offered a slightly different arrangement of the back panel connections.