AP450GX MP Server Board Set Specification Update

Release Date: March 1998

Order Number: 282963-015

The AP450GX MP Server Board Set may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

CONTENTS

REVISION HISTORY

Date of Revision	Version	Description
October 16, 1996	-001	This document is the first Specification Update for the Intel AP450GX MP Server Board Set.
December 11, 1996	-002	Updated status for Errata 1 and 6. Corrected Errata 1, 2, 6 and 9. Added Specification Clarifications 1 and 2.
January 15, 1997	-003	Updated status for Errata 7, 10, 11, 20, 31, 32, and 33. Added Specification Clarification 3. Added Documentation Changes 1 and 2. Update tables in General Information section.
February 12, 1997	-004	Updated status for Erratum 2. Added Erratum 34. Updated General Information section with new processor stepping information.
March 12, 1997	-005	Added Erratum 35. Updated tables in General Information section.
April 16, 1997	-006	Added Errata 36 and 37. Updated tables in General Information section. Deleted Errata 1 through 35, as these have now been included in the updated Technical Product Specification.
May 14, 1997	-007	Updated General Information section with new baseboard PBA entries. Added Errata 38 through 40. Removed some chart columns that were not applicable in the General Information section.
August 13, 1997	-008	Added Errata 41 and 42. Updated status for Erratum 39.
September 10, 1997	-009	Added Errata 43 and 44. Updated status for Erratum 40. Added processor module -317 and BIOS's 1.00.10.CD0 and 1.00.12.CD0 to tables in General Information section.
October 15, 1997	-010	Added the new 200 MHz/1 MB processor to the tables on pages 4, 5 and 6. Added Erratum 45. Added Specification Change 1.
November 12, 1997	-011	Removed Errata 35 through 45 and Specification Change 1 because they are documented in the Technical Product Specification revision –003. Updated the General Information section. Added Errata 46 through 48. Added Specification Clarification 1. Removed Tracker reference numbers (OEM version only).
December 10, 1997	-012	Updated the General Information section. Added BIOS 1.00.14.CD0 to tables in General Information section. Updated Errata 41 and 42.
January 14, 1998	-013	Updated the workarounds for Errata 47 and 48. Added Specification Clarification 2.
February 11, 1998	-014	Updated the General Information section.
March 11, 1998	-015	Added Specification Clarification 3. Added Erratum 49.

PREFACE

This document is an update to the specifications contained in the AP450GX MP Server Board Set Technical Product Specification (Order Number 282964). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Refer to the *Pentium® Pro Processor Specification Update* (Order Number 242689) for specification updates concerning the Pentium® Pro processor. Items contained in the *Pentium® Pro Processor Specification Update* that either do not apply to the AP450GX MP Server Board Set or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the Printed Board Assembly (PBA) revisions(s) associated with that stepping.

Refer to the *Intel 450KX/GX PCIset Specification Update* (Order Number 243109) for specification updates concerning the Intel 450GX PCIset. Items contained in the *Intel 450KX/GX PCIset Specification Update* that either do not apply to the AP450GX MP Server Board Set or have been worked around are noted in this document. Otherwise, it should be assumed that any PCIset errata for a given stepping are applicable to the Printed Board Assembly (PBA) revisions(s) associated with that stepping.

Certain Pentium Pro processor and Intel 450GX PCIset errata are also included as board set errata. These errata are included here because of their implications and/or significance to the operation of the AP450GX MP Server Board Set. Errata 10, 11, 20, 32, and 33 fall into this category.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Characterized errata may cause the behavior of the AP450GX MP Server Board Set to deviate from published specifications. Hardware and software designed to be used with any given Printed Board Assembly (PBA) and BIOS revision level must assume that all errata documented for that PBA and BIOS revision level are present.

Specification Update for the AP450GX MP Server Board Set

GENERAL INFORMATION

For a complete revision history of system and board set level components, refer to the most recent Monthly Conversion Summary document for the AP450GX.

Basic AP450GX MP Server Board Set Identification Information

Module Description	Base PBA Number	PBA Rev Number	Fab Rev	450GX Stepping	Released BIOS/SCU Revision	Suggested BIOS/SCU Revision	Notes
Baseboard	647195	-403	3.5	B0 kit	1.00.04.CD0 3.40/OVL 1.31	Latest released BIOS and SCU	
		-423	3.5	B0 Kit	1.00.04.CD0 3.40/OVL 1.31	Latest released BIOS and SCU	
		-424	3.5	B0 Kit	1.00.05.CD0 3.50/OVL 1.40	Latest released BIOS and SCU	
		-425	3.5	B0 Kit	1.00.05.CD0 3.50/OVL 1.40	Latest released BIOS and SCU	
		-426	3.5	B0 Kit	1.00.05.CD0 3.50/OVL 1.40	Latest released BIOS and SCU	
		-428	3.5	B0 Kit	1.00.05.CD0 3.61/OVL 1.50	Latest released BIOS and SCU	
		-429	3.5	B0 Kit	1.00.05.CD0 3.61/OVL 1.50	Latest released BIOS and SCU	

Basic AP450GX MP Server Board Set Identification Information (Contd.)

Module Description	Base PBA Number	PBA Rev Number	Fab Rev	450GX Stepping	Released BIOS/SCU Revision	Suggested BIOS/SCU Revision	Notes
	666107	-001	3.5	C0 Kit	1.00.06 CD0 3.50/OVL 1.40	Latest released BIOS and SCU	
		-002	3.5	C0 Kit	1.00.06 CD0 3.50/OVL 1.40	Latest released BIOS and SCU	
		-003	3.5	C0 Kit	1.00.08 CD0 3.61/OVL 1.50	Latest released BIOS and SCU	
		-004	3.5	C0 Kit	1.00.08 CD0 3.61/OVL 1.50	Latest released BIOS and SCU	
		-005	3.5	C0 Kit	1.00.08 CD0 3.61/OVL 1.50	Latest released BIOS and SCU	
		-006	3.5	C0 Kit	1.00.08 CD0 3.61/OVL 1.50	Latest released BIOS and SCU	
		-107	3.5	C0 Kit	1.00.08 CD0 3.61/OVL 1.50	Latest released BIOS and SCU	
		-108	3.5	C0 Kit	1.00.08 CD0 3.61/OVL 1.50	Latest released BIOS and SCU	
		-109	3.5	C0 Kit	1.00.14 CD0 3.80/OVL 1.60	Latest released BIOS and SCU	

Module Description	Base PBA Number	PBA Rev Number	Fab Rev	Notes
Processor Module (Fab 3.x)	647428	-107	3.1	2,4
		-108	3.1	2,4
Processor Module (Fab 4.x)	659506	-212	4.1	3,4
		-213	4.2	3,4
		-214	4.2	3,4
		-215	4.2	3,4
		-216	4.2	3,4
		-316	4.3	3,4,5,6
		-317	4.3	3,4,5,6
Processor Module (Fab 5.x)	656631	-224A	5.1	
		-225	5.1	
		-226	5.1	
		-303	5.2	
1 GB Memory Module (Tin Sockets)	632487	-401	3.5	
		-402	3.5	
		-403	3.5	
		-423	3.5	
		-424	3.5	
		-525	3.6	
1 GB Memory Module (Gold Sockets)	652238	-401	3.5	
		-402	3.5	
		-403	3.5	
		-423	3.5	
		-424	3.5	
		-525	3.6	
Termination Module	648441	-106	3.1	
		-207	3.2	

NOTES:

1. All combinations of baseboards and modules will work together unless specified.
2. Supports only the 166/512 MHz Pentium® Pro processor.
3. Supports both the 166/512 MHz and 200/512 MHz Pentium Pro processors.
4. The Fab 3.x processor modules have not been validated to work with the Fab 4.x processor modules.
5. If the sB1 stepping of the Pentium Pro processor is installed, BIOS revision 1.00.08.CD0 or later is required.
6. Refer to Erratum 34 for issues related to the sB1 stepping of the Pentium Pro processor.

The following table indicates which steppings of the Pentium Pro processor can be mixed within the same system. An “X” denotes which steppings can be mixed and a blank indicates the AP450GX MP Server Board Set does not support the given stepping combination.

Supported Processor Combinations

Stepping (Proc/Cache)	SA1/α	sA1/β	sA1/β	sB1/β	sB1/β	sB1/C1
Frequency	**166**	**166**	**200**	**166**	**200**	**200**
Cache Size	**512**	**512**	**512**	**512**	**512**	**1M**
Stepping ID	**0617**	**0617**	**0617**	**0619**	**0619**	**0169**
QDF #	**SY034**	**SY047**	**SY048**	**SL22X**	**SL22Z**	**SL25A**
SY034	**X**	**X**		**X**		
SY047	**X**	**X**		**X**		
SY048			**X**		**X**	
SL22X	**X**	**X**		**X**		
SL22Z			**X**		**X**	
SL25A						**X**

NOTES:

1. The BIOS used must support each stepping installed in the system.
2. If the sB1 stepping of the Pentium® Pro processor is installed, BIOS revision 1.00.08.CD0 or later is required.
3. Refer to Erratum 34 for issues related to the sB1 stepping of the Pentium Pro processor
4. Though Intel recommends using identical steppings of processor silicon in multiprocessor systems whenever possible (as this is the only configuration which receives full validation across all of Intel’s testing), Intel supports mixing processor steppings, and does not actively prevent various steppings of the Pentium Pro processor from working together in multiple processor (MP) systems. However, since Intel cannot validate every possible combination of devices, each new stepping of a device is fully validated only against the latest steppings of other processors and chipset components. Refer to Specification Change 1 of the *Pentium® Pro Processor Specification Update* for further details on issues related to mixed processor steppings in an MP system..

The following table lists the production BIOS versions and processor stepping supported by the board set. The table also indicates which stepping of the Pentium Pro processors are supported by each version of the BIOS. An "X" denotes which stepping are supported and a blank indicates the AP450GX MP Server Board Set does not support the given BIOS/stepping combination.

Supported BIOS/Processor Combinations

	Stepping (Proc/Cache)	sA1/α	sA1/β	SA1/β	sB1/β	SB1/β	sB1/C1
	Frequency	166	166	200	166	200	200
	Cache Size	512	512	512	512	512	1M
	Stepping ID	0617	0617	0617	0619	0619	0619
BIOS	QDF #	SY034	SY047	SY048	SL22X	SL22Z	SL25A
1.00.04.CD0		X	X	X			
1.00.05.CD0		X	X	X			
1.00.06.CD0		X	X	X			
1.00.07.CD0		X	X	X			
1.00.08.CD0		X	X	X	X	X	X
1.00.09.CD0		X	X	X	X	X	X
1.00.10.CD0		X	X	X	X	X	X
1.00.12.CD0		X	X	X	X	X	X
1.00.14.CD0		X	X	X	X	X	X

The Intel 450GX PCIset B0 kit consists of four different components as follows:

Device	Stepping	S-Spec Numbers
82451GX (MC-MIC)	B0	SU019
82452GX (MC-DP)	B0	SU057
82453GX (MC-DC)	B0	SU058
82454GX (PB)	B0	SU063

The Intel 450GX PCIset C0 kit consists of four different components as follows:

Device	Stepping	S-Spec Numbers
82451GX (MC-MIC)	C0	SU019
82452GX (MC-DP)	C0	SY053
82453GX (MC-DC)	C0	SY051
82454GX (PB)	C0	SY054

Summary Table of Changes

The following table indicates the Errata, Specification Changes, Specification Clarifications, or Documentation Changes which apply to the AP450GX MP Server Board Set. Intel intends to fix some of the errata in the future, and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future revision of the hardware or software associated with the AP450GX MP Server Board Set.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This erratum is either new or modified from the previous version of the document.

NO.	PLANS	ERRATA
1	Fixed	Board level shock and vibration testing may cause processor module capacitor fatigue
2	Fixed	IDE CD-ROM as master may cause server hang
3	NoFix	Flash boot block protect jumper in unprotected mode may cause flash corruption during a warm reset
4	Fixed	Power distribution board scan via the I2C bus may cause possible incorrect chip set register settings
5	Fixed	BIOS does not remap bad SIMMs correctly during a system reset
6	Fixed	The Fab 3.x processor module does not support the 200-MHz Pentium® Pro processor with 512-Kbyte L2 cache
7	Fixed	EISA read performance is below expectations
8	NoFix	Incorrectly inserted memory module may cause baseboard damage
9	NoFix	If address bit permuting is enabled memory resizing cannot be performed
10	Fixed	BIOS setting IOQ=8 may cause SMM handler to hang the operating system
11	Fixed	If incompatible SIMMs are installed the system may hang during reset
12	Fixed	Fan failure causes intrusion switch detection to be disabled
13	Fixed	BIOS record type 13H indicates incorrect hard drive information
14	Fixed	Memory resizing error causes BIOS to report wrong memory bank
15	Fixed	Pentium Pro processor data bus single bit ECC errors may cause excessive SMI generation
16	Fixed	Incorrectly entering administrator password may hang SCU 3.40/OVL 1.31
17	Fixed	Entering a valid password to exit BIOS “secure mode” leaves keyboard lights enabled
18	Fixed	Greater than 1.5 GB of memory installed may cause system hang
19	Fixed	BIOS does not log bad SIMM location during POST memory testing
20	Fixed	Spurious interrupts may cause virtual wire mode APIC operation to fail
21	Fixed	The SCU cannot change the state of the PCI system error option

NO.	PLANS	ERRATA
22	Fixed	The SCU incorrectly sets the baud rates for serial redirection
23	Fixed	Power and reset security switches in the BIOS setup are not available in the SCU
24	Fixed	Incorrectly initialized real time clock registers may hang operating system on the tenth of each month
25	Fixed	BIOS setting IOQ=Autodetect causes BIOS to set IOQ=8
26	Fixed	If the system temperature reaches a warning threshold temperature monitoring is disabled
27	Fixed	Using 60 ns 64 MB SIMMs and 2-way memory interleave may cause system hang during reset
28	Fixed	Location of password prompts in POST sequence may cause system security violation
29	Fixed	Clearing NVRAM (CMOS) and installing an operating system may cause a system hang
30	Fixed	Excessive single-bit ECC errors incorrectly disables single-bit error logging for memory bus and processor data bus
31	Fixed	Saving BIOS configuration after date change may cause date to be set incorrectly
32	Fixed	BIOS setting IOQ = 8 may corrupt PCI configuration cycles
33	Fixed	PCI-to-PCI bridges may cause the system to hang
34	Fixed	Board set TAP reset circuit may cause incorrect system power on
35	Fixed	INCA anomaly at power up may cause PCI bus clocks to run at 66 MHz on baseboards with the C0 stepping of Intel 450GX PCIset
36	Fixed	BIOS does not set MTRRs correctly with sA1 and sB1 mixed steppings present
37	Fixed	BIOS does not set MTRRs correctly for sA1 stepping and 4 GB memory
38	Fixed	BIOS incorrectly programs the address of the 8584 I^2C controller
39	Fixed	SCO UNIXWare* v2.11 fails to install under a certain configuration
40	Fixed	ECC memory errors may occur when the memory test warm boot option is disabled in BIOS setup
41	Fixed	Fan failure event logging may be incorrect
42	Fixed	POST error codes may occur with a 4 GB memory module and multiple PCI adapters installed
43	NoFix	Floppy drive read/write errors
44	NoFix	System temperature reading inaccuracy with fully loaded system
45	Fix	Cache mismatch error if processor fails with BIOS 12 and 1 MB Pentium Pro processor
46	NoFix	“Missing Operating System” error when installing Windows* NT 3.51 or 4.0 with 2 or more new drives which are 2 GB or larger
47	NoFix	Cirrus* 5424 video not directly supported in Windows NT 4.0
48	NoFix	Windows NT 4.0 installation fails with fully populated 4 GB memory module
49	NoFix	EISA to PCI accesses limited to less than 1 GB

NO.	PLANS	SPECIFICATION CHANGES
1	Doc	Added addendum to board set TPS for 1 MB Pentium Pro processor module
NO.	**PLANS**	**SPECIFICATION CLARIFICATIONS**
1	Doc	Power Supply Control from Real-Time Clock
2	Doc	Parts of Shadow Memory Must Be Disabled for the Onboard Adaptec* BIOS to Function Properly
3	Doc	Novell Netware* 4.1 was certified by Novell not Netware 4.11

The following table indicates the hardware or software revisions where each erratum was fixed when applicable.

CODES USED IN FOLLOWING TABLE

Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future revision of the hardware or software associated with the AP450GX MP Server Board Set.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This erratum is either new or modified from the previous version of the document.

		FIXED IN					
NO..	**PLANS**	**Baseboard (B0)**	**Baseboard (C0)**	**Proc.Mod. (4.x)**	**BIOS**	**SCU**	**Other**
1	Fixed			-213			
2	Fixed				1.00.07.CD0		
3	NoFix						
4	Fixed				1.00.05 CD0		
5	Fixed				1.00.05 CD0		
6	Fixed			-212			
7	Fixed		-001				
8	NoFix						
9	NoFix						
10	Fixed		-001				
11	Fixed		-001				
12	Fixed				1.00.05 CD0		
13	Fixed				1.00.05 CD0		
14	Fixed				1.00.05 CD0		
15	Fixed				1.00.05 CD0		
16	Fixed					3.50/OVL 1.40	
17	Fixed				1.00.05 CD0		
18	Fixed				1.00.05 CD0		
19	Fixed				1.00.06 CD0		
20	Fixed				1.00.06 CD0		
21	Fixed					3.50/OVL 1.40	
22	Fixed					3.50/OVL 1.40	
23	Fixed					3.50/OVL 1.40	

		FIXED IN					
NO..	**PLANS**	**Baseboard (B0)**	**Baseboard (C0)**	**Proc.Mod. (4.x)**	**BIOS**	**SCU**	**Other**
24	Fixed						Testview (PCDIAGS) version 3.37a
25	Fixed				1.00.05 CD0		
26	Fixed				1.00.05 CD0		
27	Fixed				1.00.05 CD0		
28	Fixed				1.00.06 CD0		
29	Fixed				1.00.05 CD0		
30	Fixed				1.00.07 CD0		
31	Fixed				1.00.06 CD0		
32	Fixed		-001				
33	Fixed		-001				
34	Fixed			-216, -316			
35	Fixed	-004 -005 -006					
36	Fixed				1.00.09 CD0		
37	Fixed				1.00.09 CD0		
38	Fixed				1.00.07 CD0		
39	Fixed				1.00.10 CD0		
40	Fixed				1.00.10 CD0		
41	Fixed				1.00.14.CD0		
42	Fixed				1.00.12.CD0		
43	NoFix						
44	NoFix						
45	Fix						
46	NoFix						
47	NoFix						
48	NoFix						
49	NoFix						

ERRATA

For Errata 1 through 45, refer to the *AP450GX MP Server Board Set Technical Product Specification* (Order Number 282964-003).

46. "Missing Operating System" Error When Installing Windows* NT 3.51 or 4.0 with 2 or More New Drives Which are 2 GB or Larger

PROBLEM: When installing Windows* NT 3.51 or 4.0 with two or more new or low-level formatted drives, the size of the first drive shown during installation is slightly larger than actual. After the first reboot of the installation process, the error message "Missing Operating System" is displayed.

IMPLICATION: The Windows NT installation fails.

WORKAROUND: Using Windows NT or MS-DOS*, create a new partition with an FDISK utility, and then restart the installation process.

STATUS: This erratum is not a SCSI BIOS issue. It will not be fixed by Intel. It results from a known issue with the Windows NT loader. Refer to Microsoft Knowledge* base ID Q114841, Q143141 and Q138364.

47. Cirrus* 5424 Video Not Directly Supported in Windows* NT 4.0

PROBLEM: Windows NT 4.0 does not directly support the Cirrus* 5424 video on the AP450GX MP Server Board Set.

IMPLICATION: There is no direct driver support provided for Cirrus 5424 under Windows NT 4.0.

WORKAROUND: A Cirrus compatible driver is supplied with Windows NT 4.0, and this can be used without issue. See Technical Advisory #0033 available through Intel Customer Support (1-800-628-8686), or your Intel Sales Representative.

STATUS: This issue will not be fixed by Intel.

48. Windows* NT 4.0 Installation Fails with Fully Populated 4 GB Memory Module

PROBLEM: The installation of Windows NT 4.0 hangs on a blue screen, and fails to complete the setup procedure, when installing on an AP450GX MP Server Board Set with greater than 3 GB of memory installed.

IMPLICATION: The problem results because Windows NT 4.0 has a limit of 3 GB for main memory.

WORKAROUND: Remove any memory in excess of 3 GB from the memory module prior to installation of Windows NT 4.0. Install Windows NT service pack 3, or greater, then repopulate memory board with the full memory. See Technical Advisory #0034 available through Intel Customer Support (1-800-628-8686), or your Intel Sales Representative.

STATUS: This issue will not be fixed by Intel.

49. EISA to PCI Accesses Limited to Less than 1 GB

PROBLEM: In a system with greater than 1 GB of memory installed, Dynamic Memory Addressing (DMA) from EISA to memory fails above 1 GB.

IMPLICATION: This limit exists because when the AP450GX server was launched its maximum memory capacity was 1 GB. The PCI-to-EISA Bridge (PCEB) was initially programmed to utilize 1 GB as its maximum addressable space. When the AP450GX was enhanced to support 2 GB, then 4 GB, of main memory the PCEB was never changed. Therefore, the PCEB is limited to accesses below 1 GB.

WORKAROUND: At this time there is no supported workaround to this issue.

STATUS: This issue will not be fixed by Intel.

SPECIFICATION CLARIFICATIONS

The specification clarifications listed in this section apply to *the AP450GX MP Server Board Set Technical Product Specification* (Order Number 282964). All specification clarifications will be incorporated into a future release of the *AP450GX MP Server Board Set Technical Product Specification*.

1. Power Supply Control Using the RTC (Real-Time Clock)

Section 1.20.6., *"*Power Control Jumper*,* J6A3," will be modified. The text in the section will be changed to read as follows:

This jumper (PWR CTRL) enables power supply control using the real-time clock. Power control from the RTC is typically used for Automatic Server Recovery. An alarm is set in the RTC by the BIOS or a utility program to power the system on or off at a predetermined time. However, this feature has never been implemented in either the BIOS or any utility program. Furthermore, LDSM (LANDesk® Server Manager) does not utilize ASR.

The last two sentences of the paragraph are additions.

2. Parts of the Shadow Memory Must be Disabled for the Onboard Adaptec BIOS to Function Properly*

Section 3.4.6., "About the Options," will be modified. The following text will be added as Section 3.4.6.1.; this section will read as follows:

When using the SCU to configure an AP450GX system, the Shadow Memory range D0000h-DFFFFh (or from D0000h to DC000h at the Shadowing ISA ROMs Option under the Memory Subsystem) cannot be set as completely disabled. Part of the memory region from D0000h-DFFFFh must be set as disabled for the onboard Adaptec* BIOS, which utilizes parts of this space for internal purposes, to function properly. The Adaptec controller will generate the following message when no memory in this range has been enabled for shadowing:

"Insufficient memory to shadow PCI ROM Bus 0 Device 0b"

"Insufficient memory to shadow PCI ROM Bus 1 Device 0c"

3. Novell Netware 4.1 was Certified at the Novell Facility not Netware 4.11*

Appendix A, Section A.1., "Certified Operating System." The following text will be changed in the table.

Version 3.12 & 4.11 should read 3.12 & 4.10.