Enterprise Server Group

Intel M440LX DP Server Board Set
Technical Product Specification

Released version 2.0
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March, 1998

The M440LX DP Server board set may contain design defects or errors known as errata. Characterized errata that may cause the M440LX DP Server board set's behavior to deviate from published specifications are documented in the M440LX DP Server Specification Update.

Revision History

Revision	Revision History	Date
Rev 1.0	Initial release of the M440LX DP Server Board Set Technical Product Specification	8/97
Rev 2.0	Update of the M440LX DP Server Board Set Technical Product Specification	3/98

This product specification applies only to standard M440LX DP Server board set with BIOS Release 4. Information in this version of the summary applies to the BIOS Release 4. Different versions of the BIOS may look and behave differently.

***NOTE**: If printing this document from an electronic file, use a PostScript printer with the appropriate PostScript print driver to insure the drawings print clearly.*

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1. Board Set Description

1.1 Product Overview

The Intel M440LX DP Server board set is a modular, dual Pentium® II processor-based server system that combines the latest technology and integrated features to provide a high-performance platform at mid-range cost efficiency.

The M440LX DP Server board set utilizes the Intel 440LX AGPset, to maximize system performance for 32-bit application software and operating systems. Additionally, by incorporating the i960® RD processor in the board set design, an Intelligent I/O subsystem, the I/O demands placed on the host processor are drastically reduced, further enhancing system performance and scalability. The i960 RD processor fully supports the Intelligent I/O industry specification, also known as I_20.

The M440LX DP Server design is complemented with an array of features. These include:

- Intel 440LX AGPset (82440LX, 82443LX PAC controller, PIIX4)
- i960 RD I/O processor
- Symbios* SCSI controllers (1 narrow, 2 ultra-wide)
- AMI MegaRAID*
- Nine I/O expansion slots (3 PCI on PCI-P, 4 PCI on PCI-S, 2 ISA, 1 shared)
- National SuperI/O* 87307 PCI/IDE controller
- Two Single Edge Contact (SEC) cartridge connectors (to accommodate dual Pentium II processors and future processor upgrades)
- Support for EDO or SDRAM ECC memory, up to 512MB (modular)
- Cirrus Logic GD54M40* SVGA video
- Server Management

The M440LX DP Server board set supports dual 266 MHz or 300 MHz Pentium II processors contained on Single Edge Contact (SEC) cartridges. These cartridges enclose the processor with 512KB of integrated ECC L2 cache to enable high-frequency operation. There is two SEC connectors on the baseboard with an embedded VRM 8.1-compliant voltage regulator (DC-to-DC converter) for connector 0, and plug-in VRM support for connector 1. The M440LX DP Server board set design will accommodate upgrades to future Pentium II processing technology.

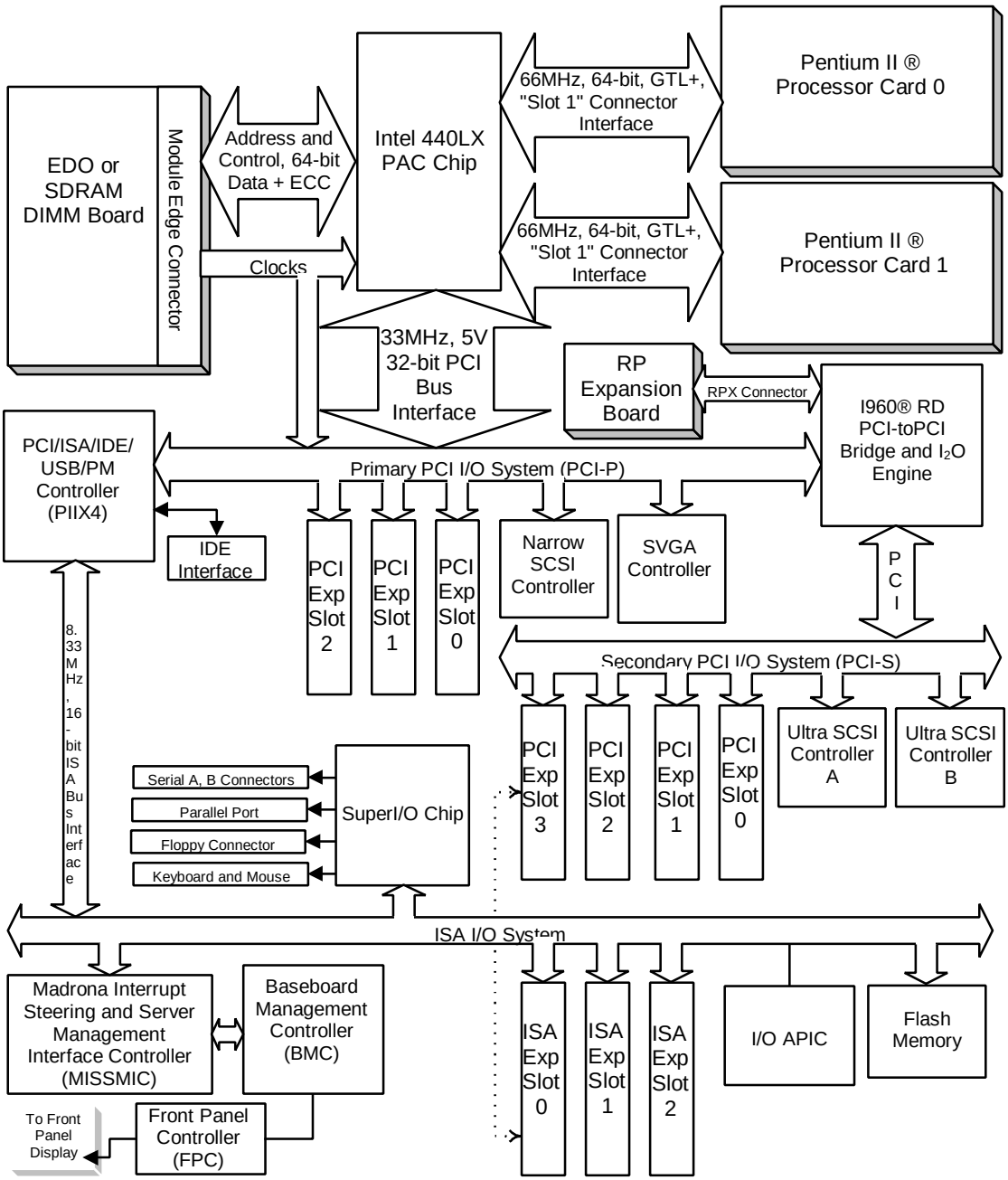

Figure 1. M440LX DP Server Functional Block Architecture

Baseboard Diagram

The following diagram shows the placement of major components and connector interfaces on the M440LX DP Server board set.

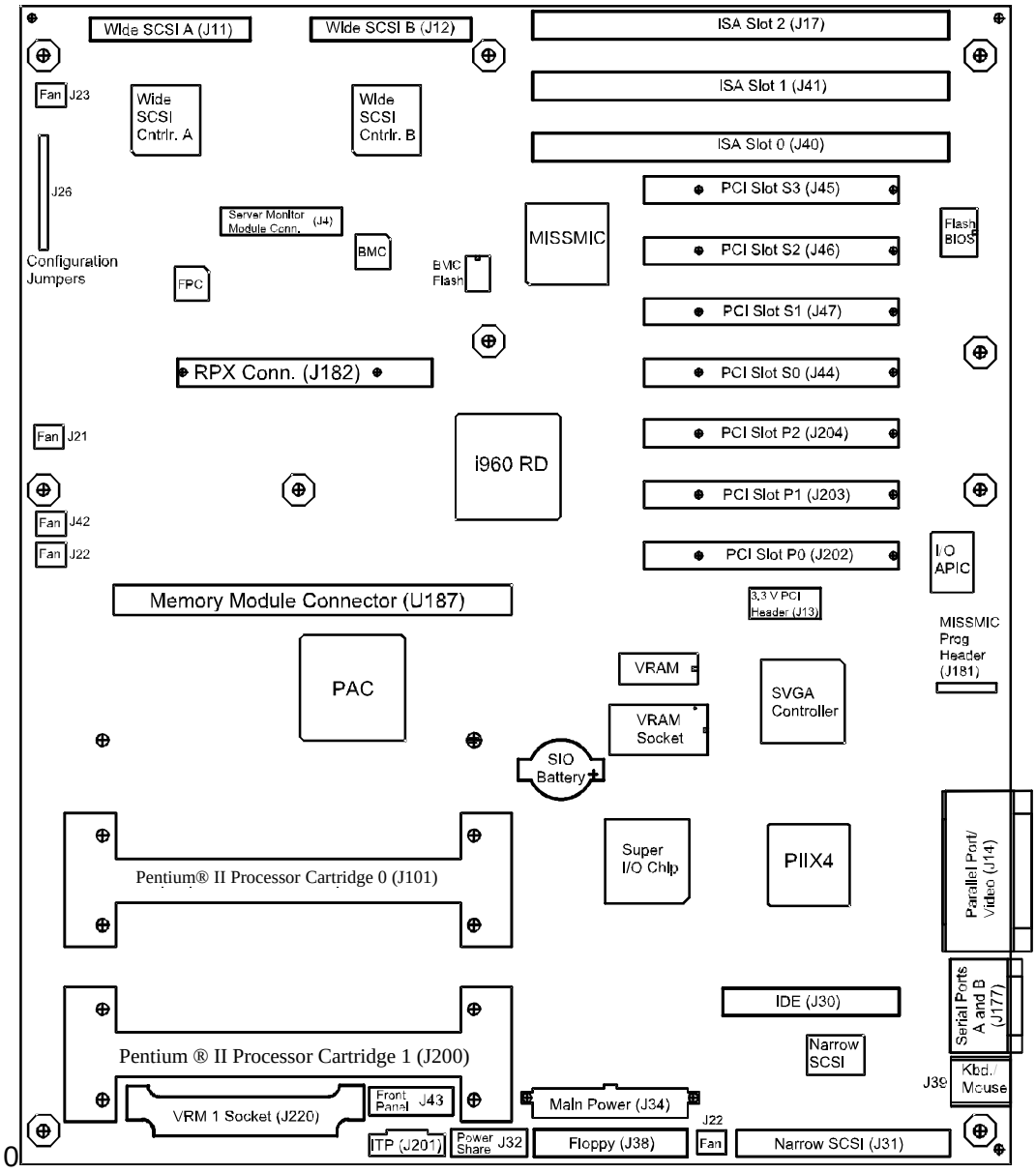

Figure 2. MB440LX DP Server board set layout

1.2 Processor/PCI Host Bridge/Memory Subsystem

The processor/PCI bridge/memory subsystem consists of one or two identical Pentium II processor SEC cartridges, a plug-in memory board, and support circuitry on the board set consisting of the following:

- Intel 82443LX PCI/A.G.P. controller (PAC) PCI host bridge and memory controller
- Dual SEC connectors that accept the Pentium II processor SEC cartridges
- 242-pin connector interface to memory module, which contains clock generation circuitry
- Processor host bus GTL+ support circuitry, including termination power supply
- Embedded DC-to-DC voltage converter for processor SEC cartridge 0 power; socket for plug-in VRM for processor SEC cartridge 1 power
- APIC bus
- Miscellaneous logic for reset configuration, processor SEC cartridge presence detection, ITP port, and server management

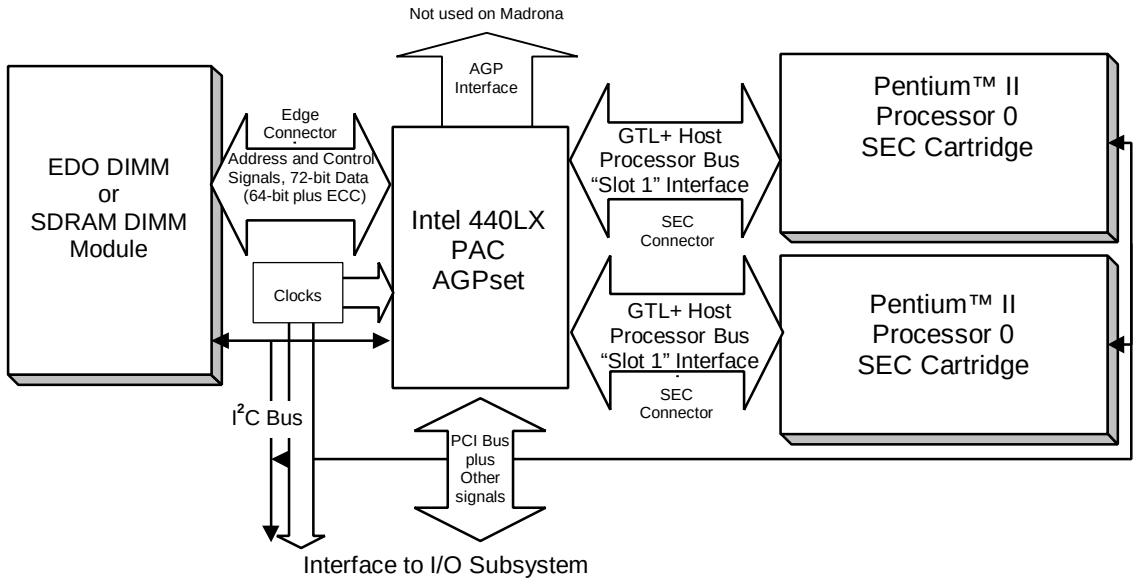

Figure 3 Processor/PCI Host Bridge/Memory Subsystem

1.3

Pentium II Processor SEC Cartridge

The M440LX DP Server board set is designed to accommodate Pentium II processors at speeds from 233 MHz to 300 MHz. Previous Intel processors utilized technology which housed the processor core/L1 cache and L2 cache in a dual-cavity PGA package. However, with the introduction of the Pentium II processor, the Single Edge Contact (SEC) cartridge was implemented. The SEC cartridge encloses the processor core/L1 cache and the L2 cache on a pre-assembled printed circuit board, approximately 2.5" x 5" in size.

The L2 cache and processor core/L1 cache is connected using a private bus that is isolated from the processor host bus. The Pentium II processor's L2 cache bus operates at half of the processor core frequency. To compensate for the cache bus speed, the internal L1 data and code caches have been enlarged to 16 KB.

The Pentium II processor SEC cartridge's external interface is designed to be multiprocessor-ready. Each processor contains a local APIC section for interrupt handling. When two SEC cartridges are installed, they must be of identical revision, core voltage, and bus/core speeds.

Retention Module

SEC Cartridge Connector

The Pentium II processor SEC connector conforms to the “Slot 1” specification, which can also accommodate future processor SEC cartridges. The baseboard provides two connectors. The processors face towards the memory module.

Processor Bus Termination/Regulation/Power

The termination circuitry required by the Pentium II processor bus (GTL+) signaling environment and the circuitry to set the GTL+ reference voltage, are implemented directly on the SEC cartridges. The baseboard provides 1.5V GTL+ termination power (VTT) and VRM 8.1-compliant DC-to-DC converters to provide processor power (VCCP) at each connector. Power for processor 0 is derived from the 12V supply, using an embedded DC-DC converter onboard. A socket is provided on the baseboard for a VRM to power processor 1, which derives power from the 5V supply.

Termination Card

If only one Pentium II processor SEC cartridge is installed in a system, a termination card *must* be installed in the vacant SEC connector to ensure reliable system operation. The termination card contains GTL+ termination circuitry, clock signal termination, and Test Access Port (TAP) bypassing for the vacant connector.

APIC Bus

Interrupt notification and generation for the Pentium II processors is done using an independent path between local APICs in each processor and the Intel I/O APIC located on the baseboard. This simple bus consists of two data signals and one clock line. Refer to the *I/O APIC and Interrupts* section later in this chapter for more information.

1.4 440LX Host Bridge

The 82443LX PCI/A.G.P. controller (PAC) is the host bridge between the Pentium II processors and I/O systems. The 82443LX PAC is a 492-pin ball-grid array (BGA) device that performs control signal translations and manages the data path. The host bridge in the PAC supports one or two processors at a processor host bus frequency of 66 MHz, with 32-bit addressing, optimized in-order and request queue (IOQ), and dynamic deferred transaction support. The GTL+ host bus connects the processor card with other resources in the system through the 440LX PAC host bridge. The host bridge translates 64-bit operations in the GTL+ signaling environment at 66 MHz to a 32-bit PCI I/O subsystem. The 440LX PAC also handles arbitration for the primary PCI bus.

The PCI interface provides greater than 100 MB/s data streamlining for PCI to DRAM accesses, while supporting concurrent processor host bus and PCI transactions to main memory. This is accomplished using extensive data buffering, with processor-to-DRAM and PCI-to-DRAM write data buffering and write-combining support for processor-to-PCI burst writes. Five PCI masters can be supported in addition to the host processor(s) and PCI to ISA bridge functions.

The 82443 PAC also contains the memory controller for M440LX DP Server. Memory amounts from 8 MB to 1 GB of DIMM memory are possible with a 64/72-bit non-interleaved pathway to main memory, located on a plug-in module. The memory controller supports SDRAM and EDO DRAMs. System clock generation is located on the memory module due to the significantly different clock requirements of EDO and SDRAM memory.

ECC is provided that can detect (SED) and correct (SEC) single-bit errors, and detect all double-bit and some multiple-bit errors (DED). Under software control, parity checking and the level of ECC desired may be configured. On power-up ECC and parity checking are disabled.

1.5 PCI I/O Subsystem (PCI-P)

The M440LX DP Server is designed with two PCI bus segments: the primary (PCI-P) and the secondary (PCI-S). Each segment is compliant with revision 2.1 of the PCI specification operating at 33 MHz. PCI-P is the primary PCI segment, produced by the PCI interface from the 82443 PAC. The secondary PCI segment, PCI-S, operates through the PCI-to-PCI bridge in the i960®RD in a hierarchical bus structure. The two hierarchical PCI segments run concurrently with the processor bus and with each other increasing throughput through independent arbitration and data buffering. A total of seven PCI slots for add-in cards (three on PCI-P, and four on PCI-S) are available. A single PCI slot on the secondary segment is physically shared with an ISA slot. The first PCI-S slot supports a half-length PCI card when the RPX module is installed. All other PCI slots support full-length cards.

All I/O is directed through the primary PCI bus segment. The primary PCI I/O bus includes: 3 PCI slots (P0, P1, and P2), the i960 RD PCI-to-PCI bridge to the secondary PCI I/O bus, the Intel PIIX4 controller, the Cirrus Logic CL-GD54M40 SVGA video controller, and the Symbios 53M810 narrow SCSI controller.

PCI-0 Arbitration

The 440LX PCI/A.G.P. controller accomplishes PCI-P arbitration. All PCI masters must arbitrate for PCI access because the primary PCI bus supports six PCI masters (slots P0 through P2, i960 RD, SCSI, PIIX4, and PAC) and one slave. Note that the PCI video is a slave-only device

PCI-to ISA/IDE/USB Controller (PIIX4)

The PIIX4 provides four specific PCI functions in a single package, PCI-to-ISA bridge, IDE interface, USB controller (not used on the MB440LX DP Server), and power management controller. Each of the four functions in the PIIX4 contain its own set of configuration registers that appear to the MB440LX DP Server system as a unique hardware controller sharing the same PCI bus interface.

The PIIX4 is packaged as a 324-pin BGA device and fully implements a 32-bit PCI master/slave interface, in accordance with the *PCI Local Bus Specification, Rev. 2.1*. The PCI interface operates at 33 MHz, using the 5V, signaling environment.

The PIIX4 provides an ISA bus interface, operating at 8.33 MHz, which supports 3 ISA connectors, flash memory, server management interface, and the National SuperI/O controller.

The fast IDE controller in the PIIX4 supports programmed I/O transfers up to 14 MB/s and bus master IDE transfers up to 32 MB/s. The PIIX4 supports two IDE channels but the MB440LX DP Server board set only utilizes the primary IDE channel. The single IDE connector, featuring 40 pins (2 x 20), is provided on the baseboard.

i960 RD I/O Processor PCI-to-PCI Bridge

The i960 RD I/O processor is a high performance, 80960JF core processor running at 66 MHz that provides the PCI-to-PCI bridge from the primary PCI bus to the secondary PCI bus on M440LX. This bridge is compliant with the PCI 2.1 specification. The i960 RD I/O processor also provides an integrated memory controller unit, a multi-channel DMA controller, and an I^2C bus interface unit. The i960 RD I/O processor also has a secondary PCI bus arbitration unit.

RP Expansion (RPX) Card Interface

The M440LX DP Server board set provides a connector interface to modular local memory for the 80960JF processor in the i960 RD I/O processor: the RPX connector. The RPX card for M440LX DP Server attaches to this interface, which contains local memory and firmware support for intelligent I/O (I_2O) operations. The RPX card can also be used for onboard RAID using the two Symbios SYM53C875 Ultra SCSI controllers on the secondary PCI segment. The RPX connector provides additional signals in anticipation of future upgrades. Refer to the RPX Module section for more information

1.6 PCI-P Narrow SCSI

A narrow SCSI host adapter, the Symbios SYM53C810 controller, is integrated into the M440LX DP Server board set. The SYM53C810 controller contains a high-performance SCSI core capable of fast, 8-bit SCSI transfers in single-ended mode. The high-performance SCSI core, PCI bus master DMA, and internal SCRIPTS* processor all meet SCSI-1 and SCSI-2 standards. The 100-pin PQFP packaged component provides programmable active negation, PCI zero wait-state bursts of faster than 110 MB/s at 33 MHz and SCSI transfer rates from 5 MB/s to 10 MB/s.

The device also offers active negation outputs. Active negation outputs reduce the chance of data errors by actively driving both polarities of the SCSI bus, avoiding indeterminate voltage levels and common-mode noise on long cable runs. The SCSI output drivers can directly drive a 48 mA single-ended SCSI bus with no additional drivers.

The SCSI data bus is 8-bits wide with even or odd parity generation. The SYM53C810 controller has a very flexible parity scheme allowing both parity senses, the ability to disable parity, and the ability to generate bad parity for testing, whether or not errors are handled correctly. The SYM53C810 controller supports variable block size and scatter/gather data transfers. It supports a SCRIPTS language for high-performance, flexibility, and ease of use. The SYM53C810 controller performs complex bus sequences without interrupts, including restore data pointers

Symbios SYM53C810 controller PCI signals

The SYM53C810 supports all of the required 32-bit PCI signals including the **PERR_L** and **SERR_L** functions. Full PCI parity is maintained on the entire data path through the SYM53C810 SCSI controller.

The extensions to memory commands (memory read multiple, memory read line, and memory write and invalidate) work with the cache line size register to give the cache controller advance knowledge of the minimum amount of data to expect. The decision to use either the memory read line or memory read multiple commands is determined by bits in the configuration space command register for this device, and if correct conditions exist for the particular transfer.

1.7 PCI Video

The M440LX DP Server has an integrated video controller, the Cirrus Logic CL-GD54M40, and support circuitry on the primary PCI bus. The CL-GD54M40 32-bit VGA Graphics Accelerator component chip contains a SVGA video controller, clock generator, and 80 MHz RAMDAC in a 160-pin PQFP. Standard video memory consists of a single 256 KB x 16 DRAM chip providing 512 KB of 60 ns video memory, with optional expansion to 1 MB for improved performance and more video modes. The CL-GD54M40 supports a variety of modes: up to 1280 x 1024 resolution and up to 64 KB colors.

This SVGA subsystem supports analog VGA monitors, single and multi-frequency, interlaced and non-interlaced, up to 87 Hz vertical retrace frequency. The connector is a standard 15-pin VGA connector.

The CL-GD54M40 supports a minimal set of 32-bit PCI signals since it never acts as a PCI master. As a PCI-P slave, the device requires no arbitration or interrupt connections.

Video Modes

The Cirrus Logic GD54M40 provides all standard IBM VGA modes. With 512 KB of video memory, the standard M440LX DP Server goes beyond standard VGA support. The following tables show all supported video modes using 512 KB, as well as 1 MB of video memory. The additional 512 KB is user-installable. These tables also show the standard and extended modes that the chip supports, including the number of colors and palette size (e.g., 16 colors out of 256 KB colors), resolution, pixel frequency, and scan frequencies.

Table 1 Standard VGA Modes

Mode(s) in Hex	Bits Per Pixel	Colors (number/palette size)	Resolution	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)
0, 1	4	16/256 KB	360 X 400	14	31.5	70
2, 3	4	16/256 KB	720 X 400	28	31.5	70
4, 5	4	4/256 KB	320 X 200	12.5	31.5	70
6	4	2/256 KB	640 X 200	25	31.5	70
7	4	Mono	720 X 400	28	31.5	70
D	4	16/256 KB	320 X 200	12.5	31.5	70
E	4	16/256 KB	640 X 200	25	31.5	70
F	4	Mono	640 X 350	25	31.5	70
10	4	16/256 KB	640 X 350	25	31.5	70
11	4	2/256 KB	640 X 480	25	31.5	60
12	4	16/256 KB	640 X 480	25	31.5	60
12+	4	16/256 KB	640 X 480	31.5	37.5	75
13	8	256/256 KB	320 X 200	12.5	31.5	70

Table 2 Extended VGA Modes

Mode(s) in Hex	BPP	Colors	Resolution	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)
14, 55	8	16/256KB	1056 X 400	41.5	31.5	70
54	8	16/256KB	1056 X 350	41.5	31.5	70
58, 6A	8	16/256KB	800 X 600	40	37.8	60
58, 6A	8	16/256KB	800 X 600	49.5	46.9	75
5C	8	256/256KB	800 X 600	36	35.2	56
5C	8	256/256KB	800 X 600	40	37.9	60
5C	8	256/256KB	800 X 600	49.5	46.9	75
5D	8	16/256KB (interlaced)	1024 X 768	44.9	35.5	87
5D	8	16/256KB	1024 X 768	65	48.3	60
5D	8	16/256KB	1024 X 768	75	56	70
5D	8	16/256KB	1024 X 768	78.7	60	75
5F	8	256/256KB	640 X 480	25	31.5	60
5F	8	256/256KB	640 X 480	31.5	37.5	75
60*	8	256/256KB (interlaced)	1024 X 768	44.9	35.5	87
60*	8	256/256KB	1024 X 768	65	48.3	60
60*	8	256/256KB	1024 X 768	75	56	70
60*	8	256/256KB	1024 X 768	78.7	60	75
64*	16	64KB	640 X 480	25	31.5	60
64*	16	64KB	640 X 480	31.5	37.5	75
65*	16	64KB	800 X 600	36	35.2	56
65*	16	64KB	800 X 600	40	37.8	60
65*	16	64KB	800 X 600	49.5	46.9	75
66*	16	32KB Direct/256KB Mixed	640 X 480	25	31.5	60
66*	16	32K Direct/256KB Mixed	640 X 480	31.5	37.5	75
67*	16	32K Direct/256KB Mixed	800 X 600	40	37.8	60
67*	16	32K Direct/256KB Mixed	800 X 600	49.5	46.9	75
6C*	16	16/256KB (interlaced)	1280 X 1024	75	48	87

* Requires 1 MB video memory option.

For more information refer to the *Cirrus Logic CL-GD54M40 Reference Manual, Cirrus Logic CL-GD54M40 Advance Product Bulletin*, or http://www.cirrus.com/

1.8 Secondary PCI I/O Subsystem (PCI-S)

The i960 RD I/O processor performs the function of PCI-to-PCI bridge on the M440LX DP Server, which extends the electrical capacity of primary PCI bus segment to form a secondary PCI segment: PCI-S. The i960 RD I/O processor forwards all PCI transactions on the primary PCI segment, that fall within specified address ranges, to the secondary PCI segment. It also transfers all PCI transactions on the secondary PCI segment, that fall within specified address ranges, to PCI-P. The i960 RD I/O processor is packaged in a 352-lead Plastic Ball Grid Array (PBGA).

The Secondary PCI bus segment contains four 120-pin, 32-bit PCI expansion slot connectors (S0, S1, S2, and S3), and two Symbios SYM53C875 SCSI-3 Ultra SCSI controllers.

Table 3 PCI-S Configuration IDs

IDSEL Value	Device
16	SYM53C875 SCSI A
17	PCI Slot S0
18	PCI Slot S1
19	PCI Slot S2
20	SYM53C875 SCSI B
21	PCI Slot S3

PCI-S Arbitration

Because the Secondary PCI bus handles seven PCI masters: slots S0 through S3, the two Ultra SCSI controllers, and the i960 RD I/O processor, all PCI masters must arbitrate for PCI access using resources supplied by the i960 RD PCI-to-PCI bridge. The i960 RD I/O processor secondary PCI interface arbitration connections are internal to the device. The internal arbitration unit parks the i960 RD I/O processor secondary PCI interface on the bus when no other agent is requesting it. This maximizes the performance of primary to secondary bus transactions when no other PCI masters own the secondary PCI bus.

Wide SCSI Subsystem

The Secondary PCI bus segment provides two embedded Symbios SYM53C875 Ultra SCSI controllers. The SYM53C875 controller supports 8-bit SCSI (10 MB/s or 20 MB/s) or 16-bit Wide SCSI (20 MB/s or 40 MB/s) transfers, in a 169-in BGA package. The SYM53C875 is a highly integrated PCI-to-SCSI solution containing a high-performance PCI bus interface, DMA controller, internal SCRIPTS engine, and a high-performance SCSI bus interface.

The SYM53C875 controller supports all of the required 32-bit PCI signals including **PERR_L** and **SERR_L**. Full PCI parity is maintained on the entire data path through the chip. The SYM53C875 controller does not support the **CLKRUN_L**, **LOCK_L**, **SBO_L**, **SDONE_L** and **TRST_L** signals. Support for these signals is specified as optional under the PCI 2.1 Specification.

PCI performance features include bursts of up to 128 Dwords for data rates of greater than 110 MB/s. The SCRIPTS engine is a special high-speed processor optimized for SCSI protocol. The SCRIPTS engine and 4 KB of internal RAM for instruction storage can execute complex SCSI bus sequences independently of the host processor. The internal DMA, in combination with the SCRIPTS engine, creates a tightly coupled connection between PCI and SCSI bus interfaces for optimum performance.

1.9 SCSI Interface

The SYM53C875 controller offers 8-bit or 16-bit SCSI operation at data transfer rates of 10, 20, or 40 MB/s. The SYM53C875 controller uses Tolerant* technology for improved data integrity when running in the fastest SCSI transfer modes. Tolerant technology includes active negation of SCSI signals when driving and programmable input signal filtering when receiving. Active negation outputs reduce the chance of data errors by actively driving both polarities of the SCSI bus avoiding indeterminate voltage levels and common-mode noise on long cable runs. The SYM53C875 controller also offers controls for external differential transceivers and a disk activity (LED) output.

The SYM53C875 controller supports the SCSI-2, 8 or 16-bits wide bus with odd parity generated per byte. SCSI control signals are the same for either bus width. All SCSI signals are active low. SCSI P-connector cabling connects easily. During component chip power-down, all inputs are disabled to reduce power consumption.

1.10 ISA I/O Subsystem

The ISA I/O subsystem on the M440LX DP Server provides three ISA slots and compatibility I/O via the I/O controller. One ISA slot is physically shared with a secondary PCI slot (PCI-S3). The second of the two dedicated slots (ISA-2) only supports half-length cards. The other two ISA slots support full-length cards. The ISA bus also supports an embedded I/O APIC, Flash BIOS, and an interface to the server management hardware. The National PC87307 SuperI/O controller, which resides on the ISA bus, supports direct connection of keyboard, mouse, floppy drive, and standard parallel and serial ports.

The ISA I/O subsystem also connects with the I/O APIC and MISSMIC. The I/O APIC handles interrupts produced by ISA devices for the MP environment. The MISSMIC is a custom ASIC that provides the host interface to the board set server management processor, performs interrupt steering and rerouting, and NMI/SMI error interrupt control.

National SuperI/O Controller - Serial, Parallel, Floppy, KB/Mouse

The National 87307 SuperI/O device contains all of the necessary circuitry to control two serial ports, one parallel port, floppy disk, and PS/2-compatible keyboard and mouse. The M440LX DP Server provides the connector interface for each. In addition, this device contains a real-time clock.

Two 9-pin connectors are provided in one stacked 9-pin D-Sub housing for Serial port A and Serial port B. By default port A is physically the top connector, port B is on the bottom. Both ports are compatible with 16550A and 16450, and may be relocated. Each serial port can be set to one of four different COMx ports, and can be enabled separately. When enabled, each port can be programmed to generate edge or level sensitive interrupts. When disabled, serial port interrupts are available to add-in cards.

The 25/15 pin connector stacks the parallel port connector over the VGA connector. The 87307 controller provides an IEEE 1284-compliant 25-pin bi-directional parallel port. BIOS programming of the 87307 controller registers enable the parallel port, and determine the port address and interrupt. When disabled, the interrupt is available to add-in cards.

The FDC on the 87307 controller is functionally compatible with the PC8477 which contains a superset of the floppy disk controllers in the DP8473 and N82077. The baseboard provides the 24 MHz clock, termination resistors, and chip selects. All other FDC functions are integrated into the 87307 controller including analog data separator and 16-byte FIFO.

The keyboard and mouse connectors are mounted within a single stacked housing. The mouse connector is stacked over the keyboard connector. External to the board they appear as two connectors. The keyboard and mouse controller is software compatible with the 8042AH and PC87911. The keyboard and mouse connectors are PS/2 compatible.

While the National PC87307 SuperI/O controller contains a Real Time Clock, the M440LX DP Server board set utilizes the RTC in the Intel PIIX4.

1.11 System Reset Control

Reset circuitry on the M440LX DP Server board set looks at resets from the front panel, PIIX4, I/O controller, and processor subsystem to determine proper reset sequencing for all types of reset. The reset logic is designed to accommodate a variety of ways to reset the system, either by a power-up, a hard reset, or a programmed (soft) reset.

The following diagram shows the critical board set signals associated with reset.

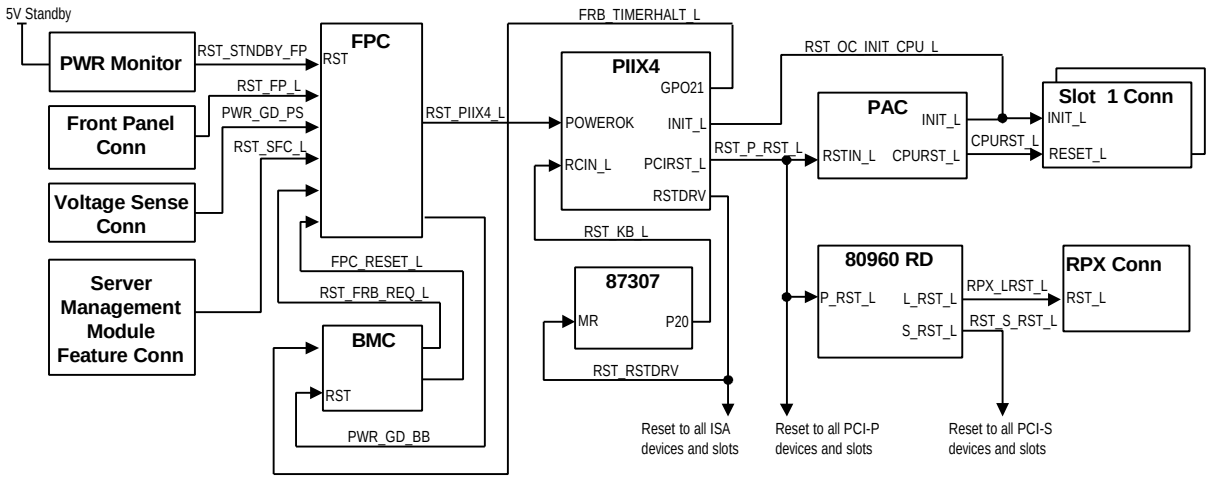

Figure 4 Reset Flow Diagram

Reset circuitry on the M440LX DP Server board set looks at resets from the front panel, PIIX4, I/O controller, and processor subsystem to determine proper reset sequencing for all types of reset.

The most common "reset" is the power-up or power-on sequence that must happen to turn on the server system. When a valid input voltage level is provided to the power supply, 5V standby power will be applied to the board set. A power monitor circuit on 5V standby will assert a signal, causing the front panel controller (FPC) to be reset. The FPC monitors and controls key events in the system related to reset and power control.

A hard reset may be initiated by software, by the user resetting the system through the front panel switch, or through the Server Management Module add-in card. For software initiated hard reset, Intel recommends using the PIIX4 Reset Control register.

A soft reset causes the processors to begin execution in a known state without flushing cache resources or internal buffers. Soft resets may be generated by the keyboard controller (located in the National 87307 controller), by the Intel PIIX4, or by the Intel 440LX PAC.

A programmed reset may be initiated by software. Although the reset control is provided in the registers of the Intel 440LX PAC, the component documentation recommends that the PIIX4 Reset Control register be used instead for programmed resets

1.12 Clock Generation and Distribution

There are three clock sources used on the M440LX DP Server board set. The memory module generates the 33.3 MHz PCI reference clock, the 66.6 MHz host clocks, and the 14.318 MHz APIC clocks. A clock generator on the board set generates a 40 MHz clock for the embedded SCSI controllers, a 24 MHz clock for the SuperI/O controller, a 16 MHz clock for the BMC, and a 14.318 MHz clock for ISA devices. The Front Panel Controller has its own crystal, providing a 12 MHz time reference to that controller, since it operates off the 5V standby. The board set also has a low skew clock buffer to distribute the PCI reference clock to all the embedded PCI devices and to all PCI slots.

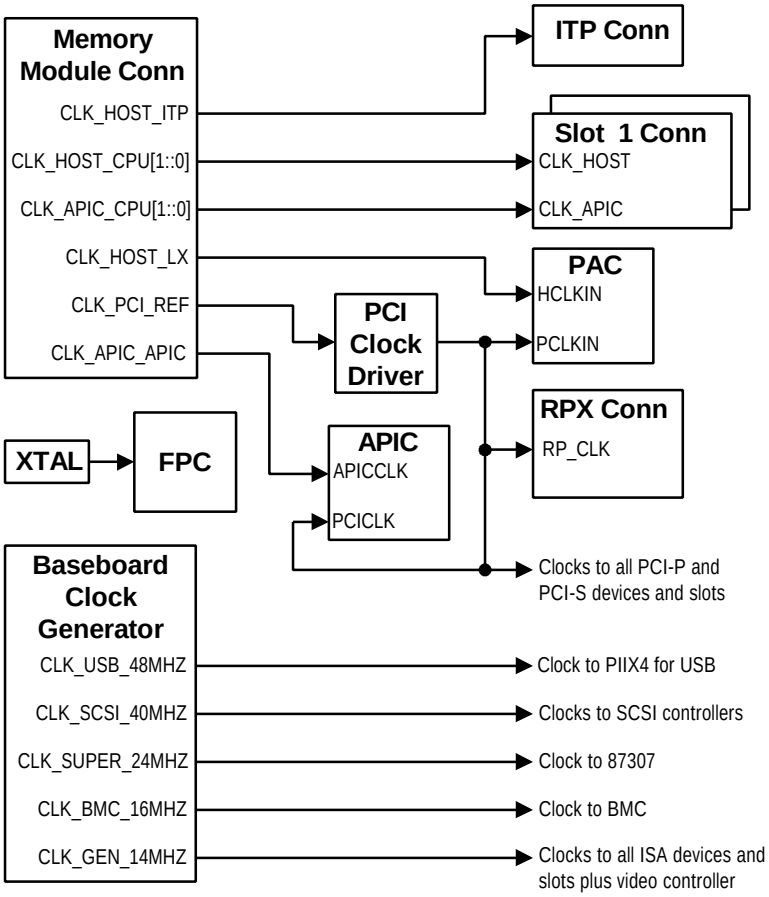

Figure 5 M440LX DP Server Board set Clock Distribution

1.13 Interrupts and I/O APIC

The M440LX DP Server interrupt architecture accommodates both PC-compatible 8259 PIC modes and dual-processor APIC mode interrupts. In addition, interrupt steering is required for offloading of PCI interrupts to the i960 RD I/O processor and control of rerouting to ISA IRQs. Special logic is required to implement this custom interrupt scheme. The M440LX DP Server Interrupt Steering and Server Management Interface Controller (MISSMIC) provides this function.

For PC-compatible mode, the Intel PIIX4 provides two 82C59-compatible interrupt controllers. The two embedded interrupt controllers are cascaded with interrupt levels 8-15 entering on the second level of the primary interrupt controller (per normal PC/AT compatibility). A single interrupt signal is presented to the processors, to which only one processor will respond.

For APIC mode, M440LX DP Server board set interrupt architecture incorporates the Intel I/O APIC device to manage and broadcast interrupts to local APICs in each processor. The I/O APIC monitors interrupt requests from devices. On occurrence of an interrupt, the I/O APIC sends a message corresponding to the interrupt across a three wire serial interface to the local APICs. The APIC bus minimizes interrupt latency time for compatibility interrupt sources, in both single and dual processor operations in Windows NT, NetWare, and the leading UNIX operating systems.

The entire board set APIC structure consists of a single I/O APIC device with 24 input interrupt requests. The I/O APIC also manages the 16 PC/AT compatibility interrupts and also manages the 8 interrupt levels associated with PCI interrupts on the Primary and Secondary PCI bus segments. This design supports more efficient interrupt processing and offloads the polling of interrupts from devices beneath the i960 RD bridge by the host processor.

The i960 RD I/O processor manages interrupts from PCI devices beneath it and services the interrupt locally with the I/O APIC providing interrupt notification to the host processor. This allows the i960 RD I/O processor to lend intelligence to handling of interrupts from add-in cards and embedded SCSI devices by intercepting the interrupt and servicing it locally. This I_2O interrupt steering logic is under program control using a 5-bit control register in the i960 RD I/O processor that determines the mapping of PCI interrupts from each device and slot. The interrupts are then logically ordered in the MISSMIC as four interrupts to the i960 RD or I/O APIC. The i960 RD I/O processor can also generate an interrupt on PCI-P using the “door bell” messaging mechanism.

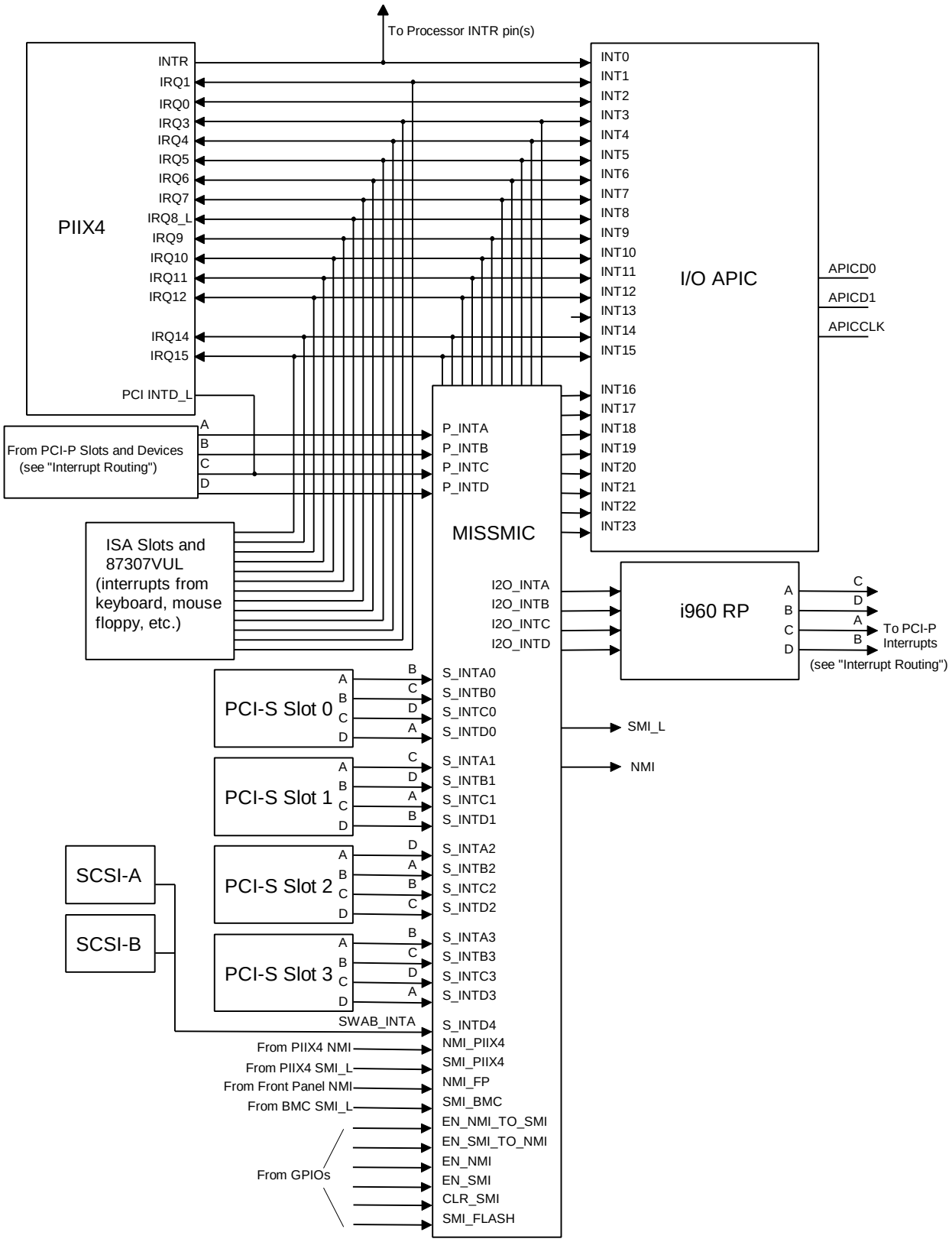

Figure 6 M440LX DP Server Interrupt Structure Interrupt Routing

The following table describes the interrupt routing of the Primary PCI bus segment interrupts. Interrupts shared between slots are cascaded to avoid conflicts, since most PCI cards use P_INTA as their external interrupt connection.

Table 4 PCI-P Interrupt Routing

PCI-P INT	I/O APIC Interrupt	PCI-P slot P0	PCI-P slot P1	8-bit SCSI	PCI-P slot P2	Cirrus SVGA	Intel i960 RD	Intel PIIX4
P_INTA	16	A	D	-	B	-	C	pull-up
P_INTB	17	B	A	-	C	-	D	pull-up
P_INTC	18	C	B	A	D	-	A	pull-up
P_INTD	19	D	C	-	A	-	B	C

Table 5 describes the interrupt routing of the Secondary PCI bus segment interrupts. Even though each interrupt has an input pin to the MISSMIC (for I_2O purposes), interrupts are cascaded between PCI-S slots to simplify logic in the MISSMIC when directing them to I/O APIC inputs.

Table 5 PCI-S Interrupt Routing

PCI-S INT	I/O APIC Interrupt	PCI-S slot S0	PCI-S slot S1	PCI-S slot S2	PCI-S slot S3	Symbios SCSI-A	Symbios SCSI-B	Intel i960 RD_INT
S_INTA	20	D	C	B	D	A	A	RD_INTA
S_INTB	21	A	D	C	A	-	-	RD_INTB
S_INTC	22	B	A	D	B	-	-	RD_INTC
S_INTD	23	C	B	A	C	-	-	RD_INTD

1.14 PCI Interrupt Rerouting

Some multi-processing (MP) operating systems are currently unable to handle interrupts from PCI slots and devices as pure PCI interrupts, via inputs 16-19 (Primary PCI bus) or 20-23 (Secondary PCI bus) of the I/O APIC. These MP operating systems expect PCI interrupts to be delivered as ISA IRQs. MP operating systems may also expect some interrupts from the PC-compatible PIC in the PIIX4 and others from the I/O APIC (Mixed Mode). Some device drivers check whether the device uses one of the traditional IRQs and if not (when the PCI interrupt is connected directly to the I/O APIC), the drivers may fail to install or run properly. The PIIX4 performs internal PCI to IRQ interrupt steering so PCI interrupts can be delivered to the APIC. However, the PCI interrupt steering feature is uni-directional, which means that it cannot redirect PCI interrupts to the I/O APIC.

For these reasons, the MISSMIC incorporates an external PCI to IRQ rerouter circuit that can be programmed to pass PCI interrupts through to inputs 16-19 and 20-23 of the I/O APIC, or deliver a specific PCI interrupt to an IRQ. Using the SCU, a PCI interrupt can be individually rerouted to one of these IRQ lines: IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, IRQ9, IRQ10, IRQ11, IRQ12, IRQ14, or IRQ15.

Interrupt Sources

The interrupt map is defined using configuration registers in the PIIX4 and the I/O controller. The I/O redirection registers in the I/O APIC are provided for each interrupt signal, which define hardware interrupt signal characteristics for APIC messages sent to local APIC(s).

Table 6 Interrupt Definitions

Interrupt	I/O APIC level	Description
INTR	INT0	Processor interrupt
NMI		NMI from MISSMIC to processor
IRQ1	INT1	Keyboard interrupt
Cascade	INT2	Interrupt signal from second 8259 in PIIX4
IRQ3	INT3	Serial port A or B interrupt from 87307VUL device, user-configurable.
IRQ4	INT4	Serial port A or B interrupt from 87307VUL device, user-configurable.
IRQ5	INT5	Parallel port - LPT2
IRQ6	INT6	Floppy disk
IRQ7	INT7	Parallel port - LPT1
IRQ8_L	INT8	RTC interrupt
IRQ9	INT9	Open
IRQ10	INT10	Open
IRQ11	INT11	Open
IRQ12	INT12	Mouse interrupt
	INT13	Reserved
IRQ14	INT14	Compatibility IDE interrupt from primary channel IDE devices 0 and 1
IRQ15	INT15	Open
P_INTA_L	INT16	PCI-P Interrupt signal A
P_INTB_L	INT17	PCI-P Interrupt signal B
P_INTC_L	INT18	PCI-P Interrupt signal C
P_INTD_L	INT19	PCI-P Interrupt signal D
S_INTA_L	INT20	PCI-S Interrupt signal A
S_INTB_L	INT21	PCI-S Interrupt signal B
S_INTC	INT22	PCI-S Interrupt signal C
S_INTD_L	INT23	PCI-S Interrupt signal D
SMI_L		System Management Interrupt. General-purpose error indicator from a control PAL that provides an SMI_L from non-traditional error sources (PERR_L, SERR_L, and others).

1.15 Baseboard Jumper Settings

A single 15-pin inline header provides a total of four 3-pin jumper blocks that control various configuration options, as shown in the figure below. The shaded areas show default jumper placement for each configurable option.

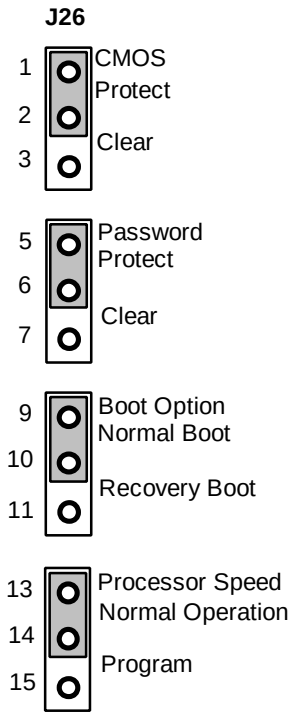

Figure 7 Configuration jumpers

Table 7 Configuration jumper options

Option	Description
CMOS Clear	If pins 1 and 2 of J26 are jumpered (default), NVRAM contents are preserved through system reset. If pins 2 and 3 of J26 are jumpered, NVRAM contents are set to manufacturing default during system reset.
Password Clear	If pins 5 and 6 of J26 are jumpered (default), the current system password is maintained during system reset. If pins 6 and 7 of J26 are jumpered, the password is cleared on reset.
Recovery or Normal BIOS boot block	If pins 9 and 10 of J26 are jumpered (default), address A16 is inverted so system BIOS does not reside at the top of flash, where the write-protected Recovery BIOS region is located. If the system BIOS is corrupted (i.e. power outage during BIOS update) and it is unable to reload a fresh copy from the floppy disk, then install the jumper between pins 10 and 11 of J26, which causes A16 to become non-inverted and enables the system to boot from the Recovery BIOS.
Processor Speed	If pins 13 and 14 of J26 are jumpered (default), the processor speed is write-protected. If pins 14 and 15 of J26 are jumpered, the processor speed is erasable and programmable via the BIOS setup program. ***WARNING: Incorrect programming of the processor speed can cause erratic system behavior or processor failure.***

1.16 Memory Modules

Although the two memory modules have different requirements and functionality, both memory modules require the use of gold plated leads on DIMMs used in the module. This is the result of electrolysis issues resulting from mixing different metal types. An oxidizing, insulating layer can build up as a result of the electrolysis. This build up can result in premature failure of memory.

Intel provides ECC circuitry as a function of the 440LX chipset. In order to enable ECC functionality, it is necessary to use ECC DIMMs.

EDO DRAM Array

The memory array on the module consists of eight 72-bit DIMM sockets. These allow for up to 1GB of DRAM when using 128MB 3.3V JEDEC standard parallel detect DIMMs. ECC bits support the detection and correction of single bit and detection of double bit errors by the memory controller in the Intel 82443 PAC. The memory controller in the 82443 PAC set can automatically detect and initialize the memory array, depending upon the type, size, and speed of installed DIMM devices. DIMMs sizes of 8, 16, 32, 64, and 128 MB are supported. A list of tested DIMMs is available through Intel.

Currently, although 1GB total memory is possible, the Pentium II processor SEC cartridge can only cache 512 MB. Therefore, it is only necessary to populate the memory module with up to 512 MB for maximum system performance. Loading the memory module with eight (50/60 ns) EDO DIMMs gives a timing profile of x-3-3-3 for a burst read and x-3-3-3 for a burst write while a loading of four DIMMs can provide a x-2-2-2 profile. *Note that faster timing is available when only four DIMMs are installed.*

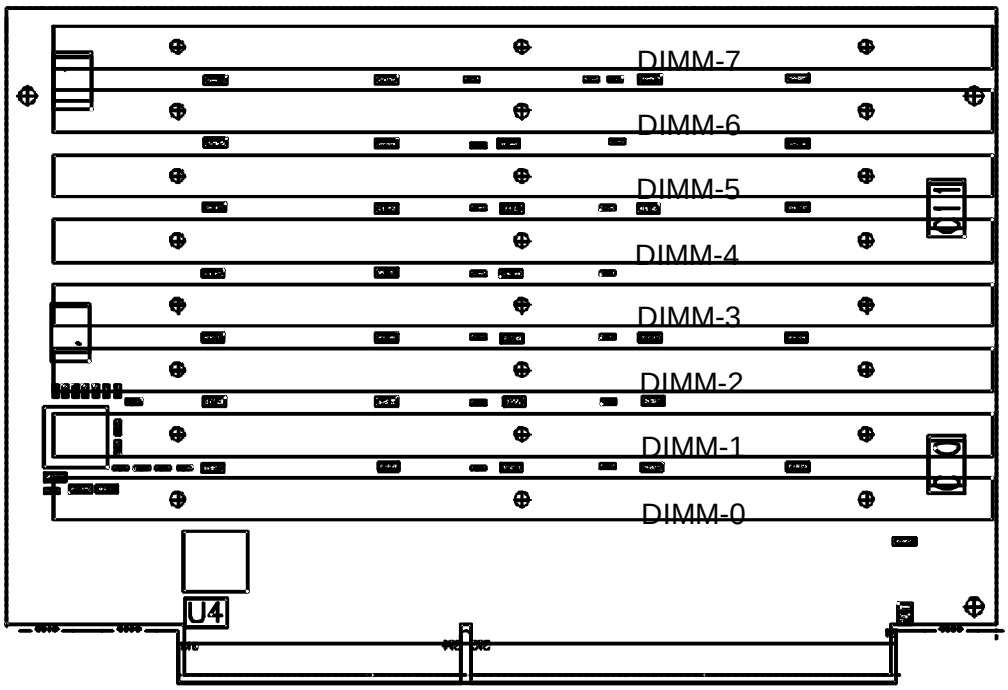

Figure 8 Memory Module Layout

Memory is partitioned as eight banks of DRAM, one bank per installed DIMM. The chipset provides a row address strobe (RCSAn_L) for each bank, plus a copy of each (RCSBn_L) to evenly distribute the loading incurred by the DIMM array, resulting in improved signal quality. Column address strobes (CDQAx_L) for all data bits are also provided. DIMM sockets should be populated in sequence, i.e. DIMM-0, then DIMM-1, and so on with DIMM-7 last. If four DIMMs are used rather than eight, faster timing is available. The following diagram shows the correspondence between installed DIMMs, RCSAn_L/RCSBn_L signals, and DRAM row boundary (DRB) values.

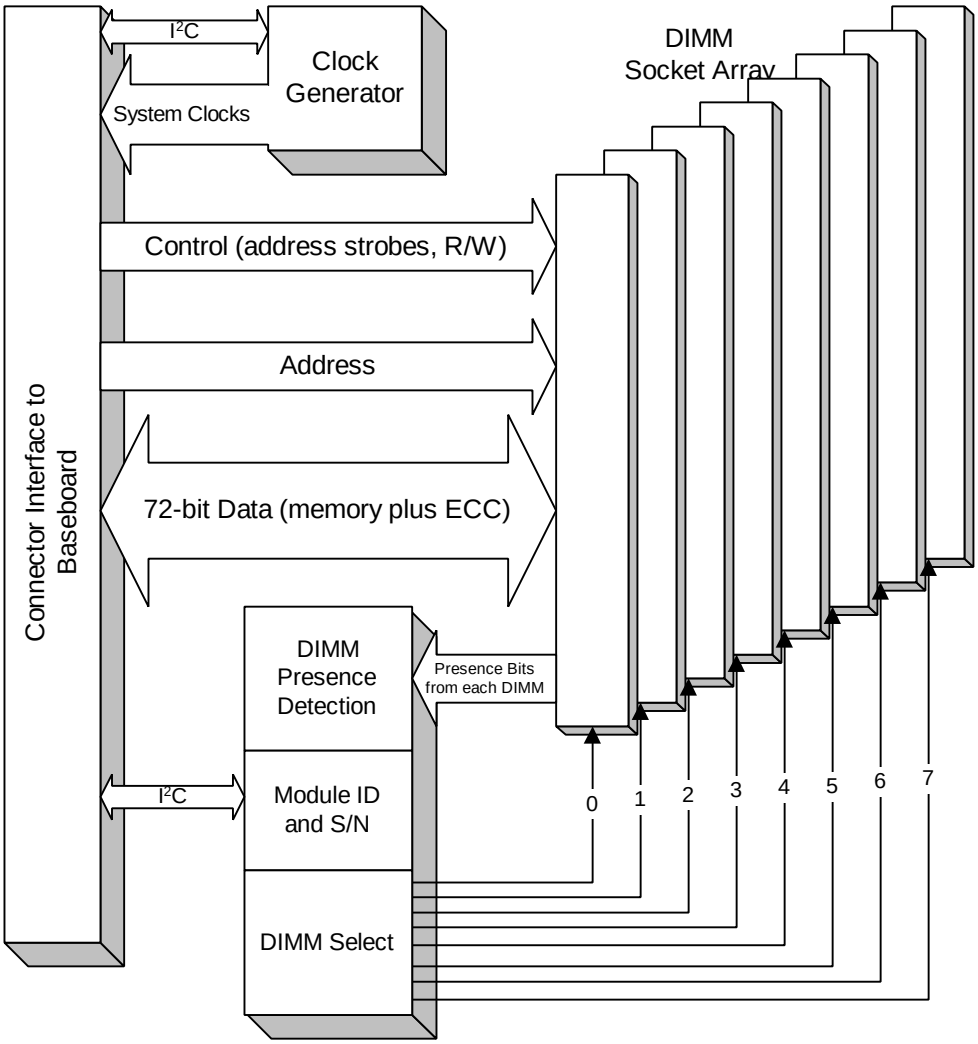

Figure 9 M440LX DP Server EDO Memory module

The MB440LX DP Server EDO memory module provides clock generation onboard. Each SDRAM DIMM requires four clock inputs, so placing clock generation on the memory module eliminates the need to run multiple clocks through the connector interface.

The Baseboard Management Controller (BMC) can access server management information stored locally on the memory module through the I^2C interface. This information includes the board type,

serial number, number of installed DIMMs, and their speed. This interface is also used to control testability features, such as the disabling of individual DIMMs or controlling of clock generation.

A 242-pin “Slot 1”-style edge connector on the module provides connection of address, data, ECC, control, I^2C, power, clocks, and other signals between memory and the baseboard. The main body of this connector interface is based on signals provided by the 440LX PAC. It is compatible with the SDRAM version of the module, since the chipset supports both EDO and SDRAM devices.

SDRAM Array

The memory array on the module consists of four 72-bit DIMM sockets . These allow for up to 512MB of DRAM when using 128MB 3.3V standard SDIMMs. ECC bits support the detection and correction of single bit and detection of double bit errors by the memory controller in the Intel 82443 PAC. The memory controller in the 82443 PAC set can automatically detect and initialize the memory array, depending upon the type, size, and speed of installed SDIMM devices. SDIMMs sizes of 8, 16, 32, 64, and 128 MB are supported. A list of tested SDIMMs is available through Intel. If fewer than 4 SDIMMs are installed, populate SDIMM sockets in this order: J1, J2, J3, J4 for optimum signal integrity.

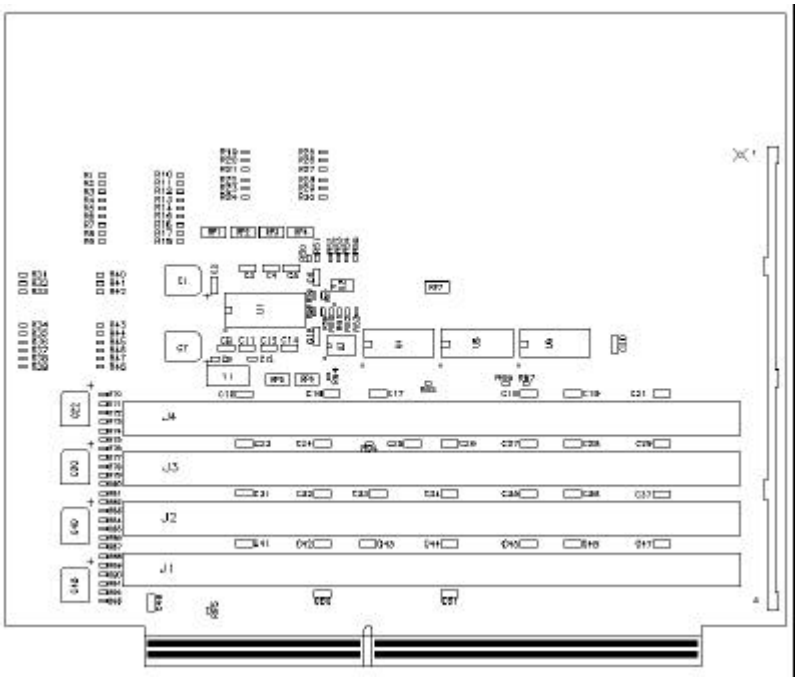

Figure 10 M440LX DP Server SDRAM Memory Module

Memory is partitioned as four banks of SDRAM, one bank per installed SDIMM. The chipset provides a row address strobe (RCSAn_L) for each bank, plus a copy of each (RCSBn_L) to evenly distribute the loading incurred by the SDIMM array, resulting in improved signal quality. Column address strobes (CDQAx_L) for all data bits are also provided. SDIMM sockets should be populated in sequence, i.e. SDIMM-0, then SDIMM-1, and so on with SDIMM-3 last. The following diagram shows the correspondence between installed SDIMMs, RCSAn_L/RCSBn_L signals, and SDRAM row boundary (DRB) values.

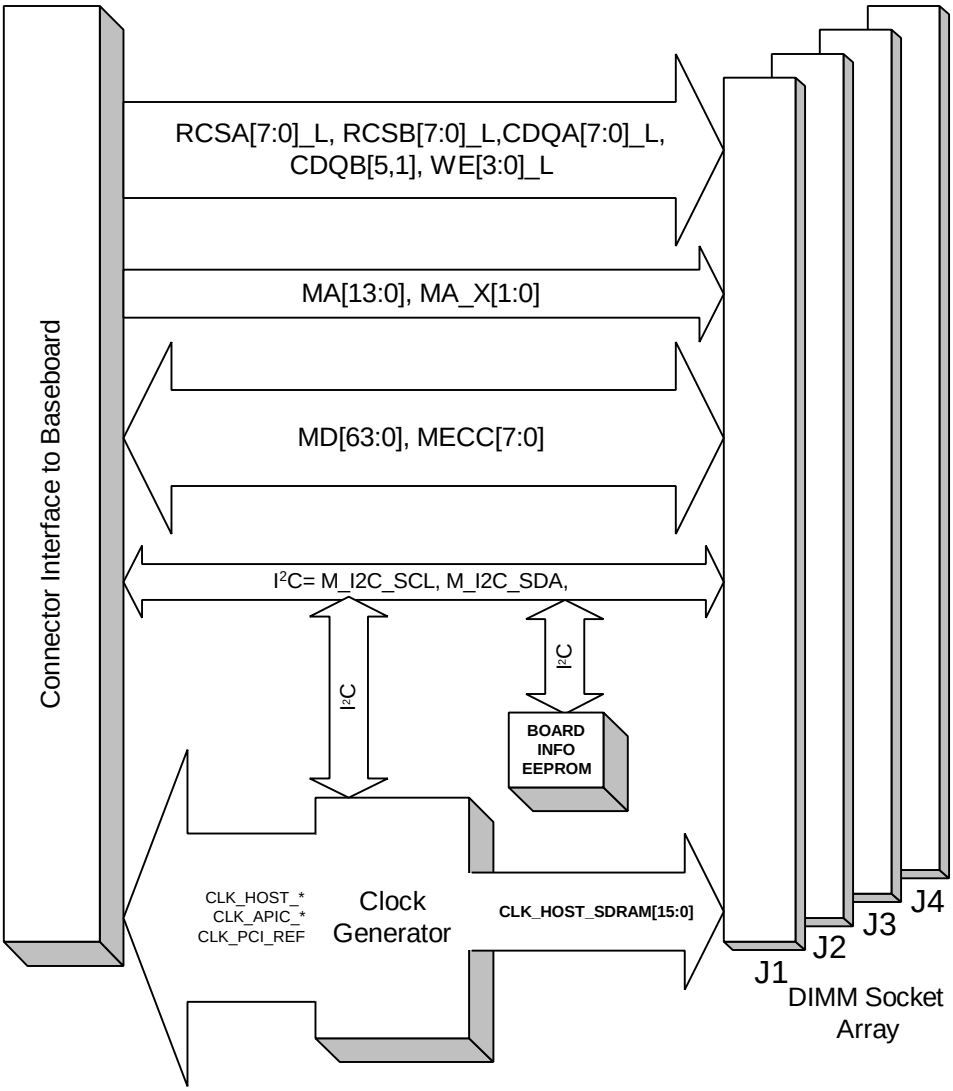

Figure 11 M440LX DP Server EDO Memory module

The M440LX DP Server SDRAM memory module provides clock generation onboard. Each SDRAM DIMM requires 4 clock inputs, so placing clock generation on the memory module eliminates the need to run multiple clocks through the connector interface.

The Baseboard Management Controller (BMC) can access server management information, stored locally on the memory module, through the I^2C interface. This information includes the board type, serial number, number of installed DIMMs, and their speed. This interface is also used to control testability features, such as the disabling of individual DIMMs or controlling of clock generation.

A 242-pin “Slot 1”-style edge connector on the module provides connection of address, data, ECC, control, I^2C, power, clocks, and other signals between memory and the baseboard. The main body of this connector interface is based on signals provided by the 82443 PAC. It is compatible with the SDRAM version of the module, since the chipset supports both EDO and SDRAM devices.

1.17 RPX Module

The RPX module is an option for the M440LX DP Server board set. Installation of the RPX module enables the use RAID configurations through the integrated Symbios SYM53C875 Ultra SCSI controllers.

For more information on I_2O see http://developer.intel.com/design/IIO/

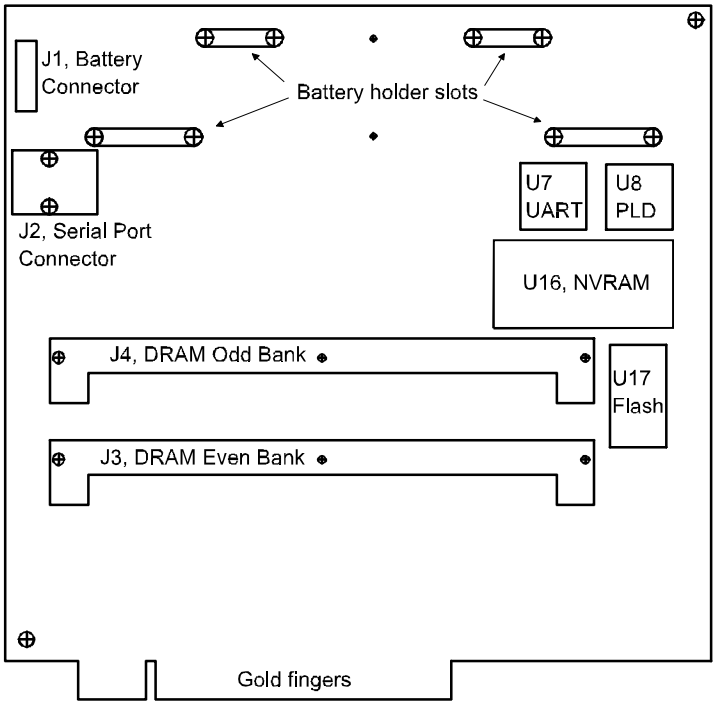

Figure 12 RPX Module Diagram

The RPX module DRAM subsystem consists of two x36 SIMM sockets providing one or two banks of interleaved DRAM. The data path and memory is protected with byte wide parity. The interleaved DRAM subsystem supports burst memory reads with a 2-0-0-0 wait state profile, and burst memory writes with a 1-0-0-0 wait state profile using 60 ns memory devices. SIMM devices of 70 ns and 50 ns are not supported on the RPX module. Both SIMM sockets must be populated with the same type and density of memory. A list of approved SIMMs is available from Intel.

The RPX module will support a single, byte wide, bank of non-volatile SRAM (NVRAM). This memory can be written on a byte-wide basis, compared to flash memory, which can also be written to, but only on a block basis. The NVRAM will reside in the memory space controlled by the bank 1 memory controller on the 960 RD I/O processor. The board design will support 8 KB or 32 KB of NVRAM. This is not a field upgrade option.

Server management logic is included on the RPX module to provide inventory management information and to monitor battery temperature. The server management information is accessible by the board set through the I^2C interface.

Battery Backup

The RPX module contains circuitry to provide battery backup of the DRAM SIMMs in the event of a system power failure. This allows critical data (such as write-back disk cache data) to be preserved. The battery is mounted on the upper portion of the RPX module.

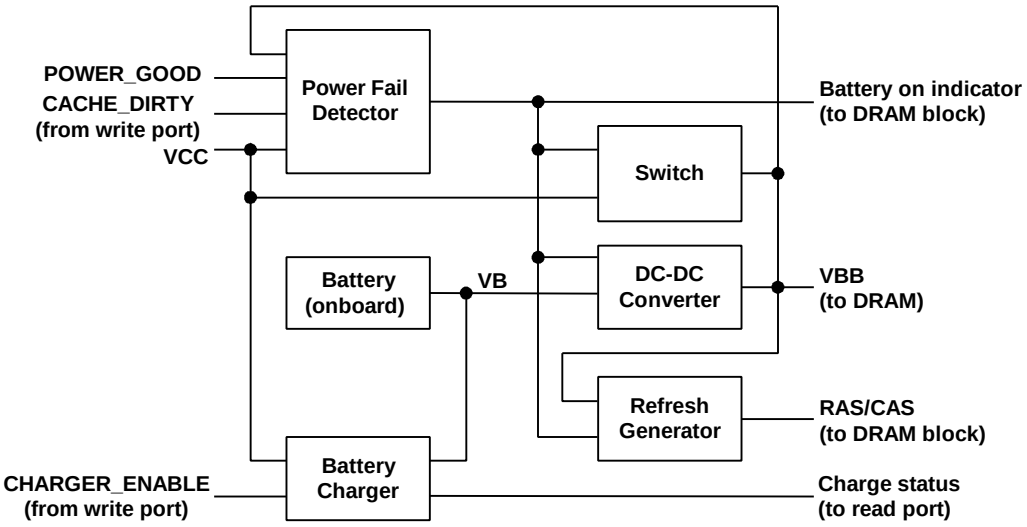

Figure 13 Battery Backup Block Diagram

The CACHE DIRTY and CHARGER ENABLE signals from the write port is used to control the battery circuitry. If there is dirty data in the cache (CDIRTY# asserted) when the power fail detector senses system power (VCC) dropping, it will switch the source of VBB from VCC to the battery. If there is no dirty data in the cache, VBB will drop when VCC drops. The battery is physically a 2.4V device, so a DC-to-DC converter is required to step this voltage up to 5V. In addition to the battery charging and switching circuitry, the battery backup block also includes circuitry to generate the DRAM refresh. This circuitry is activated when a power failure has occurred, and generates CAS# before RAS# refresh cycles.

The battery charger can be enabled or disabled via the CHARGER ENABLE bit in the write port. The status of the battery can be read through the read port to detect battery presence/absence and charge state: charge pending, charge in progress, or charge complete.

Note: The battery must be disconnected prior to removing and servicing the RPX module. Disconnecting the battery prevents potentially installing or removing a SIMM that has power applied to it.

2. Server Management

The M440LX DP Server board set Server Management features are implemented using two separate controllers and one ASIC:

- Baseboard Management Controller (BMC)
- Front Panel Controller (FPC)
- M440LX DP Server Interrupt Steering and Server Management Interface Chip (MISSMIC)

The management controllers are specially programmed to monitor various server management functions and communicate their management information on an internal I^2C-based "Intelligent Management Bus". The Intelligent Management Bus extends throughout the board set, processor SEC cartridge, and system chassis. The BMC can also be accessed from the ISA bus via the MISSMIC ASIC.

In addition to the management controllers implemented on the baseboard and processor SEC cartridge, the chassis may implement additional management controllers that connect to the Intelligent Management Bus.

For example, the Balboa-II chassis implements:

- Power Share Controller (PSC)
- Hot-swap Controller (HSC)

The following diagram illustrates M440LX server management architecture.

Figure 14 M440LX DP Server Management Architecture

2.1

Baseboard Management Controller (BMC)

The BMC is an 8051-compatible controller located on the M440LX DP Server board set. The BMC directly monitors baseboard power supply and SCSI termination voltages using a separate onboard Analog to Digital Converter (ADC), and checks the status of the fan failure indicators on the baseboard. The BMC also monitors system temperature sensors.

If enabled, the BMC will generate an internal event message when any monitored parameter is outside defined thresholds. This triggers the BMC's System Event Logging function, causing it to store the event in the System Event Log. The BMC acts as the primary communications gateway between ISA and the Intelligent Management Bus. System Management Software and BIOS goes through the BMC to communicate with other controllers and devices on the IMB, such as the FPC.

The BMC monitors processor power supply voltage levels, provides access to DIMM configuration and presence information, monitors processor thermal trip and internal error signals, and manages two I^2C thermal sensors; one for each processor. Fault Resilient Booting (FRB) Level 3 is also managed by the BMC, which controls the ability to boot using either processor in the event of a catastrophic processor failure.

A Serial I^2C EEPROM associated with the secondary baseboard temperature sensor also contains an EEPROM that is used by the Front Panel Controller (FPC) to retain system power-state during power-off conditions. Thus, the FPC and BMC must share access to that device.

The BMC incorporates several server management features related to the processor subsystem:

- Processor near-heatsink temperature measurement
- Processor internal over temperature output signal monitoring
- Processor error signal output monitoring
- VRM set point and output voltage monitoring
- Processor subsystem 1.5V and 2.5V voltage regulator output monitoring
- Facilities for fault-resilient booting

These signals and sensors are accessible by the Baseboard Management Controller (BMC).

Fault Resilient Booting

The BMC implements Fault Resilient Booting (FRB) levels 1, 2, and 3. If two processors are installed and the processor designated as the bootstrap processor fails to complete the boot process, FRB attempts to boot the system using the alternate processor.

- FRB level 1 is for recovery from a BIST failure detected during POST. This FRB recovery is fully handled by BIOS code.
- FRB level 2 is for recovery from a Watchdog timeout during POST. The Watchdog timer for FRB level 2 detection is implemented in the BMC.
- FRB level 3 is for recovery from a Watchdog timeout on Hard Reset/Power-up. Hardware functionality for this level of FRB is provided by the BMC on the processor subsystem.

FRB-3 is managed by the BMC, which controls the ability to boot using either processor in the event of a catastrophic processor failure. On power-up, a timer starts that can only be stopped by a healthy processor using the GPIO bit, FRB_TMRHLT_L, on the SuperI/O controller. If processor 0 fails to halt the FRB timer before timeout, the controller asserts STOP_FLUSH to the processor and asserts FRB_RST_L for 10ms. When the system comes out of reset, processor 0 is unable to act as the boot processor allowing the other processor to take over the boot process.

2.2 Front Panel Controller (FPC)

The FPC, located on the baseboard, manages system power on/off control, system reset, and front panel NMI buttons, along with an external I^2C interface. The device is powered from the +5V standby power supply, to stay alive when system power is switched off. The FPC controls main power to the baseboard and SEC Cartridge is responsible for monitoring all sources of power control both on and off the baseboard including the Front Panel, Server Monitor Module, PIIX4, and RTC power control signals. The FPC also detects chassis intrusion by monitoring an external switch.

2.3 I^2C Isolation Buffers and Auxiliary I^2C Connector

Buffers are provided to isolate the baseboard temperature sensors, auxiliary I^2C connector, and FPC from the rest of the I^2C bus. These buffers, running on the standby supply, keep the bus alive to the FPC even though main power is switched off. This allows the FPC to communicate with its I^2C EEPROM (in the secondary baseboard temperature sensor) at all times, and provides a way to remotely control power via the auxiliary I^2C connector. A shorted I^2C connection at the auxiliary I^2C connector will prevent restoration of main power.

2.4 M440LX DP Server Interrupt Steering and Server Management Interface Chip (MISSMIC)

Communication between the two controllers on the baseboard is done using the I^2C bus. Communication between this distributed controller network, SMI handler, and Systems Management Software (SMS) running on the server, is done using the BMC and MISSMIC. The MISSMIC functions as a bridge between the BMC and ISA bus. The MISSMIC also gates and redirects **SMI_L** and **NMI**, generating **SERR_L**, and performs PCI to IRQ rerouting. The MISSMIC also provides a mailbox register interface designed to work with SMS and **SMI_L** handler code across the ISA interface.

2.5 System Fan Interface

The M440LX DP Server board set provides several 3-pin, shrouded, and keyed fan connectors. Two of these connectors, located next to each Pentium II processor socket on the SEC cartridge, is for a standard fansink with +5V and GND only. The remaining connectors on the baseboard attach to a fan equipped with a sensor that indicates whether the fan is operating (tachometer fan). The sensor pins for these fans are routed to the BMC for failure monitoring. Each connector has the following pinout:

Table 7 Tachometer fan connector pinout

Pin	Signal
1	+12V
2	Fan Fail Sensor
3	GND

The fansink connector has the following pinout:

Table 8 Fansink connector pinout

Pin	Signal
1	+5V
2	no connect
3	GND

3. Memory and Other Resource Mappings

3.1 Extended Memory

Extended memory on M440LX DP Server is defined as all address space greater than 1MB. The Extended Memory region covers 4 GB of address space from addresses 0100000h to FFFFFFFFh, as shown in the following figure.

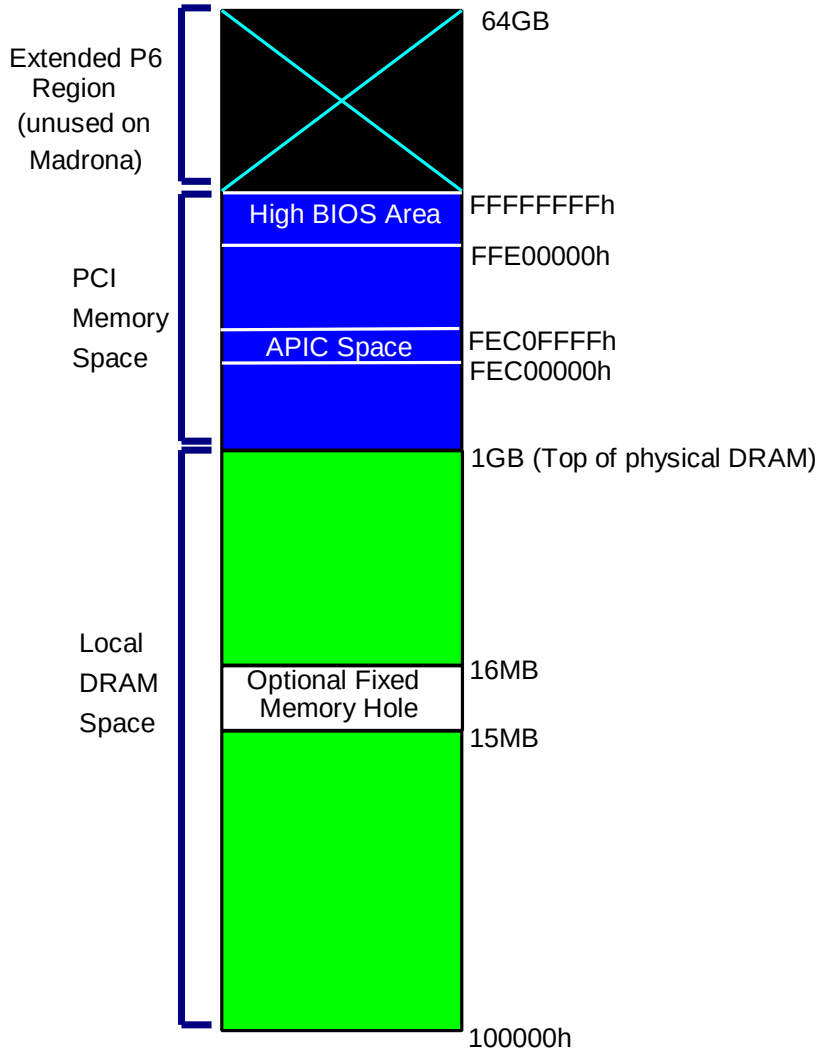

Figure 15 Extended Memory Map

3.2

I/O Map

The 82443 PAC allows I/O addresses to be mapped to the processor bus or through designated bridges in a multi-bridge system. Other PCI devices, including the PCI-to-PCI bridge and PIIX4 have built-in features that support PC-compatible I/O devices and functions, which are mapped to specific addresses in I/O space. On the M440LX DP Server board set, the PIIX4 provides the bridge to ISA functions that must be disabled in the PCI-to-PCI bridge.

The I/O map in the following table shows the location in M440LX DP Server I/O space of all directly I/O-accessible registers. PCI configuration space registers for each device control mapping in I/O and memory spaces, and other features that may affect the global I/O map. The SuperI/O controller contains configuration registers that are accessed through an index and data port mechanism.

Table 9 M440LX DP Server I/O Map

Address(es)	Resource	Device	Notes
0000h - 000Fh	DMA Controller 1	PIIX4	
0010h - 001Fh	DMA Controller 1	PIIX4	aliased from 0000h - 000Fh
0020h - 0021h	Interrupt Controller 1	PIIX4	
0022h - 0023h			
0024h - 0025h	Interrupt Controller 1	PIIX4	aliased from 0020h - 0021h
0026h - 0027h			
0028h - 0029h	Interrupt Controller 1	PIIX4	aliased from 0020h - 0021h
002Ah - 002Bh			
002Ch - 002Dh	Interrupt Controller 1	PIIX4	aliased from 0020h - 0021h
002Eh - 002Fh	Super I/O Index and Data Ports	87307	
0030h - 0031h	Interrupt Controller 1	PIIX4	aliased from 0020h - 0021h
0032h - 0033h			
0034h - 0035h	Interrupt Controller 1	PIIX4	aliased from 0020h - 0021h
0036h - 0037h			
0038h - 0039h	Interrupt Controller 1	PIIX4	aliased from 0020h - 0021h
003Ah - 003Bh			
003Ch - 003Dh	Interrupt Controller 1	PIIX4	aliased from 0020h - 0021h
003Eh - 003Fh			
0040h - 0043h	Programmable Timers	PIIX4	
0044h - 004Fh			
0050h - 0053h	Programmable Timers	PIIX4	aliased from 0040h - 0043h
0054h - 005Fh			
0060h	Keyboard Controller	87307	
0061h	NMI Status & Control Register	PIIX4	
0062h			
0063h	NMI Status & Control Register	PIIX4	aliased
0064h	Keyboard Controller	87307	
0065h	NMI Status & Control Register	PIIX4	aliased
0066h			
0067h	NMI Status & Control Register	PIIX4	aliased
0068h-006Fh			

Address(es)	Resource	Device	Notes
0070h	NMI Mask (bit 7) & RTC Address (bits 6::0)	PIIX4	
0071h	RTC Data	PIIX4	
0072h	RTC Extended Index	PIIX4	
0073h	RTC Extended Data	PIIX4	
0074h	NMI Mask (bit 7) & RTC Address (bits 6::0)	PIIX4	aliased from 0070h
0075h	RTC Data	PIIX4	aliased from 0071h
0076h-007Fh			
00A0h - 00A1h	Interrupt Controller 2	PIIX4	
00A2h- 00A3h			
00A4h - 00A15	Interrupt Controller 2)	PIIX4	aliased from 00A0h - 00A1h
00A6h 00A7h			
00A8h - 00A19	Interrupt Controller 2	PIIX4	aliased from 00A0h - 00A1h
00AAh 00ABh			
00ACh - 00ADh	Interrupt Controller 2	PIIX4	aliased from 00A0h - 00A1h
00AEh 00AFh			
00B0h - 00B1h	Interrupt Controller 2	PIIX4	aliased from 00A0h - 00A1h
00B2h	Advanced Power Management Control	PIIX4	
00B3h	Advanced Power Management Status	PIIX4	
00B4h - 00B5h	Interrupt Controller 2	PIIX4	aliased from 00A0h - 00A1h
00B6h 00B7h			
00B8h - 00B9h	Interrupt Controller 2	PIIX4	aliased from 00A0h - 00A1h
00BAh - 00BBh			
00BCh - 00BDh	Interrupt Controller 2	PIIX4	aliased from 00A0h - 00A1h
00BEh- 00BFh			
00C0h	DMA2 CH0 Base and current address	PIIX4	
00C1h	DMA2 CH0 Base and current address	PIIX4	aliased from 00C0h
00C2h	DMA2 CH0 Base and current count	PIIX4	
00C3h	DMA2 CH0 Base and current count	PIIX4	aliased from 00C2h
00C4h	DMA2 CH1 Base and current address	PIIX4	
00C5h	DMA2 CH1 Base and current address	PIIX4	aliased from 00C4h
00C6h	DMA2 CH1 Base and current count	PIIX4	
00C7h	DMA2 CH1 Base and current count	PIIX4	aliased from 00C6h
00C8h	DMA2 CH2 Base and current address	PIIX4	
00CAh	DMA2 CH2 Base and current address	PIIX4	aliased from 00C8h
00CAh	DMA2 CH2 Base and current count	PIIX4	
00CBh	DMA2 CH2 Base and current count	PIIX4	aliased from 00CAh
00CCh	DMA2 CH3 Base and current address	PIIX4	
00CDh	DMA2 CH3 Base and current address	PIIX4	aliased from 00CCh
00CEh	DMA2 CH3 Base and current count	PIIX4	
00CFh	DMA2 CH3 Base and current count	PIIX4	aliased from 00CEh
00D0h	DMA2 Status(r) Command(w)	PIIX4	
00D1h	DMA2 Status(r) Command(w)	PIIX4	aliased from 00D0h
00D2h	DMA2 Request	PIIX4	
Address(es)	**Resource**	**Device**	**Notes**
00D3h	DMA2 Request	PIIX4	aliased from 00D2h

00D4h	DMA2 Write single mastk bit	PIIX4	
00D5h	DMA2 Write single mastk bit	PIIX4	aliased from 00D4h
00D6h	DMA2 Channel mode	PIIX4	
00D7h	DMA2 Channel mode	PIIX4	aliased from 00D6h
00D8h	DMA2 clear byte pointer	PIIX4	
00D9h	DMA2 clear byte pointer	PIIX4	aliased from 00D8h
00DAh	DMA2 Master clear	PIIX4	
00DBh	DMA2 Master clear	PIIX4	aliased from 00DAh
00DCh	DMA2 Clear mask	PIIX4	
00DDh	DMA2 Clear mask	PIIX4	aliased from 00DCh
00DEh	DMA2 Read/write all mask register bits	PIIX4	
00DFh	DMA2 Read/write all mask register bits	PIIX4	aliased from 00DEh
00F0h	Clear coprocessor error	PIIX4	Resets IRQ13
03F0h - 03F7h	Floppy Disk Controller	87307	
0370h - 0375h	Secondary Floppy		
0376h	Secondary IDE		
0377h	Secondary IDE/Floppy		
04D0h	Interrupt Controller 1 Edge/Level control	PIIX4	
04D1h	Interrupt Controller 2 Edge/Level control	PIIX4	
0CA0h	Secondary PCI Interrupt Routing	MISSMIC	
0CA1h	MISSMIC Data Register	MISSMIC	Server management mailbox registers.
0CA2h	MISSMIC Control/Status Register	MISSMIC	
0CA3h	MISSMIC Flags Register	MISSMIC	
0CA4h-0CA7h	PCI to IRQ Interrupt Routing	MISSMIC	
0CF9h	Reset control	PIIX4	
0220h - 022Fh	Serial Port A		
0238h - 023Fh	Serial Port B		
02E8h - 02EFh	Serial Port B		
02F8h - 02FFh	Serial Port B		
0338h - 033Fh	Serial Port B		
03E8h - 03EFh	Serial Port A		
03F8h - 03FFh	Serial Port A (Primary)		
0278h - 027Fh	Parallel Port 3		
0378h - 037Fh	Parallel Port 2	87307	
03BCh - 03BFh	Parallel Port 1 (Primary)	87307	
0678h - 067Ah	Parallel Port (ECP)	87307	
0778h - 077Ah	Parallel Port (ECP)	87307	

Address(es)	Resource	Device	Notes
07BCh - 07BEh	Parallel Port (ECP)	87307	
0080h - 0081h	BIOS Timer		
0080h - 008Fh	DMA Low Page Register		PIIX4
0090h - 0091h	DMA Low Page Register (aliased)		PIIX4
0092h	System Control Port A (PC-AT control Port) (this port not aliased in DMA range)		PIIX4
0093h - 009Fh	DMA Low Page Register (aliased)		PIIX4
0094h	Video Display Controller		
00F8h - 00FFh	x87 Numeric Coprocessor		
0102h	Video Display Controller		
0170h - 0177h	Secondary Fixed Disk Controller (IDE)		PIIX4 (not used)
01F0h - 01F7h	Primary Fixed Disk Controller (IDE)		PIIX4
0200h - 0207h	Game I/O Port		Not used
03B4h - 03BAh	Monochrome Display Port		
03C0h - 03CFh	Video Display Controller		
03D4h - 03DAh	Color Graphics Controller		
0400h - 043Fh	DMA Controller 1, Extended Mode Registers.		PIIX4
0461h	Extended NMI / Reset Control		PIIX4
0462h	Software NMI		PIIX4
0480h - 048Fh	DMA High Page Register.		PIIX4
04C0h - 04CFh	DMA Controller 2, High Base Register.		
04D4h - 04D7h	DMA Controller 2, Extended Mode Register.		
04D8h - 04DFh	Reserved		
04E0h - 04FFh	DMA Channel Stop Registers		
0800h - 08FFh	NVRAM		
0C80h - 0C83h	EISA System Identifier Registers		PIIX4
0C84h	Board Revision Register		
0C85h - 0C86h	BIOS Function Control		
0CF8h	PCI CONFIG_ADDRESS Register		Located in PAC
0CFCh	PCI CONFIG_DATA Register		Located in PAC
46E8h	Video Display Controller		
xx00 - xx1F*	SCSI registers		Refer to SCSI chip doc.

*SCSI I/O base address is set using configuration registers.

3.3 Device Number and IDSEL Mapping

Table 10 PCI Configuration IDs and device numbers

	Primary PCI Bus		Secondary PCI Bus	
IDSEL	**Device #**	**Device**	**Device #**	**Device**
31	10100b	PIIX4	01111b	
30	10011b	i960® RD PCI-to-PCI bridge	01110b	
29	10010b		01101b	
28	10001b	CL-GD54M40 video controller	01100b	
27	10000b	PCI-P Slot 2	01011b	
26	01111b	Symbios SYM53C810	01010b	
25	01110b	PCI-P Slot 1	01001b	
24	01101b	PCI-P Slot 0	01000b	
23	01100b		00111b	
22	01011b		00110b	
21	01010b		00101b	PCI-S Slot 3
20	01001b		00100b	Wide SCSI B (SYM53C875)
19	01000b		00011b	PCI-S Slot 2
18	00111b		00010b	PCI-S Slot 1
17	00110b		00001b	PCI-S Slot 0
16	00101b		00000b	Wide SCSI A (SYM53C875)
15	00100b		N/A	
14	00011b		N/A	
13	00010b		N/A	
12	00001b		N/A	
11	00000b	Hardwired to host bridge	N/A	

4. BIOS, Setup, SCU and SCSI Utility

4.1 BIOS Overview

The term “BIOS" refers to the following:

- System BIOS, that controls basic system functionality using stored configuration values.
- Configuration Utilities (CU) consisting of Flash ROM-resident Setup utility and system memory-resident System Configuration Utility (SCU), that provides user control of configuration values stored in NVRAM and battery-backed CMOS configuration RAM.
- Flash Memory Update utility (IFLASH), that loads predefined areas of Flash ROM with Setup, BIOS, and other code/data.

The following figure shows the relationship between BIOS components and register spaces. Unshaded areas are loaded into Flash using the Flash Memory Update Utility (IFLASH).

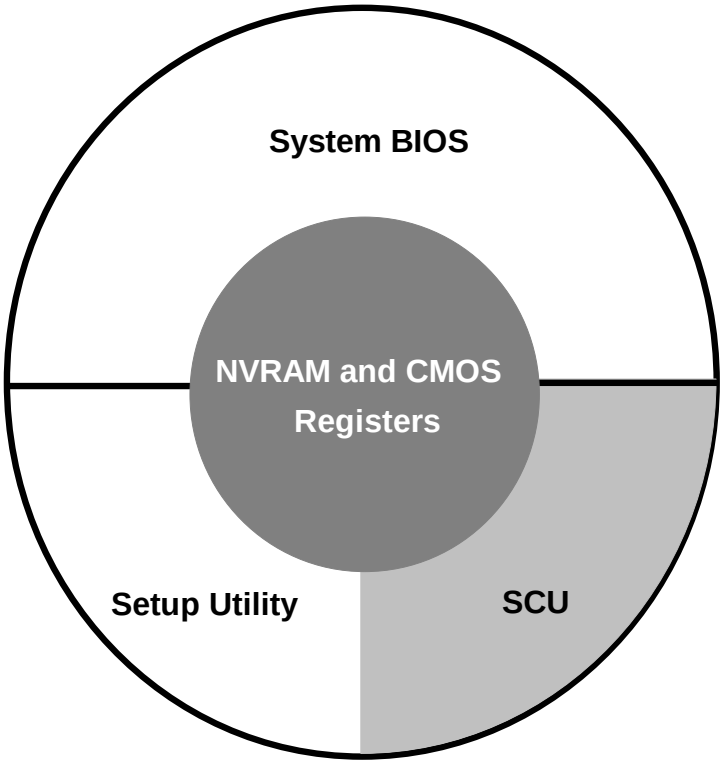

Figure 16 M440LX DP Server BIOS Architecture

4.2 System BIOS

The system BIOS is the core of the Flash ROM-resident portion of the BIOS. The system BIOS provides standard PC-BIOS services and some new industry standards, such as Plug and Play, DMI. In addition, the system BIOS provides support for these M440LX-specific features:

- Security features
- Multiple-speed processor support
- SMP support, fault resilient booting (FRB)
- Logging of critical events
- Server management features
- CMOS configuration RAM defaults
- Multiple language support
- Defective DIMM detection and re-mapping
- Automatic detection of video adapters
- PCI BIOS interface
- Option ROM shadowing
- System information reporting
- Support for ECC, SMI, user-supplied BIOS, L2 cache, I_2O, memory sizing, boot drive sequencing, and resource allocation

The BIOS Setup and System Configuration Utility (SCU) are covered in detail in the M440LX DP Server Product Guide.

5. Board Set Specifications

This chapter specifies the operational parameters and physical characteristics for M440LX DP Server. This is a board-level specification only. System specifications are beyond the scope of this document.

5.1 Absolute Maximum Ratings

Operation of M440LX DP Server at conditions beyond those shown in the following table, may cause permanent damage to the system (provided for stress testing only). Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 11 Absolute Maximum Ratings

Operating Temperature	0°C to +55°C *
Storage Temperature	-55°C to +150°C
Voltage on any signal with respect to ground	-0.3V to V_{DD} + 0.3V **
3.3V Supply Voltage with Respect to ground	-0.3 to +3.63V
5V Supply Voltage with Respect to ground	-0.3 to +5.5V

* Chassis design must provide proper airflow to avoid exceeding Pentium™ II maximum case temperature.
** V_{DD} means supply voltage for the device.

Further topics in this chapter specify normal operating conditions for M440LX DP Server.

5.2 Electrical Specifications

DC specifications for M440LX DP Server power connectors and module power budgets are summarized here. Electrical characteristics for major connector interfaces (including DC and AC specifications) can be obtained from other documents:

- PCI Connectors -- PCI Local Bus Specification Rev. 2.1
- ISA slots -- EISA Bus Specification

Power Connection

Main power supply connection is obtained using the 24-pin main connector, which attaches to the power supply via 18 AWG wire of the color shown below.

Table 12 24-pin Main power connector pinout

Pin	Signal	Color	Pin	Signal	Color
1	+5 Vdc	Red	13	+5 Vdc	Red
2	+5 Vdc	Red	14	+5 Vdc	Red
3	-5 Vdc	White	15	+5 Vdc	Red
4	-12Vdc	Blue	16	+5 Vdc	Red
5	COM	Black	17	COM	Black
6	COM	Black	18	COM	Black
7	COM	Black	19	COM	Black
8	COM	Black	20	COM	Black
9	COM	Black	21	COM	Black
10	+3.3 Vdc	Orange	22	+3.3 Vdc	Orange
11	+12 Vdc	Yellow	23	+3.3 Vdc	Orange
12	+12 Vdc	Yellow	24	+12 Vdc	Yellow

Appendix A

For further information, the following documents are available. Please contact you Intel Sales representative for more information.

The Balboa II Chassis Technical Product Specification

The M440LX DP Server Performance Report

The M440LX DP Server Product Guide

The Symbios SDMS 4.0 User Guide

The M440LX DP Server system Data Sheet

The MTA Testview User's Guide

The table below shows the status of every Madrona SKU and when SRA will be acheived:

PRODUCT CODE	DESCRIPTION
Production Systems	
SMADN000BN00	BASE SYSTEM - No CPU, No Memory, 2 fans, 1 power supply, with CD
SMADN000RN00	REDUNDANT SYSTEM - No CPU, No Memory, 3 fans, 2 power supplies
SMADU300RPS00	REDUNDANT SYSTEM - Dual 300 MHz CPU, 2 fans, 2 p/s, RPX board, SDRAM mem
SMADN000BXN00	CD-LESS BASE SYSTEM - No CPU, No Memory, No CD, 1 fan, 1 power supply
Accessories	
ABAL22NDHDA	SCSI BKPLN KIT -5X Drive Tray, EMI Clips, scsi Cable, Backplane, Docs
ABAL2RPWRA	PWR SHARE UPGD KIT - Power Shr Bd, cover, cables, power cord
ABAL2COOLA	REDUNDANT FAN KIT - 1 Fan, housing, 2 adapters
ABAL2360PS1A	POWER SPLY - 1 X 360 W Power Supply (stand alone or use w/pwr shr kit)
ABALRACKADPT	RACK ADAPTER - Rack rails, Modified cover
AMAB2INTKIT	INTEGRATORS' KIT - Hardware, screws, rails, etc.
AMAB2PKGKIT	PACKAGING KIT - Intel packaging material (for integrators' use)
Boards	
BMAD440LX	Madrona Baseboard
BMADKIT266UP	Klamath UP Kit - w/CPU 266 - CPU assembly, Term(remove), Ret'n Mech(remove), Heat sink
BMADKIT266UG	Klamath DP Kit - w/CPU 266 - CPU assembly, VRM, Heat sink
BMADKIT300UP	Klamath UP Kit - w/CPU 300 - CPU assembly, Term(remove), Ret'n Mech(remove), Heat sink
BMADKIT300UG	Klamath DP Kit - w/CPU 300
BMADMEM00E	EDO Memory Board
BMADMEM00S	SDRAM Memory Board
BMADRPXA	MAD01 RPX Mod
SPARES:	

PRODUCT CODE	DESCRIPTION
FRU669496	CPU retention mechanism
FRU676936	Country Kit
FRU679191	PBA, SCSI Backplane
FRU659708	PBA, Power Share Board
FRU665001	Chassis Assy
FRU676752	Blower 97MM, 10CFM
FRU673833	Fan, 92MM, 45CFM
FRU651034	PBA, Front Panel
FRU660391	SLT1TERM Terminator Bd
FRU651013	Cable, Frontpanel-BB
FRU665240	Cable, Floppy
FRU665233	Cable, Wide, SCSI, Top
FRU651014	Cable, Front Panel HSBP1
FRU665235	Cable, Wide, SCSI, Bottom
FRU651015	Cable, Front Panel HSBP2
FRU670098	Cable, Alarm PK
FRU651012	Cable, Intrusion, Front
FRU665241	Cable, Narrow SCSI
FRU665236	Cable, IDE
FRU676453	IDE Bracket
FRU648336	Fan Bracket
FRU678540	EPAC Blower Duct
FRU657372	Module Rail Assy
FRU648331	Card Guide
FRU651016	PSB,Cable_24,Balboa
FRU651011	PSB,Cable_Per,Bay,Balboa
FRU651017	Cable, PSB_ Control, Balboa
FRU692292	**Top Covers, Balboa2**
FRU692302	**Side Covers, Balboa2**

APPENDIX A: ERRATA

These errata items have been listed in the Specification Update for the M440LX DP Server product during previous revisions of the M440LX DP Server Board Set Technical Product Specification.

The following table indicates the Errata, Specification Changes, Specification Clarifications, and documentation changes which apply to the Intel Columbus II chassis. Intel intends to fix some of the errata in the future, and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future revision of the hardware or software associated with the M440LX DP Server.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This erratum is either new or modified from the previous version of the document.

#	Status	Summary
1	NoFix	CD-ROM option in boot order does not remain ordered.
2	Fixed	Country Kit manual viewer fails with more than 64MB of installed memory.
3	Fixed	Floppy and IDE disk errors on SCO MP/Server test.
4	Fixed	AMI MegaRAID* power console does not work with Microsoft Windows NT* 4.0.
5	NoFix	Windows NT Server 4.0 fails to boot with Hauppauge WIN/TV installed.
6	NoFix	Re-mapping on memory errors may not work for SDRAMs.
7	NoFix	Clock speed setting shown in setup incorrect if F9 is pressed.
8	Fix	3COM 3C509 NIC installed to the secondary PCI bus causes system hang.
9	NoFix	Windows NT 4.0 does not see the keyboard when mouse is not attached.
10	Fixed	AC surge failure on the 360W power supply.
11	Fixed	Adaptec AHA-3940UW does not work when installed on the M440LX DP Server system.
12	Fix	Write Protect Boot Sector BIOS setting does not function properly.
13	Fix	I^2C information on EDO Memory Module incorrect

1. CD-ROM option in boot order does not remain ordered.

PROBLEM: When the IDE CD-ROM is removed and replaced with a SCSI CD-ROM (connected to the narrow SCSI), the SCSI CD-ROM drive is located at the bottom of the list of bootable devices in the BIOS setup. When you select to boot from the CD-ROM and exit BIOS, the system correctly boots from the CD, but on the next reboot of the system, the CD-ROM is returned to the bottom of the bootable device list in BIOS.

IMPLICATION: This issue can make installing software from bootable CD-ROMs problematic as each reboot will require entering the BIOS and correcting the boot order.

WORKAROUND: None.

STATUS: This issue will not be fixed because it is a function of the Symbios BIOS. When a bootable CD-ROM is inserted into the SCSI CD-ROM reader, the BIOS will identify the CD-ROM as a bootable device. However, when no bootable media is inserted in the SCSI CD-ROM, the Symbios BIOS does not identify the CD-ROM as a bootable device. Because of this feature of the Symbios BIOS, the system BIOS only provides the SCSI CD-ROM as a bootable device when bootable media is installed. This is a feature of Symbios and Intel can not change this feature.

2. Country Kit manual viewer failure with more than 64MB of installed memory.

PROBLEM: The DOS Acrobat Viewer (ACRODOS.EXE) used for displaying manuals on the country kit CD (and also on the RPX CD-ROM) fails when more than 64MB of memory is installed in the system. Both CDs use ROM-DOS for an Operating System. This occurs just after the manual documents are copied out to RAM disk. The trap is gracefully handled. The trap information is flashed to the screen for a moment and the ACRODOS executable exits back to the main menu.

IMPLICATION: On systems with greater than 64MB of installed memory, the manuals are not viewable.

WORKAROUND: View the manuals on a system with less than 64MB of system memory.

STATUS: This issue has been resolved and is fixed in the Q1 release of M440LX BIOS available February 1998.

3. Floppy and IDE disk errors during the SCO MP/Server test.

PROBLEM: The SCO MP Server test run completes with several IDE and floppy disk errors. The MP Stress test is a server-specific 8-hour test that exercises all peripherals (hard disks, floppies, CD-ROM, tape, video) while connecting to and transferring files from an NFS server and an FTP server. The test would consistently give errors writing to and reading from both floppy disks. Also, it indicated errors from the CD-ROM, hard disk and tape tests.

IMPLICATION: The MP Server test is a highly specific test suite that stresses the system. Although it is highly unlikely that this issue will be visible to the end-user, it is possible to have performance issues resulting from extremely heavy server activity

WORKAROUND: None Identified.

STATUS: This issue has been resolved in OpenServer 5.0.4 and was driver related.

4. The AMI MegaRAID Power Console does not work with Microsoft Windows NT 4.0.

PROBLEM: The AMI MegaRAID firmware for the MB440LX RPX module does not function correctly with the AMI Power Console, v3.05b, management software in Windows NTS 4.0 SP3.

IMPLICATION: Array management is problematic without the MegaRAID Power Console.

WORKAROUND: None Identified.

STATUS: This issue is fixed with drivers available on the next version of the M440LX DP Server Country Kit RPX CD-ROM.

5. Windows NT Server 4.0 fails to boot with the Hauppauge WIN/TV add-in card installed.

PROBLEM: When the Hauppauge WIN/TV add-in card is installed in the MB440LX server platform with Windows NT 4.0, the system will fail to boot. This adapter is not part of the supported hardware list.

IMPLICATION: This adapter cannot be installed or used on the MB440LX Server Platform.

WORKAROUND: None Identified.

STATUS: Intel will not fix this issue.

6. Re-mapping on memory errors may not work for SDRAMs.

PROBLEM: The BIOS attempts to resize the memory if it discovers a bad memory location during the Power On Self Test (POST). The symptoms: the system will display a message ' Memory error, reconfiguring DRAM geometry' on the screen, and will hang. The memory re-mapping may not work under the following two situations, due to design limitations-

(1) SDRAM memory is used, AND the error occurs in the first populated row (the first side, in case of a double-sided DIMM) AND the bad location is outside the first 8 MBs.

-OR-

(2) EDO memory is being used AND the first populated DIMM is of size 128MB AND the bad memory location is not in the range [8MB, 32MB] the re-mapping will work if the error is in the first 8MB, or is above 32MB.

In any case, if the bad DIMM is not the first DIMM, there is no problem. In the most common configuration using 32MB EDO DIMMs, there is no problem.

IMPLICATION: If either of the above two situations occur, the system will not boot. It is important to note that this issue only exists in the above two situations.

WORKAROUND: None Identified.

STATUS: Intel will not fix this issue as exposure is very minimal.

7. Processor clock speed setting shown in setup is incorrect if F9 is pressed.

PROBLEM: Pressing F9 in setup to restore default settings, will show the incorrect clock speed setting. Actual processor clock speed is not changed, merely the information shown in setup.

IMPLICATION: Confusion could result if end-users attempt to use this feature.

WORKAROUND: Manually set the speed in BIOS and the speed setting will remain.

STATUS: Intel does not plan to fix this issue.

8. The 3Com 3C509 NIC installed to the secondary PCI bus causes clients to drop-off and the server to hang.

PROBLEM: With one 3Com 3C509 NIC installed in the primary PCI bus and one installed in the secondary bus, running network connectivity testing will show that clients begin to drop off of the NIC installed to the secondary PCI bus. This issue is Network Operating System (NOS) independent. The issue has been identified as a timing issue with the i960® RD processor.

IMPLICATION: In very large configuration, it is possible for clients to be dropped.

WORKAROUND: None Identified.

STATUS: This is not a valid problem report and has not been reproduced. It appears that this issue resulted from the use of down rev'd drivers. This issue is closed.

9. Windows NT 4.0 does not see the keyboard when the mouse is not attached.

PROBLEM: When installing Windows NT 4.0, the keyboard will not function if the mouse is not installed. When the keyboard is plugged into the mouse port and no mouse is installed, the keyboard will work properly. If Windows NT is installed and the mouse is subsequently removed, the issue is not seen.

IMPLICATION: If a mouse is not installed when the OS installation occurs, the system will hang after installation is complete.

WORKAROUND: Install Windows NT with keyboard in mouse port and the issue does not occur. Install Windows NT with the keyboard and mouse installed and this issue does not occur.

STATUS: This issue will not be fixed by Intel engineering.

10. AC Surge Failure on 360W Power Supply

PROBLEM: A system using three power supplies with Fab7.0 PSB failed AC surge testing during 2kV unidirectional surge. The failure occurred after approximately 15 minutes of surging at this level. The middle power supply remained in a failed state when AC was reapplied to the supply. Both LEDs were unlit, meaning no power was available. It has been determined that this failure is isolated to the surge testing completed by Intel on all power supplies.

IMPLICATION: This issue is invisible to end-users, but will be readily apparent to OEMs who perform additional power supply testing.

WORKAROUND: None identified.

STATUS: This issue is fixed in the revisions S6 and 00 of the MB440LX power supply.

11. The Adaptec AHA-3940UW SCSI controller does not correctly initialize.

PROBLEM: The Adaptec SCSI BIOS is not initialized at boot time and cannot be used.

IMPLICATION: This adapter cannot be installed on the MB440LX Server Platform.

WORKAROUND: None identified.

STATUS: This issue was the result of a defective adapter card. This is not a valid issue.

12. The Write Protect Boot Sector BIOS Setting Does Not Function Properly.

PROBLEM: When a system is configured to use the Write Protect Boot Sector setting in BIOS, it is still possible to write to the boot device's boot sector.

IMPLICATION: This is a potential, though small, security issue if this feature is used for security.

WORKAROUND: None identified.

STATUS: The issue works according to published specifications. The Boot Sector Protect option is only functional in DOS. This issue is closed.

13. I^2O information on EDO Memory Module incorrect

PROBLEM: A silkscreen error on the EDO memory module causes a resistor to be mis-placed, which disables EDO DIMM information reporting through the I^2C bus. This only affects 3rd party software implementations.

IMPLICATION: If a 3rd party server management software attempts to query the I^2C bus for EDO DIMMs, then no information will be reported and the request will time out.

WORKAROUND: None identified.

STATUS: The issue is under investigation by Intel engineering.