Enterprise Server Group

Intel N440BX Server
Technical Product Specification

Version 1.0
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February, 1998

The Intel N440BX Server may contain design defects or errors known as errata. Characterized errata that may cause the N440BX Server's behavior to deviate from published specifications are documented in the N440BX Server Specification Update.

Revision History

Revision	Revision History	Date
Rev 1.0	Initial release of the Intel N440BX Server Technical Product Specification	2/98

***NOTE**: If printing this document from an electronic file, use a PostScript printer with the appropriate PostScript print driver to insure the drawings print clearly.*

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1. Board Set Descriptions

1.1. Product Overview

The Intel N440BX Server is a flat baseboard design featuring a dual Pentium® II processor-based server system that combines the latest technology and integrated features to provide a high-performance platform optimized for 100 MHz system bus operation.

The N440BX Server baseboard utilizes the Intel 440BX PCIset, the latest in chipset technology from Intel, to maximize system performance for 32-bit application software and operating systems. The N440BX Server baseboard high performance is driven by an 100 MHz processor/memory architecture enabled by the Intel 440BX PCIset.

The N440BX Server design is complemented with an array of features. These include:

- Two Single Edge Contact (SEC) cartridge connectors (to accommodate dual Pentium II processors and future processor upgrades).
- Using dual processors, the system is fully MPS 1.4 compliant (with appropriate Slot 1 Pentium II processor extensions). In addition, support is provided for MP operating systems that may not be fully MPS 1.4 compliant.
- System design based on Intel 440BX, PIIX4, and I/O APIC devices.
- 100 MHz main memory interface supporting up to 1GB of PC/100-compliant commodity SDRAM DIMMs.
- PCI I/O system, compliant with revision 2.1 of the PCI specification. PCI interface is provided by the NBX host bridge
- Dual function PCI SCSI controller (Symbios 53C876*) providing Ultra wide and legacy narrow SCSI channels.
- Intel EtherExpress™ PRO/100+ 10/100 NIC with integrated physical layer (Intel 82558)
- Cirrus Logic CL-GD5480* 2D PCI video controller with 2MB of video memory onboard.
- PCI IDE controller (in PIIX4) providing dual independent Ultra DMA/33 IDE interfaces, each able to support 2 IDE drives.
- National SuperI/O* 87309 I/O controller which provides floppy, parallel, serial, keyboard, mouse).
- 4 PCI expansion slots, 2 ISA expansion slots (1 shared with a PCI slot).
- Compatibility I/O device integrating floppy, dual serial and parallel ports.
- Integration of server management features, including thermal, voltage, fan, and chassis monitoring into one controller. Introduction of Emergency Management Port (EMP) feature.

- Optional Universal Serial Bus (USB) support.

The N440BX Server baseboard supports dual 333, 350, 400, 450 MHz Pentium II processors contained on Single Edge Contact (SEC) cartridges. The SEC cartridges enclose the processor with 512KB of integrated ECC L2 cache to enable high-frequency operation. Two SEC cartridge connectors are embedded on the N440BX Server baseboard. The N440BX Server baseboard design will accommodate identified upgrades to future Intel processing technology.

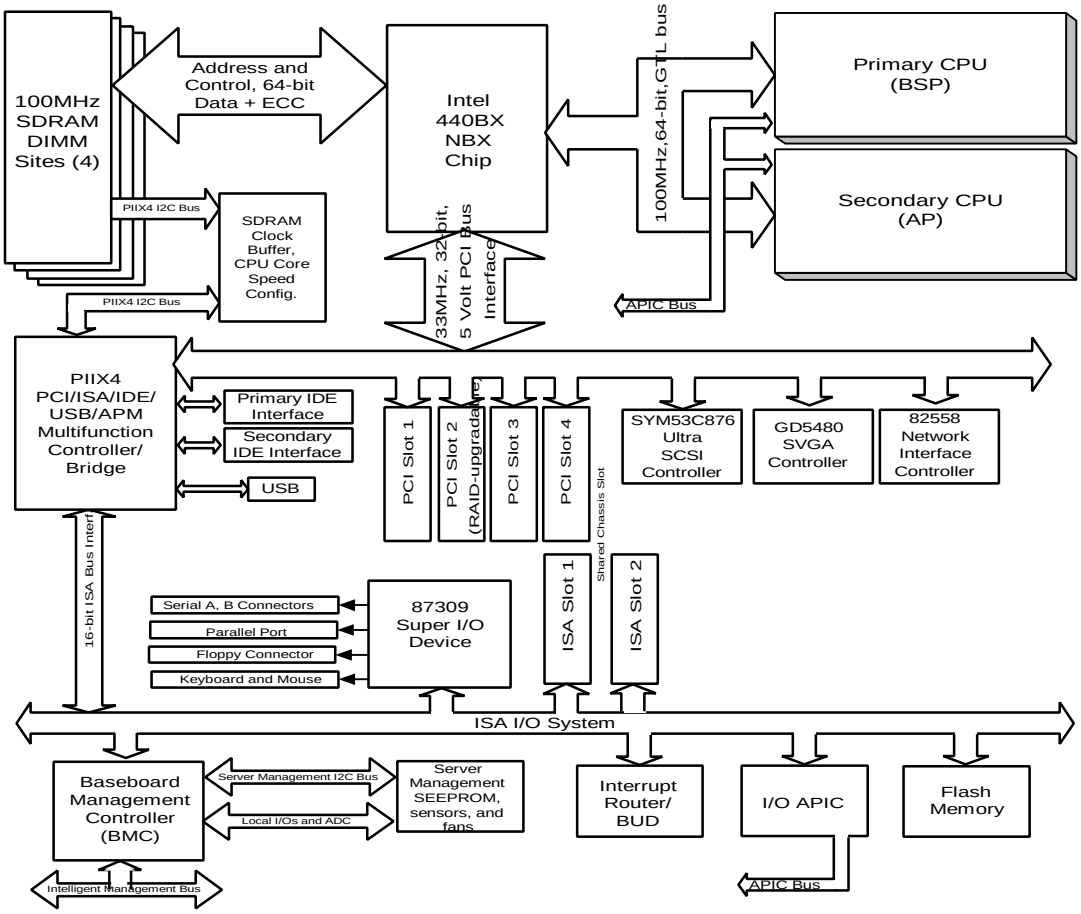


Figure 1 N440BX Server Functional Block Architecture

1.2. Baseboard Diagram

The following diagram shows the placement of major components and connector interfaces on the N440BX Server baseboard. A mechanical layout is available in the appendix.

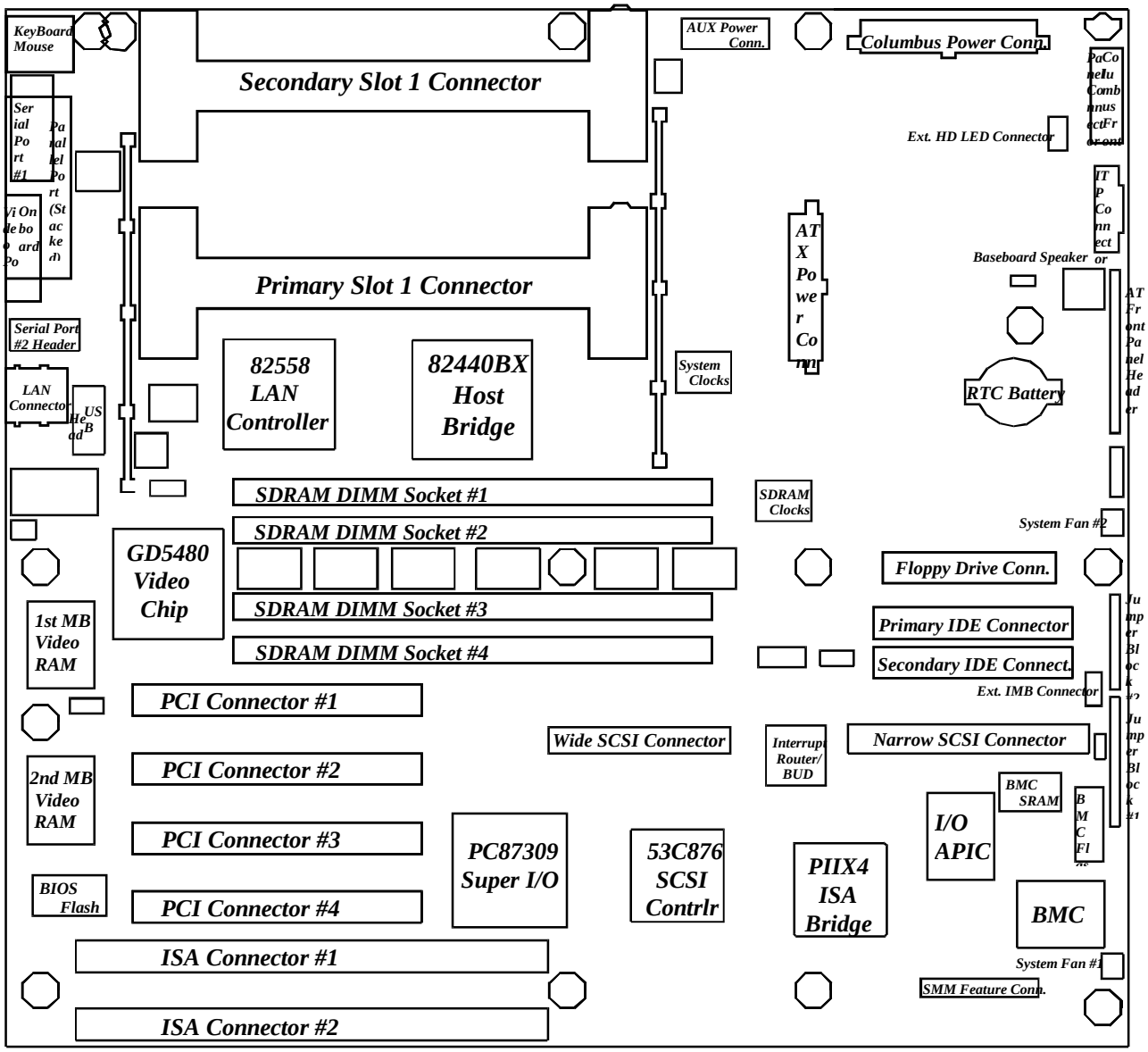


Figure 2 N440BX Baseboard Layout

1.3. Baseboard Architecture Overview

N440BX Server baseboard architecture is based on a design supporting dual processor operation using Pentium II SEC cartridges and the Intel 440BX PCIset. N440BX provides a PCI-based I/O subsystem containing embedded devices for video, NIC, SCSI, and IDE, along with an ISA bridge to support compatibility devices. The baseboard also provides Server Management, and monitoring hardware support and interrupt control that supports dual processor and PC/AT compatible operation. This section provides an overview of these N440BX Server subsystems:

- Support for one to two identical Pentium II processor SEC cartridges.
- Two "Slot 1" edge connectors operating at 100MHz
- Two embedded VRM 8.1-compliant voltage regulators for primary and secondary processor cards.
- Intel 440BX chipset providing processor host interface, PCI bridge, and memory controller with 100MHz pathway to memory.
- 4 DIMM sockets that support PC/100-compliant SDRAM devices.
- 33MHz, 5V PCI segment with four expansion connectors and four embedded devices.
- PCI/ISA/IDE Accelerator (PIIX4) for PCI-to-ISA bridge, and PCI IDE interface, USB controller, and power management controller.
- PCI video controller - Cirrus Logic GD5480.
- PCI dual function SCSI controller - Symbios SYM53C876, supporting narrow and wide SCSI interfaces onboard.
- "RAID-upgradeable" PCI slot with special interrupt capabilities supporting I^2O RAID card by AMI (RAIDExpress* 762)**.**
- PCI Network Interface Controller (NIC) with integrated physical layer - Intel 82558.
- ISA bus segment with two expansion connectors and four embedded devices.
- National Semiconductor 87309 SuperI/O controller chip providing all PC-compatible I/O (floppy, parallel, serial, keyboard, mouse).
- I/O APIC
- Flash memory for system BIOS.
- Server management host interface.
- Interrupt Router and BUD (Basic Utility Device) implemented using an Altera PLD.
- Single server management micro-controller providing monitoring, alerting, and logging of critical system information from embedded sensors on baseboard. N440BX introduces the EMP (Emergency Management Port) interface for remote access to this information, along with reset and power control, via external modem.

1.4. Pentium II Processor(s)

The N440BX Server is optimized to function only with the Pentium II processor SEC cartridges. The Pentium II processor is the third generation in the Pentium Pro microprocessor family. Like the Pentium II processor, the Pentium II processor core/L1 cache appears on one side of a pre-assembled printed circuit board, approximately 2.5" x 5" in size, with the L2 cache on the backside. The L2 cache and processor core/L1 cache connect using a private bus isolated from the processor host bus. This Pentium II processor L2 cache bus operates at half of the processor core frequency. Initially, only caching of 512MB of main memory is supported; all accesses above 512MB are not cached, resulting in slower accesses to the memory in that range. In the future, the processor will support caching of more than 512MB.

The Pentium II processor package follows Single Edge Contact (SEC) cartridge form factor, and provides a thermal plate for heatsink attachment with a plastic cover located opposite the thermal plate.

The Pentium II internal core can operate at frequencies of 333MHz, 350MHz and 400MHz. The initial baseboard design uses the 350MHz and 400 MHz version.

The Pentium II processor's external interface is designed to be MP-ready. Each processor contains a local APIC section for interrupt handling. When two processors are installed, the pair must be of identical revision, core voltage, and bus/core speeds. If only one processor is installed, the other Slot 1 connector must have a terminator card installed.

1.5. VRM

The N440BX Server provides two embedded VRM 8.1-compliant voltage regulator (DC-to-DC converter) to provide VCC_P to each of the Pentium II processors. One VRM is powered from the 5V supply and the other by the 12V supply. Each VRM automatically determines the proper output voltage as required by each processor.

1.6. 440BX Host Bridge / Memory Controller

N440BX architecture is designed around the Intel 440BX PCIset. This device provides 100MHz processor host bus interface support, DRAM controller, PCI bus interface, AGP interface (not used on N440BX), and power management functions. The host bus/memory interface in the NBX is optimized for 100MHz operation, using 100MHz SDRAM main memory. The PCI interface is PCI 2.1-compliant, providing a 33 MHz / 5V signaling environment for embedded controllers and slots in the single PCI segment on N440BX. The NBX memory controller supports up to 1 GB of ECC memory, using PC/100 compliant Synchronous DRAM (SDRAM) devices on DIMM plug-in modules. ECC can detect and correct single-bit errors, and detect multiple-bit errors.

The AGP interface on the NBX is not used on N440BX, and not within the scope this document.

1.6.1. Memory

The N440BX Server baseboard only supports 100MHz, PC/100-compliant SDRAM DIMMs. Two types of memory devices on the DIMMs are supported: registered or unbuffered. The baseboard provides four DIMM sites. Only ECC (72-bit) DIMMs are specified for use in the N440BX Server system.

The PIIX4 provides a local IMB interface to SDRAM DIMM information, SDRAM clock buffer control, and processor core speed configuration. The BIOS code uses this interface during auto-configuration of the processor/memory subsystem, as part of the overall server management scheme.

1.6.2. PCI I/O Subsystem

The primary I/O bus for N440BX Server is PCI, compliant with revision 2.1 of the PCI specification. The PCI bus on N440BX Server supports embedded SCSI, network control, video, and a multi-function device that provides a PCI-to-ISA bridge, bus master IDE controller, Universal Serial Bus (USB) controller, and power management controller. The PCI bus also supports four slots for full-length PCI add-in cards (one shared with an ISA slot).

1.7. PCI SCSI Subsystem

The embedded SCSI controller on N440BX Server is the Symbios SYM53C876 dual function controller. This device provides both Ultra wide and legacy narrow SCSI interfaces as two independent PCI functions[1]. PCI slot 2 is RAID-upgradeable, providing additional support for an Intelligent I/O (I^2O) RAID controller by AMI.

1.8. PCI Network Interface Subsystem

The network interface on N440BX Server is implemented using an Intel 82558, which provides a 10/100Mbit Ethernet interface supporting 10baseT and 10baseTX, integrated with an RJ45 physical interface. The 82558 also provides Wake-On-LAN functionality if the power supply supports a minimum of 800mA of 5V standby current (configurable via baseboard jumper).

[1] The PIIX4 and SYM53C876 are “Multi-function” PCI devices that provide separate sets of configuration registers for each function, while sharing a single PCI hardware connection. Refer to the PCI specification.

1.9. PCI Video Subsystem

The embedded SVGA-compatible video controller on N440BX Server is a Cirrus Logic GD5480 SGRAM GUI Accelerator. The SVGA subsystem also contains 2MB of SGRAM (synchronous graphics RAM), which is provided as a factory build option and is not upgradeable.

1.10. ISA I/O Subsystem

N440BX Server contains a full-featured ISA I/O subsystem with two full length ISA slots (one shared with a PCI slot), and local ISA bus interface to embedded SuperI/O, I/O APIC, Flash BIOS, Basic Utility Device (BUD), and server management features.

1.11. National 87309 SuperI/O Controller

Compatibility I/O on N440BX Server is implemented using a National PC87309VLJ component. This device integrates a floppy disk controller, keyboard and mouse controller, two enhanced UARTs, full IEEE 1284 parallel port, and support for power management. The chip provides separate configuration register sets for each supported function. Connectors are provided for all compatibility I/O devices.

1.12. I/O APIC

The N440BX Server baseboard incorporates an Intel S82093AA Advanced Programmable Interrupt Controller to handle interrupts in accordance with Multiprocessor Specification 1.4.

1.13. Flash BIOS

The BIOS for the N440BX Server baseboard resides in an Intel 28F008S5 FlashFile Memory Family, 8Mbit, symmetrically blocked (64KB) flash device.

1.14. Server Management Subsystem

The N440BX Server incorporates a Dallas 82CH10 micro-controller as baseboard management controller (BMC). The BMC controls and monitors server management features on the baseboard, and provides the ISA interface to two independent IMB-based serial buses. In previous Intel Server baseboard products, the Server Management features were handled by three controllers. On the N440BX Server, all functions of the former Front Panel Controller (FPC) and the Processor Board Controller (PBC) are integrated into the BMC. This includes power supply on/off control, hard reset control, video blanking, watchdog timers, Fault Resilient Booting (FRB) functionality, and all temperature, voltage, fan and chassis intrusion monitoring. The BMC can be polled for current status, or configured to automatically send an alert message when an error condition is detected either manually or by software.

In addition, the N440BX Server baseboard provides a new server management feature: EMP (Emergency Management Port). This allows, when using an external modem, remote reset, power up/down control, and access to the event log, or run-time information. This port also supports console redirection and with additional software support, the EMP can also be used to download firmware and BIOS upgrades in future upgrades.

1.15. Basic Utility Device

The N440BX Server provides the Basic Utility Device (BUD) for ISA and PCI interrupt routing, SMI/NMI routing, and PCI arbitration expansion. The physical device is an Altera 7128 CPLD. Other features formerly handled by an external CPLD on previous servers, such as the host ISA interface to server management functions, now appear in the BMC.

1.16. Retention Module

The Pentium II processor retention module is used to add stability to the SEC connector. The implementation of the retention module is different than found on other Intel manufactured baseboards. For example; the material used, it is a single module, and the screws that are used instead of captive nuts are differences in the design of the module.

1.16.1. Cartridge Connector

The Pentium II processor SEC connector conforms to the “Slot 1” specification, which can also accommodate future processor SEC cartridges. The baseboard provides two SEC cartridge connectors. Processors and Slot 1 connectors are keyed to ensure proper orientation.

1.16.2. Processor Heat/Fan Sinks

The N440BX Server baseboard is not dependent on having fansinks. The term “fansinks” comes from the fan assembly that attaches to the SEC cartridge. The use of the fansink is not required, unless the thermal characteristics of the chassis require extra cooling. For the proper cooling of the processor please refer to the Pentium II processor specifications.

1.17. Processor Bus Termination/Regulation/Power

The termination circuitry required by the Pentium II processor bus (GTL+) signaling environment and the circuitry to set the GTL+ reference voltage, are implemented directly on the SEC cartridges. The baseboard provides 1.5V GTL+ termination power (VTT), and VRM 8.1-compliant DC-to-DC converters to provide processor power (VCCP) at each connector. Power for primary processor is derived from the +12V supply, and the secondary processor utilizes the +5V supply using an embedded DC-DC converter onboard. Both VRM’s are on the baseboard.

1.18. Termination Card

Logic is provided on the baseboard to detect the presence and identity of installed processor or termination cards. If only one Pentium II processor SEC cartridge is installed in a system, a termination card *must* be installed in the vacant SEC connector to ensure reliable system operation. The termination card contains GTL+ termination circuitry, clock signal termination, and Test Access Port (TAP) bypassing for the vacant connector. ***The board will not boot if a termination card is not installed in the vacant slot.***

1.19. Functional Architecture

The following diagram illustrates the functional architecture of the N440BX Server baseboard, with dotted lines showing major functional blocks. This chapter describes the operation of each block and associated circuitry. In addition, this chapter provides high level descriptions of functionality distributed between functional blocks (e.g., interrupt structure, clocks, resets, and server management).

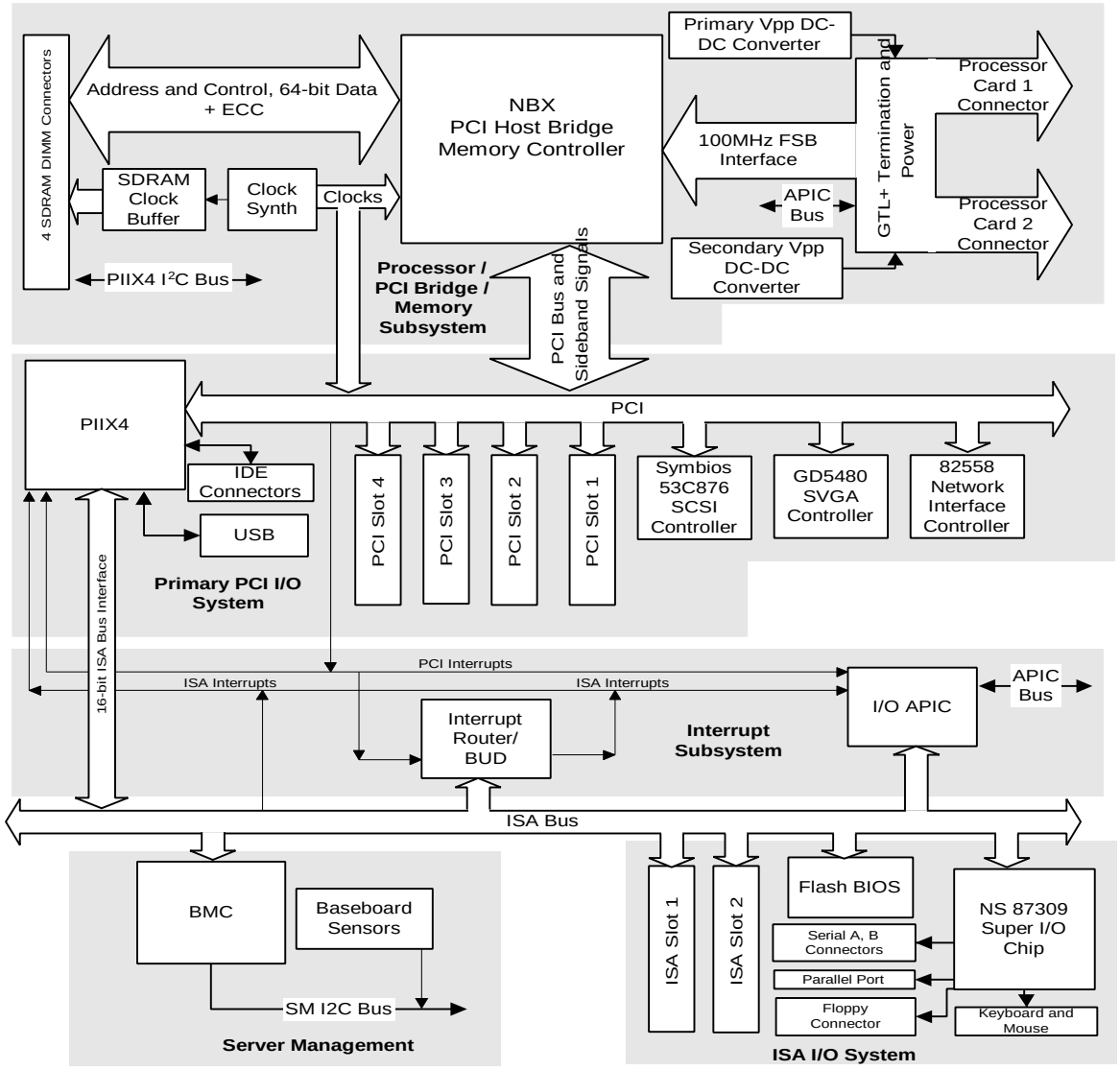


Figure 3-1. N440BX Server Baseboard Functional Blocks

1.20. Processor/PCI Host Bridge/Memory Subsystem

The processor/PCI bridge/memory subsystem consists of support for one to two identical Pentium II processor cartridges, and up to four SDRAM DIMMs. This support circuitry on the baseboard consists of the following:

- Intel 440BX (NBX) PCI host bridge, memory, and power management[2] controller chip.
- Dual 100MHz system bus Slot 1 edge connectors that accept identical Pentium II processor cards (if using 1 processor, a GTL+ terminator card goes in the empty slot).
- Four 168-pin DIMM connectors for interface to SDRAM memory.
- Processor host bus GTL+ support circuitry, including termination power supply.
- Embedded DC-to-DC voltage converters for processor power.
- APIC bus.
- Miscellaneous logic for reset configuration, processor card presence detection, and ITP port.

1.20.1. NBX Host Bridge

The NBX is a BGA device with a 3.3V core and mixed 5V, 3.3V, and GTL+ signal interface pins. The PCI host bridge in the NBX provides the sole pathway between processor and I/O systems, performing control signal translations and managing the data path in transactions with PCI resources onboard. This includes translation of 64-bit operations in the GTL+ signaling environment at 100MHz, to a 32-bit PCI Rev. 2.1 compliant, 5V signaling environment at *33MHz*. The NBX also handles arbitration for PCI bus master access. For more information on N440BX Server arbitration specifics, refer to "PCI Arbitration" later in this chapter. Although the NBX is capable of being clocked to operate with multiple processor system bus frequencies, on N440BX Server the host bridge only supports a 100MHz system bus. The device also features 32-bit addressing (not 36-bit), 4 or 1 deep in-order and request queue (IOQ), dynamic deferred transaction support, and Desktop Optimized (DTO) GTL bus driver support (gated transceivers for reduced power operation). The PCI interface provides greater than 100 MB/s data streamlining for PCI to SDRAM accesses (120 MB/s for writes), while supporting concurrent processor host bus and PCI transactions to main memory. This is accomplished using extensive data buffering, with processor-to-SDRAM and PCI-to-SDRAM write data buffering and write-combining support for processor-to-PCI burst writes.

[2] Refer to "Power Management" later in this chapter, for information on how NBX and PIIX4 power management features are used on N440BX Server.

1.20.2.NBX Memory Controller

The NBX performs the function of memory controller for N440BX Server. Total memory of 32MB to 256MB per DIMM is supported. Although the memory controller supports a variety of memory devices, the N440BX Server implementation only supports PC/100 compliant, 72-bit, unbuffered or registered SDRAM DIMMs. For complete information on supported devices, refer to the *PC/100 SDRAM Specification*, *4-Clock 100MHz 64-bit and 72-bit Unbuffered SDRAM DIMM*, and *4-Clock 100MHz 64-bit and 72-bit Unbuffered SDRAM DIMM* documents.

The NBX provides ECC that can detect and correct single-bit errors (SED/SEC), and detect all double-bit and some multiple-bit errors (DED). Parity checking and ECC can be configured under software control; higher performance is possible if ECC is disabled (1 clock savings). At initial power-up, ECC and parity checking are disabled.

1.20.3.SDRAM Memory DIMM Sites

N440BX Server provides 4 connectors that accept 168-pin JEDEC, 3.3V, 72-bit unbuffered or registered SDRAM DIMMs. You cannot use EDO DIMMs, only SDRAM DIMMs are allowed. You can mix various sizes of DIMMs, mixing unbuffered and registered DIMMs is not allowed. Best performance is obtained using unbuffered DIMMs. Registered DIMMs stack memory devices on each DIMM for greater memory capacity, but they require additional time (1 clock) for memory accesses.

1.21. Processor Termination/Regulation/Power

The termination circuitry required by the Pentium II processor bus signaling environment (GTL+), and the circuitry to set the GTL+ reference voltage are implemented directly on the processor card. The baseboard provides 1.5V GTL+ termination power, and two VRM 8.1-compliant DC-to-DC converters to provide processor VCC_P power at each connector. Power for primary processor is derived from the +12V supply, using an embedded DC-DC converter onboard. A second DC-DC converter is also embedded for secondary processor, which derives power from the +5V supply . Each VRM looks at the VID bits for its respective processor to automatically determine proper output voltage. Refer to the *VRM 8.1 DC-DC Converter Specification* for more information.

1.21.1.Termination Card

If only one processor card is installed in a system, a termination card *must* be installed in the other Slot 1 connector to start the system. The N440BX Server baseboard contains circuitry that will hold off reset if a processor slot is left vacant. The board will not boot if a termination card is not installed in this case.

The termination card contains GTL+ termination circuitry, clock signal termination, and Test Access Port (TAP) bypassing for the vacant connector.

1.22. APIC Bus

Interrupt notification and generation for the dual processors is done using an independent path between local APICs in each processor and the Intel I/O APIC located on the baseboard. This simple bus consists of 2 data signals and one clock line. PC-compatible interrupt handling is done by the PIIX4, with all interrupts delivered to the processor via the INTR line. However, reduced interrupt latency is possible when the APIC bus delivers interrupts in uni-processor operation (if supported by the OS). ***Refer to "Interrupts and I/O APIC" later in this chapter for more information***.

1.23. Miscellaneous Processor/Memory Subsystem Circuitry

In addition to the circuitry described above, the processor subsystem contains the following:

- Processor core frequency configuration circuitry
- DIMM presence detection and auto-configuration logic
- Processor card presence detection circuitry
- ITP port for boundary scan support.

1.24. Processor Core Frequency and Memory Configuration Logic

The PIIX4 provides an independent IMB segment, the PIIX4 System Management Bus (PIIX4 SMB), supporting an IMB EEMUX device (PCF8550) for configuration of processor core speed. The PIIX4 IMB segment also provides access to information stored in IMB ROMs on installed DIMMs, and control of the SDRAM clock buffer that gates synchronous clocks to each DIMM. This feature allows a defective DIMM to be disabled, and total memory resized automatically. BIOS code controls these features using IMB operations performed by the PIIX4. Refer to "Server Management", for a description of the other two IMB segments on N440BX Server, and information on how the PIIX4 SMB fits into the overall server management scheme.

1.25. Processor Card Presence Detection

Logic is provided on the baseboard to detect the presence and identity of installed processor or termination cards. A termination card *must* be installed in a vacant processor card slot to ensure reliable system operation. If the logic senses an empty connector, the system will not power up, preventing operation of the system with an improperly terminated GTL+ processor bus.

1.26. PCI I/O Subsystem

All I/O for N440BX Server, including PCI and PC-compatible, is directed through the PCI interface. On N440BX Server, the PCI bus supports the following embedded devices and connectors:

- Four 120-pin, 32-bit, 5 Volt, PCI expansion slot connectors, one is Intelligent I/O (I^2O) ready
- PIIX4 PCI-to-ISA bridge / IDE / USB / Power Management (and PIIX4 SMB) controller
- PCI video controller, Cirrus Logic CL-GD5480
- PCI Ultra SCSI Controller, Symbios Logic SYM53C876
- PCI Network Interface Controller, Intel 82558

Each device under the PCI host bridge has its IDSEL signal connected to one bit out of the PCI Address/Data lines AD[31::11], which acts as a device select on the PCI bus. This determines a unique PCI device ID value for use in configuration cycles. The following table shows the bit to which each IDSEL signal is attached, along with its corresponding device number. ***Refer to "Accessing Configuration Space" in Chapter 4 for more information.***

Table 3-1. PCI Configuration IDs

IDSEL Value	Device
22	PCI Slot 1
23	PCI Slot 2
24	SCSI
25	PCI Slot 3
26	NIC
27	PCI Slot 4
29	PIIX4
31	Video

1.27. PCI Arbitration

The N440BX Server PCI bus supports 8 PCI masters: NIC, PCI slots 1 through 4, SCSI, PIIX4, and NBX (video is always a slave). All PCI masters must arbitrate for PCI access, using resources supplied by both NBX and custom arbitration logic. The NBX uses internal arbitration connections within its host interface, and the PCI interface on the NBX provides 5 REQ_L/GNT_L pairs for external devices or bridges. Logic in the BUD, which is attached to the REQ0_L/GNT0_L signals, provides support for an additional master on "Round Robin" basis.

One of the arbitration extensions goes to the SCSI controller, which contains an internal arbiter for bus master access to each SCSI interface (wide and narrow).

The PIIX4 operates with a private arbitration scheme using the NBX P_PHOLD_L / P_PHOLDA_L signals, so that access time capability for ISA masters is guaranteed.

The following table defines the arbitration connections on the N440BX Server:

Table 3-2. PCI Arbitration Connections

Baseboard Signals	Device
P_PHOLD_L/P_PHLDA_L	PIIX4
P_REQ1_L/P_GNT1_L	PCI Slot 2
P_REQ2_L/P_GNT2_L	PCI Slot 3
P_REQ3_L/P_GNT3_L	PCI Slot 4
P_REQ4_L/P_GNT4_L	NIC
S_REQ0A_L/S_GNT0A_L	PCI Slot 1
S_REQ0B_L/S_GNT0B_L	SCSI

1.27.1.PCI Connectors

Pins are numbered with respect to the module edge connector: B side signals appear on the front (component side) of the expansion board, A side on the back. Signals that are not connected are labeled with the signal mnemonic followed by “(nc)”.

1.27.2.RAID-upgradeable PCI Slot

The N440BX Server provides support in PCI slot 2 for an I^2O RAID controller by AMI. This PCI add-in card utilizes the onboard SCSI controller chip along with its own built-in intelligence to provide a complete I^2O RAID controller subsystem onboard. N440BX Server interrupt structure is designed to allow the AMI RAID card to intercept PCI interrupts from the onboard SCSI chip when this card is installed in slot 2. If no RAID card is installed, the interrupts pass through the PCI interrupt swizzle on N440BX Server. Refer to “Interrupts and I/O APIC” later in this chapter for more information on N440BX Server interrupt structure. Refer to the AMI Web site for details on the RAID card.

1.27.3.PCI Bus Termination

Certain PCI signals on N440BX Server have “functional” termination, i.e., either pull-up or pull-down resistors. In addition, certain PCI signals may require additional termination to meet signal quality requirements. These are driven through the board topology definition and simulation process, and are not specified in this document. The table in the appendix describes functional termination for PCI signals on N440BX Server. ACK64_L, PRSNT1_L, PRSNT2_L, REQ_L, REQ64_L, SBO_L, SDONE, and TRST_L are terminated at each PCI device and slot. All other signals listed in the table below are bussed, and require only a single pull-up or pull-down resistor. This also applies to the boundary scan signals TCK, TDI, and TMS which are unused in the system (TDO is unterminated).

The N440BX Server implementation of TRST_L does not follow the PCI guideline, but instead implements a more robust solution by providing individual pull-down resistors for each slot. This is done to compensate for numerous PCI components that violate the PCI input low leakage current (I_{il}) specification. If an add-in card directly connects the TRST_L pin on one of these components to the PCI connector, the system would not work with that card installed if the TRST_L signals were bussed and the standard pull-down guideline were used.

SBO_L and SDONE are unused on N440BX Server, but have separate pull-up resistors for each slot per the PCI specification. PRSNT1_L and PRSNT2_L are also not used, and are terminated on each connector with 0.1µF caps to ground on each slot. ACK64_L and REQ64_L have pull-up resistors since 64-bit PCI is not supported on N440BX Server. REQ_L for each slot also has a separate pull-up resistor since these signals are not bussed. Note that REQ_L from onboard PCI components do not require pull-up resistors since they are always driven.

1.28. PIIX4

The PIIX4 is a multi-function PCI device, providing four PCI functions in a single package: PCI-to-ISA bridge, PCI IDE interface, PCI USB controller, and power management controller. Each function within the PIIX4 has its own set of configuration registers and once configured, each appears to the system as a distinct hardware controller sharing the same PCI bus interface. Refer to “Accessing Configuration Space” for more information on programming configuration space for multi-function devices.

The PIIX4 on N440BX Server primary role is to provide the gateway to all PC-compatible I/O devices and features. N440BX Server uses the following PIIX4 features:

- PCI interface
- ISA bus interface
- Dual IDE interfaces
- Power management control
- System reset control
- ISA-compatible interrupt control
- PC-compatible timer/counters and DMA controllers
- Baseboard plug-n-play support
- General purpose I/O
- Real-time Clock and CMOS configuration RAM.

Following are descriptions of each supported PIIX4 feature on the N440BX Server, and related connector pinouts.

1.28.1. PIIX4 PCI Interface

The PIIX4 fully implements a 32-bit PCI master/slave interface, in accordance with the *PCI Local Bus Specification, Rev. 2.1*. On the N440BX Server, the PCI interface operates at 33 MHz, using a 5V signaling environment.

1.28.2.ISA Interface

Function 0 in the PIIX4 provides an ISA bus interface, operating at 8.33 MHz, that supports two ISA expansion connectors, Flash memory, server management interface, and the SuperI/O chip (PC87309VLJ). Refer to “ISA I/O Subsystem”, later in this chapter, for more information.

1.28.3.PCI Bus Master IDE Interface

Function 1 in the PIIX4 provides a PCI bus master controller for dual IDE channels, each capable of programmed I/O (PIO) operation for transfer rates up to 14 MB/s, and Ultra DMA operation for transfer rates up to 33 MB/s. Each IDE channel supports two drives (0 and 1). Two IDE connectors, each featuring 40 pins (2 x 20), are provided on the baseboard, pinout is specified in the appendix. Unused signals are labeled with the signal mnemonic followed by the N440BX Server implementation in parentheses: “p/u” = pull-up resistor, “nc” = no connection.

1.28.4.Power Management Controller

One of the embedded functions in the PIIX4 is a power management controller. On N440BX Server, power management features are obtained using ACPI-compatible software control. For a complete discussion of power management architecture on N440BX Server, refer to “Power Management” later in this chapter.

1.28.5.Compatibility Interrupt Control

The PIIX4 provides the functionality of two 82C59 PIC devices, for ISA-compatible interrupt handling. For a complete discussion of interrupt handling on N440BX Server, refer to “Interrupts and I/O APIC” later in this chapter.

1.28.6.Real-time Clock

The PIIX4 contains an MC14681A compatible real-time clock with battery backup from an external battery. The device also contains 242 bytes of general purpose battery backed CMOS system configuration RAM. On N440BX Server, these functions are duplicated in the SuperI/O chip. However, the N440BX Server implementation uses the PIIX4 RTC and CMOS facilities.

1.28.7.General Purpose Input and Output Pins

The PIIX4 provides a number of general purpose input and output pins. Some of the pins are multiplexed with specific signals and are unavailable as GPIOs, and some perform dedicated GPIO functions on N440BX Server, as shown in the following table.

Table 3-3. PIIX4 General Purpose Input/Output Pin Assignments

Signal	Name	Description
GPI0	IOCHK_L	Monitors ISA IOCHK_L.
GPI1	PCI_PME_L	Pulled up to 3V_standby with 1KΩ. Connected to PCI conn. pin A19
GPI2	EEMUX_OVERRIDE_L	Jumper indicates whether processor core speed is set via the SMB (high) or fixed at 200MHz (low). Normally high via 10KΩ pullup to VCC3.
GPI3	PSWRD_CLR_L	State of password clear jumper.
GPI4	CMOS_CLR_L	State of CMOS clear jumper.
GPI5	APICREQ_L	Used as APICREQ_L.
GPI6	IRQ8_L	Used as IRQ8_L.
GPI7	CPU0_TTL_VID0	Monitors VID bit 0 for VRM attached to processor 0.
GPI8	PX4_THRM_L	Connects with BMC for thermal monitoring.
GPI9	Unused	Pulled up to 3V standby with 10KΩ. Available - battery low feature not used.
GPI10	ACPI_ACI_L	Monitors BMC output for server management.
GPI11	Unused	Pulled up to 3V standby with 10KΩ. Available - SMBALERT feature not used.
GPI12	PWR_CNTL_NIC	Monitors NIC power state.
GPI13	CPU0_TTL_VID1	Monitors VID bit 1 for VRM attached to processor 0.
GPI14	CPU0_TTL_VID2	Monitors VID bit 2 for VRM attached to processor 0.
GPI15	CPU0_TTL_VID3	Monitors VID bit 3 for VRM attached to processor 0.
GPI16	CPU0_TTL_VID4	Monitors VID bit 4 for VRM attached to processor 0.
GPI17	CPU1_TTL_VID0	Monitors VID bit 0 for VRM attached to processor 1.
GPI18	CPU1_TTL_VID1	Monitors VID bit 1 for VRM attached to processor 1.
GPI19	CPU1_TTL_VID2	Monitors VID bit 2 for VRM attached to processor 1.
GPI20	CPU1_TTL_VID3	Monitors VID bit 3 for VRM attached to processor 1.
GPI21	CPU1_TTL_VID4	Monitors VID bit 4 for VRM attached to processor 1.
GPO0	FRB_TIMER_HALT_L	Stops FRB timer.

Table 3-4. PIIX4 General Purpose (con't)

Signal	Name	Description
GPO1	LA17	Implements this signal. Not Available as GPO.
GPO2	LA18	Implements this signal. Not Available as GPO.
GPO3	LA19	Implements this signal. Not Available as GPO.
GPO4	LA20	Implements this signal. Not Available as GPO.
GPO5	LA21	Implements this signal. Not Available as GPO.
GPO6	LA22	Implements this signal. Not Available as GPO.
GPO7	LA23	Implements this signal. Not Available as GPO.
GPO8	F_SERR_L	Causes BUD to assert SERR_L.
GPO9	EN_SLOT_IRQ9	Selects source for IRQ9 assertion. High = PCI slot, low = PIIX4 GPO29.
GPO10	EEMUX_WP	Implements WP signal to IMB EEMUX for processor core speed control.
GPO11	Not connected	Available as GPO.
GPO12	APICACK_L	Implements this signal. Not Available as GPO.
GPO13	APICCS_L	Implements this signal. Not Available as GPO.
GPO14	IRQ0	Implements this signal. Not Available as GPO.
GPO15	Not connected	Available as GPO.
GPO16	PX4_RTC_PWRDN_L	Causes system to power down.
GPO17	EN_NMI_TO_SMI_L	Causes BUD to route all incoming NMIs to SMI.
GPO18	CLR_SMI	Clears latched SMI source in BUD.
GPO19	EN_NMI	Enables NMI assertion by BUD.
GPO20	Not connected	Available as GPO.
GPO21	SCW_PD_L	SCSI termination power down control.
GPO22	Not connected	Available as GPO.
GPO23	X_OE_L	Implements this signal. Not available as GPO.
GPO24	FLASH_PE_L	Indicates a Flash BIOS programming cycle to the BUD.
GPO25	DIS_NON_FLASH_SMI	Connects with BUD for secure Flash programming (see "Flash ROM BIOS" below).
GPO26	VM_EN_L	Voltage margining control signal.
GPO27	VM_UP_L	Voltage margining control signal.
GPO28	FD_DRATE0	Floppy connector signal.
GPO29	SCI_IRQ9_PIIX4	Generates IRQ9 from PIIX4 if selected by GPO9.
GPO30	SP_EN	Speaker override control.

1.29. SCSI Subsystem

N440BX Server provides an embedded dual-function, PCI SCSI host adapter: Symbios Logic SYM53C876. The SYM53C876 contains two independent SCSI controllers that share a single PCI bus master interface as a multi-function device. Internally, each controller is identical, capable of operations using either 8- or 16-bit SCSI providing 10 MB/s (Fast-10) or 20 MB/s (Fast-20) throughput, or 20 MB/s (Ultra) or 40 MB/s (Ultra-wide). In the N440BX Server implementation, controller (A) attaches to a 68-pin 16-bit (wide) SCSI connector interface, controller (B) attaches to a 50-pin 8-bit (narrow) SCSI connector interface. Each controller has its own set of PCI configuration registers and SCSI I/O registers. As a PCI 2.1 bus master, the SYM53C876 supports burst data transfers on PCI up to the maximum rate of 132 MB/sec using on-chip buffers. Refer to the SYM53C876 PCI-Dual Channel SCSI Multi-Function Controller Data Manual for more information on the internal operation of this device, and descriptions of SCSI I/O registers.

1.29.1.Symbios Logic SYM53C876 PCI Signals

The SYM53C876 supports all of the required 32-bit PCI signals including the PERR_L and SERR_L functions. Full PCI parity is maintained on the entire data path through the chip. The device also takes advantage of PCI interrupt signaling capability, using PCI_INTB_L (for controller A, wide SCSI) and PCI_INTC_L (for controller B, narrow) on the N440BX Server board. Please see the Interupt routing figure. The figure below shows the PCI signals supported by the SYM53C876.

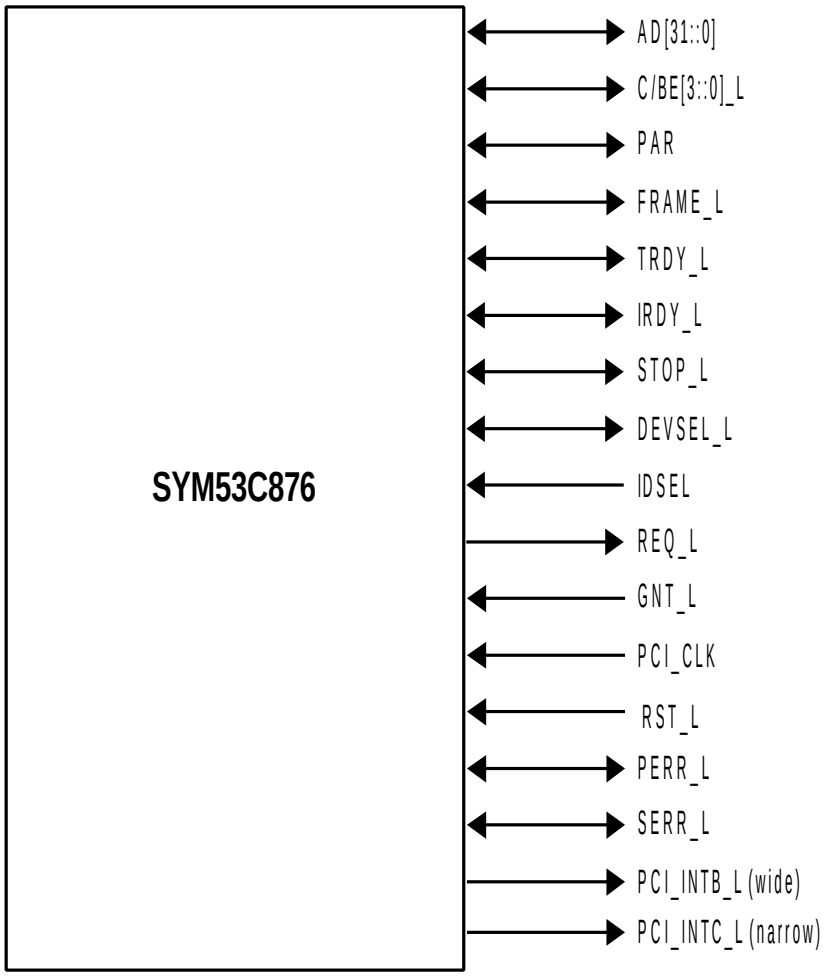


Figure 3-2. Embedded SCSI PCI Signals

1.29.2.SYM53C876 Supported PCI Commands

The SYM53C876 supports PCI commands as shown in the following table:

Table 3-5. Embedded SCSI Supported PCI Commands

C/BE [3::0] _L	Command	SYM53C876 Support	
		Target	Master
0000	Interrupt Acknowledge	No	No
0001	Special Cycle	No	No
0010	I/O Read	Yes	Yes
0011	I/O Write	Yes	Yes
0100	Reserved	No	No
0101	Reserved	No	No
0110	Memory Read	Yes	Yes
0111	Memory Write	Yes	Yes
1000	Reserved	No	No
1001	Reserved	No	No
1010	Configuration Read	Yes	No
1011	Configuration Write	Yes	No
1100	Memory Read Multiple	Yes	Yes
1101	Dual Address Cycle	No	No
1110	Memory Read Line	Yes*	Yes
1111	Memory Write and Invalidate	Yes**	Yes

* Defaults to Memory Read
** Defaults to Memory Write

The extensions to memory commands (memory read multiple, memory read line, and memory write and invalidate) work with the cache line size register to give the cache controller advance knowledge of the minimum amount of data to expect. The decision to use either the memory read line or memory read multiple commands is determined by a bit in the configuration space command register for this device.

1.29.3.SCSI Interfaces

The SYM53C876 contains two independent SCSI controllers: A for Wide SCSI, B for Narrow. Each controller supports 8-bit or 16-bit Fast-10 and Fast-20 SCSI operation at data transfer rates of 10, 20, or 40 MB/s. Each maintains its own set of configuration and run-time registers (refer to chapter 5 for details). On the N440BX Server board, the only difference between each controller is the connector to which it attaches.

Each SCSI interface on the N440BX Server offers active negation outputs, controls for external differential transceivers, a disk activity output, and a SCSI terminator power down control. Active negation outputs reduce the chance of data errors by actively driving both polarities of the SCSI bus, avoiding indeterminate voltage levels and common-mode noise on long cable runs. The SCSI output drivers can directly drive a 48 mA single-ended SCSI bus with no additional drivers (the SCSI segment can handle up to 15 devices). SCSI termination power is always on, regardless of the register settings for SYM53C876 SCSI termination power control features.

1.29.4.SCSI Bus

The SCSI data bus is 8- or 16-bits wide with odd parity generated per byte. SCSI control signals are the same for either bus width. To accommodate 8-bit devices on the 16-bit Wide SCSI connector, the SYM53C876 assigns the highest arbitration priority to the low byte of the 16-bit word. This way, 16-bit targets can be mixed with 8-bit if the 8-bit devices are placed on the low data byte. For 8-bit mode, the unused high data byte is self-terminated and need not be connected. During chip power down, all inputs are disabled to reduce power consumption. Please see the Appendix for pin outs of the narrow and wide SCSI connectors.

1.30. PCI Video

N440BX Server provides a Cirrus Logic CL-GD5480 video controller, along with video SGRAM and support circuitry for an embedded SVGA video subsystem. The CL-GD5480 64-bit VGA Graphics Accelerator chip contains an SVGA video controller, clock generator, BitBLT engine, and RAMDAC. 256K x 32 SGRAM chips provide 2 MB (factory build option, no socket) of 10ns video memory. The SVGA subsystem supports a variety of modes: up to 1600 x 1200 resolution, and up to 16.7 M colors. It also supports analog VGA monitors, single- and multi-frequency, interlaced and non-interlaced, up to 100 Hz vertical retrace frequency. The N440BX Server board also provides a standard 15 pin VGA connector, and external video blanking logic for server management console redirection support.

1.31. Video Chip PCI Signals

The CL-GD5480 supports a minimal set of 32-bit PCI signals since it never acts as a PCI master. As a PCI slave the device requires no arbitration or interrupt connections.

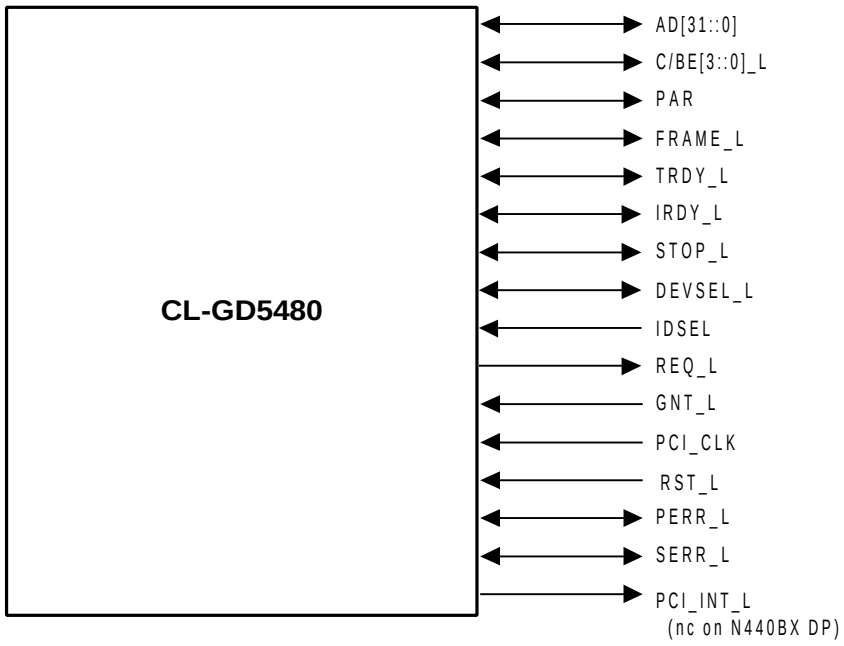


Figure 3-3. Video Controller PCI Signals

1.31.1. Video Controller PCI Commands

The CL-GD5480 supports the following PCI commands:

Table 3-6. Video Chip Supported PCI Commands

		CL-GD5480 Support	
C/BE[3::0]_L	**Command Type**	**Target**	**Master**
0000	Interrupt Acknowledge	No	No
0001	Special Cycle	No	No
0010	I/O Read	Yes	No
0011	I/O Write	Yes	No
0100	Reserved	No	No
0101	Reserved	No	No
0110	Memory Read	Yes	No
0111	Memory Write	Yes	No
1000	Reserved	No	No
1001	Reserved	No	No
1010	Configuration Read	Yes	No
1011	Configuration Write	Yes	No
1100	Memory Read Multiple	No	No
1101	Dual Address Cycle	No	No
1110	Memory Read Line	No	No
1111	Memory Write and Invalidate	No	No

1.31.2. Video Modes

The CL-GD5480 supports all standard IBM VGA modes. Using 2MB (standard) of SGRAM, N440BX Server supports special Cirrus Logic extended modes. The following tables show the standard and extended modes that this implementation supports, including the number of colors and palette size (e.g., 16 colors out of 256 K colors), resolution, pixel frequency, and scan frequencies.

Table 3-7. Standard VGA Modes

Mode(s) in Hex	Colors (number /palette size)	Resolution	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)
0, 1	16/256K	360 X 400	14	31.5	70
2, 3	16/256K	720 X 400	28	31.5	70
4, 5	4/256K	320 X 200	12.5	31.5	70
6	2/256K	640 X 200	25	31.5	70
7	Mono	720 X 400	28	31.5	70
D	16/256K	320 X 200	12.5	31.5	70
E	16/256K	640 X 200	25	31.5	70
F	Mono	640 X 350	25	31.5	70
10	16/256K	640 X 350	25	31.5	70
11	2/256K	640 X 480	25	31.5	60
12	16/256K	640 X 480	25	31.5	60
12+	16/256K	640 X 480	31.5	37.5	75
13	256/256K	320 X 200	12.5	31.5	70

Table 3-8. Extended VGA Modes

Mode(s) in Hex	Colors	Resolution	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)	Memory Option
58, 6A	16/256K	800 X 600	36	35.2	56	1MB
58, 6A	16/256K	800 X 600	40	37.8	60	1MB
58, 6A	16/256K	800 X 600	50	48.1	72	1MB
58, 6A	16/256K	800 X 600	49.5	46.9	75	1MB
5C	256/256K	800 X 600	36	35.2	56	1MB
5C	256/256K	800 X 600	40	37.9	60	1MB
5C	256/256K	800 X 600	50	48.1	72	1MB
5C	256/256K	800 X 600	49.5	46.9	75	1MB
5C	256/256K	800 X 600	56.25	53.7	85	1MB
5C	256/256K	800 X 600	68.2	63.6	100	1MB
5D	16/256K (interlaced)	1024 X 768	44.9	35.5	43	1MB
5D	16/256K	1024 X 768	65	48.3	60	1MB
5D	16/256K	1024 X 768	75	56	70	1MB
5D	16/256K	1024 X 768	78.7	60	75	1MB
5E	256/256K	640 X 400	25	31.5	70	1MB
5F	256/256K	640 X 480	25	31.5	60	1MB
5F	256/256K	640 X 480	31.5	37.9	72	1MB
5F	256/256K	640 X 480	31.5	37.5	75	1MB
5F	256/256K	640 X 480	36	43.3	85	1MB
5F	256/256K	640 X 480	43.2	50.9	100	1MB
60	256/256K (interlaced)	1024 X 768	44.9	35.5	43	1MB
60	256/256K	1024 X 768	65	48.3	60	1MB
60	256/256K	1024 X 768	75	56	70	1MB
60	256/256K	1024 X 768	78.7	60	75	1MB
60	256/256K	1024 X 768	94.5	68.3	85	1MB
60	256/256K	1024 X 768	113.3	81.4	100	1MB
64	64K	640 X 480	25	31.5	60	1MB
64	64K	640 X 480	31.5	37.9	72	1MB
64	64K	640 X 480	31.5	37.5	75	1MB
64	64K	640 X 480	36	43.3	85	1MB
64	64K	640 X 480	43.2	50.9	100	1MB
65	64K	800 X 600	36	35.2	56	1MB
65	64K	800 X 600	40	37.8	60	1MB
65	64K	800 X 600	50	48.1	72	1MB
65	64K	800 X 600	49.5	46.9	75	1MB
65	64K	800 X 600	56.25	53.7	85	1MB
65	64K	800 X 600	68.2	63.6	100	1MB
66	32K	640 X 480	25	31.5	60	1MB
66	32K	640 X 480	31.5	37.9	72	1MB
66	32K	640 X 480	31.5	37.5	75	1MB
66	32K	640 X 480	36	43.3	85	1MB
66	32K	640 X 480	43.2	50.9	100	1MB
67	32K	800 X 600	36	35.2	56	1MB
67	32K	800 X 600	40	37.8	60	1MB
67	32K	800 X 600	50	48.1	72	1MB
67	32K	800 X 600	49.5	46.9	75	1MB

Table 3-8. Extended VGA Modes (cont.)

Mode(s) in Hex	Colors	Resolution	Pixel Freq. (MHz)	Horiz. Freq. (KHz)	Vert. Freq. (Hz)	Memory Option
67	32K	800 X 600	56.25	53.7	85	1MB
67	32K	800 X 600	68.2	63.6	100	1MB
68	32K (interlaced)	1024 X 768	44.9	35.5	43	2MB
68	32K	1024 X 768	65	48.3	60	2MB
68	32K	1024 X 768	75	56	70	2MB
68	32K	1024 X 768	78.7	60	75	2MB
68	32K	1024 X 768	94.5	68.3	85	2MB
68	32K	1024 X 768	113.3	81.4	100	2MB
6C	16/256K (interlaced)	1280 X 1024	75	48	43	1MB
6D	256/256K (interlaced)	1280 X 1024	75	48	43	2MB
6D	256/256K	1280 X 1024	108	65	60	2MB
6D	256/256K	1280 X 1024	135	80	75	2MB
6D	256/256K	1280 X 1024	157.5	91	85	2MB
6E	32K	1152 X 864	94.5	63.9	70	2MB
6E	32K	1152 X 864	108	67.5	75	2MB
6E	32K	1152 X 864	121.5	76.7	85	2MB
6E	32K	1152 X 864	143.5	91.5	100	2MB
71	16M	640 X 480	25	31.5	60	1MB
71	16M	640 X 480	31.5	37.9	72	1MB
71	16M	640 X 480	31.5	37.5	75	1MB
71	16M	640 X 480	36	43.3	85	1MB
71	16M	640 X 480	43.2	50.9	100	1MB
74	64K (interlaced)	1024 X 768	44.9	35.5	43	2MB
74	64K	1024 X 768	65	48.3	60	2MB
74	64K	1024 X 768	75	56	70	2MB
74	64K	1024 X 768	78.7	60	75	2MB
74	64K	1024 X 768	94.5	68.3	85	2MB
74	64K	1024 X 768	113.3	81.4	100	2MB
78	32K	800 X 600	36	35.2	56	1MB
78	16M	800 X 600	40	37.8	60	2MB
78	16M	800 X 600	50	48.1	72	2MB
78	16M	800 X 600	49.5	46.9	75	2MB
78	16M	800 X 600	56.25	53.7	85	2MB
78	16M	800 X 600	68.2	63.6	100	2MB
7B	256/256K (interlaced)	1600 X 1200	135	62.5	48	2MB
7B	256/256K	1600 X 1200	162	75	60	2MB
7C	256/256K	1152 X 864	94.5	63.9	70	1MB
7C	256/256K	1152 X 864	108	67.5	75	1MB
7C	256/256K	1152 X 864	121.5	76.7	85	1MB
7C	256/256K	1152 X 864	143.5	91.5	100	1MB
7D	64K	1152 X 864	94.5	63.9	70	2MB
7D	64K	1152 X 864	108	67.5	75	2MB
7D	64K	1152 X 864	121.5	76.7	85	2MB
7D	64K	1152 X 864	143.5	91.5	100	2MB

For more information refer to the *Cirrus Logic CL-GD5480 Technical Reference Manual*.

1.32. Network Interface Controller (NIC)

N440BX Server supports a 10BASE-T/100BASE-TX network subsystem based on the Intel 82558 Fast Ethernet PCI Bus Controller. This device is similar in architecture to its predecessor (Intel 82557), except with an integrated physical layer interface. The advantage of this controller is that no external devices are required to implement an embedded network subsystem, except TX/RX magnetics, 2 status LEDs, and a connector.

The 82558 is a highly integrated PCI LAN controller for 10 or 100 Mbps Fast Ethernet networks. As a PCI bus master, the 82558 can burst data at up to 132 MB/s. This high-performance bus master interface can eliminate the intermediate copy step in RX/TX frame copies, resulting in faster frame processing. The network OS communicates with the 82558 using a memory-mapped I/O interface, PCI interrupt connected directly to the BUD (Basic Utility Device), and two large receive and transmit FIFOs, which prevent data overruns or under runs while waiting for access to the PCI bus, as well as enabling back to back frame transmission within the minimum 960ns inter-frame spacing. The figure below shows the PCI signals supported by the 82558:

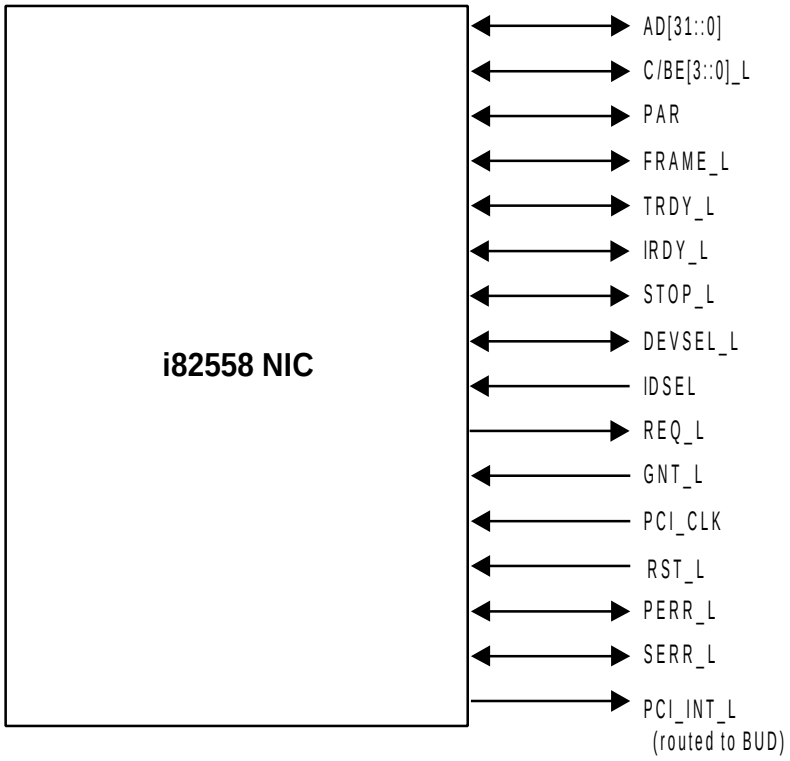


Figure 1-4. Embedded NIC PCI Signals

1.32.1.Supported Network Features

The 82558 contains an IEEE MII compliant interface to the components necessary to implement a IEEE 802.3 100BASE-TX network connection. N440BX Server supports the following features of the 82557 controller:

- Glueless 32-bit PCI Bus Master Interface (Direct Drive of Bus), compatible with PCI Bus Specification, revision 2.1
- 82596-like chained memory structure, with improved dynamic transmit chaining for enhanced performance
- Programmable transmit threshold for improved bus utilization
- Early receive interrupt for concurrent processing of receive data
- On-chip counters for network management
- Autodetect and autoswitching for 10 or 100 Mbps network speeds
- Support for both 10 Mbps and 100 Mbps Networks, full or half duplex-capable, with back-to-back transmit at 100 Mbps
- Integrated physical interface to TX magnetics.

The magnetics component terminates the 100BASE-TX connector interface. A Flash device stores the network ID.

1.32.2.NIC Connector and Status LEDs

The 82558 drives LEDs on the network interface connector that indicate transmit/receive activity on the LAN, valid link to the LAN, and 10/100 Mbps operation.

1.33. ISA I/O Subsystem

On the N440BX Server, the PIIX4 provides a bridge to an ISA I/O subsystem that supports the following connectors and devices:

- Two ISA slots, one physically shared with PCI slot 1
- Flash memory for BIOS ROM and extensions
- National Semiconductor PC87309VLJ SuperI/O chip, which supports the following:
    - Two PC-compatible serial ports
    - Enhanced parallel port
    - Floppy controller
    - Keyboard/Mouse ports

The ISA I/O subsystem also connects with the Intel I/O APIC and BMC. The I/O APIC relays interrupts produced by ISA devices in dual processor operation (or in uni-processor operation for increased performance with certain OS implementations. The BUD, a programmable logic device performs rerouting of PCI interrupts as ISA interrupts for MP OS implementations that are not fully MPS 1.4 compatible, and management interrupt (NMI_L and SMI_L) control. Refer to “Interrupts and I/O APIC” later in this chapter for more information on these devices and how they are used in the N440BX Server interrupt structure. The BMC controls server management features on N440BX Server. Refer to “Server Management” later in this chapter for details. For details on pin out and termination please refer to the Appendix.

1.34. Compatibility I/O Controller Subsystem

The National PC87309VLJ SuperI/O device is a plug and play (PnP) compatible standard I/O subsystem chip. This device contains all of the necessary circuitry to control two serial ports, one parallel port, floppy disk, and PS/2-compatible keyboard and mouse. N440BX Server provides the connector interface for each. In addition, the SuperI/O contains a real-time clock, which is unused on N440BX Server.

Note:

Unlike it predecessor (87307), the PC87309VLJ provides no general purpose I/O bits or programmable chip selects. All GPIOs required by N440BX Server subsystems are supplied by the PIIX4 as specified above.

1.34.1.Serial Ports

Two connectors are provided, one 9-pin D-Sub in the stacked housing for Serial port A, and the second via 10-pin header for Serial port B. Both ports are compatible with 16550A and 16450 UARTs, supporting relocatable I/O addresses. Each serial port can be set to 1 of 4 different COM ports, and can be enabled separately. When enabled, each port can be programmed to generate edge or level sensitive interrupts. When disabled, serial port interrupts are available to add-in cards. The pinout for the two connectors are available in the appendix.

1.34.2.Parallel Port

The 25/15 pin high rise connector stacks the parallel port connector over the VGA and serial Port A connector. The 87309 provides an IEEE 1284-compliant 25-pin bi-directional parallel port. BIOS programming of the SuperI/O registers enable the parallel port, and determine the port address and interrupt. When disabled, the interrupt is available to add-in cards. Pin out of the Parallel port is available in the appendix.

1.34.3.Floppy Disk Controller

The FDC on the SuperI/O is functionally compatible with the PC8477, which contains a superset of the floppy disk controllers in the DP8473 and N82077. The baseboard provides the 24 MHz clock, termination resistors, and chip selects. All other FDC functions are integrated into the SuperI/O, including analog data separator and 16-byte FIFO. Pinout is available in the appendix.

1.34.4.Keyboard and Mouse Connectors

The keyboard and mouse connectors are mounted within a single stacked housing. The mouse connector is stacked over the keyboard connector. External to the board they appear as two connectors. The keyboard and mouse controller are software compatible with the 8042AH and PC87911. The keyboard and mouse connectors are PS/2 compatible, with pinout available in the appendix.

1.34.5.Front Panel Header (AT, System)

An inline AT header is provided for AT-style front panel connections, e.g., power, LED indicators, and reset as well has a Front panel 2x16 post socket header. Both pin outs are available in the appendix.

1.34.6.Flash ROM BIOS

An 8Mbit flash memory (Intel 28F008S5) provides non-volatile storage space for BIOS and general purposes. The device is byte wide, of the Smart 5 FlashFile family and symmetrically blocked. The Flash device is directly addressed as 16 64-kbyte blocks of 8-bit ISA memory. Refer to the *Byte-Wide Smart 5 FlashFile Memory Family 4, 8, and 16 MB Data Book* for additional device information.

1.34.7.Secure Flash Programming Mechanism

On N440FX DP, the BUD detects any write operation to Flash and asserts SMI_L. The SMI_L handler (part of BIOS) then looks for a signature from the Flash Memory Update utility (FMUP) before allowing any writes to Flash. This prevents accidental loading of non-compatible BIOS code into Flash.

1.35. System Reset Control

Reset circuitry on the N440BX Server board monitors reset from the front panel, PIIX4, I/O controller, and processor subsystem to determine proper reset sequencing for all types of reset. The reset logic is designed to accommodate a variety of ways to reset the system, which can be divided into the following categories:

- Power-up reset
- Hard reset
- Soft (programmed) reset

1.35.1.Power-up Reset

Power-up reset occurs on the initial application of power to the system. The power supply asserts its "power good" signal within 400 to 2000ms of its output voltages being stable. The BMC monitors this signal, and asserts its power good output 30 to 40ms after detecting the power supply's power good signal asserted (the onboard VRMs are designed to provide stable processor power 30 to 40ms after the main power is stable).

1.35.2.Hard Reset

Hard reset may be initiated by software, or by the user resetting the system through the front panel. For software initiated hard reset, the PIIX4 Reset Control register should be used. The front panel reset is routed to the PIIX4 through the reset and power micro-controller. Both sources of hard reset cause the PIIX4 to assert ISA bus reset (RST_RSTDRV) and PCI reset (RST_P_RST_LB). RST_RSTDRV resets the ISA subsystem, while RST_P_RST_L resets the PCI bus. The NBX receives the PCI reset signal and propagates it to the processor subsystem

1.35.3.Soft Reset

Soft resets may be generated by the keyboard controller (RST_KB_L), or by the chip set in the processor subsection (RST_INIT_REQ_L). The two sources of soft reset are combined in the reset logic, and routed to the processor subsection via the RST_INIT_CPU_L signal. Soft reset causes the processors to begin execution in a known state without flushing caches or internal buffers.

A programmed reset may be initiated by software. Although reset control is provided by registers in the NBX, the chip's documentation recommends that the PIIX4 Reset Control register be used instead for programmed resets. Refer to the 440*BX Host Bridge EDS* or *440BX Component Specification* for more information.

1.35.4.Reset Diagram

Reset flows throughout the N440BX Server board as shown in the following figure.

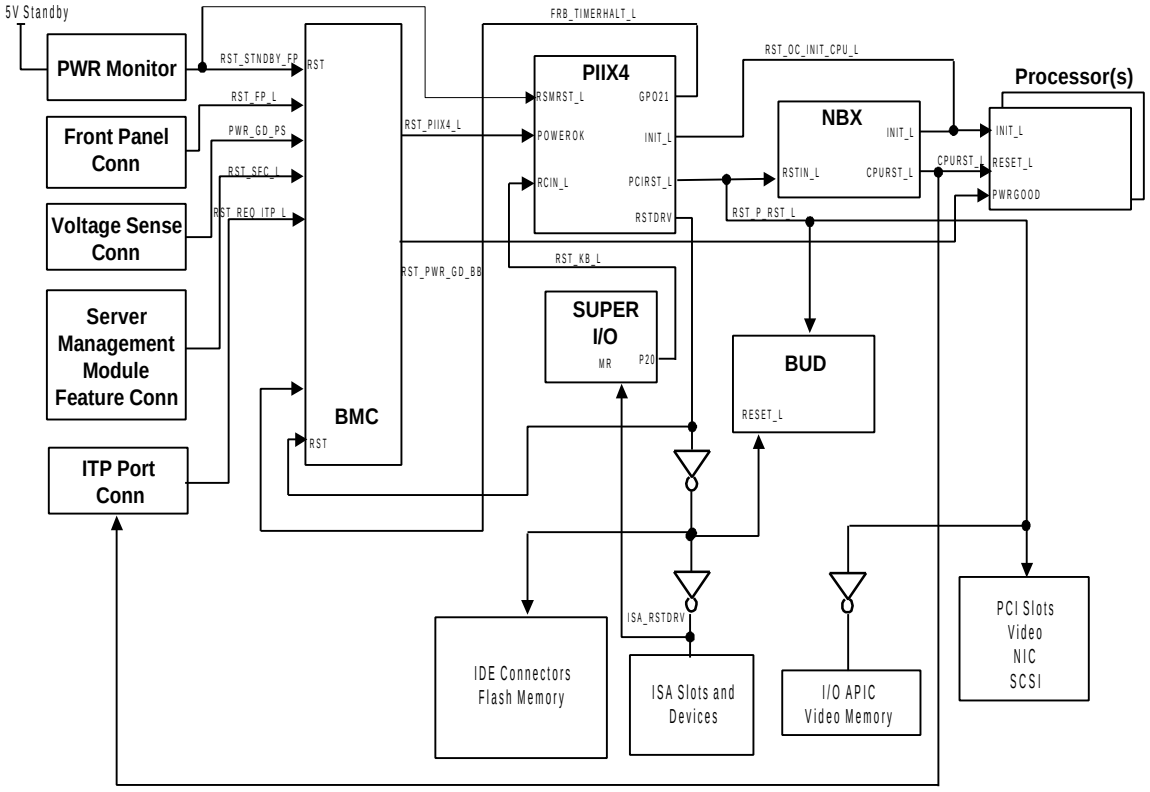


Figure 3-5. Reset Flow Diagram

1.36. Clock Generation and Distribution

All buses on N440BX Server operate using synchronous clocks. Clock synthesizer/driver circuitry on the baseboard generates clock frequencies and voltage levels as required, including the following:

- 100 MHz at 2.5V logic levels - Both Slot 1 connectors, the NBX, the ITP port
- 100 MHz at 3.3V logic levels - SDRAM DIMMs
- 33.3 MHz at 3.3V logic levels - Reference clock for the PCI bus clock driver
- 14.31818 MHz at 2.5V logic levels - Processor and I/O APIC bus clock

There are 4 main synchronous clock sources on the N440BX Server board: 100MHz host clock generator for processors and SDRAM, 48 MHz clock for PIIX4 and SuperI/O chips, 33.3 MHz PCI reference clock, and 14.318 MHz APIC and ISA clocks. For information on processor/SDRAM clock generation, refer to the *Mixed Voltage Clock Synthesizer/Driver Specification with SDRAM Support*. In addition, N440BX Server provides asynchronous clock generators: 40 MHz clock for the embedded SCSI controller, 32 KHz clock for the PIIX4 RTC, 22.1 MHz clock for the BMC, and a 25 MHz clock for the NIC. The following figure illustrates clock generation and distribution on the N440BX Server board.

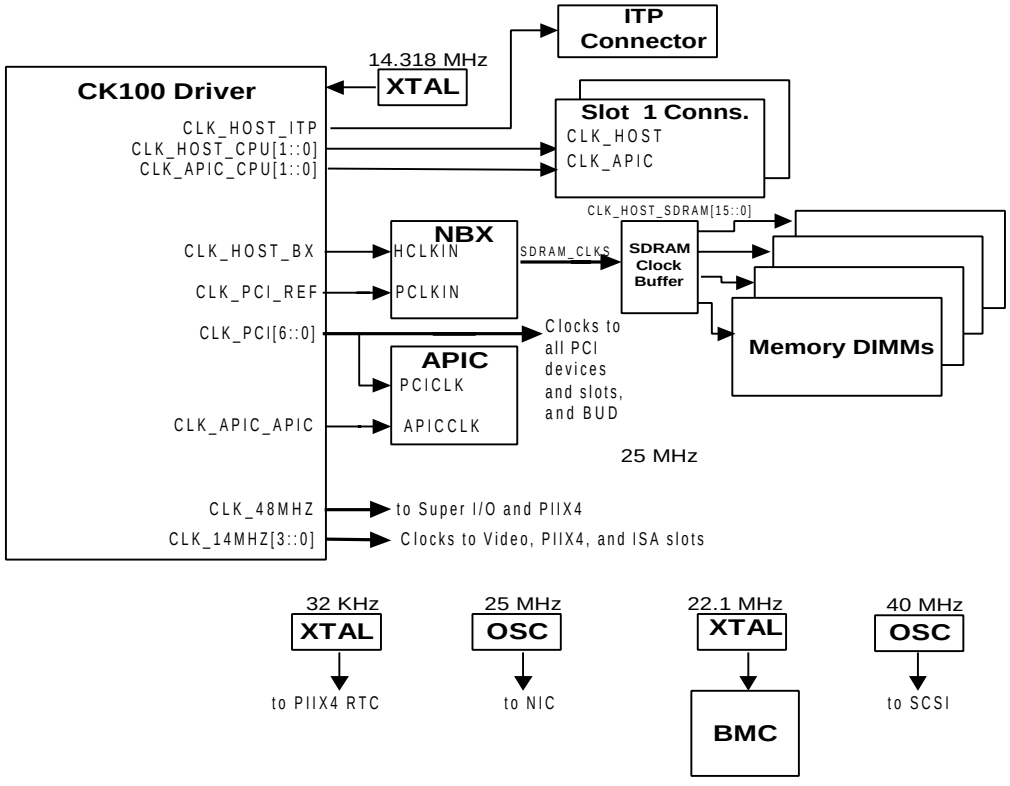


Figure 3-6. Clock Generation and Distribution

1.37. Interrupts and I/O APIC

N440BX Server interrupt architecture accommodates both PC-compatible PIC mode, and dual-processor APIC mode interrupts. In addition, N440BX Server provides a PCI to ISA interrupt rerouting mechanism for compatibility with some multiprocessor operating systems which do not fully support the APIC.

1.37.1. PIIX4 Compatibility Interrupt Controller

For PC-compatible mode, the PIIX4 provides two 82C59-compatible interrupt controllers embedded in the device. The two controllers are cascaded with interrupt levels 8-15 entering on level 2 of the primary interrupt controller (standard PC configuration). A single interrupt signal is presented to the processors, to which only one processor will respond for servicing. The PIIX4 and SuperI/O contain configuration registers that define which interrupt source logically maps to I/O APIC INTx pins. In PIC mode, the PIIX4 provides a way to direct PCI interrupts onto one of the interrupt request levels 1-15. Note that this is only useful in compatibility mode since the redirected interrupts are not sourced on the outputs of the PIIX4.

1.37.2.Intel I/O APIC

For APIC mode, the N440BX Server interrupt architecture incorporates the Intel I/O APIC device, to manage and broadcast interrupts to local APICs in each processor. The I/O APIC monitors interrupt requests from devices, and on occurrence of an interrupt sends a message corresponding to the interrupt via the APIC bus to each local APIC. The APIC bus minimizes interrupt latency time for compatibility interrupt sources, in both single and dual processor operation. The I/O APIC can also supply greater than 16 interrupt levels to the processor(s). The APIC bus consists of an APIC clock, and two bi-directional data lines.

N440BX Server APIC structure consists of a single I/O APIC device with 24 input interrupt requests. Compatibility interrupt levels 0 through 15 appear on inputs 0 through 15. The I/O APIC also manages 8 interrupt levels associated with PCI interrupts: PCI interrupts A through D are routed to APIC inputs 16 through 19. This supports more efficient interrupt processing. The PIIX4 also contains I/O APIC features that are not used in the N440BX Server platform.

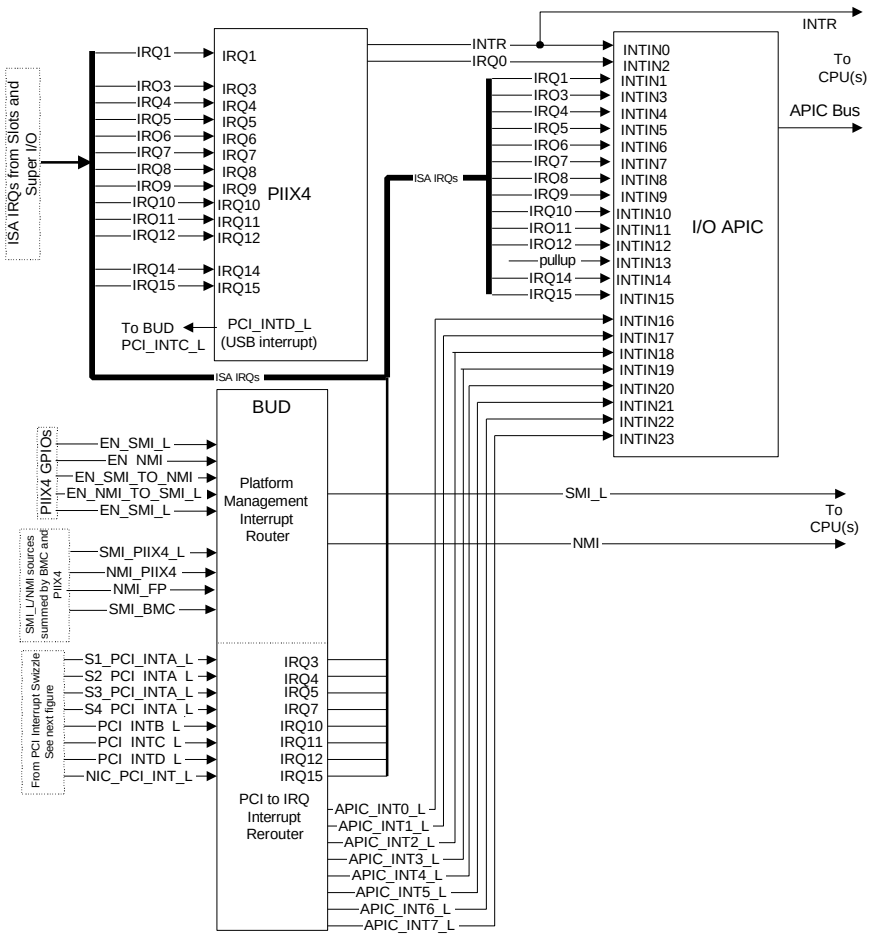


Figure 3-7. Interrupt Structure

1.38. Interrupt Sources

The following table recommends the logical interrupt mapping of interrupt sources on N440BX Server. The actual interrupt map is defined using configuration registers in the PIIX4 and the I/O controller, and PCI to IRQ interrupt rerouter in the BUD. I/O Redirection Registers in the I/O APIC are provided for each interrupt signal, which define hardware interrupt signal characteristics for APIC messages sent to local APIC(s). Use the information provided in this table to determine how to program each interrupt.

Table 3-9. Interrupt Definitions

Interrupt	I/O APIC level	Description
INTR	INT0	Processor interrupt
NMI		NMI from BUD to processor
IRQ0	INT2	Timer interrupt from PIIX4
IRQ1	INT1	Keyboard interrupt
IRQ2		Interrupt signal from second 8259 internal to PIIX4
IRQ3	INT3	Serial port A or B interrupt from 87309VLJ device, user-configurable.
IRQ4	INT4	Serial port A or B interrupt from 87309VLJ device, user-configurable.
IRQ5	INT5	
IRQ6	INT6	Floppy disk
IRQ7	INT7	Parallel port
IRQ8_L	INT8	RTC interrupt
IRQ9	INT9	
IRQ10	INT10	
IRQ11	INT11	
IRQ12	INT12	Mouse interrupt
	INT13	
IRQ14	INT14	Compatibility IDE interrupt from primary channel IDE devices 0 and 1
IRQ15	INT15	Secondary IDE interrupt
PCI_INTA_L	INT16	PCI Interrupt signal A
PCI_INTB_L	INT17	PCI Interrupt signal B
PCI_INTC_L	INT18	PCI Interrupt signal C
PCI_INTD_L	INT19	PCI Interrupt signal D
SMI_L		System Management Interrupt. General-purpose error indicator from various sources. Controlled by BUD.

1.38.1. PCI Add-in Card Slot Interrupt Sharing

The following figure shows how PCI interrupts, shared between slots and embedded controllers, are routed to the BUD. The BUD manages each PCI_INT_A from each slot, cascaded PCI_INTs B through C from each slot, and PCI interrupts from SCSI and NIC devices, to avoid conflicts (since most PCI cards use PCI_INTA_L as their interrupt pin). The arrows indicate the direction of interrupt flow from slot to slot, with final destination at the BUD interrupt inputs. The BUD then delivers each interrupt to the appropriate PIIX4 compatibility IRQ and I/O APIC INTIN pins.

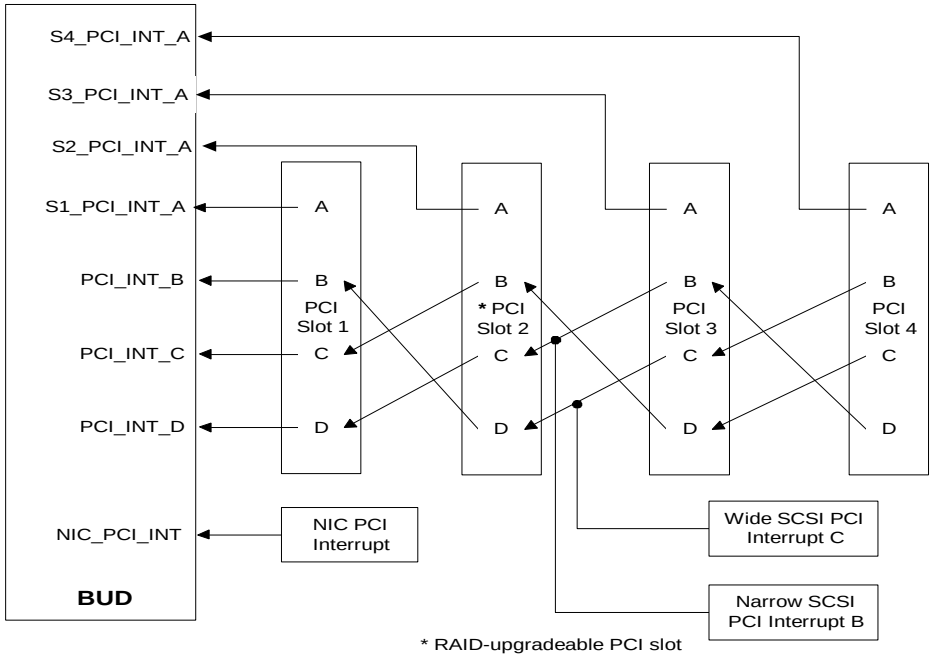


Figure 3-8. PCI Slot Interrupt Swizzle

1.38.2. PCI Interrupt Rerouting

Some multiprocessor operating systems are unable to handle interrupts from PCI slots and devices as pure PCI interrupts, via inputs 16-19 (allocated to PCI) of the I/O APIC. Rather, they expect PCI interrupts to be delivered as ISA IRQs. Multiprocessor operating systems may also expect some interrupts from the PC-compatible PIC in the PIIX4, and others from the I/O APIC (Mixed Mode). Some device drivers check whether the device uses one of the traditional IRQs, and if not (when the PCI interrupt is connected directly to the I/O APIC), the driver fails to install or run properly. The PIIX4 performs internal PCI to IRQ interrupt steering so that PCI interrupts can be delivered to the PIC. However, the PCI interrupt steering feature is unidirectional, which means that it cannot redirect PCI interrupts to the I/O APIC.

For these reasons, N440BX Server incorporates an external PCI to IRQ rerouter circuit in the BUD, that can be programmed to pass PCI interrupts through to inputs 16-19 of the I/O APIC, or deliver a specific PCI interrupt to an ISA IRQ. Under software control, a PCI interrupt can be individually rerouted to an ISA IRQ signal. This functionality is contained in the BUD.

Two 8-bit registers are provided in the rerouter circuit, with each nibble of a register controlling a specific PCI Interrupt line via PIO commands. The PIIX4 decodes the address of the PIO command and produces a chip select, which is controlled using the PIIX4 Programmable Chip Select Control register (78h - 79h). The rerouter uses only 2 bytes of the minimum 4 selectable, so aliases are provided. Refer to “PCI Interrupt to IRQ Routing Control” for run-time programming information. Refer to PIIX4 Programmable Chip Select Control register description for initialization-time requirements.

1.38.3.Working with PCI Interrupts

The N440BX DP Server baseboard shares PCI bus resources with onboard devices. The list below gives some guidelines to reduce the possibility of conflicts and performance restrictions.

1) Try to stay away from installing a LAN adapter in Slot 3. Either the configuration may not work or it may reduce the performance quality on the network. If the server needs an additional LAN adapter, install it in Slot 1 or 2 and this will allow for maximum throughput. Slot 4 could have the same results as Slot 3 and should not be used if possible

2) When configuring a RAID controller in the N440BX Server baseboard, Slots 1 and 2 are better for performance and configuration. This is due to the onboard resources that are being used. Another consideration is to have this RAID pack as the boot device. (Refer to Table 14 Boot Order.)

When integrating peripherals into a server system, taking into consideration the architecture of the PCI bus and the onboard resources can help in making the right choices and offering a reliable server.

1.39. Boot Order

The baseboard boot order for non-multi-boot cards is outlined in the following table. On the N440BX Server baseboard multi-boot cards will always sign-on ahead of all other cards and onboard SCSI.

Table 1 Boot Order

Order	Boot Device
1	Onboard IDE
2	Onboard SCSI
3	PCI Slot 1
4	PCI Slot 2
5	PCI Slot 3
6	PCI Slot 4

1.40. System Management Interrupt Handling

N440BX Server is designed to report these types of system errors: ISA bus, PCI bus, ECC memory, and System limit. Errors are reported by the BMC and PIIX4 using SMI_L. SMI is used for server management and advanced error processing. All errors can be intercepted by SMI for preprocessing (if SMI_L is enabled), or handled directly by NMI handlers. Some errors have to generate an NMI even if they are intercepted by the SMI, because the traditional way to handle errors in PC architecture is via the NMI. NMI/SMI handling logic in the BUD emulates non-ISA errors as ISA-compatible using NMI and SMI_L.

1.41. Basic Utility Device (BUD)

In addition to the PCI arbitration and interrupt rerouting functions described above, the BUD also gates and redirects SMI_L and NMI to generate SERR_L, and performs other miscellaneous logic functions (e.g., PCI arbitration expansion). The BUD contains an I/O mapped ISA interface for control of PCI-to-IRQ interrupt rerouting. Functional specifications for BUD signal pins are given in the following table.

Table 3-10. BUD Signal Descriptions

Signal	Pin	Type*	Description
AD0	92	I	Driven by ISA address bit SA0.
AD1	93	I	Driven by ISA address bit SA1.
APIC_INT0_L	32	O	INT0 signal to I/O APIC via series 10Ω resistor.
APIC_INT1_L	30	O	INT1 signal to I/O APIC via series 10Ω resistor.
APIC_INT2_L	31	O	INT2 signal to I/O APIC via series 10Ω resistor.
APIC_INT3_L	7	O	INT3 signal to I/O APIC via series 10Ω resistor.
APIC_INT4_L	33	O	INT4 signal to I/O APIC via series 10Ω resistor.
APIC_INT5_L	40	O	INT5 signal to I/O APIC via series 10Ω resistor.
APIC_INT6_L	9	O	INT6 signal to I/O APIC via series 10Ω resistor.
APIC_INT7_L	5	O	INT7 signal to I/O APIC via series 10Ω resistor.
BMC_SUSCLK	85	O	BMC suspend clock. The BUD divides the 32KHz PX4_SUSCLK (pin 41) by 256 to generate BMC_SUSCLK for BMC timestamping of SM events.
CLK_APIC	29	I	APIC clock from CK100 driver
CLK_PCI_BUD	90	I	Synchronous PCI master clock from CK100 driver
CLR_SMI	61	I	Driven by a PIIX4 GPIO bit 18 to clear a latched SMI condition. On assertion, clears the latched SMI signal in the BUD.
CPU_NMI	69	O	NMI to the processor(s), asserted when EN_NMI (pin 46) and NMI_PIIX4 (pin 50) are asserted, or when the Front Panel NMI switch is pressed.
CPU_SMI_L	83	O	Generates an SMI_L to the processor(s). This signal is gated by EN_SMI_L (pin 35) assertion and pending NMI request.
D0	94	I/O	Connects to ISA bus data bit SD0.
D1	96	I/O	Connects to ISA bus data bit SD1.
D2	97	I/O	Connects to ISA bus data bit SD2.
D3	98	I/O	Connects to ISA bus data bit SD3.
D4	99	I/O	Connects to ISA bus data bit SD4.
D5	100	I/O	Connects to ISA bus data bit SD5.
D6	1	I/O	Connects to ISA bus data bit SD6.
D7	2	I/O	Connects to ISA bus data bit SD7.
DIS_NON_FLASH_SMI	8	I	Driven by PIIX4 GPIO bit 25 as part of secure Flash programming mechanism.
EN_NMI	46	I	Driven by PIIX4 GPIO bit 19 to gate NMI generation (other than Front Panel NMI).
EN_NMI_TO_SMI_L	36	I	Driven by PIIX4 GPIO bit 17 to redirect NMI to SMI.
EN_SMI_L	35	I	Driven by PIIX4 GPIO bit 9, to enable the generation of SMI to the processor(s).
EN_SMI_TO_NMI	62	I	Driven by the BMC to redirect SMI_L to NMI, which is controlled from the ISA interface using BMC mailbox registers. SMI_L redirection occurs by default.
F_SERR	54	I	Driven by PIIX4 GPIO bit 8 to force assertion of SERR_L on PCI. The BUD converts the signal to a pulse synchronous with PCI, which generates SERR_L.

* I = Input, O = Output

Table 3-10. BUD Signal Descriptions (cont.)

Signal	Pin	Type*	Description
FLASH_PE_L	48	I	Driven by PIIX4 GPIO bit 24 to indicate a Flash BIOS programming cycle. The BUD generates SMI_L in response, which supports the secure Flash programming mechanism on N440BX DP (see "Flash ROM BIOS" above).
IORD_L	87, 14	I	I/O read command driven by the ISA IORD_L signal.
IOWR_L	10	I	I/O write command driven by the ISA IOWC_L signal.
IRQ3	12	O	ISA IRQ3 signal from PCI to IRQ re-router in the BUD.
IRQ4	68	O	ISA IRQ4 signal from PCI to IRQ re-router in the BUD.
IRQ5	13	O	ISA IRQ5 signal from PCI to IRQ re-router in the BUD.
IRQ7	44	O	ISA IRQ7 signal from PCI to IRQ re-router in the BUD.
IRQ10	65	O	ISA IRQ10 signal from PCI to IRQ re-router in the BUD.
IRQ11	67	O	ISA IRQ11 signal from PCI to IRQ re-router in the BUD.
IRQ12	49	O	ISA IRQ12 signal from PCI to IRQ re-router in the BUD.
IRQ15	64	O	ISA IRQ15 signal from PCI to IRQ re-router in the BUD.
ISA_BALE	72	I	Driven by ISA BALE signal.
ISA_RSTDRV_L	88	I	Reset to the BUD from ISA interface reset signal.
NMI_FP_L	42	I	Front Panel NMI directly from the momentary push button switch on the Front Panel (in parallel with BMC connection). Pressing of this switch is captured by NMI latch circuitry in the BUD.
NMI_PIIX4	50	I	NMI indication from the PIIX4, which causes the assertion of CPU_NMI (pin 69) to occur if EN_NMI (pin 46) is also asserted.
P_GNT0_L	25	I	GNT0_L signal from NBX for arbitration expansion logic in BUD
P_INT_B_L	19	I	Interrupt B from cascaded PCI_INTB,C,D_L PCI slot interrupt swizzle, and SCSI controller PCI_INTB_L (wide).
P_INT_C_L	18	I	Interrupt C from cascaded PCI_INTB,C,D_L PCI slot interrupt swizzle, and SCSI controller PCI_INTC_L (narrow).
P_INT_D_L	17	I	Interrupt D from cascaded PCI_INTB,C,D_L PCI slot swizzle.
P_INT_NIC_L	20	I	Interrupt from NIC PCI_INTA_L
P_INT_PCI1_L	24	I	Interrupt from PCI slot 1 PCI_INTA_L
P_INT_PCI2_L	23	I	Interrupt from PCI slot 2 PCI_INTA_L
P_INT_PCI3_L	22	I	Interrupt from PCI slot 3 PCI_INTA_L
P_INT_PCI4_L	21	I	Interrupt from PCI slot 4 PCI_INTA_L
P_REQ0_L	79	O	REQ_L signal to NBX from PCI arbitration logic expansion logic in BUD.
P_SERR_L	80	O	PCI SERR_L signal forced by the BUD.
PD_CS_L	57	I	Driven by PIIX4 PCS0 as part of ISA I/O interface to the BUD.
PS_FRAME_L	37	I	FRAME_L signal from PCI interface for arbitration expansion logic in BUD.
PS_IRDY_L	55	I	IRDY_L signal from PCI interface for arbitration expansion logic in BUD.
PS_STOP_L	6	I	STOP_L signal from PCI interface for arbitration expansion logic in BUD.
PS_TRDY_L	52	I	TRDY_L signal from PCI interface for arbitration expansion logic in BUD.
PX4_SUSCLK	41	I	PIIX4 suspend clock. 32KHz clock source for BMC suspend clock.
RST_P_RST_L	89	I	Reset to the BUD from PCI interface reset signal.
S_GNT0A_L	71	O	GNT_L signal to PCI slot 1
S_GNT0B_L	84	O	GNT_L signal to SCSI controller chip
S_REQ0A_L	45	I	REQ_L signal from PCI slot 1
S_REQ0B_L	47	I	REQ_L signal from SCSI controller chip
SMI_BMC_L	27	I	Driven by the BMC to indicate the occurrence of an SMI condition.
SMI_PIIX4_L	56	I	Asserted by the PIIX4 on occurrence of an SMI_L condition, to indicate a request for handler service.

TCK	62	I/O	
Signal	**Pin**	**Type***	**Description**
TDI	4	I/O	IEEE 1149.1 Boundary Scan Signals
TDO	73	I/O	(for prototype only)
TMS	15	I/O	

* I = Input, O = Output

2. Server Management

2.1. Overview

On N440BX Server, three serial buses that follow IMB protocol provide independent pathways for server management functions. The PIIX4 system management bus mentioned above (PIIX4 SMB) connects with each DIMM, and controls SDRAM clocks and processor speed configuration. A single micro-controller referred to as the Baseboard Management Controller (BMC) manages the other two IMB segments:

- Server Management Bus supporting 8K SEEPROM and processor/baseboard temperature sensors.
- Intelligent Management Bus (IMB) supporting connectors to system-wide server management devices.

In addition, the BMC manages sensors directly using I/O and ADC lines, controls the Emergency Management Port (EMP), detects and reports system fan failures, and manages Fault Resilient Booting (FRB). The BMC provides the Host ISA and IMB interfaces to server management features on N440BX Server. The following diagram illustrates server management architecture on the N440BX Server baseboard.

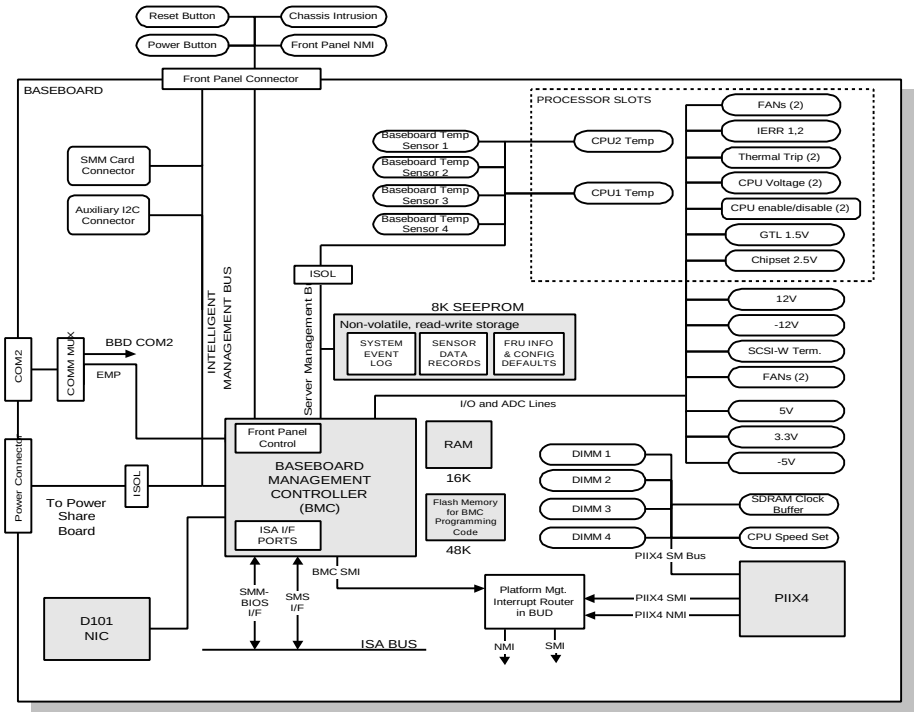


Figure 3-9. Server Management Block Diagram

2.2. Server Management Bus

The Server Management Bus (SMB) is a single master, open-drain, serial bus which is electrically and timing compatible with the 100 Kbps version of the IMB bus specification. The SMB extends throughout the baseboard providing an independent pathway for the BMC to communicate with 4 baseboard and 2 processor slot temperature sensors. In addition, the SMB supports an 8K SEEPROM device for non-volatile storage of the System Event Log (SEL), Sensor Data Record Repository (SDRR), FRU information, and configuration defaults. The BMC controls access to this device and manages the data structures within (refer to BMC description below).

Buffers are provided to isolate the baseboard and processor temperature sensors from the rest of the SMB. These buffers, running on 5V_Standby, keep the bus alive to the BMC even though main power is switched off. This allows the BMC to communicate with its SEEPROM at all times.

2.3. Intelligent Management Bus

The Intelligent Management Bus (IMB) is a multi-master, open-drain, serial bus which is also electrically and timing compatible with the 100 Kbps version of the IMB bus specification. The IMB attaches to connectors on the baseboard creating a server management network that extends throughout the baseboard and system chassis, providing an independent pathway for communications between the BMC and system-level server management devices (e.g., Hot-swap SCSI controller). In addition, the IMB provides inter-chassis communications extensions for a complete server management network solution.

The communication protocol for the IMB is defined in the *Intelligent Management Bus Communications Protocol Specification*. The protocol is designed to work with micro-controllers and other IMB masters, and slave devices such as IMB temperature sensors.

The IMB attaches to the following connector interfaces on the N440BX Server board:

- Auxiliary IMB connector
- Server Monitor Module (SMM) card feature connector
- Front panel connector
- Auxiliary power connector (via isolation buffer)

The N440BX Server board provides the main pull-ups on the clock (IMB_SCL) and data (IMB_SDA) lines of the IMB. This termination is sized to drive the full IMB, i.e., capacitive loading for not only the board, but for the chassis, SMM Card IMB, and auxiliary IMB connections. Sufficient pull-up capability is provided on the isolated side of the IMB for the BMC, SMM Card, SMM Card IMB, Front Panel IMB, and aux. IMB connections. These pull-ups are driven by 5V Standby. Since a full set of pull-ups is provided on the board, additional pull-ups are not necessary for external devices connecting to the IMB. Only the N440BX Server board should provide pull-ups for these connections.

Following are definitions of aux. IMB, SMM card, aux. power and main front panel connectors.

Auxiliary IMB Connector

The auxiliary IMB connector has the following pinout.

Table 3-11. Auxiliary IMB Connector Pinout

Pin	Signal
1	Local IMB SCL
2	GND
3	Local IMB SDA

Caution:

A shorted IMB connection at the auxiliary IMB connector will disrupt proper operation of the IMB.

2.3.1. SMM Card Feature Connector

The SMM card feature connector attaches to the IMB. In addition to IMB signals, the 26-pin connector provides the following signals as shown in the table below:

Table 3-12. SMM Card Feature Connector Pinout

Pin	Signal	Description
1	CPU_SMI_L	System Management Interrupt
2	LOCAL_IMB_SCL	IMB clock line
3	GND	Ground
4	Reserved	-
5	PWR_CNTRL_SFC_L	Host power supply on/off control
6	LOCAL_IMB_SDA	IMB serial data line
7	5VSTNDBY	+5V standby indication (power OK)
8	KEYLOCK_SFC_L	Keyboard lock signal
9	CPU_NMI	Non-maskable interrupt indication
10	VCC3	3.3V power supply status input
11	RST_SFC_L	Baseboard reset signal from Server Monitor Module
12	GND	Ground
13	GND	Ground
14	Reserved	-
15	SECURE_MODE_BMC	Secure mode indication
16	GND	Ground
17	SFC_CHASSIS_INSTRUSION_L	Chassis intrusion indication
18	Reserved	-
19	Reserved	-
20	GND	Ground
21	Reserved	-
22	Reserved	-
23	Reserved	unused
24	Reserved	-
25	Key pin (nc)	Connector key
26	Reserved	-

2.3.2. Auxiliary Power Connector

A 14-pin connector is provided for power supply status indication, as well as the IMB IMB connection. Other power connector pin outs are specified in the ***Appendix***. The aux. power connector has the following pinout:

Table 3-13. Auxiliary Power Connector Pinout

Pin	Signal	Pin	Signal
1	+5V Sense Return	2	+5V Sense
3	+3V Sense	4	+3V Sense Return
5	IMB Clock line	6	IMB Data line
7	GND	8	POWER_GOOD
9	PS_POWER_ON	10	GND
11	+5V standby	12	nc (Key)
13	Reserved	14	GND

2.4. Chassis Intrusion

The chassis intrusion header has been added to the baseboard of the N440BX Server. It is a 3-pin, shrouded and keyed connector located near the NIC indicator LEDs. Intrusion has occurred when the signal is open, chassis is secure when pulled to ground. The chassis intrusion header has the following pin out.

Table 2 Chassis Intrusion Pin-out

Pin	Signal
1	Chassis Intrusion
2	GND
3	Chassis Intrusion

2.4.1. Front Panel Connector

A 16-pin header is provided that attaches to the system front panel, which contains reset, NMI, and power control switches, LED indicators, as well as the IMB IMB connection. The connector has the following pinout:

Table 3-14. Front Panel Connector Pinout

Pin	Signal	Pin	Signal
1	GND	2	Hard disk activity LED
3	Front panel reset switch	4	Front panel power switch
5	+5V	6	nc (key)
7	Front panel NMI switch	8	+5V
9	Fan failure indicator LED	10	Chassis intrusion switch
11	Power fault LED	12	+5V standby
13	IMB Data line	14	GND
15	IMB Clock line	16	GND

2.5. Baseboard Management Controller (BMC)

On N440BX Server, all server management functionality formerly distributed between three controllers is concentrated in the BMC. The BMC and associated circuitry are powered from 5V_Standby, which remains active when system power is switched off. The BMC is implemented using a Dallas Semiconductor DS82CH10 micro-controller.

The primary function of the BMC is to autonomously monitor system platform management events, and log their occurrence in the non-volatile SEL. (Sensor Error Log). These events include such as over-temperature and over-voltage conditions, fan failure, or chassis intrusion. While monitoring, the BMC maintains the non-volatile SDRR (Sensor Data Record Repository), from which run-time information can be retrieved. The BMC provides an ISA host interface to SDRR information, so software running on the server can poll and retrieve the current status of the platform. A shared register interface is defined for this purpose.

SEL contents can be retrieved after system failure, for analysis by field service personnel using system management tools, such as Intel LANDesk® Server Manager. Since the BMC is powered by 5V_Standby, SEL (and SDRR) information is also available via the IMB. An Emergency Management Card, such as the Intel LANDesk SMM card, can obtain the SEL and make it remotely accessible using a LAN or telephone line connection. N440BX Server introduces the Emergency Management Port (EMP), which allows remote access to the SEL and other features using the COM2 port. During its watch, the BMC performs the following functions:

- Baseboard temperature and voltage monitoring
- VID Bit reading
- Processor presence monitoring and FRB control
- Baseboard fan failure detection and indicator control
- SEL interface management
- SDR Repository interface management
- SDR/SEL time stamp clock
- Baseboard Field Replaceable Unit (FRU) information interface
- System management watchdog timer
- Periodic SMI timer
- Front panel NMI handling
- Event receiver
- ISA host and IMB interface management
- Secure mode control, video blank and floppy write protect monitoring and control, front panel lock/unlock initiation.
- Sensor event initialization agent
- Wake-on LAN (WOL) via Magic Packet support

- ACPI Support

2.5.1. BMC Front Panel Control

The BMC performs all front panel controller functions on N440BX Server. These include control of system power, hard-resets, and the power failure LED. The BMC drives system power-on/off or hard reset from the following sources:

- Front panel push-button
- SMM card feature connector signal (controlled by secure mode)
- Transition of PIIX real-time clock alarm/suspend signal
- Command from IMB via front panel connector, aux. IMB, or SMM card
- Magic Packet signal from NIC
- Command from EMP
- Command from ISA interface
- BMC watchdog timer

2.5.2. Secure Mode

The BMC monitors the SECURE_MODE signal from the baseboard keyboard controller. When the system is powered up, and SECURE_MODE asserted, the BMC prevents power off or reset via the front panel power and reset push buttons. A 'Secure Mode Violation Attempt' event is flagged by the BMC whenever a front panel push button is pressed. The BMC also provides options for blanking the onboard video, and write-protecting the onboard floppy interface when Secure Mode is active. Refer to the *N440BX Server BIOS External BIOS Specification*, for more information.

2.5.3. Power Fault LED

The BMC controls the front panel Power Fault LED signal. The BMC asserts this signal whenever it attempts to power on the system without success, and when the BMC detects a power supply failure. The BMC can also be directed to assert this signal via an IMB 'Force Power Fault LED On' command.

2.6. Emergency Management Port (EMP)

The COM2 serial port on the N440BX Server can be configured for use as an Emergency Management Port (EMP). EMP provides a level of system management via RS-232 during powered-down, pre-boot, and post-boot situations. This allows System Management Software (SMS) interactions via point-to-point RS-232 connections, or external modem. EMP provides access to these basic management features:

- System power up
- System power down (Not available in restricted mode).
- System Reset (Not available in restricted mode).
- Access to the System Event Log, FRU, and Sensor Data Records.
- Access to BIOS Console Redirection.
- Password Protection

The EMP is intended for use in a secure environment. A simple password can be configured to provide a rudimentary level of security on the interface. System configuration options can be used to disable this interface.

The COM2 port can be used on N440BX Server for three different purposes: EMP, console redirection, or normal COM usage. If the BMC is using the port for EMP purposes, it is unavailable to the BIOS or SMS during this mode. If the System BIOS is using the port for console redirection, it is unavailable to the BMC or SMS (since the machine is still doing POST). Under normal usage COM2 appears to the OS as a normal serial port; in this case the BMC and System BIOS cannot use the port.

The N440BX Server EMP architecture supports several remote access modes, selectable using the F2 BIOS Setup Screen, as follows:

1. **Pre-boot only mode** - The EMP is only available while the machine is powered off and during POST. Just prior to booting the OS, the System BIOS disables the EMP by sending a command to the BMC. COM2 is then available as a normal serial port.
2. **SMS activated mode** - Essentially the same as Pre-boot only, except that SMS software may elect to take ownership or release control of COM2. This mode allows SMS to configure the system for remote access.
3. **Always active mode** - EMP and Console Redirect are available under the same conditions as listed in #1 above. However, the System BIOS leaves the port enabled for run-time EMP and SMS usage. The BIOS configures the hardware such that the O/S can not “see” the port.
4. **Always disabled mode** - EMP and Console Redirection are not available under any conditions.

5. **Restricted mode -** This option can be selected in conjunction with either the 'Pre-boot Only' or 'Always Active' modes listed above, using the BIOS setup interface. When activated, Power Down control, Front Panel NMI, and Reset Control via the EMP are disabled. Power On control, System Event Log access, FRU Inventory, and Sensor Data Repository access remain enabled. Console redirection operation is unaffected by Restricted Mode.

2.6.1. EMP Password

The BMC implements a simple password mechanism for the EMP, activated by BIOS setup. If the password is active, a correct password must be received on the EMP before any other commands are accepted. The password must be entered every time COM2 is switched over to EMP operation. It must also be re-entered if the EMP has been inactive for more than 30 seconds. Only BIOS setup can set or clear the password, it cannot be changed remotely.

2.7. Fault Resilient Booting

The BMC implements Fault Resilient Booting (FRB) levels 1, 2, and 3. If two processors are installed and the processor designated as the BSP fails to complete the boot process, FRB attempts to boot the system using the alternate processor.

- FRB level 1 is for recovery from a BIST failure detected during POST. This FRB recovery is fully handled by BIOS code.
- FRB level 2 is for recovery from a Watchdog time out during POST. The Watchdog timer for FRB level 2 detection is implemented in the BMC.
- FRB level 3 is for recovery from a Watchdog time out on Hard Reset / Power-up. Hardware functionality for this level of FRB is provided by the BMC on the processor subsystem.

FRB-3 is managed by the BMC, which controls the ability to boot using either processor in the event of a catastrophic processor failure. On power up, a timer starts that can only be stopped by a healthy processor using the GPIO bit, FRB_TMRHLT_L, on the PIIX4. If processor 0 fails to halt the FRB timer before time out, the controller asserts STOP_FLUSH to the processor and asserts FRB_RST_L for 10ms. When the system comes out of reset, processor 0 is prevented from acting as the BSP, allowing the other processor to take over the boot process.

2.8. System Fan Interface

N440BX Server provides four 3-pin, shrouded, and keyed fan connectors. Two of these connectors, located next to each Pentium II processor card on the baseboard, are for a fansink. The remaining two connectors on the baseboard attach to chassis fans equipped with a sensor that indicates whether the fan is operating. The sensor pins for these fans are routed to the BMC for failure monitoring. The two connector types have the following pinout:

Table 3-15. Chassis Fan Connector Pinout

Pin	Signal
1	GND
2	Fan Sensor
3	+12V

Table 3-16. Fansink Connector Pinout

Pin	Signal
1	GND
2	+12V
3	Fan Sensor

The following table details the baseboard jumper functions.

Table 3 Board Jumper description

Function	**Pins (default in bold)**	**What it does at system reset**
CMOS clear	1-2, Protect	Preserves the contents of NVRAM.
	2-3, Erase	Replaces the contents of NVRAM with the Intel manufacturing default settings.
Password clear	5-6, Protect	Maintains the current system password.
	6-7, Erase	Clears the password.
Recovery Boot	9-10, Normal	System attempts to boot using the BIOS stored in flash memory.
	10-11, Recovery	BIOS attempts a recovery boot, loading BIOS code from a floppy diskette into the flash device. This is typically used when the BIOS code has been corrupted.
Boot Block Write Protect	13-14, Protect	BIOS boot block is write-protected
	14-15	BIOS boot block is erasable and programmable
		CAUTION: Programming the boot block incorrectly will prevent the system from booting.
Clock Enable	1-2, Protect	Processor speed configuration is protected.
	2-3, Enable	Processor speed configuration is enabled. Changes can be made in BIOS/SCU.
FRB Timer Enable	5-6, Enable	FRB operation is enabled (system boots from processor 1 if processor 0 fails)..
	6-7, Disable	FRB is disabled..
Chassis Intrusion Detection	9-10, Enable	Switch installed on chassis indicates when cover has been removed.
	10-11, Disable	Chassis intrusion switch is bypassed.
Host Bus In-order Queue	13-14, Max	Host in-order queue depth is set at maximum to increase system performance
	14-15, Min (1)	Host in-order queue depth is set at 1 Normally used for debugging and slower legacy PCI/ISA add-in cards.

3. Memory and Other Resource Mappings

This chapter describes the initial programming environment including address maps for memory and I/O, techniques and considerations for programming ASIC registers, and hardware options configuration. ***Chapter 3 is referenced from the R440LX DP server and needs to be updated to represent the N440BX Server configuration.***

3.1. Memory Space

At the highest level, Pentium® II processor address space is divided into 4 regions, as shown in the following figure. Each region contains sub-regions, as described in the following sections. Attributes can be independently assigned to regions and sub-regions using PAC registers.

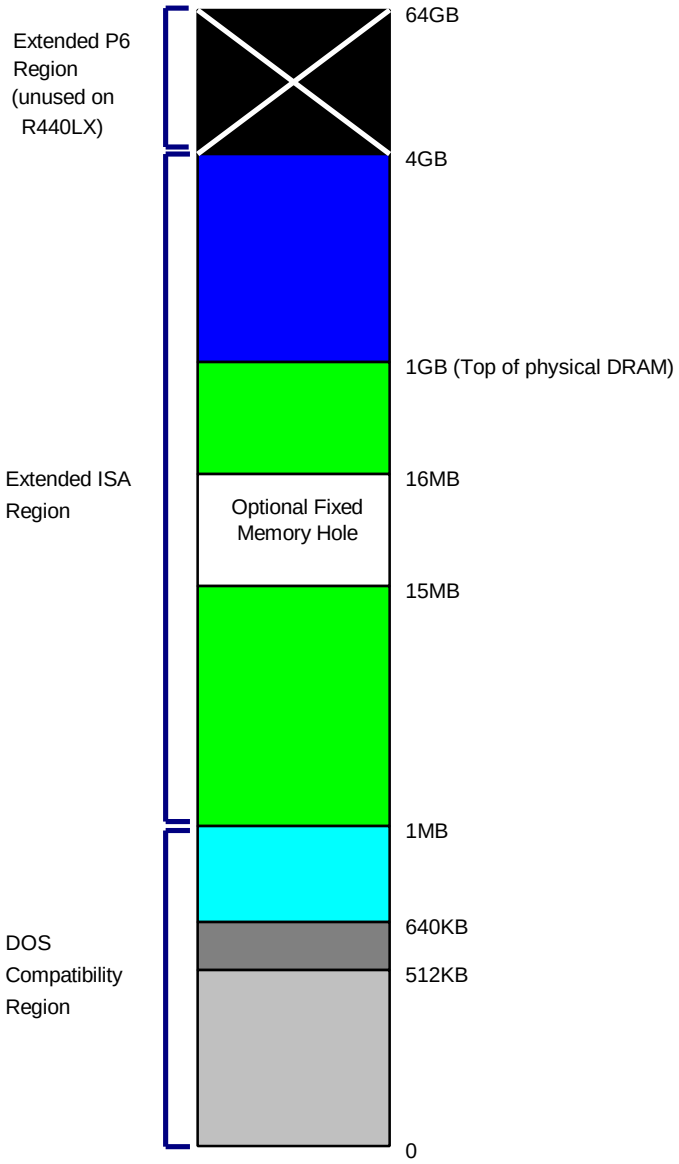


Figure 15. Pentium II processor memory address space

3.2. DOS Compatibility Region

The first region of memory below 1MB was defined for early PCs, and must be maintained for compatibility reasons. This region is divided into sub-regions as shown in the following figure.

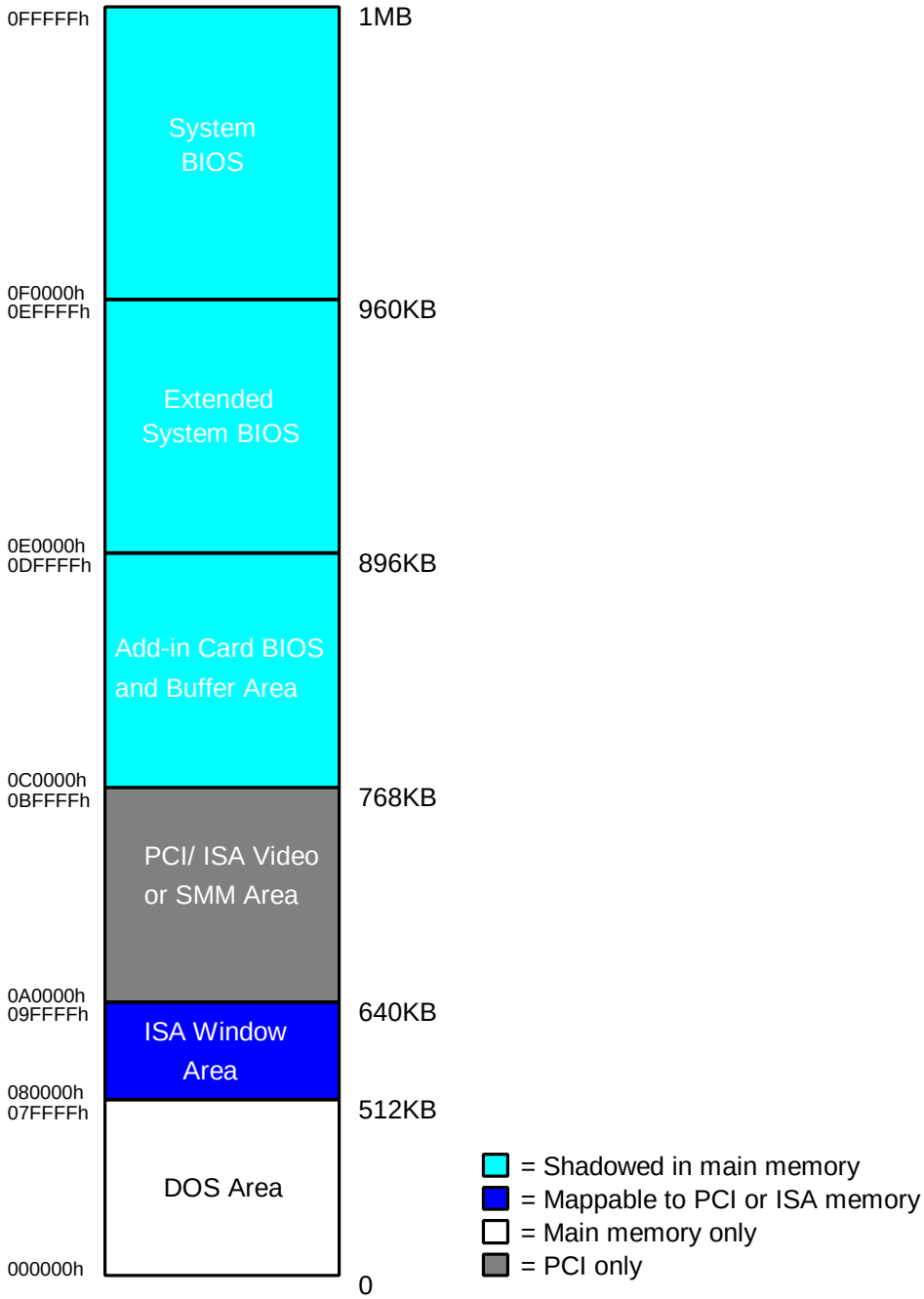


Figure 16. DOS Compatibility Region

3.3. DOS Area

The DOS region is 512KB in the address range 0 to 07FFFFh. This region is fixed and all accesses go to main memory.

3.4. ISA Window Memory

The ISA Window Memory is 128KB between the addresses of 080000h to 09FFFFh. This area can be mapped to the PCI bus or main memory.

3.5. Video or SMM Memory

The 128KB Graphics Adapter Memory region at 0A0000h to 0BFFFFh is normally mapped to the VGA controller on the PCI bus. This region is also the default region for SMM space. The SMM region can be remapped by programming the SMRAM Control Register in the PAC.

3.6. Add-in Card BIOS and Buffer Area

The 128KB region between addresses 0C0000h and 0DFFFFh is divided into eight segments of 16KB segments mapped to ISA memory space, each with programmable attributes, for expansion card buffers. Historically, the 32KB region from 0C0000h to 0C7FFFh has contained the video BIOS location on a video card. However, on N440BX Server, the video BIOS is located in the Extended BIOS or System BIOS areas.

3.7. Extended System BIOS

This 64KB region from 0E0000h to 0EFFFFh is divided into 4 blocks of 16KB each, and may be mapped with programmable attributes to map to either main memory or to the PCI bus. Typically, this area is used for RAM or ROM.

3.8. System BIOS

The 64KB region from 0F0000h to 0FFFFFh is treated as a single block. By default this area is normally Read/Write disabled with accesses forwarded to the PCI bus. Through manipulation of R/W attributes, this region can be shadowed into main memory.

3.9. Extended Memory

Extended memory on N440BX Server is defined as all address space greater than 1MB. The Extended Memory region covers 4GB of address space from addresses 0100000h to FFFFFFFFh, as shown in the following figure.

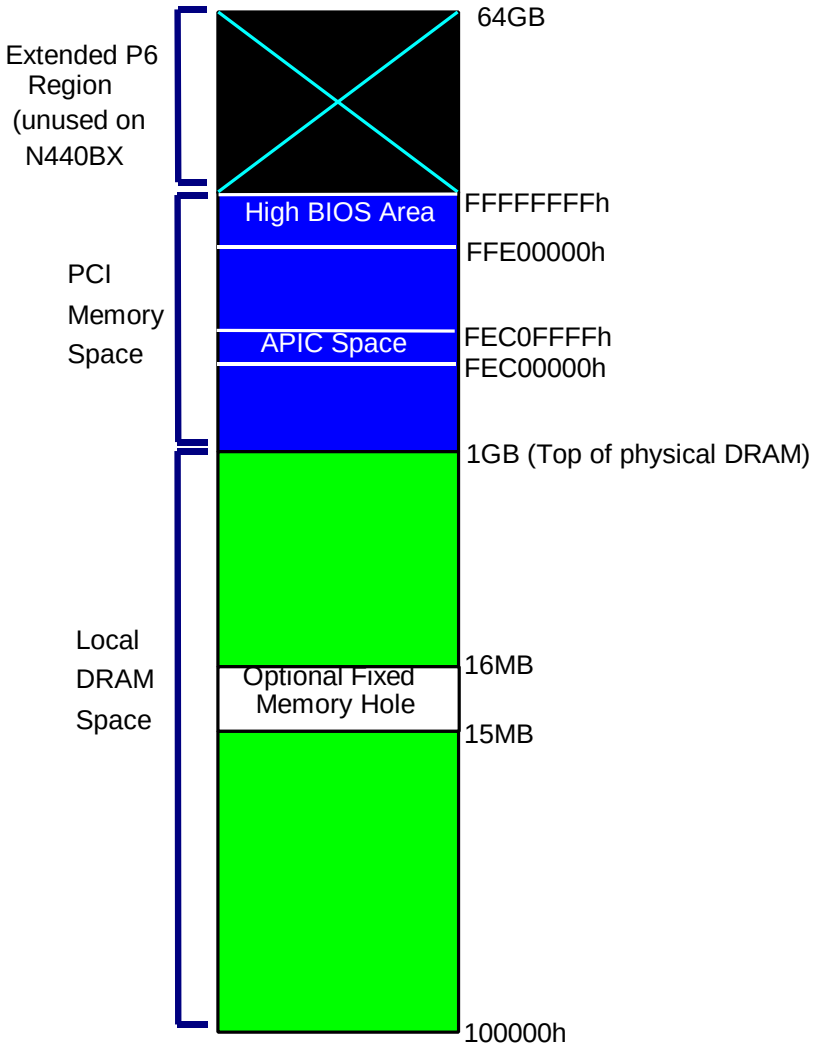


Figure 17 Extended Memory Map

3.10. Main Memory

All installed SDRAM greater than 1MB is mapped to local main memory, up to the top of physical memory that is located at 1GB. Memory between 1MB to 15MB is considered to be standard ISA extended memory. 1MB of memory starting at 15MB can be optionally mapped to the PCI bus memory space. The remainder of this space, up to 1GB, is always mapped to main memory.

3.11. PCI Memory Space

Memory addresses between 1GB and 4GB are mapped to the PCI bus. This region is divided into three sections: High BIOS, APIC Configuration Space, and General-purpose PCI Memory.

The General-purpose PCI Memory area is typically used for memory-mapped I/O to PCI devices. The memory address space for each device is set using PCI configuration registers

3.12. High BIOS

The top 2MB of Extended Memory is reserved for the system BIOS, extended BIOS is for PCI devices, and A20 aliasing by the system BIOS. The Pentium II processor begins executing from the High BIOS region after reset. Only 256KB of the high BIOS area is actually required by the BIOS, but 2MB is required by Pentium II processor MTRR programming.

3.13. I/O APIC Configuration Space

A 64KB block located 20MB below 4GB (0FEC00000h to 0FEC0FFFFh) is reserved for the I/O APIC configuration space.

I/O APIC units are located beginning at a base address determined by subtracting 013FFFF0h from the reset vector. The first I/O APIC is located at FEC00000h. Each I/O APIC unit is located at FEC0x000h where x is the I/O APIC unit (0 through F).

3.14. Extended Pentium II Processor Region (above 4GB)

A Pentium II processor-based system can have up to 64GB of addressable memory. However, the 82440BX PCIset only supports 32-bit addressing, with the BIOS operating in 4GB of address space (the memory DIMMs provide up to 512MB of main memory). All accesses to the region from 4GB to 64GB are claimed by the PAC and terminated. Write data is dropped and zeroes are returned on reads.

3.15. Memory Shadowing

Any block of memory that can be designated as read-only or write-only can be “shadowed” into memory located on the Pentium II processor bus. Typically, this is done to allow ROM code to execute more rapidly out of RAM. ROM is designated read-only during the copy process while RAM at the same address is designated write-only. After copying, the RAM is designated read-only and the ROM is designated write-only (shadowed). Processor bus transactions are routed accordingly. Transactions originating from the PCI bus or ISA masters and targeted at shadowed memory blocks will not appear on the processor's bus.

3.16. SMM Mode Handling

A Pentium II processor asserts SMMEM_L in its Request Phase if it is operating in System Management Mode (SMM). SM code resides in SMRAM. SMRAM can overlap with memory residing on the Pentium II processor bus or memory normally residing on the PCI bus. The PAC determines where SMRAM space is located through the value of the SMM Range configuration space register.

The SMRAM Enable bit in the SMRAM Enable configuration register will determine how the SM accesses are handled by the PAC component. When the SMRAM Enable bit is zero (SMRAM disabled), accesses to the SMM Range with SMMEM_L asserted are ignored by the PAC. When the SMRAM Enable bit is one (SMRAM enabled), accesses to the SMM range with SMMEM_L asserted are claimed by the PAC.

If the SMMEM_L signal is not asserted, the SMM Range is not decoded regardless of the state of the SMRAM Enable bit (this allows SMRAM to overlap with memory normally residing on the processor bus).

In summary, when the SMMEM_L signal is asserted, the SMM Range is similar to a Memory Space Gap, where the SMM Enable bit either enables or disables the memory gap.

The SMI_L signal may be asserted in the Response Phase by a device in SMM power-down mode.

Refer to the System Management RAM Control Register (SMRAM 72h)

3.17. I/O Map

The PAC allows I/O addresses to be mapped to the processor bus or through designated bridges in a multi-bridge system. Other PCI devices, including PIIX4, have built-in features that support PC-compatible I/O devices and functions, which are mapped to specific addresses in I/O space. On N440BX Server, the PIIX4 provides the bridge to ISA functions. The I/O map in the following table shows the location in N440BX Server I/O space of all directly I/O-accessible registers. PCI configuration space registers for each device control mapping in I/O and memory spaces, and other features that may affect the global I/O map. All configuration space registers for PCI devices are described in Chapter 5. The SuperI/O controller contains configuration registers that are accessed through an index and data port mechanism.

Table 4 N440BX I/O Map

Address(es)	Resource	Notes
0000h - 000Fh	DMA Controller 1	
0010h - 001Fh	DMA Controller 1	aliased from 0000h - 000Fh
0020h - 0021h	Interrupt Controller 1	
0022h - 0023h		
0024h - 0025h	Interrupt Controller 1	aliased from 0020h - 0021h
0026h - 0027h		
0028h - 0029h	Interrupt Controller 1	aliased from 0020h - 0021h
002Ah - 002Bh		
002Ch - 002Dh	Interrupt Controller 1	aliased from 0020h - 0021h
002Eh - 002Fh	SuperI/O Index and Data Ports	
0030h - 0031h	Interrupt Controller 1	aliased from 0020h - 0021h
0032h - 0033h		
0034h - 0035h	Interrupt Controller 1	aliased from 0020h - 0021h
0036h - 0037h		
0038h - 0039h	Interrupt Controller 1	aliased from 0020h - 0021h
003Ah - 003Bh		
003Ch - 003Dh	Interrupt Controller 1	aliased from 0020h - 0021h
003Eh - 003Fh		
0040h - 0043h	Programmable Timers	
0044h - 004Fh		
0050h - 0053h	Programmable Timers	aliased from 0040h - 0043h
0054h - 005Fh		
0060h, 0064h	Keyboard Controller	Keyboard chip select from 97307
0061h	NMI Status & Control Register	
0063h	NMI Status & Control Register	aliased
0065h	NMI Status & Control Register	aliased
0067h	NMI Status & Control Register	aliased
0070h	NMI Mask (bit 7) & RTC Address (bits 6::0)	
0072h	NMI Mask (bit 7) & RTC Address (bits 6::0)	aliased from 0070h
0074h	NMI Mask (bit 7) & RTC Address (bits 6::0)	aliased from 0070h
0076h	NMI Mask (bit 7) & RTC Address (bits 6::0)	aliased from 0070h
0071h	RTC Data	
0073h	RTC Data	aliased from 0071h
0075h	RTC Data	aliased from 0071h
0077h	RTC Data	aliased from 0071h

Table 5 N440BX I/O Map (cont.)

Address(es)	Resource	Notes
0080h - 0081h	BIOS Timer	
0080h - 008Fh	DMA Low Page Register	PIIX4
0090h - 0091h	DMA Low Page Register (aliased)	PIIX4
0092h	System Control Port A (PC-AT control Port) (this port not aliased in DMA range)	PIIX4
0093h - 009Fh	DMA Low Page Register (aliased)	PIIX4
0094h	Video Display Controller	
00A0h - 00A1h	Interrupt Controller 2	PIIX4
00A4h - 00A15	Interrupt Controller 2 (aliased)	PIIX4
00A8h - 00A19	Interrupt Controller 2 (aliased)	PIIX4
00ACh - 00ADh	Interrupt Controller 2 (aliased)	PIIX4
00B0h - 00B1h	Interrupt Controller 2 (aliased)	PIIX4
00B2h	Advanced Power Management Control	PIIX4
00B3h	Advanced Power Management Status	PIIX4
00B4h - 00B5h	Interrupt Controller 2 (aliased)	PIIX4
00B8h - 00B9h	Interrupt Controller 2 (aliased)	PIIX4
00BCh - 00BDh	Interrupt Controller 2 (aliased)	PIIX4
00C0h - 00DFh	DMA Controller 2	PIIX4
00F0h	Clear NPX error	Resets IRQ13
00F8h - 00FFh	x87 Numeric Coprocessor	
0102h	Video Display Controller	
0170h - 0177h	Secondary Fixed Disk Controller (IDE)	PIIX4 (not used)
01F0h - 01F7h	Primary Fixed Disk Controller (IDE)	PIIX4
0200h - 0207h	Game I/O Port	Not used
0220h - 022Fh	Serial Port A	
0238h - 023Fh	Serial Port B	
0278h - 027Fh	Parallel Port 3	
02E8h - 02EFh	Serial Port B	
02F8h - 02FFh	Serial Port B	
0338h - 033Fh	Serial Port B	
0370h - 0375h	Secondary Floppy	
0376h	Secondary IDE	
0377h	Secondary IDE/Floppy	
0378h - 037Fh	Parallel Port 2	
03B4h - 03BAh	Monochrome Display Port	
03BCh - 03BFh	Parallel Port 1 (Primary)	
03C0h - 03CFh	Video Display Controller	
03D4h - 03DAh	Color Graphics Controller	
03E8h - 03EFh	Serial Port A	
03F0h - 03F5h	Floppy Disk Controller	
03F6h - 03F7h	Primary IDE - Sec. Floppy	
03F8h - 03FFh	Serial Port A (Primary)	
0400h - 043Fh	DMA Controller 1, Extended Mode Registers.	PIIX4

Table 22 N440BX I/O Map (cont.)

Address(es)	Resource	Notes
0461h	Extended NMI / Reset Control	PIIX4
0462h	Software NMI	PIIX4
0480h - 048Fh	DMA High Page Register.	PIIX4
04C0h - 04CFh	DMA Controller 2, High Base Register.	
04D0h - 04D1h	Interrupt Controllers 1 and 2 Control Register.	
04D4h - 04D7h	DMA Controller 2, Extended Mode Register.	
04D8h - 04DFh	Reserved	
04E0h - 04FFh	DMA Channel Stop Registers	
0678h - 067Ah	Parallel Port (ECP)	
0778h - 077Ah	Parallel Port (ECP)	
07BCh - 07BEh	Parallel Port (ECP)	
0800h - 08FFh	NVRAM	
0C80h - 0C83h	EISA System Identifier Registers	PIIX4
0C84h	Board Revision Register	
0C85h - 0C86h	BIOS Function Control	
0CA9h	DISMIC Data Register	Server management mailbox registers.
0CAAh	DISMIC Control/Status Register	
0CABh	DISMIC Flags Register	
0CF8h	PCI CONFIG_ADDRESS Register	Located in PAC
0CF9h	PAC Turbo and Reset control	PIIX4
0CFCh	PCI CONFIG_DATA Register	Located in PAC
46E8h	Video Display Controller	
xx00 - xx1F*	SCSI registers	Refer to SCSI chip doc.

*SCSI I/O base address is set using configuration registers.

3.18. Accessing Configuration Space

All PCI devices contain PCI configuration space, accessed using mechanism #1 defined in the *PCI 2.1 Local Bus Specification*. The PIIX4 is accessed as a multi-function PCI device, with 3 sets of configuration registers.

If dual processors are used, only the processor designated as the BSP should perform PCI configuration space accesses. Precautions should be taken to guarantee that only one processor is accessing configuration space at a time.

Two Dword I/O registers in the PAC are used for the configuration space register access:

- CONFIG_ADDRESS (I/O address 0CF8h)
- CONFIG_DATA (I/O address 0CFCh)

When CONFIG_ADDRESS is written to with a 32-bit value selecting the bus number, device on the bus, and specific configuration register in the device, a subsequent read or write of CONFIG_DATA initiates the data transfer to/from the selected configuration register. Byte enables are valid during accesses to CONFIG_DATA; they determine whether the configuration register is being accessed or not. Only full Dword reads and writes to CONFIG_ADDRESS are recognized as a configuration access by the PAC. All other I/O accesses to CONFIG_ADDRESS are treated as normal I/O transactions.

3.18.1. CONFIG_ADDRESS Register

CONFIG_ADDRESS is 32 bits wide and contains the field format shown in the following figure. Bits [23::16] choose a specific bus in the system. Bits [15::11] choose a specific device on the selected bus. Bits [10::8] choose a specific function in a multi-function device. Bits [7::2] select a specific register in the configuration space of the selected device or function on the bus.

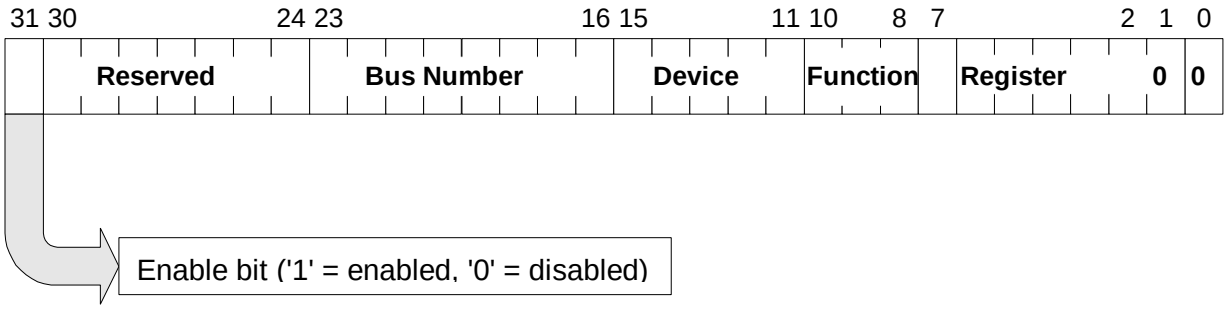


Figure 18 CONFIG_ADDRESS Register

3.18.2. Device Number and IDSEL Mapping

Each device under a PCI bridge has its IDSEL input connected to one bit out of the PCI bus address/data signals AD[31::11] for the PCI bus. Each IDSEL-mapped AD bit acts as a chip select for each device on PCI. The host bridge responds to a unique PCI device ID value, that along with the bus number, cause the assertion of IDSEL for a particular device during configuration cycles. The following table shows the correspondence between IDSEL values and PCI device numbers for the PCI bus. The lower 5-bits of the device number are used in CONFIG_ADDRESS bits [15::11].

Table 23 PCI Configuration IDs and Device Numbers

	PCI Bus	
IDSEL	**Device #**	**Device**
31	10100b	PIIX4
30	10011b	
29	10010b	CL-GD5480 video chip
28	10001b	
27	10000b	82558 NIC
26	01111b	PCI Slot 4
25	01110b	
24	01101b	
23	01100b	PCI Slot 3
22	01011b	Symbios 53C876
21	01010b	PCI Slot 2
20	01001b	PCI Slot 1
19	01000b	
18	00111b	
17	00110b	
16	00101b	
15	00100b	
14	00011b	
13	00010b	

IDSEL	Device #	Device
12	00001b	
11	00000b	Hardwired to host bridge

3.19. Error Handling

The N440BX Server is designed to report the following types of system errors: ISA bus, PCI bus, ECC memory, and System limit. Errors are reported using SMI_L. SMI is used for server management and advanced error processing. All errors can be intercepted by SMI for preprocessing (if SMI_L is enabled), or handled directly by NMI handlers. Some errors have to generate an NMI even if they are intercepted by the SMI, because the traditional way to handle errors in PC architecture is via the NMI. The N440BX emulates non-ISA errors as ISA-compatible using NMI and SMI_L.

Three error handlers are required: BIOS NMI handler, OS NMI handler, and SMI handler. The SMI has the highest priority to process the errors and is OS-transparent. The OS NMI handler can process all errors as well, even when the SMI is disabled. In this case, some errors are SMI resources that can be routed to the NMI. The BIOS NMI handler processes the ISA-compatible errors and disables the NMI only.

3.20. Hardware Initialization and Configuration

This section describes the following:

- System initialization
- Programming considerations for various portions of the I/O system

3.21. System Initialization Sequence

A Pentium II processor system based on the 82440BX PCIset is initialized and configured in the following manner.

System power is applied. The power-supply provides resets using the RST_PWR_GD_BB signal. PCI reset (RST_P_RST_L) is driven to tri-state the PCI bus in order to prevent PCI output buffers from short circuiting when the PCI power rails are not within the specified tolerances. The PAC asserts G_CPURST_L to reset the processor(s).

The PAC is initialized, with its internal registers set to default values.

Before G_CPURST_L is deasserted, the PAC asserts BREQ0_L. Processor(s) in the system determine which host bus agents they are, Agent 0 or Agent 1, according whether their BREQ0_L or BREQ1_L is asserted. This determines bus arbitration priority and order.

The processor(s) in the system determines which processor will be the BSP by issuing Bootstrap Inter-Processor Interrupts (BIPI) on the APIC data bus. The non-BSP processor becomes an application processor and idles, waiting for a Startup Inter-Processor Interrupt (SIPI).

The BSP begins by fetching the first instruction from the reset vector.

PAC registers are updated to reflect memory configuration. SDRAM is sized and initialized.

All PCI and ISA I/O subsystems are initialized and prepared for booting.

3.22. Server Management Programming Interface

DISMIC mailbox registers provide a mechanism for communications between IMB server management bus agents, and SMS or SMI handler code running on the server. DISMIC mailbox register space, physically located in the device, is mapped to BMC external data memory and ISA I/O space. This shared register space consists of three byte-wide registers:

- Flags Register - provides semaphores for use in various defined operations
- Control/Status Register - accepts commands and returns completion codes
- Data Register - provides a port for transactions that exchange data

In addition to the ports described above, the DISMIC contains a port 070h snoop register. See the section titled "Port 70h Snoop Register" below for further information.

SMS and SMI handler code interacts with the register interface using a variety of read and write commands encapsulated in messages. The origin of a message is specified during a particular transaction using Control Codes that are unique to the transaction, allowing the interface to allocate priority to various sources, and control SMI handler and SMS precedence (the SMI handler can always abort or temporarily interrupt any transaction).

3.22.1. Port 70h Snoop Register

The Port 70h Snoop Register reads back the state of bit 7 of I/O port 70h (RTC NMI enable bit) to the BMC. This register shadows any ISA write to port 70h. Due to architectural constraints in the DISMIC, the contents of this register cannot be made available for direct I/O read access at an alternate address location on the ISA bus. Access to the register's contents is provided only through the BMC using a command defined for this purpose.

3.23. PCI Interrupt to IRQ Routing Control

Embedded in a separate programmable logic device is logic for rerouting of PCI interrupts to ISA IRQs. Two I/O locations are reserved by the BIOS using the PIIX4 Programmable Chip Select Control register, for control of the PCI to IRQ re-router feature: CA4h and CA5h. Writes to the upper and lower nibble of each byte determine whether the interrupt is passed through to the I/O APIC, or rerouted to an ISA IRQ input on the PIIX4. The following figure shows the PCI interrupt line associated with each nibble. The following table defines the encoding of each nibble.

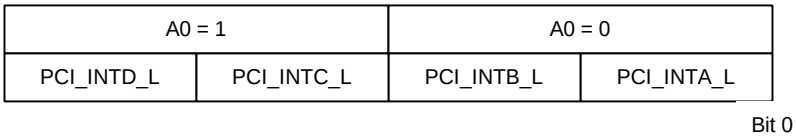


Figure 19 PCI to IRQ Rerouter Control Bytes

The following table reviews PCI to IRQ nibble encoding.

Table 24 PCI to IRQ Rerouter Nibble Encoding

Value	Meaning
0000b	Pass interrupt through to I/O APIC (default)
0001b	Reserved
0010b	Reserved
0011b	Reroute PCI_INTn_L to IRQ3
0100b	Reserved
0101b	Reroute PCI_INTn_L to IRQ5
0110b	Reserved
0111b	Reroute PCI_INTn_L to IRQ7
1000b	Reserved
1001b	Reroute PCI_INTn_L to IRQ9
1010b	Reroute PCI_INTn_L to IRQ10
1011b	Reroute PCI_INTn_L to IRQ11
1100b	Reserved
1101b	Reserved
1110b	Reserved
1111b	Reroute PCI_INTn_L to IRQ15

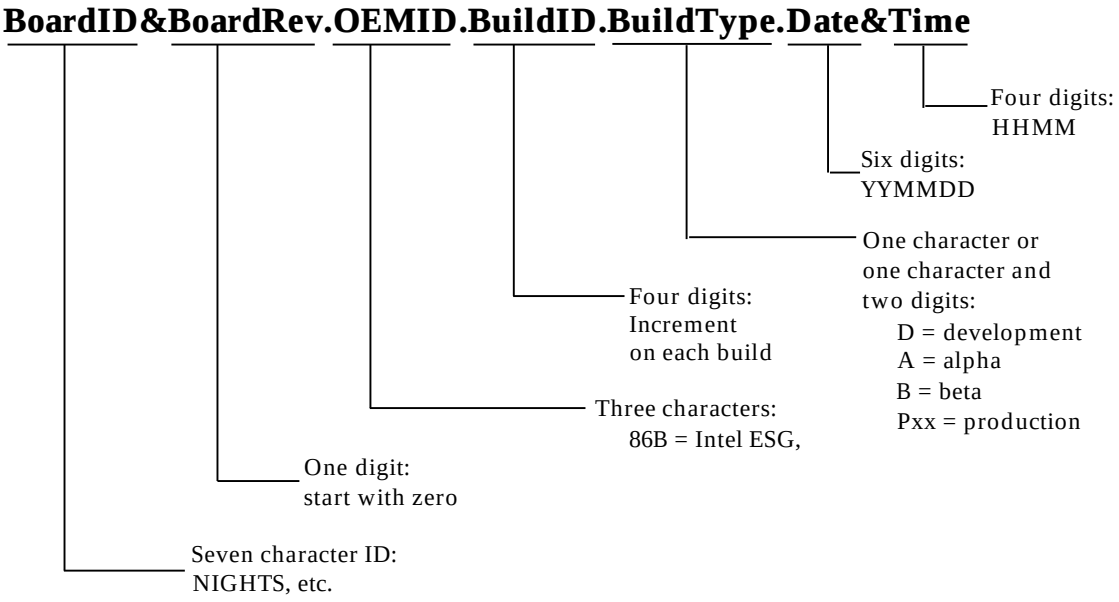
4. BIOS, Setup, SSU and SCSI Utility

4.1. This section is based on the R440LX and needs to be updated.

4.2. Revision History Format

The BIOS Revision Identification is used to track board, OEM, and build revision information for any given BIOS. This identifier can be a maximum of 32 characters. The first 28 characters have been defined using the following format:

The figure below illustrates a standard 32-byte BIOS ID.



5. Board Set Specifications

This chapter specifies the operational parameters and physical characteristics for the N440BX Server. This is a board-level specification only. System specifications are beyond the scope of this document.

5.1. Absolute Maximum Ratings

Operation of the N440BX Server at conditions beyond those shown in the following table may cause permanent damage to the system (provided for stress testing only). Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

Table 6-1. Absolute Maximum Ratings

Operating Temperature	0°C to +55°C *
Storage Temperature	-40°C to +70°C
Voltage on any signal with respect to ground	-0.3V to V_{DD} + 0.3V **
3.3V Supply Voltage with Respect to ground	-0.3 to +3.63V
5V Supply Voltage with Respect to ground	-0.3 to +5.5V

* Chassis design must provide proper airflow to avoid exceeding Pentium II maximum case temperature.
** V_{DD} means supply voltage for the device.

Further topics in this chapter specify normal operating conditions for N440BX Server.

5.2. Electrical Specifications

DC specifications for N440BX Server power connectors and module power budgets, are summarized here. Electrical characteristics for major connector interfaces (including DC and AC specifications), can be obtained from other documents:

- PCI Connectors -- PCI Local Bus Specification Rev. 2.1
- ISA slots -- EISA Bus Specification

5.3. Power Connection

Main power supply connection is obtained using either the 20-pin ATX-style connector or the 24-pin Columbus II-style connector. A third connector is provided for power supply control in the Columbus II chassis. The following tables define the pin outs and wire gauge/color for each of these connectors.

Table 6-2. 20-pin ATX-style Main Power Connector Pin out

Pin	Signal	18 AWG Color	Pin	Signal	18 AWG Color
1	+3.3 VDC	Orange	11	+3.3 VDC 3.3 V sense	Orange Brown
2	+3.3 VDC	Orange	12	-12 VDC	Blue
3	COM	Black	13	COM	Black
4	+5 VDC	Red	14	PS-ON*	Green
5	COM	Black	15	COM	Black
6	+5 VDC	Red	16	COM	Black
7	COM	Black	17	COM	Black
8	PWR-OK	Gray	18	-5 VDC	White
9	5 V Standby	Purple	19	+5 VDC	Red
10	+12 VDC	Yellow	20	+5 VDC	Red

Warning: Do not attempt to plug the ATX 20-pin connector into the 24-pin Columbus II chassis-style connector. Damage to the baseboard will occur.

Table 6-3. 24-pin Columbus II chassis-style Power Connector Pin out

Pin	Signal	18 AWG Color	Pin	Signal	18 AWG Color
1	+5 VDC	Red	7	COM	Black
13	+5 VDC	Red	19	COM	Black
2	+5 VDC	Red	8	COM	Black
14	+5 VDC	Red	20	COM	Black
3	-5 VDC	White	9	COM	Black
15	+5 VDC	Red	21	COM	Black
4	-12 VDC	Blue	10	+3.3 VDC	Orange
16	+5 VDC	Red	22	+3.3 VDC	Orange
5	COM	Black	11	+12V	Yellow
17	COM	Black	23	+3.3 VDC	Orange
6	COM	Black	12	+12 VDC	Yellow
18	COM	Black	24	+12 VDC	Yellow

Table 6-4. 14-pin Auxiliary Power Connector Pin out

Pin	Signal	24 AWG Color	Pin	Signal	24 AWG Color
1	5V Remote Sense Return	Black	8	Power Good	Gray
2	5V Remote Sense	Red	9	PS on	Green
3	3.3V Remote Sense	Orange	10	COM	Black
4	3.3V Remote Sense Return	Black	11	5V Standby	Purple
5	N/C	None	12	KEY	-
6	N/C	None	13	N/C	None
7	COM	Black	14	COM	Black

5.4. Power Consumption

The following table shows the power consumed on each supply line for a N440BX Server baseboard with 2 processors, 4 DIMMs, 4 PCI slot loads (2A @ 5V per slot), and 1 ISA slot load (Server Monitor Module board).

NOTE:

The following numbers are provided as an example. Actual power consumption will vary depending on the exact N440BX Server configuration. Refer to the appropriate system chassis document for more information.

Table 6-5. Power Consumption

Device(s)	3.3V	+5V	+12V	-12V	5V Standby	
Processors	3.04A	8.17A	3.41A			
Memory DIMMs	3.58A					
GTL Termination	2.91A					
NBX	1.20A					
Baseboard	.32A	2.56A	.2A	.15A	.08A	
Fans			1.0A			
Keyboard/Mouse		.5A				
PCI slots		8A				
ISA slot		.1A	1.0A			
Total Current	**11.05 A**	**19.33 A**	**5.61**	**.15A**	**.08A**	**Total**
Total Power	**36.47 W**	**96.65 W**	**67.32W**	**1.8W**	**.4W**	**202.74W**

5.5. Power Supply Specifications

This section provides power supply design guidelines for a N440BX Server-based system, including voltage and current specifications, and power supply on/off sequencing characteristics.

Table 6-6. Power Supply Voltage Specification

Item	Min	Nom	Max	Units	Tolerance
VOLTAGE TOLERANCE:					
3.3 Volts	3.14	3.30	3.46	V	+5%
5 Volts	4.80	5.00	5.25	V	+5%
+12 Volts	11.40	12.00	12.60	V	+5%
-12 Volts	-11.40	-12.00	-12.60	V	+5%
-5 Volts	-4.75	-5.00	-5.25	V	+5%
5 Volts Standby	+4.75	+5.00	+5.25	V	+5%

Table 6-7. Transient and Remote Sense/Sink Currents

Item	Min	Nom	Max	Units
TRANSIENT CURRENTS:				
Max dI/dt:				
5 Volts			0.5	A/µs
3.3 Volts			TBD	A/µs
+12 Volts			TBD	A/µs
-12 Volts			0.3	A/µs
-5 Volts			0.3	A/µs
5 Volts Standby			0.5	A/µs
Amplitude:				
5 Volts			7.0	A
3.3 Volts			0.5	A
+12 Volts			3.0	A
-12 Volts			0.5	A
-5 Volts			0.5	A
5 Volts Standby			0.01	A
REMOTE SENSE:				
Fuse Rating:		N/A		A
Sense Trace Resistance:			0.05	Ω
SINK CURRENT (While Voltage Form Off):				
Off Voltage:				
Item	**Min**	**Nom**	**Max**	**Units**
5 Volts			0.2	V
3.3 Volts			0.1	V
+12 Volts			0.1	V
-12 Volts			0.1	V
-5 Volts			0.1	V

Table 6-8. Ramp Rate/ Ramp Shape/ Sequencing/ Power Good & Power On Signals

Item	Min	Nom	Max	Units	Comments

Ramp Rate(On):					
5 Volts	5		70	ms	From 10% to within regulation
3.3 Volts	5		70	ms	From 10% to within regulation
+12 Volts	5		70	ms	From 10% to within regulation
-12 Volts	5		70	ms	From 10% to within regulation
-5 Volts	5		70*	ms	From 10% to within regulation
5 Volts Standby	5		70	ms	From 10% to within regulation
Ramp "Shape"(On & Off):					Monotonic
Sequencing: **(with respect to 5 Volts)**					See Figure 6-1
3.3 Volts					
+12 Volts					
-12 Volts					
-5 Volts					
5 Volts Standby					
Power Good Signal					See Figure 6-2
Vil			0.4	V	
Vih	3.5			V	
Iil	4.0			mA	
Iih			0.2	mA	
Timing requirements				TBD	
Power On Signal				TBD	
Vol			0.4	V	
Voh	3.5			V	
Iol	4.0			mA	
Ioh			0.2	mA	
Timing requirements				TBD	
etc.					

* -5V must not ramp up before +12V

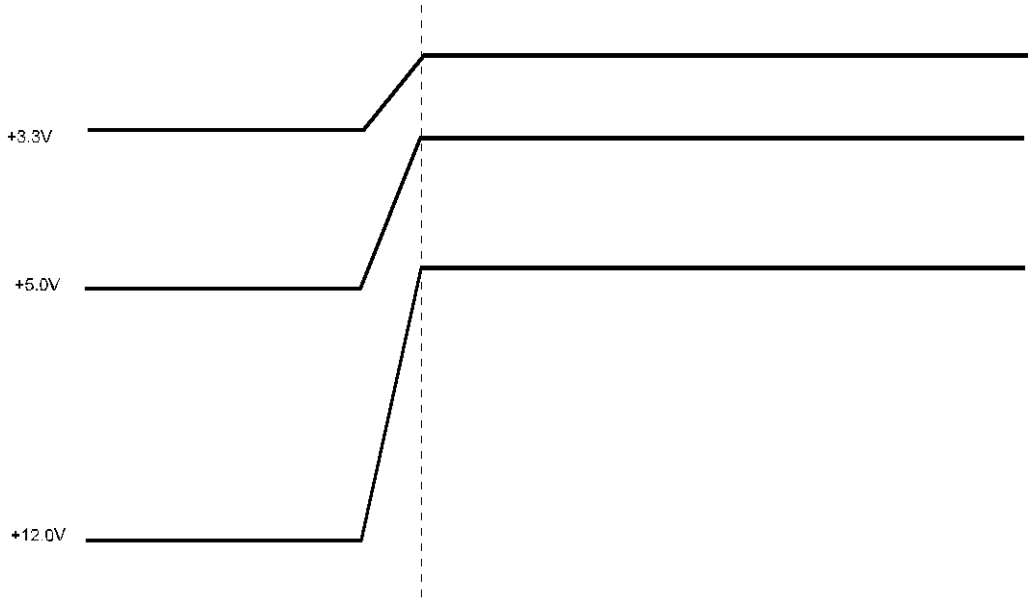
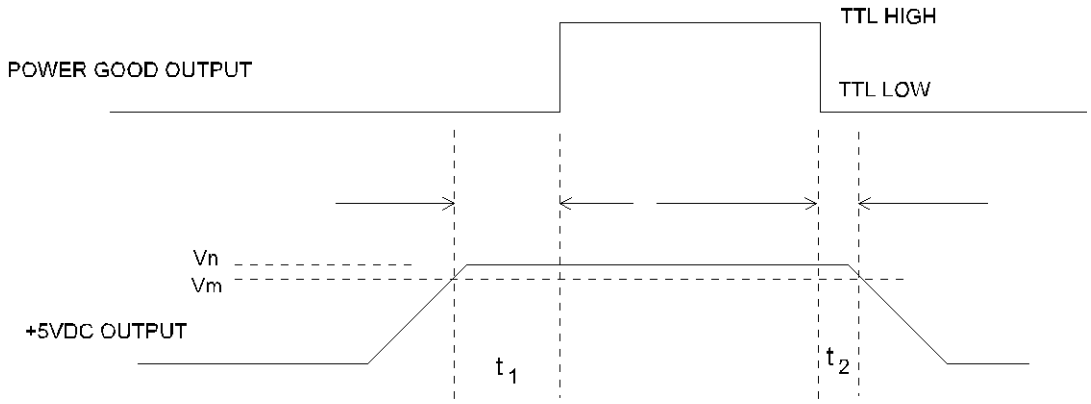


Figure 6-1. DC Voltage Sequencing



Vn: Nominal Output Voltage +5Vdc
Vm: Minimum Output Voltage +4.75Vdc
t1: Power Good turn on Delay (100-1500mSec)
t2: Power Good turn off time (1mSec minimum)

Figure 6-2. Power Good Signal Characteristics