N440BX Purpose-Built Server

Critical Parameters for SDRAM DIMM Qualification

Revision 1.0
April, 1998

Revision History

Revision	Revision History	Date
0.5	Preliminary release	3/3/98
0.8	Grammatical corrections	3/24/98
1.0	Incorporated further grammatical corrections	4/8/98

Table of Contents

1. Introduction

The information provided in this document is intended as a quick reference guide to identify and define critical areas pertinent to memory architecture of Intel's N440BX server product line and is provided as a convenience to our customers only. ***The information is provided as a guide only and is subject to change as memory vendor requirements and policies change. This information is provided as is and Intel assumes no responsibility for the accuracy of the data in this paper and does not commit to update this information. Users of this information should satisfy themselves as to the applicability and accuracy of the information provided herein prior to acting upon such information. Intel assumes no responsibility for the accuracy of the data in this paper.***

Everything you need to build high-performance, Intel Pentium® II processor-based servers

The Intel N440BX server board, the latest in Pentium® II technology and the Intel 82440BX PCIset are key ingredients you need to build robust servers. Designed for dual processing using the latest high-performance Intel Pentium® II processors with 100MHz System Bus, the N440BX server board is the foundation for creating purpose-built servers designed for the most demanding business environments. It comes with everything you need to quickly build your servers and install at your customers fast: drivers, documentation, management software, diagnostics, and tremendous flexibility and genuine Intel quality.

Product Highlights … relating to memory

- High-performance Server board for the Intel Pentium® II processor… speeds from 266/66 to 400/100 MHz.
- Fully supports Intel 82440BX PCIset and the PC SDRAM specification for Unbuffered SPD parts.
- Enabled CMTL to perform BASIC and ADVANCED testing parameters.
- CTML fully tests for compatibility, stress, mechanical fit, thermal, shock and other server-critical parameters.
- Genuine Intel quality, reliability, and support built into the purpose-built server.

The objective of this document is to identify and define critical areas in the new Synchronous DRAM specification (“PC SDRAM”), so a “fully compatible” device among all vendor designed parts is available for the N440BX Server board. The PC SDRAM specification removes extra functionality from the current JEDEC standard SDRAM specification. Intel Corporation has assisted the memory vendors and integrator so it is easy to design and manufacture a highly competitive DIMM. Intel Corporation wished to insure a DIMM is available for the main stream volume server boards which take the newer Pentium® II technology.

Synchronous DRAM AC/DC Parameters as Required by Intel

DC Specifications

Absolute Maximum D.C. Rating

Symbol	Parameter	Min	Max	Units	Notes
Vin, Vout	Voltage on any pin w.r.t V_{SS}	-0.5	V_{DD} + 0.5	V	
V_{DD}, V_{DDQ}	Voltage Supply pins pin w.r.t V_{SS}	-0.5	4.5	V	
Ts	Storage Temperature	-55	125	°C	

D.C Operating Requirements

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{DD}	Supply Voltage		3.0	3.6	V	
V_{DDQ}	I/O Supply Voltage		3. 0	3.6	V	
I_{il}	Input Leakage Current	$0 < V_{in} < V_{DDQ}$	-10	+10	µA	1,2
Icclp	Icc Low Power	CKE low, all banks closed	0	2	ma	
Iccslfrf	Icc Self Refresh Current		0	400/500ua	ua	16M/ 64M
Iccac	Icc active	All banks open, ping-pong reads,BL=4		140/165	ma	16M/ 64M 3
V_{oh}	Output High Voltage (For full I/V relationships see IBIS Section)	I_{oh} = -4 mA	2.4		V	
V_{ol}	Output Low Voltage (For full I/V relationships see IBIS Section)	I_{ol} = 4 mA		0.4	V	
C_{in}	Input Pin Capacitance	@1Mhz	2.5	5.0	pF	Target 3.75pf
$C_{I/O}$	I/O Pin Capacitance	@1Mhz	4.0	6.5	pF	Target 5.25pf
C_{clk}	Pin Capacitance	@1Mhz	2.5	4.0	pF	Target 3.25pf
L_{pin}	Pin Inductance			10	nH	2
Ta	Ambient Temperature	No Airflow	0	65	°C	

Notes:

1 Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs.
2 This is a recommendation, not an absolute requirement. The actual value should be provided with the component data sheet.
3 No Activate or Precharge currents should be included in the Iccac value.

A.C. Specifications

Maximum AC Operating Requirements

Symbol	Parameter	Min	Max	Units	Notes
V_{ih}	Input High Voltage	2.0	V_{DDQ}+2.0	V	1,2
V_{il}	Input Low Voltage	V_{SSQ} – 2.0	0.8	V	1,2

Notes:

1 The overshoot and undershoot voltage duration is <=3ns with no input clamp diodes
2 The VDDQ and VSSQ are the operating parameters (not absolute max. parameters)

Refresh Rate

The refresh rate for all devices is assumed at a maximum of 15.6us per row per the table below.

Symbol	Parameter	Min	Max	Units	Notes
Tref	Refresh rate / row	15.6		usec	1

Notes:

1 The overall array refresh is determined by multiplying the specified row refresh rate by the number of rows in the total array.

Characteristics for Input and Output Buffers

SDRAM DQ Buffer Output Drive Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
t_{rh}	Output Rise Time	measure in linear region: 1.2v - 1.8v	2.8	3.9	5.6	Volts / nS	1, 2, 3
t_{fh}	Output Fall Time	measure in linear region: 1.2v - 1.8v	2.0	2.9	5.0	Volts / nS	1, 2, 3
$I_{ol(AC)}$	Switching Current Low	Vout = 1.65 V	75.4		---	mA	
	(Test Point)	Vout = 1.65 V	---		202.5	mA	
$I_{oh(AC)}$	Switching Current High	Vout = 1.65 V	-73.0		---	mA	
	(Test Point)	Vout =1.65 V	---		-248.0	mA	

Notes:

1. Output rise and fall time must be guaranteed across VDD, process and temperature range.
2. Rise time specification based on 0 pF plus 50 Ohms to VSS.
3. Fall time specification based on 0 pF plus 50 Ohms to VDD.
4. Minimum VDD and VSS clamp described below.
5. All measurements done with respect to VSS.

A.C. Timing Parameters

100/66Mhz AC Timing Parameters For C_L=2 and 3

Parameter	Symbol	Speed Grade 66Mhz		Speed Grade[1] 100Mhz		Unit	Notes Ta 0-65C, Vcc 3.0v - 3.6v
		Min	***Max***	***Min***	***Max***		
Clock Period	***Tclk***						
		15		***10***		ns	
Clock High Time	Tch	***5***		***3***		ns	Rated @1.5V
Clock Low Time	Tcl	***5***		***3***		ns	
Input Setup Times	***Tsi***					ns	
DQM#/CS#		***3***		***2***		ns	
Other		***3***		***2***		ns	
Input Hold Times	***Thi***					ns	
DQM#/CS#		***1.5***		***1***		ns	
Other		***1.5***		***1***		ns	
Output Valid From Clock	***Tac***					ns	
CAS Latency = 2			***10.0***		***7.0***	ns	limited application, 2 banks *all outputs switching*
CAS Latency = 2			***9.0***		***6.0***	ns	LVTTL levels, Rated @ 50 pf *all outputs switching* *5.2ns @ 0pf*

CAS Latency = 3			***9.0***		***6.0***	ns	LVTTL levels, Rated@50pf *all outputs switching* *5.2ns @ 0pf*
Output Hold From Clock	Toh	***3***		***3***		ns	3ns @ 50pf Need 1.8ns @ 0pf
CAS to CAS Delay	tccd	***1***		***1***		Tclk	
CAS Bank Delay	Tcbd	***1***		***1***		Tclk	
CKE to Clock Disable	Tcke	***1***		***1***		Tclk	
RAS Precharge Time	Trp	***3/2***		***3/2***		Tclk	Trp=2 a SPD Option for 100Mhz
RAS Active Time	Tras	***5***		***5***		Tclk	
Activate to Command Delay (RAS to CAS Delay)	Trcd	***2***		***3/2***		Tclk	Trcd =2 a SPD Option for 100Mhz
RAS to RAS Bank Activate Delay	Trrd	***2***		***2***		Tclk	
RAS Cycle Time	Trc	***8***		***8/7***		Tclk	7 clks for trp=2
DQM to Input Data Delay	Tdqd	***0***		***0***		Tclk	
Write Cmd. to Input Data Delay	Tdwd	***0***		***0***		Tclk	
Mode Register set to Active delay	Tmrd	***3***		***3***		Tclk	
Precharge to O/P in High-Z	Troh	****CL***		****CL***		Tclk	
DQM to Data in HiZ for read	Tdqz	***2***		***2***		Tclk	
DQM to Data mask for write	Tdqm	***0***		***0***		Tclk	Data Masked on the same clock
Data-in to PRE Command Period	Tdpl	***2***		***2***		Tclk	
Data-in to ACT (PRE) Command period (Auto precharge)	Tdal	***5***		***5***		Tclk	
Power Down Mode Entry	Tsb		***1***		***1***	Tclk	
Self Refresh Exit Time	Tsrx	***10***		***1***		Tclk	10ns for 66Mhz
Power Down Exit Set up Time	Tpde	***1***		***1***		Tclk	Timing is asynchronous. If Tset is not met by rising edge of CLK then CKE is assumed latched on next cycle.
Clock Stop During Self Refresh or Power Down	Tclkstp	***200***		***200***		Tclk	If the clock is stopped during self refresh or powerdown, 200 clocks are required before CKE is high

******CL* **= CAS Latency**

Device Options

Via SPD control on a memory module, Intel's 82440BX PCIset can be programmed to effectively use either CL2 or CL3 devices and different values of Trcd and Trp. The N440BX Server board stores this information in the SDRAM Control Register (76h-77h). Below is a matrix for 66Mhz devices and the target for 100Mhz devices.

	CL	Trcd	Trp
66Mhz	3 clks	3 clks	3 clks
	2 clks	2 clks	3 clks
	2 clks	2 clks	2 clks
100Mhz	3 clks	3 clks	3 clks
	3 clks	2 clks	2clks
	3 clks	3 clks	2clks
	3 clks	2 clks	3 clks
	2 clks	3 clks	3 clks
	2 clks	3 clks	2 clks
	2 clks	2 clks	3 clks
	2 clks	2 clks	2 clks

The Power of Pentium®II Processor Inside

Building servers around the Intel Pentium® II processor gives you the strongest competitive position you can have. The new Pentium® II processor running at 350, 400 and 450 MHz is the fastest processor on the market today. Our 100 MHz System Bus provides even greater throughput on memory and L2 cache access. The N440BX lets you configure servers with one or two Pentium® II processors, for greater flexibility and expandability.

Genuine Intel Quality and Reliability

The Intel N440BX carries Intel’s promise of exceptional quality, which is your assurance of exceptional reliability and availability. Servers based on Intel server boards are running mission critical applications, databases, and 7 x 24 websites for businesses of all sizes. Downtime is not an option in most businesses — and not a danger with genuine Intel server boards. Support is just a phone call or Web site visit away.

Features	**Benefits**
Supports dual Intel Pentium® II processors at 350 MHz and beyond with 512 Kbytes of L2 cache	Build entry-level servers with plenty of headroom for growth
100 MHz System Bus speed	Higher system bandwidth, highest performance on the market today
Advanced Intel 82440BX chip set	Support for the latest Intel Pentium® II processors, memory, and drive technologies
Advanced Emergency Management Port	Remote management lowers cost of

(EMP)	ownership
Integrated dual-channel SCSI, LAN, and graphics (with 2 Mbytes SGRAM)	Validated and tested SCSI, LAN, and graphics support saves integration time and money.
DIMM sockets support 1 Gbyte SDRAM ECC memory	Greater memory expandability and reliability
Five full-length slots: 3 PCI, 1 ISA, 1 shared PCI/ISA	On-board integration yields more available slots for greater configuration flexibility
Intel LANDesk® Server Manager software	Built-in server management features for lower cost of ownership.
Modified server AT form factor	Easy, low-cost integration into ATX compatible chassis

Visit the N440BX server board support Web site at:

http://support.intel.com/support/motherboards/server/n440bx

View the PC SDRAM specifications at:

http://www.intel.com/design/pcisets/memory/