Intel® Server Platform SR870BN4

Specification Update

Revision 15.0

February 2007

Enterprise Platforms and Services Division Marketing

Revision History

Date	Revision	Modifications
August 2003	1.0	Initial release.
October 2003	2.0	Revised erratum 13. Added errata 22-23.
December 2003	3.0	Added Documentation Change 2,
January 2004	4.0	Added Product Scope TA# A96556-009 in SBNMB000, TA# C27422-007 in SBNMB000X, and TA# A96472-002 in Chassis
February 2004	5.0	Added errata 24, added Documentation Changes 3-4
March 2004	6.0	Added errata 25
April 2004	7.0	Added errata 26
July 2004	8.0	Added errata 27 and 28, Updated errata 22, 23, 25, and 26.
November 2004	9.0	Added Documentation Change 5
May 2005	10.0	Updated product scope table, erratum 28.
August 2005	11.0	Updated product scope table, added Errata 29
September 2005	12.0	Added Errata 30
November 2006	13.0	Added Erratum 31, RoHS PN updates
December 2006	14.0	Added Errata 32
February 2007	15.0	Revised Errata 32 to include a workaround

Disclaimers

The SR870BN4 Server System may contain design defects or errors known as errata that may cause the product to deviate from the published specifications. Current characterized errata are documented in this Specification Update.

Information in this document is provided in connection with Intel products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Intel's Terms and Conditions of Sale for such products, Intel assumes no liability whatsoever, and Intel disclaims any express or implied warranty, relating to sale and/or use of Intel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. Intel products are not intended for use in medical, life saving, or life sustaining applications. Intel may make changes to specifications and product descriptions at any time, without notice.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Intel, Itanium, Pentium, and Xeon are trademarks or registered trademarks of Intel Corporation.

*Other brands and names may be claimed as the property of others.

Contents

Preface

This document is an update to the specifications contained in the *SR870BN4 Boardset and System Technical Product Specifications*. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain specification changes, specification clarifications, errata, and document changes.

Refer to the *Intel® Itanium™ 2 Processor Specification Update* for specification updates concerning the Itanium™ 2 processor. Items contained in the *Intel® Itanium™ 2 Processor Specification Update* that either do not apply to the SR870BN4 or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the Printed Board Assembly (PBA) revisions(s) associated with that stepping.

Nomenclature

- **Specification Changes** are modifications to the current published specifications for Intel® server boards. These changes will be incorporated in the next release of the specifications.
- **Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.
- **Documentation Changes** include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.
- **Errata** are design defects or errors. Errata may cause the server board behavior to deviate from published specifications. Hardware and software designed to be used with any given processor stepping must assume that all errata documented for that processor stepping are present on all devices.

Product Scope

Below are the specific boards, BIOS and components covered by this update. The information in the table shows BIOS and firmware revisions associated with the PBA and TA numbers as they were shipped from the factory. Updated revisions of the BIOS and firmware may be available on IBL and not currently implemented in the factory.

SBNMB000 System			
TA #	**BIOS**	**Firmware**	**Change Description**
A96556-002	P01, Build 720	BMC 11 HSC 03B SDR 10	Gold Release
A96556-003	P03, Build 760	BMC 14 HSC 03B SDR 14	Production Release
A96556-004	P04, Build 831	BMC 16 HSC 03B SDR 14	Update to BIOS and BMC, P64H2 B1 stepping, SCSI backplane PLD code update.
A96556-005	P06, Build 882	BMC 20 HSC 03B SDR 16	Update to BIOS and BMC, Processor board to Rev -307, SCSI backplane to Rev -310, I/O Riser to Rev-420, Resource CD version -005, safety and packaging label modified to comply with China certification requirements.
A96556-006	P01, Build 897	BMC 20 HSC 03B SDR 16	Update BIOS to support Itanium® 2 processors with up to 6MB L3 Cache, add -005 chassis as alternate.
A96556-007	P01, Build 897	BMC 20 HSC 03B SDR 16	Update Processor board to Rev -320, I/O Baseboard to Rev -540, I/O Riser to Rev -500, Resource CD version -006. Add ISM 6.1 CD, bezel badge.
A96556-008	P01, Build 897	BMC 20 HSC 03B SDR 16	Update to -501 I/O Riser
A96556-009	P01, Build 897	BMC 20 HSC 03B SDR 16	PCI slot rocker switch changes from a 1-piece to a more robust 2-piece design; Top cover latches are adjusted to reduce the possibility of damaging the latches
A96556-010	P01, Build 897	BMC 20 HSC 03B SDR 16	Change to chassis revision A18841-015, power distribution board to A22017-302
A96556-011	P01, Build 897	BMC 20 HSC 03B SDR 16	Removal of LS-240 drive, change I/O board to A52336-550.
A96556-012	P01, Build 897	BMC 20 HSC 03B SDR 16	Change to -552 I/O Board.

A96556-013	PR4.1, Build 925	BMC 30 HSC 12 SDR 19	Change to -500 memory board. Change to BIOS PR4.1, BMC 30, HSC 12, and SDR 19. Updated Resource CD and ISM CD.
A96556-014	PR4.1, Build 925	BMC 30 HSC 12 SDR 19	Power supply with additional safety label
A96556-015	PR4.1, Build 925	BMC 30 HSC 12 SDR 19	Removed Hot-plug PCI attention switches
A96556-016	PR2.1, Build 936	BMC 32 HSC 14 SDR 19	Updated BIOS to version that supports Itanium® 2 Processor with up to 9MB L3 Cache, updated Firmware, DVD-ROM replaced with CD-RW/DVD-ROM combo drive.
A96556-017	PR2.1, Build 936	BMC 32 HSC 14 SDR 19	Modified power supply to allow the fans to run while in standby.
A96556-018	PR2.1, Build 936	BMC 32 HSC 14 SDR 19	Modified power supply to allow the fans to run slowly while in standby.
A96556-019	PR2.1, Build 936	BMC 32 HSC 14 SDR 19	Changed to a non-brominated material for the IO rug, long PCI divider, and short PCI divider. .
A96556-020	PR2.1, Build 936	BMC 32 HSC 14 SDR 19	Added WEEE mark to safety label .
D48100-001	PR2.4 Build 976	BMC 35 HSC 15 SDR 21	RoHS compliant version. Updated BIOS/FW to support transition to Itanium® 2 Processor 9000 Series

SBNMB000X System			
TA #	**BIOS**	**Firmware**	**Change Description**
C27422-002	P04, Build 831	BMC 16 HSC 03B SDR 14	Production Release
C27422-003	P06, Build 882	BMC 20 HSC 03B SDR 16	Update to BIOS and BMC, Processor board to Rev -307, SCSI backplane to Rev -310, I/O Riser to Rev-420, Resource CD version -005, safety and packaging label modified to comply with China certification requirements.
C27422-004	P01, Build 897	BMC 20 HSC 03B SDR 16	Update BIOS to support Itanium® 2 processors with up to 6MB L3 cache, add -005 chassis as alternate.
C27422-005	P01, Build 897	BMC 20 HSC 03B SDR 16	Update Processor board to Rev -320, I/O Baseboard to Rev -540, I/O Riser to Rev -500, Resource CD version -006. Add ISM 6.1 CD, bezel badge.
C27422-006	P01, Build 897	BMC 20 HSC 03B SDR 16	Update to -501 I/O Riser

C27422-007	P01, Build 897	BMC 20 HSC 03B SDR 16	PCI slot rocker switch changes from a 1-piece to a more robust 2-piece design; Top cover latches are adjusted to reduce the possibility of damaging the latches
C27422-008	P01, Build 897	BMC 20 HSC 03B SDR 16	Change to chassis revision A18841-015, power distribution board to A22017-302
C27422-009	P01, Build 897	BMC 20 HSC 03B SDR 16	Removal of LS-240 drive, change I/O board to A52336-550.
C27422-010	P01, Build 897	BMC 20 HSC 03B SDR 16	Change to -552 I/O Board
C27422-011	PR4.1, Build 925	BMC 30 HSC 12 SDR 19	Change to -500 memory board. Change to BIOS PR4.1, BMC 30, HSC 12, and SDR 19. Updated Resource CD and ISM CD.
C27422-012	PR4.1, Build 925	BMC 30 HSC 12 SDR 19	Power supply with additional safety label
C27422-013	PR4.1, Build 925	BMC 30 HSC 12 SDR 19	Removed Hot-plug PCI attention switches
C27422-014	PR2.1, Build 936	BMC 32 HSC 14 SDR 19	Updated BIOS to version that supports Itanium® 2 Processor with up to 9MB L3 Cache, updated Firmware, DVD-ROM replaced with CD-RW/DVD-ROM combo drive.
C27422-015	PR2.1, Build 936	BMC 32 HSC 14 SDR 19	Modified power supply to allow the fans to run while in standby.
C27422-016	PR2.1, Build 936	BMC 32 HSC 14 SDR 19	Modified power supply to allow the fans to run slowly while in standby.
C27422-017	PR2.1, Build 936	BMC 32 HSC 14 SDR 19	Changed to a non-brominated material for the IO rug, long PCI divider, and short PCI divider. .
C27422-018	PR2.1, Build 936	BMC 32 HSC 14 SDR 19	Added WEEE mark to safety label. .
C27422-019	PR2.1, Build 936	BMC 32 HSC 14 SDR 19	Updated with new combo DVD drive
D48233-001	PR2.4, Build 976	BMC 35 HSC 15 SDR 21	RoHS compliant version. Updated BIOS/FW to support transition to Itanium® 2 Processor 9000 Series

BBACPUBOARD Processor Board

Baseboard PBA #	BIOS	Firmware	Change Description
A55955-304	Beta 2, Build 674	N/A	Initial Release
A55955-305	Beta 2, Build 674	N/A	Capacitor change to slow inrush current of 12V rail
A55955-306	P04, Build 831	N/A	BIOS update
A55955-307	P06, Build 882	N/A	BIOS update
A55955-310	P06, Build 882	N/A	SNC-M C1 stepping
A55955-320	P01, Build 897	N/A	BIOS update, resistor changes to correct AC boot cycling issue
A55955-321	PR4.1, Build 925	N/A	Change to BIOS PR4.1
A55955-322	PR2.1, Build 936	N/A	Change to BIOS PR2.1, which supports Itanium® 2 Processor with up to 9MB L3 Cache
A55955-350	PR2.4, Build 976	N/A	RoHS compliant version. Updated BIOS/FW to support transition to Itanium® 2 Processor 9000 Series

BBADDRMEM1GB Memory Board			
Baseboard PBA #	**BIOS**	**Firmware**	**Change Description**
A14986-403	N/A	N/A	Initial Release
A14986-500	N/A	N/A	Corrected routing to support 1Gbit based DIMMs
A14986-550	N/A	N/A	RoHS compliant version.

BBAMIDPLANE Midplane Board			
Baseboard PBA #	**BIOS**	**Firmware**	**Change Description**
A28311-300	N/A	N/A	Initial Release
A28311-350	N/A	N/A	RoHS compliant version.

BBAIOBOARD I/O Board			
Baseboard PBA #	**BIOS**	**Firmware**	**Change Description**
A52336-527	N/A	N/A	Initial Release
A52336-529	N/A	N/A	SIOH stepping change
A52336-530	N/A	N/A	P64H2 stepping change

A52336-540	N/A	N/A	Change capacitor to reduce battery current, new version of U4J1 clock chip, corrected issue on I2C bus which caused systems to intermittently fail to power up after an AC power cycle at high temperature, remove JTAG support from PCI slot 4, remove debug LEDs related circuitry
A52336-550	N/A	N/A	Change SIOH from C1 to C2 stepping.
A52336-551	N/A	N/A	Replace jumper block J5H1 and related jumpers with zero ohm resistors.
A52336-552	N/A	N/A	Fix for SR870BN4 erratum #26
A52336-570	N/A	N/A	RoHS compliant version

BBARFRECH4 I/O Riser Board			
Baseboard PBA #	**BIOS**	**Firmware**	**Change Description**
A72649-413	Beta 2, Build 674	BMC 10	Initial Release
A72649-414	Beta 2, Build 674	BMC 10	Update LAN EEPROM, remove boot block jumper
A72649-415	P04, Build 831	BMC 16	BIOS and BMC update
A72649-420	P06, Build 882	BMC 20	BIOS and BMC update, ICH B0 stepping, rework fix to 5V standby circuit
A72649-500	P01, Build 897	BMC 20	Integration of fix to 5V standby circuit, new battery and battery holder, conditioning of power to USB devices during power up, BIOS update.
A72649-501	P01, Build 897	BMC 20	PLD change
A72649-502	PR4.1, Build 925	BMC 30	Change to BIOS PR4.1, BMC 30, and SDR 19.
A72649-503	PR2.1, Build 936	BMC 32	Change to BIOS PR2.1, which supports Itanium® 2 Processor with up to 9MB L3 Cache, BMC 32.
A72649-550	PR2.4, Build 976	BMC 35	RoHS compliant version. Updated BIOS/FW to support transition to Itanium® 2 Processor 9000 Series

BBASCSIHSBP SCSI Backplane			
Baseboard PBA #	**BIOS**	**Firmware**	**Change Description**
A73789-301	N/A	N/A	Initial Release
A73789-302	N/A	N/A	Update PLD code to resolve power ramp issue.
A73789-310	N/A	N/A	New version of GEM359 Enclosure Management Controller
A73789-311	N/A	N/A	Change to HSC 12
A73789-312	N/A	N/A	Change to HSC 14
A73789-350	N/A	N/A	RoHS compliant version

BBAPDB Power Distribution Board			
Baseboard PBA #	**BIOS**	**Firmware**	**Change Description**
A22017-301	N/A	N/A	Initial Release
A22017-302	N/A	N/A	Add jumper to J1, pins 1-2
A22017-350	N/A	N/A	RoHS compliant version

BBAFPNL Front Panel Board			
Baseboard PBA #	**BIOS**	**Firmware**	**Change Description**
A24009-301	N/A	N/A	Initial Release
A24009-350	N/A	N/A	RoHS compliant version

BBAHPIBBOARD Hot Plug Indicator Board			
Baseboard PBA #	**BIOS**	**Firmware**	**Change Description**
A24011-405	N/A	N/A	Initial Release
A24011-410	N/A	N/A	Removed Attention Switches
A24011-450	N/A	N/A	RoHS compliant version

Chassis			
Part Number	**BIOS**	**Firmware**	**Change Description**
A18841-012	N/A	N/A	Initial Release
A18841-014	N/A	N/A	PCI slot rocker switch changes from a 1-piece to a more robust 2-piece design; Top cover latches are adjusted to reduce the possibility of damaging the latches
A18841-015	N/A	N/A	Increase size of cutouts on front flanges, add PEM nuts to the back of I/O bay module to support cable management arm bracket
A18841-016	N/A	N/A	Removed access holes for PCI Hot-Plug Attention Switches
A18841-017	N/A	N/A	RoHS compliant version

Processor/Memory Module			
Part Number	**BIOS**	**Firmware**	**Change Description**
A47021-009	N/A	N/A	Initial Release
A47021-010	N/A	N/A	Change to non-brominated material
A47021-011	N/A	N/A	RoHS compliant version

Summary Tables of Changes

The following tables indicate the errata and the document changes that apply to the Intel® Server Platform SR870BN4. Intel intends to fix some of the errata in a future stepping of components, and to account for the other outstanding issues through documentation or specification changes as noted. The tables use the following notations:

Doc: Intel intends to update the appropriate documentation in a future revision.

Fix: Intel intends to fix this erratum in a future release of the component.

Fixed: This erratum has been previously fixed.

NoFix: There are no plans to fix this erratum.

Shaded: This erratum is either new or has been modified from the previous specification update.

Table 1. Errata Summary

No.	Plans	Description of Errata
1.	Fixed	Quiet Boot with Add-In Video Card Causes Loss of Video and Boot Problems
2.	NoFix	Self-powered USB Hubs Generate Error Message in Windows* Server 2003
3.	Fixed	Some PCI Cards in Slot 8 Result in Video Corruption During Boot
4.	NoFix	BIOS Recovery from LS240 Fails if Media is in the CD-/DVD-ROM Drive
5.	Fixed	RTC Loses Time Intermittently on a Limited Number of Platforms
6.	NoFix	BIOS Administrator Password is not Case Sensitive
7.	Fixed	System freeze when hot adding/replacing QLA2342
8.	Fixed	Hitachi* DK32CJ Hard Drives Will Not Power Up
9.	Fixed	Momentary loss of Power Good May Force Processor Speed to 800MHz Upon Reset
10.	Fixed	Fluctuating Fan Speeds
11.	Fixed	Windows Server 2003 Install will not complete if Service Partition Already Exists
12.	NoFix	Non-Volatile Variable Messages in EFI Shell
13.	Fixed	Cannot Uninstall ISM 6.0 RC1
14.	NoFix	Chassis Sags When Rack-Mounted
15.	NoFix	Event Log Messages Indicate Network Disconnects/Reconnects During Stress Testing with Onboard NIC
16.	Fixed	Field Diagnostics Compatibility Issue with BIOS RC5
17.	Fixed	MCA Handler Not Logging P64H2 Target Aborts
18.	NoFix	HSC Does Not Support Negative Numbers
19.	Fixed	AC Boot Cycling Issues at Low 3.3V Standby Voltage
20.	NoFix	Platform Event Filter Settings Can Cause System to Get Stuck in a Continuous Reset or Power-Cycle Loop
21.	NoFix	Pressing the SDINIT button early in POST will cause a system hang and FRB3 failure

22.	Fixed	Legacy OS Boot Option in EFI Boot Manager Has No Function
23.	Fixed	Memory Based on 1Gbit Components Not Working Properly
24.	NoFix	FRB Diable Jumper Does Not Work
25.	Fixed	Platform Diagnostics Cache Test hangs in Complete Mode w/ 1.4GHz/4M procs
26.	Fixed	No CMOS battery error at POST, in SEL or OM on failure
27.	NoFix	Using Restore EFI Boot Manager Options in the Save/Restore Configuration Utility Will Cause Network Boot to Fail
28.	Fixed	"Shell: Cannot read from file – Device Error" Displayed after Completion of .nsh Script
29.	Fix	Cannot Install or Boot OS on Emulex* LP9802 SAN with EFI BIOS/FW
30.	Fix	Syscfg Utility Cannot Restore Option ROM Settings for PCI Slot 4 - 8 in BIOS
31.	Fixed	Potential Electrical Marginality in Intel® Itanium® 2 Processor Integer Register File
32.	NoFix	System may hang / reset when doing processor test using Platform Diagnostic Utility

Table 2. Documentation Changes

No.	Plans	Description of Documentation Change
1.	Doc	PCI Add-in Video supported only in slots 1-3
2.	Doc	Itanium® 2 Processors 1.40GHZ with 1.5MB L3 Cache and Low Voltage Itanium® 2 Processors are not supported
3.	Doc	USB 2.0 Supported on SR870BN4
4	Doc	Attention Switch Support for Hot Plug PCI Slots Removed
5	Doc	SM is required for OS Watchdog Timer support

Following are in-depth descriptions of each erratum / documentation change indicated in the tables above. The errata and documentation change numbers below correspond to the numbers in the tables.

Errata

1. Quiet Boot with Add-In Video Card Causes Loss of Video and Boot Problems

Problem When Quiet Boot is set to “Enabled” with a video card in the system (Ex: Slot 1), the system will boot to the logo (press ESC to View Post Messages, [F2] to enter Setup) screen, and subsequently the picture disappears, a loud beep will sound, and then the monitor will turn off. A manual reset is needed to bring the system back to working order

Status This issue is fixed in BIOS RC5.

2. Self-powered USB Hubs Generate Error Message in Windows* Server 2003

Problem When a self-powered USB hub is used in Windows* Server 2003, the following message:”The Generic USB Hub is connected to a hub that does not have enough power to support it.”

Status This issue will not be fixed. S870BN4 will only support self-powered hubs.

3. Some PCI Cards in Slot 8 Result in Video Corruption During Boot

Problem Some add-in adapters installed in slot 8 may result in the adapter BIOS writing on top of the BIOS messages on the display. This may include abnormal color changes and blinking colors.

Status Resolved in BIOS RC4.

4. BIOS Recovery from LS240* Fails if Media is in the CD-/DVD-ROM Drive

Problem BIOS Recovery from LS240 fails if there is any media in the CD-ROM/DVD-ROM drive.

Status This issue will not be fixed. When performing a BIOS Recovery operation from a LS240 diskette, the user must ensure there is no CD-ROM/DVD in the CDROM/DVD drive.

5. RTC Loses Time Intermittently on a Limited Number of Platforms

Problem The Real Time Clock (RTC) has been seen to lose time intermittently on a very limited number (5-10%) of SR870BN4 platforms.

Investigations have shown that residue on the battery can cause the battery holder to intermittently lose connection with the battery and therefore not increment the RTC. There is no functional impact to the platform. Further investigation of this issue has shown that the Battery sense was causing the battery voltage to "droop" below the lower critical threshold. When the voltage passes the lower threshold, a SEL event will be logged. As it returns to normal passing back across the threshold, another SEL event will be logged. This is a "false" failure. An actual failing battery would drop below the lower threshold and remain below.

Status This issue has been fixed in I/O Board PBA # A52336-540. Workaround if this issue is seen is to clean the battery and the contacts within the battery holder with alcohol (using a chem wipe) and to avoid leaving any residue on the battery before reseating it on the IO Riser board.

6. BIOS Administrator Password is not Case Sensitive

Problem The BIOS Administrator password is not case sensitive. There is no differentiation between uppercase and lowercase letters when setting or entering a BIOS password.

Status This issue will not be fixed. This is expected behavior of the core BIOS.

7. System freeze when hot adding/replacing QLA2342

Problem When either hot adding or hot replacing the QLA2342 card, the system may seem to lock up. After hot adding the card and while installing the driver, the system appears to lock up and freeze for several minutes. Eventually it will beome unfrozen and finished the install process. The card appears in Device Manager as normal. Attempts to shut the card off in the O/S may cause the system to appear to hang again for about 10 minutes before the card will be succesfully shut off.

Booting the system with the card inplace does not cause any problems

Status This issue is fixed in BIOS RC6.

8. Hitachi* DK32CJ Hard Drives Will Not Power Up

Problem Hitachi DK32CJ hard drives will not power up in the Tiger system.

Status This issue has been fixed via a PLD change implemented in SCSI backplanes with PBA # A73789-302.

9. Momentary loss of Power Good May Force Processor Speed to 800MHz Upon Reset

Problem If there is a momentary loss of power good from a D2D, when the SR870BN4 resets it can come up with the processor speeds set to 800MHz instead of 900MHz or 1GHz. Investigation shows that in BMC14 and older, the CVDR does not get reprogrammed with a reset that occurs from a momentary loss of power good from a D2D

Status Fixed in BMC16.

10. Fluctuating Fan Speeds

Problem An issue has been seen where some systems may have fluctuating fan speeds. Investigation of this issue has found that the margins set for the normal minimum and lower critical values for operation were right on the threshold of the fans in the system.

Status Fixed in SDR14.

11. Windows* Server 2003 Install will not complete if Service Partition Already Exists

Problem Install of Windows* Server 2003 Build 3718 will not complete if a service partition has been previously created on the hard drive. An error will appear indicating the drive is unformatted, damaged or formatted with an incompatible file system.

Status This issue is fixed in the Service Partition included on Resource CD revision 005.

12. Non-Volatile Variable Messages in EFI Shell

Problem After upgrading to BIOS RC5, non-volatile variable messages may be displayed during the boot to EFI shell. Ex:

```
set: path already exists as a non-volatile variable
Exit status code: Access Denied
alias: dir already exists as a non-volatile variable
Exit status code: Access Denied
```

This behavior is a result of the change to EFI version 14.61, which occurred in BIOS RC5. EFI version 14.61 changed some of its variables from non-volatile to volatile.

Workaround To remove these messages, either perform a BIOS recovery, or delete the non-volatile variable using the *set -d* or *alias -d* commands. Ex:

```
set –d path

alias –d dir
```

Status This issue will not be fixed.

13. Cannot Uninstall ISM 6.0 RC1

Problem After installing Intel Server Management 6.0 RC1, the "JAVA 2 Runtime Environment Standard Edition v. 1.3.1_03" is not listed in "Add or Remove Program" in Control Panel. As a result, the ISM 6.0 JAVA component can not be uninstalled.

Status This issue is fixed in the ISM 6.1 RC2 release.

14. Chassis Sags When Rack-Mounted

Problem The Tiger 4 chassis was designed to have .050" of clearance between the chassis and the adjacent "U" boundary when rack-mounted. Intel has observed that the bottom face of the chassis can bow outward and slightly exceed the .050" spec.

Status This issue will not be fixed.

15. Event Log Messages Indicate Network Disconnects/Reconnects During Stress Testing with Onboard NIC

Problem During network stress testing with Windows Server 2003, event log entries were intermittently seen that indicate that the network connection quickly dropped and reconnected. This was only seen on systems when connected directly to another system via a crossover cable. No test failures were observed and no packet or data corruption occurred.

Workaround The issue was only seen when direct-connected to another system via a crossover cable. When the systems were networked through a switch, the event log entries did not occur.

Status This issue will not be fixed.

16. Field Diagnostics Compatibility Issue with BIOS RC5

Problem With BIOS RC5, if the non-volatile variables are deleted, the SR870BN4 Field Diagnostics will generate errors and not run.

Status This issue is fixed in the version of Field Diagnostics included in Resource CD revision 005. The previous versions expect certain variables to be in non-volatile memory. If these variables are deleted, the Field Diagnostics will not run properly. Workaround is to perform a recovery to RC4, which will restore the variables back into non-volatile memory. If the normal iflash64 update is done to upgrade to RC5, the non-volatile variables will be maintained.

For those developing your own EFI utilities, you must account for this change in EFI 1.10.14.61. If your utility is modifying any of the environment variables, please make sure to check the storage type of the environment variable and save it back to the same storage type. Otherwise, you may see similar issues.

17. MCA Handler Not Logging P64H2 Target Aborts

Problem If a "Target Abort" is issued when there is a "Master Abort" already present in the system, the P64H2's RAS register does not see the "Target Abort"; it only sees the Master Abort.

Status This issue will be fixed in BIOS RC7 for Itanium® 2 Processors at 1GHz and below, and BIOS RC1 for Itanium® 2 Processors at 1.3 GHz and above.

18. HSC Does Not Support Negative Numbers

Problem The HSC is configured to support unsigned numbers only. It is possible to set the SDR values of the SCSI Backplane temperature threshold to a negative number. However, the HSC will interpret this value as a positive number. As a result, you may see false SEL events indicating that the lower threshold has been crossed.

Status This issue will not be fixed. Do not use negative values for the SCSI Backplane temperature threshold.

19. AC Boot Cycling Issues at Low 3.3V Standby Voltage

Problem Some systems have intermittently experienced boot issues during AC boot cycling when 3.3V standby was margined to -6%. Root cause was determined to be a reset signal that should have been deasserted, but was in a TTL indeterminate voltage level due to the low voltage on 3.3V standby and caused the system to be held in reset.

Workaround Disable ITP/JTAG on the processor board. This can be done by jumpering pins 5-6 on J7C1 on the processor board.

Status This issue is fixed in CPU board PBA# A55955-320.

20. Platform Event Filter Settings Can Cause System to Get Stuck in a Continuous Reset or Power-Cycle Loop

Problem Certain conditions can cause the system to get stuck in a continuous reset or power-cycle action, depending on what chassis action is defined for such events via the SMU. The IPMI 1.5 specification allows recovery from this condition by providing a PEF Startup Delay parameter, which postpones PEF triggered actions during certain intervals of BMC operation. The PEF Startup Delay causes Platform Event Filtering-triggered power-down, reset, and power-cycle actions to be postponed when the system is either powered up or is reset locally via a pushbutton or other local 'front-panel' user interface. The current default value is 60 seconds which is not enough to allow the user to boot to the EFI shell and run SMU to disable PEF.

Workaround It is highly recommended to set the PEF Startup Delay time to the maximum setting of 255 seconds. This could be done by booting the system into EFI Shell and running the SMU and setting the PEF Startup Delay. If a system enters such a continuous reset or power-cycle state, increasing this delay will give the user sufficient time to run the SMU and disable the PEF event. The alerting condition can then be addressed.

Status This issue will not be fixed.

21. Pressing the SDINIT button early in POST will cause a system hang and FRB3 failure

Problem If the SDINIT button is pressed early on in POST, the system will hang. Eventually, the system's FRB3 timer will expire and cause a reset. The FRB3 failure will cause one or more processors to be disabled until a processor retest is enabled in BIOS setup.

Workaround None.

Status This issue will not be fixed.

22. Legacy OS Boot Option in EFI Boot Manager Has No Function

Problem The Legacy OS Boot Option in the EFI Boot Manager currently has no function. PAL support for this has been removed.

Workaround None.

Status This boot option is removed in BIOS PR3.0

23. Memory Based on 1Gbit Components Not Working Properly

Problem Memory based on 1Gbit DRAM components currently do not function properly. This is due to a memory address line that is routed incorrectly. Additionally, a timing change in the BIOS is necessary in order to comply with the JEDEC specification for 1Gbit memory components.

Workaround None.

Status These issues have been fixed in -500 memory board and BIOS PR3.0 for the Itanium® 2 Processor with up to 6MB L3 Cache and BIOS PR8.0 for the Itanium® 2 Processor with up to 3MB L3 Cache..

24. FRB Disable Jumper Does Not Work

Problem Jumper J7A3 pin 4-pin 5 is defined as an FRB Disable jumper. This debug feature is not correctly implemented.

Workaround None.

Status This issue will not be fixed.

25. Platform Diagnostics Cache Test hangs in Complete Mode w/ 1.4GHz/4M Itanium® 2 Processors

Problem System hangs when running the Platform Diagnostics cache test in complete mode w/ 1.4GHz/4M Itanium® 2 Processors. The hang does not occur when the test is run in the default Quick mode.

Workaround Run Cache Test in quick mode for 1.4GHz/4M Itanium® 2 Processors

Status This issue has been fixed in fixed in Platform Diagnostics version 1.0, build 13..

26. No CMOS battery error at POST, in SEL or OM on failure

Problem If the cmos battery is removed from the system, the SEL and OM do not report an error about the cmos battery voltage or about it not being present.

The system may halt on POST w/ a CMOS Date/Time Not Set error message, but this behavior is inconsistent (seen on the first boot after removal of the battery, but not on subsequent boots).

Status This issue has been fixed by removing C1A3 on the -552 I/O base board.

27. Using Restore EFI Boot Manager Options in the Save/Restore Configuration Utility Will Cause Network Boot to Fail

Problem Using Save/Restore EFI Boot Manager Options to copy EFI boot configuration from one server to another will cause network boot to fail on the restored server. This is because the MAC address from the original system is copied to the restored system.

Workaround Use the EFI Boot Manager or the *bcfg* shell command to manually configure Boot Manager Options.

Status This issue will not be fixed .

28. "Shell: Cannot read from file – Device Error" Displayed after Completion of .nsh Script

Problem The following error shows up on the screen immediately after a .nsh has completed in the EFI shell. "shell: Cannot read from file – Device Error". The script still executes properly.
This issue occurs on BIOS Versions PR9.2 and PR4.1.

Status This issue have been fixed in BIOS versions with build number 928 and greater.

29. Cannot Install or Boot OS on Emulex* LP9802 SAN with EFI BIOS/FW

Problem The system may hang during OS installation or during boot phase when Emulex LP9802 HBA is being used with EFI BIOS/FW.
This issue has been found on system BIOS PR2.1/PR1.3 for Itanium® 2 Processor with up to 9MB L3 cache and PR6.0/PR5.1 for Itanium® 2 Processor with up to 6MB L3 cache.

Status This issue has been fixed in BIOS PR2.3 for Itanium® 2 Processor with up to 9MB L3 cache and will be fixed in BIOS PR6.1 for Itanium® 2 Processor with up to 6MB L3 cache.

30. Syscfg utility Cannot Restore Option ROM Settings for PCI Slot 4-8 in BIOS

Problem Option ROM settings for PCI slot 4-8 cannot be restored successfully by Syscfg utility.

Status Will be fixed in next BIOS release

31. Potential Electrical Marginality in Intel® Itanium® 2 Processor Integer Register File

Problem Under certain specific and complex environmental and data conditions a signal race condition can occur that may affect some registers in the Intel® Itanium® 2 Processor (up to 9MB L3 cache –codename Madison 9MB family of products) integer register file.

Implication: This issue may result in a nested OS fault, an application fault or other unexpected behavior, A nested fault may manifest in Unix/Linux as a “Kernel Panic” and in Windows* as a “blue screen”.

Workaround: None at this time.

Status Fixed for Madison 9MB family of processors shipped after Septermber 2006. For further details see the *Intel® Itanium® 2 Processor Specification Update* Erratum E167.

32. System may hang / reset when doing processor test using Platform Diagnostic Utility

Problem System may hang / reset when doing processor test running Platform Diagnostic Utility Ver1.0 Build 19 through Resource CD with Intel® Itanium® 2 Processor up to 9MB L3 cache –codename Madison 9MB family of products.

Implication: This issue is caused by software compatibility. There is no real hardware damage. This issue doesn’t exist with Intel® Itanium® 2 Processor 9000 Series

Workaround: Running the utility standalone from hard drive (not through Resource CD) will fix this issue.

- In the root directory of system EFI partition, create a directoty as \efi\service\diagnostics, and make it as the current directory

- Copy all files from directoy \Utilities\FieldDiags\ on Resource CD to \efi\service\diagnostics
- Execute fielddiags.efi. This will extract all the files.
- Excute fielddiags.nsh. This will launch the diagnostic utility GUI. You can do the test as usual.

Status Will not Fix

Documentation Changes

1. PCI Add-in Video supported only in slots 1-3

If your system configuration requires the use of an add-in PCI Video card, the card must be installed in PCI slot 1, 2, or 3.

2. Itanium® 2 Processors 1.40GHZ with 1.5MB L3 Cache and Low Voltage Itanium® 2 Processors are not supported

Itanium® 2 Processors 1.40GHZ with 1.5MB L3 Cache and Low Voltage Itanium® 2 Processors are not supported on the SR870BN4 server platform. Beginning with BIOS PR3, installation of these processors will cause BIOS POST to halt and display a message indicating that unsupported processors are installed and requiring them to be removed from the system.

3. USB 2.0 Supported on SR870BN4

USB 2.0 is supported on SR870BN4 beginning with BIOS RC4 for the Itanium® 2 Processor with up to 3MB L3 cacheand all released versions of BIOS for the Itanium® 2 Processor with up to 6MB L3 cache.

4. Attention Switch Support for Hot Plug PCI Slots Removed

The Attention Switch feature for hot-plug PCI slots has been removed on SR870BN4 platform. This feature has not been functional on all production-released BIOS versions.

5. ISM is required for OS Watchdog Timer support

The BIOS Setup offers a control item that allows the OS load watchdog timer to be enabled or disabled. The default for the OS load watchdog timer function is Disabled. This menu item is located under the System Management Submenu. It is to be noted that the system must have Intel® Server Management (ISM) V6.0, or later loaded in order to refresh the timer or disable it.