Upgrading the OCPRF100 Server System to support Intel® 700MHz Pentium® III Xeon™ Processors

Revision 1.0

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Enterprise Platforms Group
Server Products Division

Revision History

Date	Revision Number	Modifications
June 6, 2000	1.0	Initial release.

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The OCPRF100 and/or the SRPM8 platform or their components may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are available on request.

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1. Introduction

This document explains the revisions of hardware and firmware/BIOS that are required to upgrade an OCPRF100 server system to a system that is capable of supporting 700MHz Pentium III Xeon processors. This document also provides information on the upgrade process and dependencies.

There are four basic steps to this upgrade:

1. Verify current firmware/BIOS and upgrade as necessary.

2. Check the server for compatible hardware and install as necessary.

3. Install compatible Cascades large cache processors.

4. Verify that the BIOS correctly identifies the 700MHz Pentium III Xeon processors during the power on self-test.

2. Before You Begin

Prior to upgrading your system, locate and have available the *OCPRF100 Server System Product Guide*. Also, ensure that all applicable hardware is available, including the required tools as outlined in the product guide. Follow all safety and warning precautions, and pay special attention to ESD (Electrostatic Discharge) protection measures when handling boards. Only a technically qualified service person should integrate and configure system hardware.

It is recommended that you be familiar with the following chapters below in the product guide, as they will be referenced during this upgrade procedure:

Chapter 5 Working Inside the System

Chapter 6 Upgrading Boardset Components

Note: If the product guide is unavailable, it may be obtained from http://support.intel.com/support/motherboards/server/ocprf100/manual.htm

3. System Hardware Requirements

Ensure that the processor and system boards used in the OCPRF100 system are at the recommended revision level to support 700MHz Pentium III Xeon processors with a large cache. The recommended revision levels are listed below.

3.1 SRPM8 Mezzanine Board

Production revision 753356–300 and later SRPM8 Mezzanine boards will support 700MHz Pentium III Xeon processors with a large cache. Earlier revisions of the Mezzanine board are unsupported when using 700MHz Pentium III Xeon processors.

3.2 OCPRF100 Profusion Board

Production revision 736365-315 and later OCPRF100 Profusion boards will support 700MHz Pentium III Xeon processors with a large cache.

3.3 OCPRF100 IO Board

Production revision 702647-504 and later OCPRF100 I/O boards will support 700MHz Pentium III Xeon processors with a large cache. When available, the PCI-X capable SRPM8 I/O board will also support 700MHz Pentium III Xeon processors.

3.4 Processor Requirements

The 700MHz Intel® Pentium® III Xeon™ processors come in many different configurations. OCPRF100-based servers support a limited number of these configurations. Supported processors include 5/12 volt, 1 or 2 MB cache, 700MHz processors running on a front side bus of 100 MHz. No other 700MHz processors are supported. Please contact your Intel representative to confirm which steppings of these processors have been validated for use in this system.

OCPRF100-based systems support one to eight processors. The following are restrictions on those processors:

- Processors below 700MHz cannot be mixed with processors at or above 700MHz.
- All the processors in the system must have the same cache size.
- Processors above 700MHz are not supported at this time.

4. BIOS and Firmware Requirements

Ensure that the BIOS, and firmware (BMC, FPC, HSC, and SDR) are at the recommended version to support 700MHz Pentium III Xeon processors with a large cache. The latest version of BIOS and firmware is available on the Intel Business Links (IBL) website under Content View /Server/OCPRF100/Software.

4.1 BIOS/Firmware

Table 4-1, OCPRF100 Recommended BIOS/Firmware

BIOS	BMC	FPC	HSC	FRU/SDR
PR15	25	18	05	v3.4.2 or v3.4.E

Table 4-2, J6A1 Jumper Settings

	15/16	13/14	11/12	9/10	7/8	5/6	3/4	1/2
700MHZ	X	X						
650MHZ	X			X				
600MHZ	X							
550MHZ		X	X	X				
500MHZ		X	X					
450MHZ			X	X				
400MHZ			X					
350MHZ		X		X				
300MHZ		X						

X=Closed or Jumpered

Note: A diagram of jumper block J6A1 is on the underside of the system top cover.

4.2 Upgrade Instructions

The instructions below describe how to upgrade the BIOS, and firmware code. Please note that the BIOS and firmware must be updated prior to installing 700MHz Pentium III Xeon processors in the system. The system should be updated in the following order. This is the preferred upgrade path. If this is not possible, see section 5.3, entitled "Alternate Upgrade Procedures."

1. Ensure you have 550MHz or lower speed Intel® Pentium® III Xeon™ processors installed in the system initially.
2. Ensure that jumpers are set to the correct processor speed setting for the current processors installed. See table 5-2.
3. Update the BMC, FPC, and HSC using Fwupdate Utility 1.35 or later if necessary.
4. Update the BIOS to Production Release 15 or later version.
5. Power off the system.
6. Go to Chapter 6 of this document and upgrade the Mezzanine board(s) as required per the instructions.

4.3 Alternate Upgrade Procedure

Warning: This procedure will not work if BIOS PR5 is installed. Please insure the system has any BIOS installed other than PR5 for the alternate procedure.

1. Follow steps 1 through 7 in Chapter 5 of this guide entitled "Working Inside The System.
2. Install Mezzanine board(s) as per instructions in Chapter 6 of the OCPRF100 Product Guide.
3. Install 700MHZ Intel® Pentium® III Xeon™ processors.
4. Ensure that jumpers are set for 700MHZ. See table 5-2.
5. Power on system. As system begins to boot, error message 8177 " BIOS does not support current processor stepping" is displayed. This is normal until the BIOS is upgraded.
6. Update the BIOS to Production Release 15 or later version.
7. Update the BMC, FPC, and HSC using Fwupdate Utility 1.35 or later if necessary.
8. Update the FRU/SDR files to version 3.4.2[1] or 3.4.E[2]
9. Re-boot system and verify that BIOS correctly identifies the 700MHz Intel® Pentium® III Xeon™ processors during the power on self-test.

Note: The FRU/SDR utility should be run after the boardset upgrade and processor installation to ensure that sensor threshold values are programmed correctly.

[1] SRPM8 FRU/SDR files.

[2] OCPRF100 FRU/SDR files with 550MHZ and below or 700MHz Pentium III Xeon processor support.

5. Working Inside The System

Refer to Chapter 5 of the OCPRF100 Product Guide entitled "Working Inside the System" for instructions on removing the boardset. Follow all safety and precautionary guidelines. Before removing the covers to work inside the system, observe the following safety guidelines.

1. Power off all peripheral devices connected to the system.
2. Power off the system.
3. Unplug the AC power cords from the system or outlet.
4. Label and disconnect all peripheral cables and all telecommunication lines connected to I/O ports or connectors on the back of the system.
5. Provide electrostatic discharge (ESD) protection by wearing an anti-static wrist strap attached to the chassis ground of the system (any unpainted metal surface) when handling components.
6. Remove the Top Cover Assembly.
7. Remove the existing processors.

5.1 Upgrading Boardset Components

Refer to Chapters 5 and 6 of the OCPRF100 Product Guide

1. In order to remove the Profusion carrier tray, and Mezzanine board(s), follow the instructions in Chapters 5 and 6 of the OCPRF100 Product Guide detailing removal of each sub-assembly.
2. Replace the existing Mezzanine board(s) with the new Mezzanine board, PBA 753356–300 or higher. Since the jumper block is more accessible at this time, please ensure that jumper settings are set correctly for the 700MHz Pentium III Xeon processors prior to re-installing the Profusion carrier sub-assembly. See Table 5-2.
3. Re-install the Profusion carrier tray sub-assembly as outlined in Chapter 5 and 6 of the OCPRF100 Product Guide.
4. Install the 700MHz Pentium III Xeon processors.
5. Replace top cover, connect all peripherals, connect AC power, and power on system.
6. Power on system and update FRU/SDR files to version 3.4.2[3] or 3.4.E[4]
7. Re-boot system and verify that BIOS correctly identifies the 700MHz Pentium III Xeon processors during the power on self-test.

[3] SRPM8 FRU/SDR files.

[4] OCPRF100 FRU/SDR files with 550MHZ and below or 700MHz Pentium III Xeon processor support.

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Appendix A: Glossary

Term	Definition
BIOS	Basic Input / Output System – PC software, typically contained in a nonvolatile memory chip, which the PC uses to boot itself and which contains all the code required to control the keyboard, display screen, disk drives, serial communications, and other miscellaneous functions
BMC	Baseboard Management Controller – a microcontroller on the system baseboard, usually providing the majority of server management functionality
FRU	Field Replaceable Unit – a module or component which will typically be replaced in its entirety as part of a field service repair operation
HSC	Hot-swap Controller – the microcontroller that implements the SAF-TE command set and controls the fault lights and drive power on a hot-swap RAID backplane
SDR	Sensor Data Record – a data record that provides platform management sensor type, locations, event generation, and access information