Errata

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6. The SPI can Send Wrong Byte

If the SPI is in master mode, it will restart the old transfer if new data is written on the same clock edge as the previous transfer is finished.

Problem Fix/Workaround

When writing to the SPI, first wait until it is ready, then write the byte to transmit.

5. Reset During EEPROM Write

If reset is activated during EEPROM write the result is not what should be expected. The EEPROM write cycle completes as normal, but the address registers are reset to 0. The result is that both the address written and address 0 in the EEPROM can be corrupted.

Problem Fix/Workaround

Avoid using address 0 for storage, unless you can guarantee that you will not get a reset during EEPROM write.

4. SPI Interrupt Flag can be Undefined After Reset

In certain cases when there are transitions on the SCK pin during reset, or the SCK pin is left unconnected, the start-up value of the SPI interrupt flag is be unknown. If the flag is not reset before enabling the SPI interrupt, a pending SPI interrupt may be executed.

Problem Fix/Workaround

Clear the SPI interrupt flag before enabling the interrupt.

3. Verifying EEPROM in System

EEPROM verify in In-System Programming mode cannot operate with maximum clock frequency. This is independent of the SPI clock frequency.

Problem Fix/Workaround

Reduce the clock speed, or avoid using the EEPROM verify feature.

2. Serial Programming av Voltaages below 3.0 Volts

At voltages below 3.0 Volts, serial programming might fail.

Problem Fix/Workaround

Keep VCC at 3.0 Volts or higher during In-System Programming

1. Skip Instruction with Interrupts

A skip instruction (SBRS, SBRC, SBIS, SBIC, CPSE) that skips a two-word instruction needs three clock cycles. If an interrupt occurs during the first or second clock cycle of this skip-instruction, the return address will not be stored correctly on the stack. In this situation, the address of the second word in the two-word instruction is stored. This means that on return from interrupt, the second word of the two-word command will be decoded and executed as an instruction. The AT90S4414 has two two-word instructions: LDS and STS.

Note: This can only occur if all of the following conditions are true:

- A skip instruction is followed by a two-word instruction.
- The skip instruction is actually skipping the two-word instruction.

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- Interrupts are enabled, and at least one interrupt source can generate an interrupt.

- An interrupt arrives in the first or second cycle of the skip instruction.

Note 2: This will only cause problems if the address of the following LDS or STS command points to an address beyond 400 Hex.

Problem Fix/Workaround

For C-programs, use the IAR compiler version 1.40b or later. The compiler will never generate the sequence.

For assembly program, avoid skipping a two word instruction if interrupts are enabled.