SGS-THOMSON MICROELECTRONICS

TDA9103

DEFLECTION PROCESSOR FOR MULTISYNC MONITOR

HORIZONTAL

- DUAL PLL CONCEPT
- 150kHz MAXIMUM FREQUENCY
- SELF-ADAPTIVE (EX : 30 TO 85kHz)
- X-RAY PROTECTION INPUT
- DC ADJUSTABLE DUTY-CYCLE
- INTERNAL 1st PLL LOCK/UNLOCK IDENTIFICATION
- 4 OUTPUTS FOR S-CORRECTION
- WIDE RANGE DC CONTROLLED H-POSITION
- ON/OFF SWITCH (FOR PWR MANAGEMENT)
- TWO H-DRIVE POLARITIES

VERTICAL

- VERTICAL RAMP GENERATOR
- 50 TO 150Hz AGC LOOP
- DC CONTROLLED V-AMP, V-POS, S-AMP AND S-CENTERING
- ON/OFF SWITCH

B+ REGULATOR

- INTERNAL PWM GENERATOR FOR B+ CURRENT MODE STEP-UP CONVERTER
- DC ADJUSTABLE B+ VOLTAGE
- OUTPUT PULSES SYNCHRONISED ON HORIZONTAL FREQUENCY
- INTERNAL MAXIMUM CURRENT LIMITATION

EWPCC

- VERTICAL PARABOLA GENERATOR WITH DC CONTROLLED KEYSTONE AND AMPLITUDE

GENERAL

- ACCEPT POS. OR NEG. H AND V SYNC POLARITIES
- SEPARATED H AND V TTL INPUT
- SAFETY BLANKING OUTPUT

DESCRIPTION

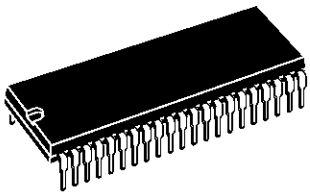
The TDA9103 is a monolithic integrated circuit assembled in a 42 pins shrunk dual in line plastic package.

This IC controls all the functions related to the horizontal and vertical deflection in multimodes or multisync monitors.

As can be seen in the block diagram, the TDA9103 includes the following functions :

- Positive or Negative sync polarities,
- Auto-sync horizontal processing,
- H-PLL lock/unlock identification,
- Auto-sync Vertical processing,
- East/West signal processing block,
- B+ controller,
- Safety blanking output.

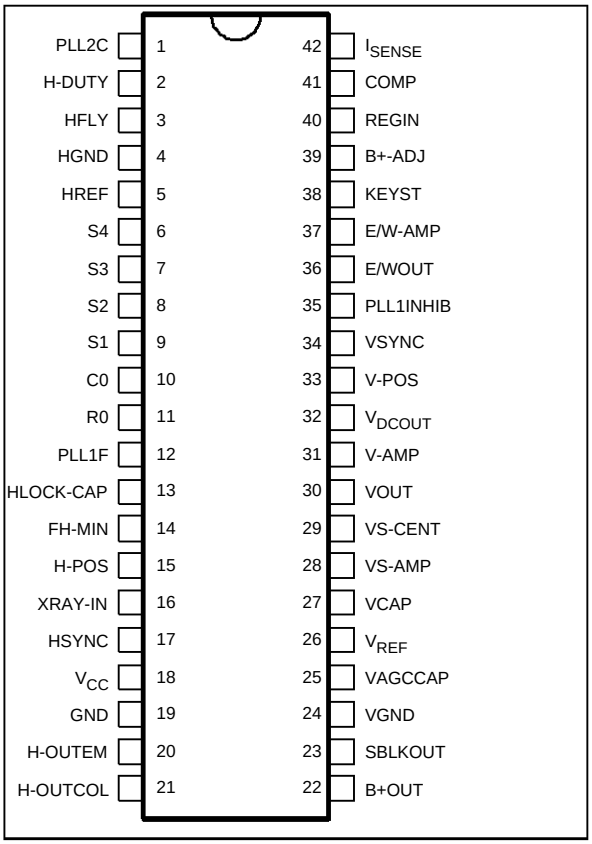
This IC, combined with TDA9205 (RGB preamp), STV9420/21 or 22 (O.S.D. processor), ST7271 (micro controller) and TDA8172 (vertical booster), allows to realize very simple and high quality multimodes or multisync monitors.



SHRINK42
(Plastic Package)

ORDER CODE : TDA9103

PIN CONNECTIONS



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PIN-OUT DESCRIPTION

Pin N°	Name	Function
1	PLL2C	Second PLL Loop Filter
2	H-DUTY	DC Control of Horizontal Drive Output Pulse Duty-cycle. If this pin is grounded, the horizontal and vertical outputs are inhibited. By connecting a capacitor on this pin a soft-start function may be realized on h-drive output.
3	H-FLY	Horizontal Flyback Input (positive Polarity)
4	H-GND	Horizontal Section Ground. Must be connected only to components related to H blocks.
5	H-REF	Horizontal Section Reference Voltage. Must be filtered by capacitor to Pin 4
6	S4	Hor S-CAP Switching
7	S3	Hor S-CAP Switching
8	S2	Hor S-CAP Switching
9	S1	Hor S-CAP Switching
10	C0	Horizontal Oscillator Capacitor. To be connected to Pin 4.
11	R0	Horizontal Oscillator Resistor. To be connected to Pin 4.
12	PLL1F	First PLL Loop Filter. To be connected to Pin 4.
13	HLOCK-CAP	First PLL Lock/Unlock Time Constant Capacitor. Capacitor filtering the frequency change detected on Pin13. When frequency is changing, a blanking pulse is generated on Pin 23, the duration of this pulse is proportionnal to the capacitor on Pin 13. To be connected to Pin 4.
14	FH-MIN	DC Control for Free Running Frequency Setting. Comming from DAC output or DC voltage generated by a resistor bridge connected between Pin 5 and 4.
15	H-POS	DC Control for Horizontal Centering
16	XRAY-IN	X-RAY Protection Input (with internal latch function)
17	H-SYNC	TTL Horizontal Sync Input
18	V_{CC}	Supply Voltage (12V Typical)
19	GND	Ground
20	H-OUTEM	Horizontal Drive Output (emiter of internal transistor). See description on pages 15-16.
21	H-OUTCOL	Horizontal Drive Output (open collector of internal transistor). See description on pages 15-16.
22	B+ OUT	B+ PWM Regulator Output
23	SBLK OUT	Safety Blanking Output. Activated during frequency changes, when X-RAY input is triggered or when VS is too low.
24	VGND	Vertical Section Signal Ground
25	VAGCCAP	Memory Capacitor for Automatic Gain Control Loop in Vertical Ramp Generator
26	V_{REF}	Vertical Section Reference Voltage
27	VCAP	Vertical Sawtooth Generator Capacitor
28	VS-AMP	DC Control of Vertical S Shape Amplitude
29	VS-CENT	DC Control of Vertical S Centering
30	VOUT	Vertical Ramp Output (with frequency independant amplitude and S-correction)
31	V-AMP	DC Control of Vertical Amplitude Adjustment
32	V_{DCOUT}	Vertical Position Reference Voltage Output Temperature Matched with V-AMP Output
33	V-POS	DC Control of Vertical Position Adjustment
34	VSYNC	Vertical TTL Sync Input
35	PLL1INHIB	TTL Input for PLL1 Output Current Inhibition (To be used in case of comp sync input signal)
36	E/WOUT	East/West Pincushion Correction Parabola Output
37	E/W-AMP	DC Control of East/West Pincushion Correction Amplitude
38	KEYST	DC Control of Keystone Correction
39	B+ ADJ	DC Control of B+ Adjustment
40	REGIN	Regulation Input of B+ Control Loop
41	COMP	B+ Error Amplifier Output for Frequency Compensation and Gain Setting
42	I_{SENSE}	Sensing of External B+ Switching Transistor Emiter Current

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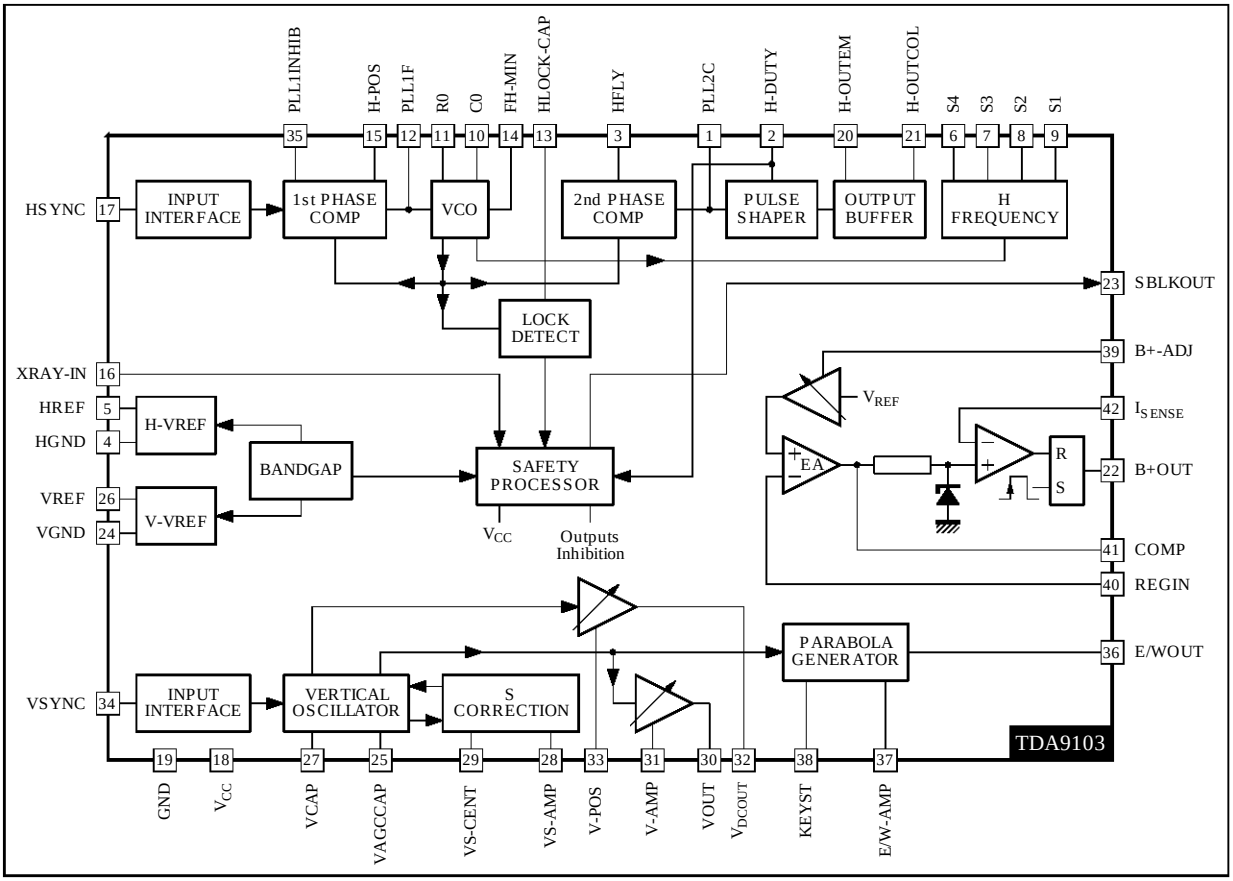
BLOCK DIAGRAM



QUICK REFERENCE DATA

Parameter	Value	Unit
Horizontal Frequency Range	15 to 150	kHz
Autosynch Frequency Range (for Given R0, C0)	1 to 3.7	FH
± Hor Sync Polarity Input	YES	
Compatibility with Composite Sync on H-SYNC Input	YES (1)	
Lock/Unlock Identification on 1st PLL	YES	
DC Control for H-Position	YES	
X-RAY Protection	YES	
Hor DUTY Adjust	YES	
Stand-by Function	YES	
Hor S-CAP Switching Control	YES	
Two Polarities H-Drive Outputs	YES	
Supply Voltage Monitoring	YES	
PLL1 Inhibition Possibility	YES	
Safety Blanking Output	YES	
Vertical Frequency Range	35 to 200	Hz
Vertical Autosync Range (for a Given Capacitor Value)	50 to 150	Hz
Vertical -S- Correction	YES	
Vertical -C- Correction	YES	
Vertical Amplitude Adjustment	YES	
Vertical Position Adjustment	YES	
Automatic B+ Adjustment Control Loop	YES	
B+ Adjustment	YES	
East/West Parabola Output	YES	
PCC (Pin Cushion Correction) Amplitude Adjustment	YES	
Keystone Adjustment	YES	
Reference Voltage	YES (2)	
Mode Detection	NO	
Dynamic Focus	NO	
Blanking Output	NO	

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Notes : 1. See application diagram.
2. One for Horizontal section and one for Vertical section.

ABSOLUTE MAX RATING

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage (Pin 18)		13.5	V
V_{IN}	Max Voltage on	Pins 2, 14, 15, 28, 29, 31, 33, 37, 38, 39 Pin 3 Pins 17, 34 Pin 40 Pin 42 Pin 16	8 1.8 6 8 8 5.5	V
VESD	ESD Succeptibility Human Body Model, 100pF Discharge through 1.5kΩ EIAJ Norm, 200pF Discharge through 0Ω		 2 300	 kV V
T_{stg}	Storage Temperature		-40, +150	°C
T_j	Max Operating Junction Temperature		150	°C
T_{oper}	Operating Temperature		0, +70	°C

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THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-a)}$	Junction-Ambient Thermal Resistance	Max.	65	°C/W

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HORIZONTAL SECTION

Operating conditions

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
VCO						
R0min	Oscillator Resistor Min Value	Pin 11	6			kΩ
C0min	Oscillator Capacitor Min Value	Pin 10	390			pF
Fmax	Maximum Oscillator Frequency				150	kHz
HsVR	Horizontal Sync Input Voltage Range	Pin 17	0		5.5	V
INPUT SECTION						
MinD	Minimum Input Pulses Duration	Pin 17	0.7			µS
Mduty	Maximum Input Signal Duty Cycle	Pin 17			25	%
OUTPUT SECTION						
I3m	Maximum Input Peak Current on Pin 3				2	mA
IS1 to IS4	Maximum Current on S1 to S4 Outputs	Pins 6 to 9			0.5	mA
VS1 to VS4	Maximum Voltage on S1 to S4 Outputs	Pins 6 to 9			V_{CC}	V
HOI1	Horizontal Drive Output Max Current	Pin 20, sourced current			20	mA
HOI2	Horizontal Drive Output Max Current	Pin 21, sunk current			20	mA
DC CONTROL VOLTAGES						
DCadj	DC Voltage Range on DC Controls	V_{REF-H} = 8V, Pins 2-14-15	2		6	V

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Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
SUPPLY AND REFERENCE VOLTAGES						
V_{CC}	Supply Voltage	Pin 18	10.8	12	13.2	V
I_{CC}	Supply Current	Pin 18, See Figure 1		40	60	mA
V_{REF-H}	Reference Voltage for Horizontal Section	Pin 5, I = 2mA	7.4	8	8.6	V
I_{REF-H}	Max Sourced Current on V_{REF-H}	Pin 5			5	mA
V_{REF-V}	Reference Voltage for Vertical Section	Pin 26, I = 2mA	7.4	8	8.6	V
I_{REF-V}	Max Sourced Current on V_{REF-V}	Pin 26			5	mA
INPUT SECTION/PLL1						
V_{INTH}	Hor Input Threshold Voltage Pin 17	Low level voltage High level voltage	 2		0.8	V V
V_{VCO}	VCO Control Voltage Range	V_{REF-H} = 8V, Pin 12	1.6		6.2	V
VCOG	VCO Gain, dF/dV Pin 12	R0 = 6.49kΩ, C0 = 680pF		15		kHz/V
Hph	Horizontal Phase Adj Range (Pin 15)	% of Hor period		±12.5		%
FFadj	Free Running Frequency Adj Range (Pin 14)	Without H-sync Signal		±20		%
S1th	VCO Input Voltage for S1 Switching	Pin 12 voltage, V_{REF-H} = 8V	1.85	2	2.25	V
S2th	VCO Input Voltage for S2 Switching	Pin 12 voltage, V_{REF-H} = 8V	2.25	2.4	2.65	V
S3th	VCO Input Voltage for S3 Switching	Pin 12 voltage, V_{REF-H} = 8V	2.9	3	3.3	V
S4th	VCO Input Voltage for S4 Switching	Pin 12 voltage, V_{REF-H} = 8V	3.5	3.7	3.9	V
F0	Free Running Frequency	$V_{14} = V_{REF}/2$ R0 = 6.49kΩ C0 = 680pF	23.5	25	27.5	kHz
VS1D to VS4D	Low Level Output Voltage on S1 to S4 Outputs	Pins 6 to 9, I = 0.5mA		0.2	0.4	V
CR	PLL1 Capture Range (F0 = 27kHz) Fh Min Fh Max	See conditions on Figure 1	 94		28	kHz
PLLinh	PLL 1 Inhibition (Pin 35) PLL ON PLL OFF	 V_{35} V_{35}	 2		0.8	V
SECOND PLL AND HORIZONTAL OUTPUT SECTION						
FBth	Flyback Input Threshold Voltage	Pin 3	0.65	0.75		V
Hjit	Horizontal Jitter			100		ppm
HDmin HDmin	Minimum Hor Drive Output Duty-cycle Maximum Hor Drive Output Duty-cycle	Pin 20 or 21, V_2 = 2V Pin 20 or 21, V_2 = 6V	 45	30 50	35	% %
HDvd	Horizontal Drive Low Level Output Voltage	V_{21}-V_{20}, Iout = 20mA, Pin 20 to GND		1.1	1.7	V
HDem	Horizontal Drive High Level Output Voltage (output on Pin 20)	Pin 21 to V_{CC}, I_{OUT} = 20mA	9.5	10		V
XRAYth	X-RAY Protection Input Threshold Voltage	Pin 16		1.6	1.8	V
ISblkO	Maximum Output Current on Safety Blanking Output	I_{23}			10	mA
VSblkO	Low-Level Voltage on Safety Blanking Output	V_{23} with I_{23} = 10mA		0.25	0.5	V
Vphi2	Internal Clamping Voltage on 2nd PLL Loop Filter Output (Pin 1)	Vmin Vmax		1.6 3.2		V V
V_{OFF}	Pin 2 Threshold Voltage to Stop H-out, V-out B+out and to Activate S-BLK.OFF Mode when $V_2 < V_{OFF}$	V_2		1		V

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B+ SECTION

Operating Conditions

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
EAOI	Maximum Error Amplifier Output Current	Sourced by Pin 41 Sunk by Pin 41			0.5 2	mA mA
FeedRes	Minimum Feedback Resistor	Resistor between Pins 40 and 41	5			kΩ

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Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
OLG	Error Amplifier Open Loop Gain	At low frequency (see Note 1)		85		dB
UGBW	Unity Gain Bandwidth	(see Note 1)		6		MHz
IRI	Regulation Input Bias Current	Current sourced by Pin 40 (PNP base)		0.2		µA
EAOI	Maximum Guaranted Error Amplifier Output Current	Current sourced by Pin 41 Current sunk by Pin 41	0.5 2			mA mA
CSG	Current Sense Input Voltage Gain	Pin 42		3		
MCEth	Max Curent Sense Input Threshold Voltage	Pin 42		1.2		V
ISI	Current Sense Input Bias Current	Current sunk by Pin 42 (NPN base)		1		µA
Tonmax	Maximum External Power Transistor on Time	% of H-period @ f0 = 27kHz		75		%
B+OSV	B+ Output Low Level Saturation Voltage	V_{22} with I_{22} = 10mA		0.25		V
IV_{REF}	Internal Reference Voltage	On error amp (+) input for V_{39} = 4V		4.9		V
V_{REFADJ}	Internal Reference Voltage Adjustment Range	2V < V_{39} < 6V		±14		%

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EAST WEST PARABOLA GENERATOR

Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Vsym	Parabola Symetry Adjustment Capability (for Keystone Adjustment ; with Pin 38)	See Figure 2 ; internal voltage V_{38} = 2V V_{38} = 4V V_{38} = 6V		 3.2 3.5 3.8		V
Kadj	Keystone Adjustment Capability B/A ratio A/B ratio	See Figure 2 ; V_{37} = 4V V_{38} = 2V V_{38} = 6V		 2.3 2.0		
Paramp	Parabola Amplitude Adjustment Capability Maximum Amplitude on Pin 36 Maximum Ratio between Max and Min	V_{38} = 4.3V, V_{28} = 2V V_{37} = 2V 2V < V_{37} < 6V	 3.3 2.4	 3.8 3	 4.3	V

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VERTICAL SECTION

Operating Conditions

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
VSVR	Vertical Sync Input Voltage Range	On Pin 34	0		5.5	V

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Electrical Characteristics (V_{CC} = 12V, T_{amb} = 25°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{BIASP}	Pin 23-28-29 Bias Current (Current Sourced by PNP Base)	For $V_{23\text{-}28\text{-}29}$ = 2V		2		µA
I_{BIASN}	Pin 31 Bias Current (Current Sunk by NPN Base)	For V_{31} = 6V		0.5		µA
VSth	Vertical Sync Input Threshold Voltage	Pin 34; High-level Low-level	2		 0.8	V V
VSBI	Vertical Sync Input Bias Current (Current Sourced by PNP Base)	V_{34} = 0.8V		1		µA
V_{RB}	Voltage at Ramp Bottom Point	On Pin 27		2/8		$V_{REF\text{-}V}$
V_{RT}	Voltage at Ramp Top Point (with Sync)	On Pin 27		5/8		$V_{REF\text{-}V}$
V_{RTF}	Voltage at Ramp Top Point (without Sync)	On Pin 27		VRT-0.1		V
I_{R27}	Output Current Range on Pin 27 during Ramp Charging Time. Current to Charge Capacitor between Pin 27 and Ground	V_{28} = 2V (Note 2), 2V < V_{27} < 5V Min current Max current	 100	 15 135	 20	 µA µA
VSW	Minimum Vertical Sync Pulse Width	Pin 34	5			µS
VSmDut	Vertical Sync Input Maximum Duty-cycle	Pin 34			15	%
VSTD	Vertical Sawtooth Discharge Time Duration	On Pin 27, with 150nF cap		85		µS
VFRF	Vertical Free Running Frequency (V_{28} = 2V)	Measured on Pin 27 Cosc (Pin27) = 150nF		100		Hz
ASFR	AUTO-SYNC Frequency Range (see Note 3)	With C_{27} = 150nF ±5%	50		150	Hz
RATD	Ramp Amplitude Thermal Drift	On Pin 30 (see Note 1) (0°C < T_{amb} < 70°C)		100		ppm/°C
RAFD	Ramp Amplitude Drift Versus Frequency	V_{31} = 6V, C_{27} = 150nF 50Hz < F < 120Hz		200		ppm/Hz
Rlin	Ramp Linearity on Pin 27 $\Delta I_{27}/I_{27}$	V_{28} = 2V, V_{25} = 4.3V 2.5V < V_{27} < 4.5V		0.5		%
Rload	Minimum Load on Pin 25 for less than 1% Vertical Amplitude Drift		50			MΩ
Vpos	Vertical Position Adjustment Range Voltage on Pin 32	V_{33} = 2V V_{33} = 4V V_{33} = 6V	 3.65	3.2 3.5 3.8	3.3	V V V
I_{VPOS}	Max Current on Vertical Position Control Output (Pin 32)			±2		mA
Vor	Vertical Output Voltage Range (on Pin 30) (Peak to Peak Voltage on Pin 30)	V_{31} = 2V V_{31} = 4V V_{31} = 6V	 3.75	2 3 4	2.2	V V V
V_{OUTDC}	DC Voltage on Vertical Output (Pin30)	See Note 4		7/16		$V_{REF\text{-}V}$
V0I	Vertical Output Maximum Output Current	On Pin 30		±5		mA
dVS	Max Vertical S-Correction Amplitude (V_{28} = 2V Inhibits S-CORR; V_{28} = 6V gives Maximum S-CORR) (see Figure 3)	ΔV/V30pp at T/4 ΔV/V30pp at 3T/4		-4 +4		% %
Ccorr	C-Correction Adjustment Range Voltage on Pin 27 for Maximum Slope on the Ramp (with S-Correction) (see Figure 4)	V_{29} = 2V V_{29} = 4V V_{29} = 6V		3 3.5 4		V V V

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Notes : 1. These parameters are not tested on each unit. They are measured during our internal qualification procedure which includes characterization on batches comming from comers of our processes and also temperature characterization.
2. When 2V are applied on Pin 28 (Vertical S-Correction control), then the S-Correction is inhibited, consequently the sawtooth have a linear shape.
3. It is the frequency range for which the VERTICAL OSCILLATOR will automatically synchronize, using a single capacitor value on Pin 27 and with a constant ramp amplitude.
4. Typically 3.5V for Vertical reference voltage typical value (8V).

Figure 1 : Testing Circuit

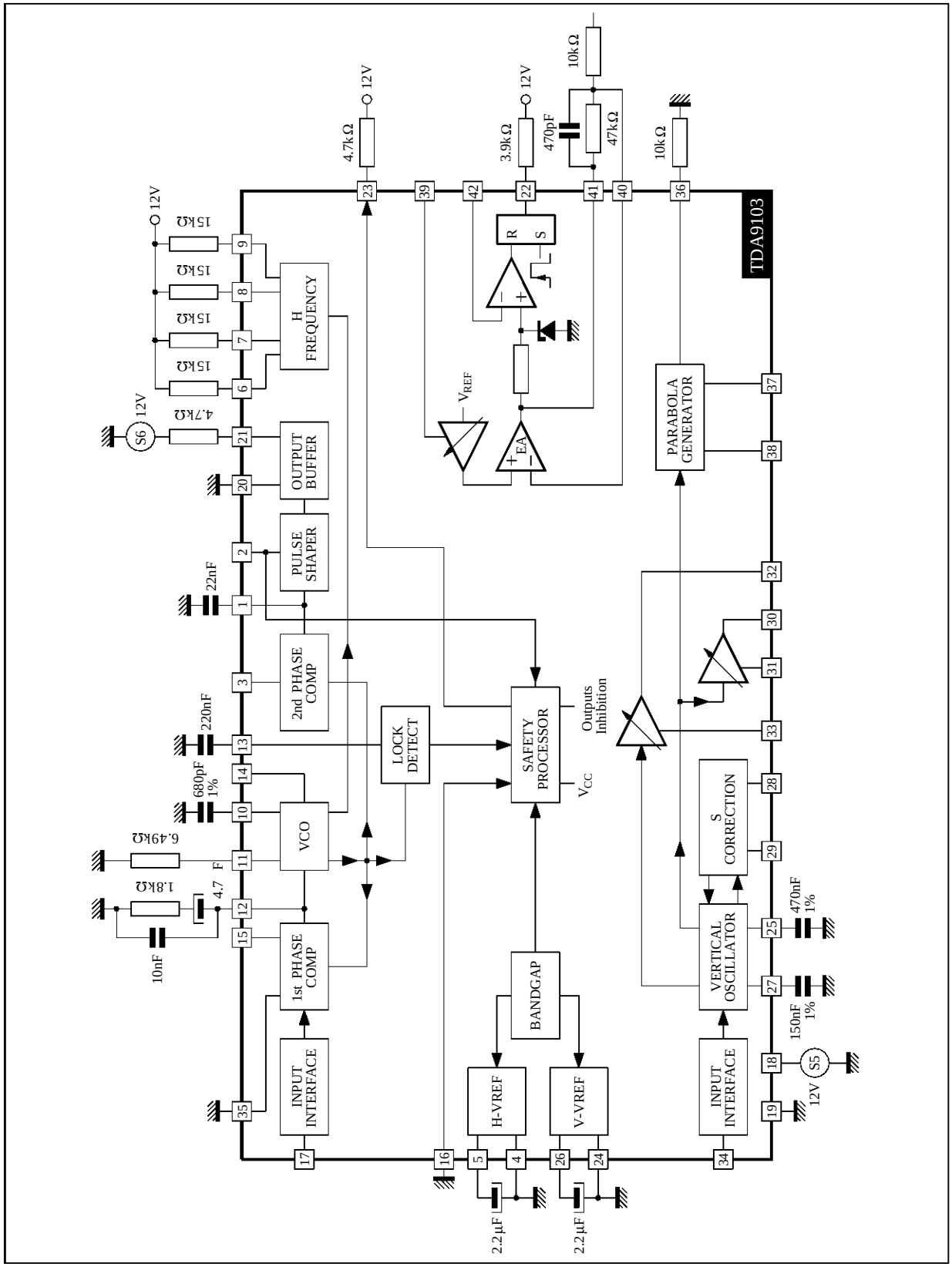

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Figure 2 : Keystone Adjustment

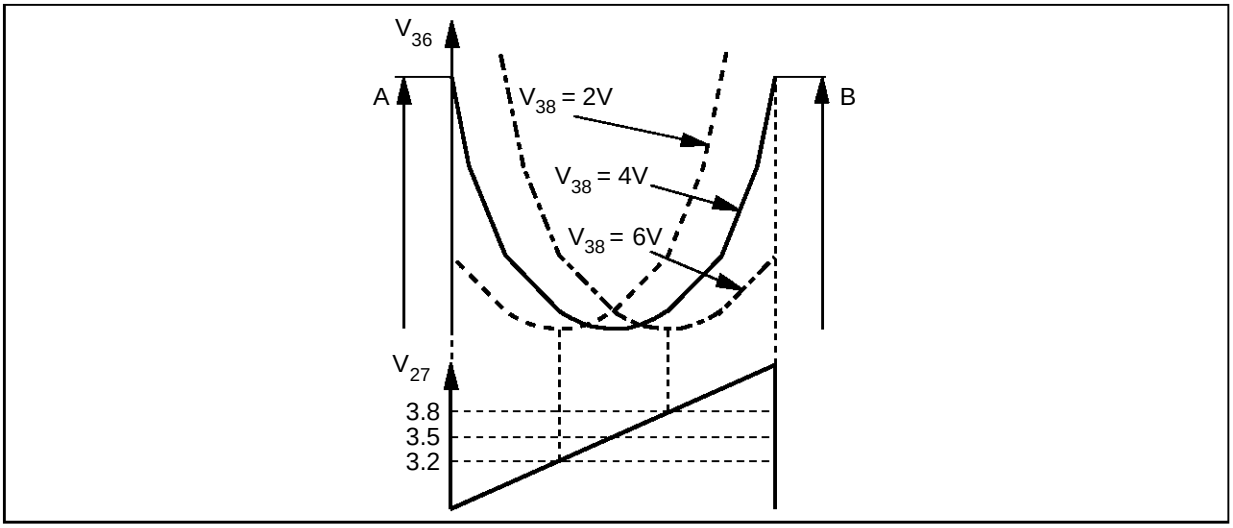


Figure 3 : S Amplitude Adjustment

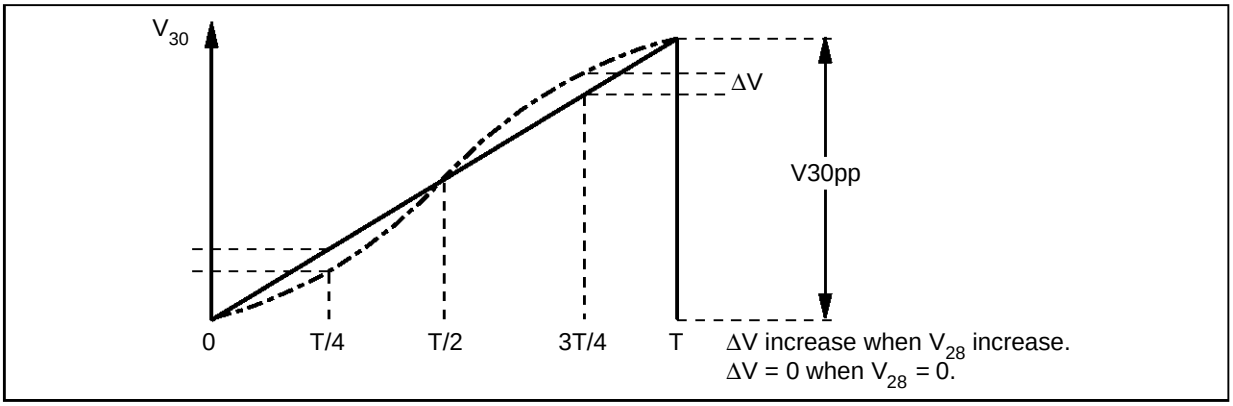
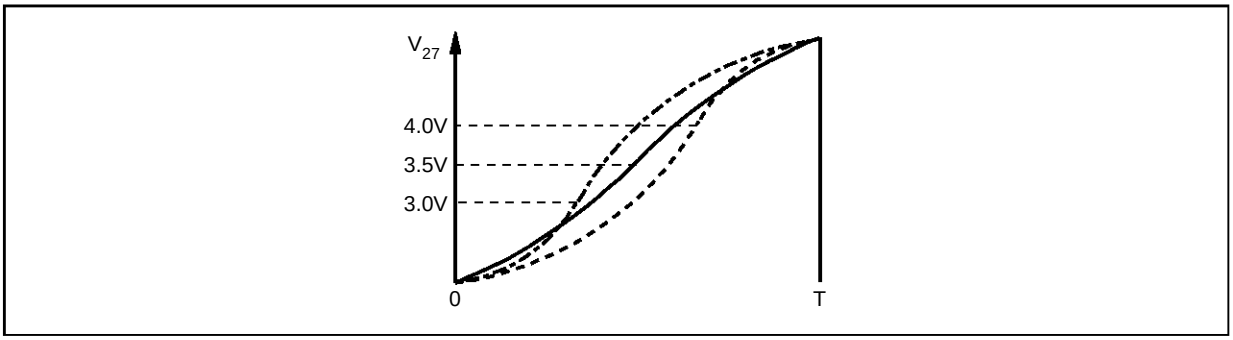


Figure 4 : C Correction Adjustment



OPERATING DESCRIPTION

GENERAL CONSIDERATIONS

Power Supply

The typical value of the power supply voltage V_{CC} is 12V. Perfect operation is obtained if V_{CC} is maintained in the limits : 10.8V $\rightarrow$ 13.2V.

In order to avoid erratic operation of the circuit during the transient phase of V_{CC} switching on, or switching off, the value of V_{CC} is monitored and the outputs of the circuit are inhibited if it is too low.

In order to have a very good power supply rejection, the circuit is internally powered by several internal voltage references (The unique typical value of which is 8V). Two of these voltage references are externally accessible, one for the vertical part and one for the horizontal part. These voltage references can be used for the DC control voltages applied on the concerned pins by the way of potentiometers or digital to analog converters (DAC's). Furthermore it is possible to filter the a.m. voltage references by the use of external capacitor connected to ground, in order to minimize the noise and consequently the "jitter" on vertical and horizontal output signals.

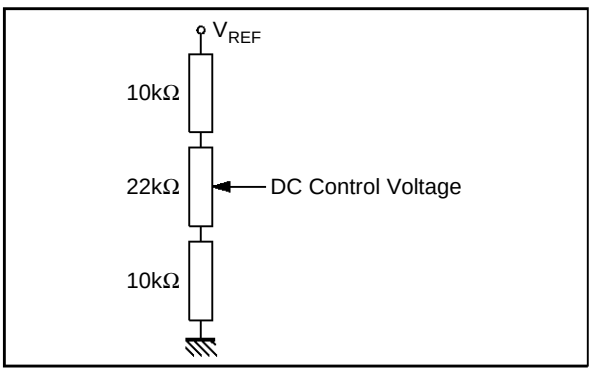
DC Control Adjustments

The circuit has 10 adjustment capabilities : 3 for the horizontal part, 1 for the SMPS part, 2 for the E/W correction, 4 for the vertical part.

The corresponding inputs of the circuit has to be driven with a DC voltage typically comprised between 2 and 6V for a value of the internal voltage reference of 8V.

More precisely, the control voltages have to be maintained between $V_{REF}/4$ and $3/4 \cdot V_{REF}$. The application of control voltages outside this range is not dangerousfor the circuit but the good operation is not guaranted (except for Pin 2 : duty cycle adjusment. See outputs inhibition paragraph).

Figure 5 : Example of Practical DC Control Voltage Generation



The input currents of the DC control inputs are typically very low (about a few µA). Depending on the internal structure of the inputs, the input currents can be positive or negative (sink or source).

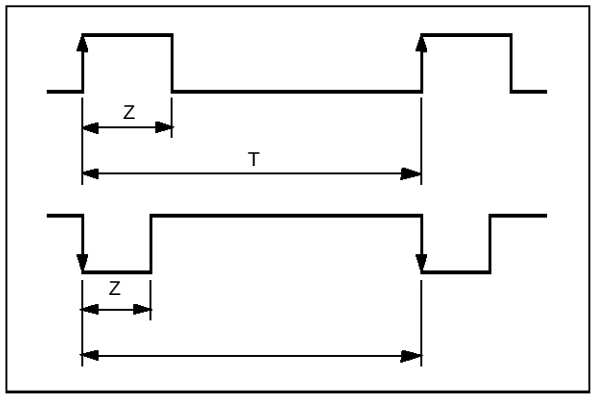
HORIZONTAL PART

Input section

The horizontal input is designed to be sensitive to TTL signals typically comprised between 0 and 5V. The typical threshold of this input is 1.6V. This input stage uses an NPN differential stage and the input current is very low.

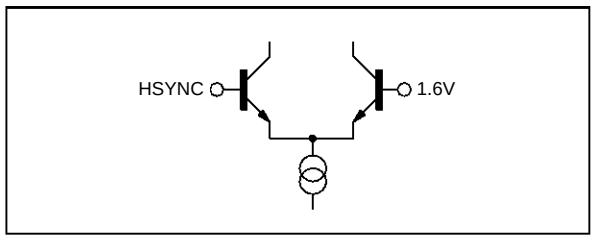
Concerning the duty cycle of the input signal, the following signals may be applied to the circuit.

Figure 6



Using internal integration, both signals are recognized on condition that $Z/T \leq 25\%$. Synchronisation occurs on the leading edge of the rectified signal. The minimum value of Z is 0.7µs.

Figure 7 : Input Structure

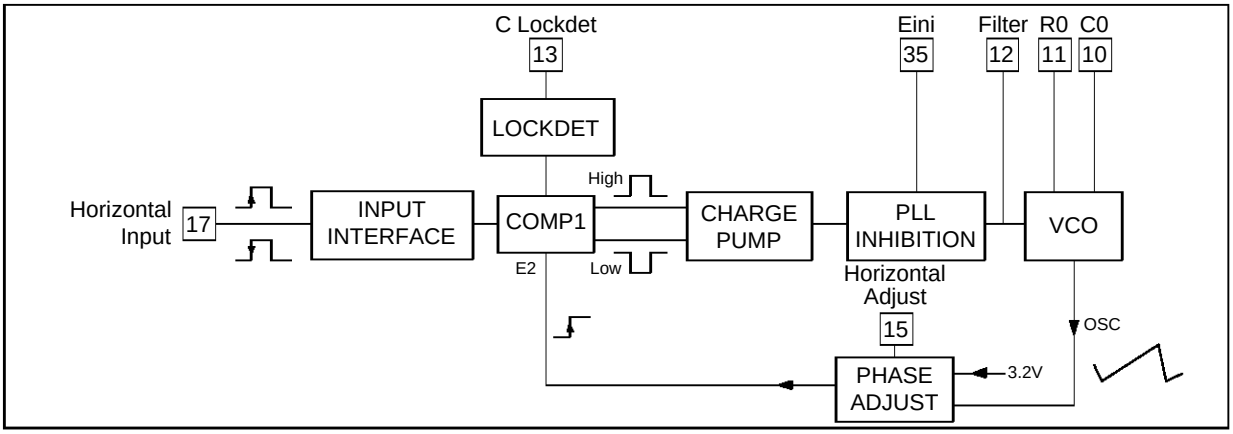


PLL1

The PLL1 is composed of a phase comparator, an external filter and a Voltage Controlled Oscillator (VCO).

The phase comparator is a "phase frequency" type, designed in CMOS technology. This kind of phase detector avoids locking on false frequencies. It is followed by a "charge pump", composed of 2 current sources sink and source (I = 1mA typ.)

Figure 8 : Principle Diagram

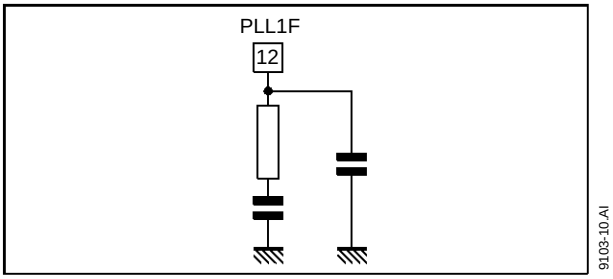


The dynamic behaviour of the PLL is fixed by an external filter which integrates the current of the charge pump. A "CRC" filter is generally used.

PLL1 is inhibited by applying a high level on Pin 35 (PLLinhib) which is a TTL compatible input. The inhibition results from the opening of a switch located between the charge pump and the filter (see Figure 8).

The VCO uses an external RC network. It delivers a linear sawtooth obtained by charge and discharge of the capacitor, by a current proportionnal to the current in the resistor. typical thresholds of sawtooth are 1.6V and 6.4V.

Figure 9



The control voltage of the VCO is typically comprised between 1.6V and 6V. The theoretical frequency range of this VCO is in the ratio 1 → 3.75, but due to spread and thermal drift of external components and the circuit itself, the effective frequency range has to be smaller (e.g. 30kHz → 82kHz). In the absence of synchronisation signal the control voltage is equal to 1.6V typ. and the VCO oscillates on its lowest frequency (free frequency). The synchro frequency has to be always higher than the free frequency and a margin has to be taken. As an example for a synchro range from 30kHz to 82kHz, the suggested free frequency is 27kHz. To compensate for the spread of external components and of the circuit itself, the free frequency may be adjusted by a DC voltage on Pin 14 (Fmin adjust) (see Figure10 for details).

The PLL1 ensures the coincidence between the leading edge of the synchro signal and a phase reference obtained by comparison between the sawtooth of the VCO and an internal DC voltage adjustable between 2.4V and 4V (by Pin 15). So a ±45° phase adjustment is possible.

Figure 10 : Details of VCO and Fhmin Adjustment

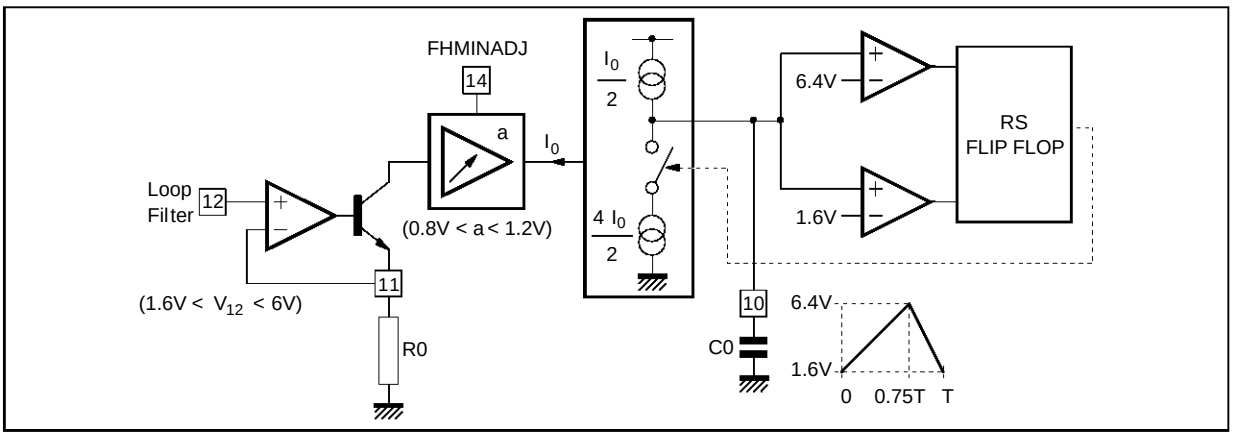


Figure 11 : Safety Functions Block Diagram

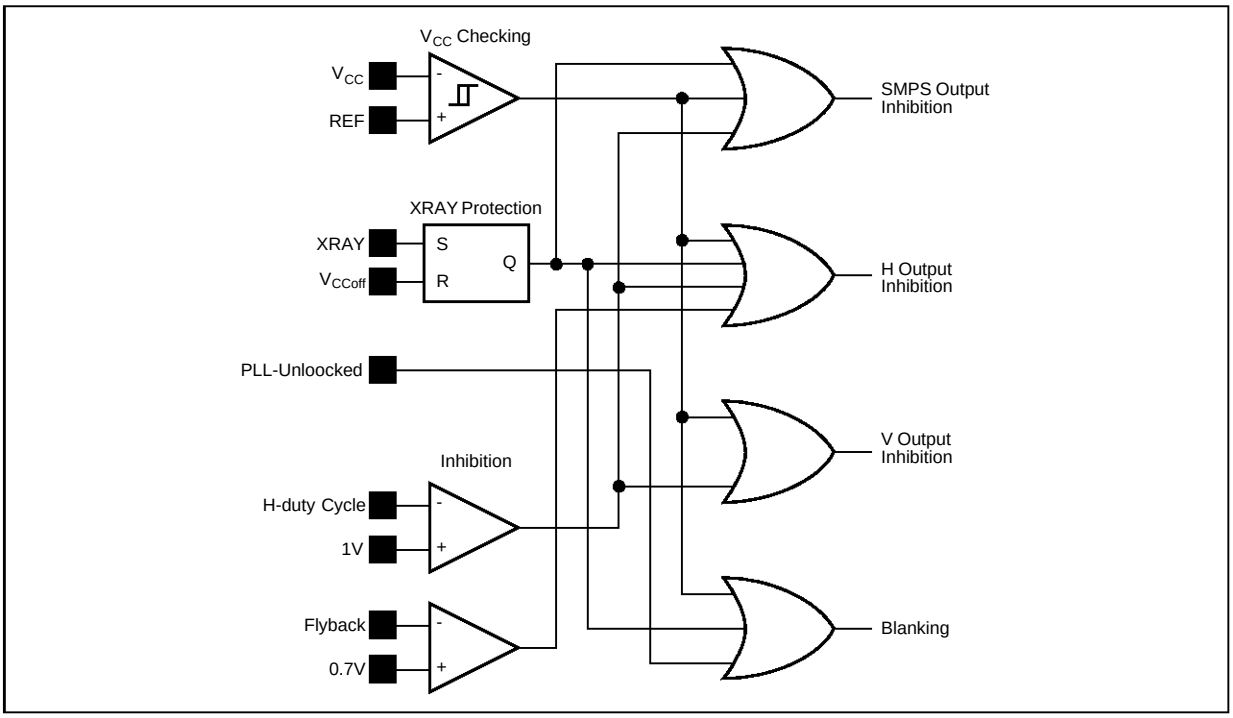
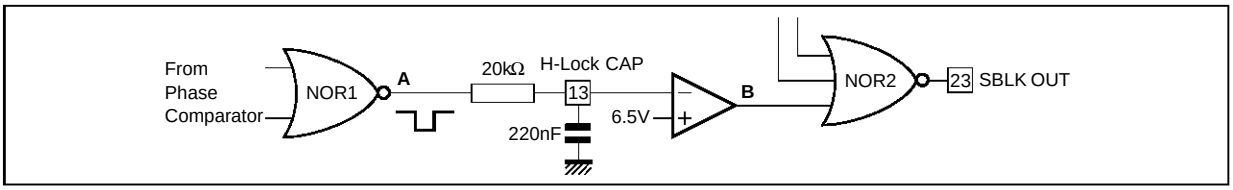


Figure 12 : LOCK/UNLOCK Block Diagram



The TDA9103 also includes a LOCK/UNLOCK identification block which sense in real-time wheather the PLL is locked on the incomming horizontal sync signal or not. The resulting information is available on safety blanking output (Pin 23) where it is mixed with others information (see Figure 11). The block diagram of the LOCK/UNLOCK function is described in Figure 12.

The NOR1 gate is receiving the phase comparator output pulses (which also drives the charge pump). When the PLL is locked, on point **A** there is a very small negative pulse (100ns) at each horizontal cycle, so after R-C filter, there is a high level on Pin 13 which force SBLK to high level (provided other inputs on NOR2 are also at low level).

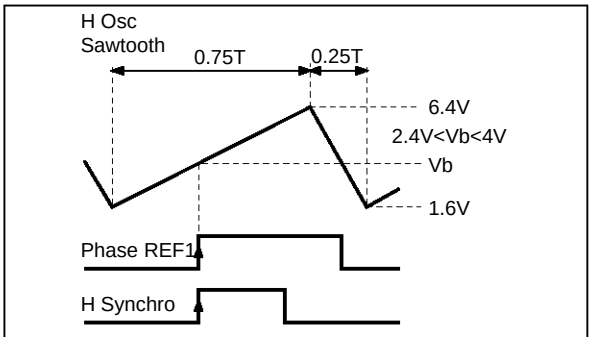
When the PLL is unlocked, the 100ns negative pulse on **A** becomes much larger and consequently the average level on Pin 13 will decrease. When it reaches 6.5V, point **B** goes to high level forcing NOR2 open collector output to "0".

The status of Pin 13 is approximately the following :

- Near 0V when there is no H-SYNC,
- Between 0 and 4V with H-SYNC frequency different from VCO,
- Between 4 and 8V when H-SYNC frequency = VCO frequency but not in phase,
- Near to 8V when PLL is locked.

It is important to notice that Pin 13 is not an output pin and must only be used for filtering purpose (see Figure 12).

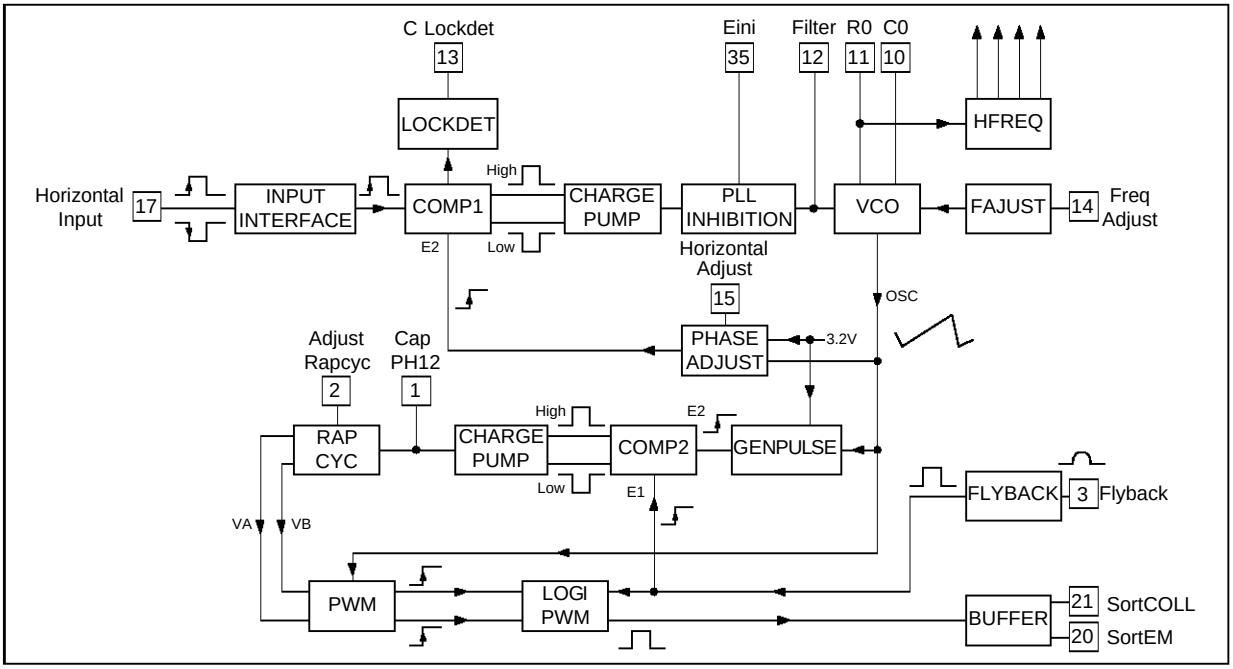
Figure 13 : PLL1 Timing Diagram



Phase REF1 is obtained by comparison between the sawtooth and a DC voltage adjustable between 2.4V and 4V. The PLL1 ensures the exact coincidence between the signals phase REF and HSYNS. A ± 45° phase adjustment is possible.

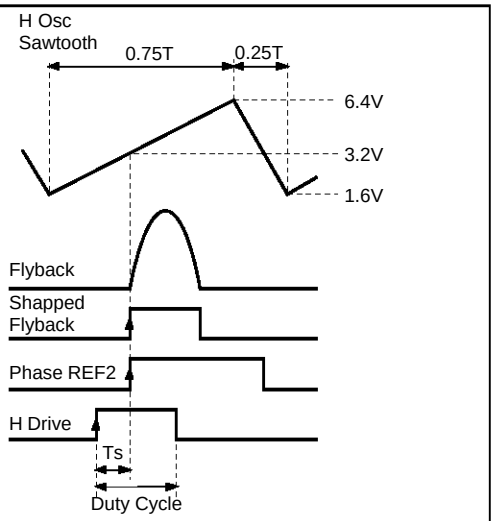
PLL2

Figure 14 : Dual PLL Block Diagram



The PLL2 ensures the coincidence between the leading edge of the shaped flyback signal and a phase reference signal obtained by comparison of the sawtooth of the VCO and a constant DC voltage (3.2V) (see Figure 15).

Figure 15 : PLL2 Timing Diagram

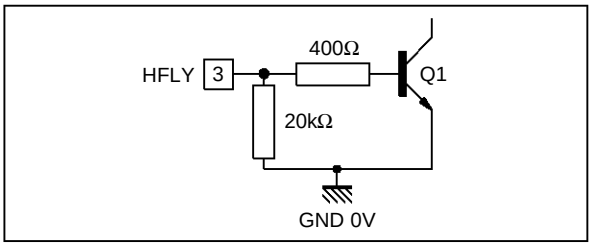


Phase REF2 is obtained by comparison between the sawtooth and a 3.2V (constant). The PLL2 ensures the exact coincidence between the signals phase REF2 and the flyback signal. The duty cycle of H-drive is adjustable between 30% and 50%.

The phase comparator of PLL2 is similar to the one of PLL1, it is followed by a charge pump with a ±0.5mA (typ.) output current.

The flyback input is composed of an NPN transistor. This input has to be current driven. The maximum recommanded input current is 2mA (see Figure 16).

Figure 16 : Flyback Input Electrical Diagram



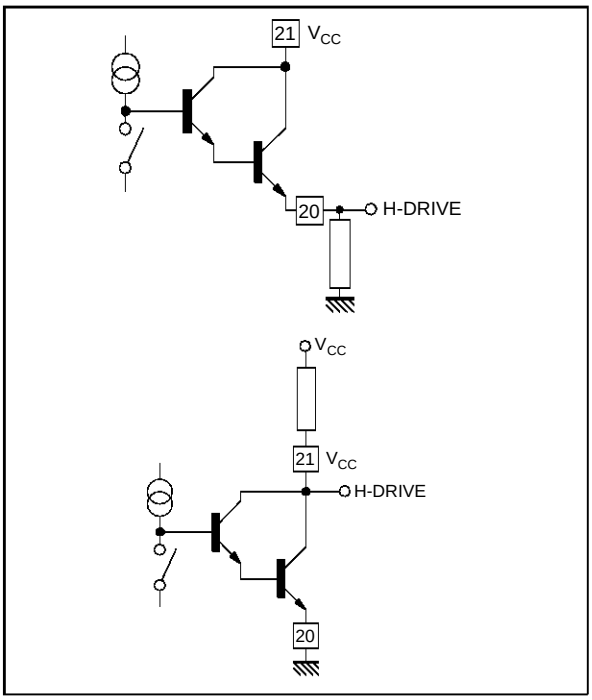
Output Section

The H-drive signal is transmitted to the output through a shaping block ensuring a duty cycle adjustable from 30% to 50%. In order to ensure a reliable operation of the scanning power part, the output is inhibited in the following circumstances :

- V_{CC} too low.
- Xray protection activated.
- During the flyback.
- Output voluntarily inhibited.

The output stage is composed of a Darlington NPN bipolar transistor. Both the collector and the emitter are accessible.

Figure 17 : Output stage simplified diagram, showing the two possibilities of connection



The output Darlington is in off-state when the power scanning transistor is also in off-state.
The maximum output current is 20mA, and the corresponding voltage drop of the output darlington is 1.1V typically.
It is evident that the power scanning transistor cannot be directly driven by the integrated circuit. An interface has to be designed between the circuit and the power transistor which can be of bipolar or MOS type.

Outputs inhibition : the application of a voltage lower than 1V (typ.) on Pin 2 (duty cycle adjust) inhibits the horizontal, vertical and SMPS outputs. This is not memorised.

X-ray protection : the activation of the X-ray protection is obtained by application of a high level on the X-ray input (>1.6V). Consequences of X-ray protection are :
- Inhibition of H drive output.
- Inhibition of SPMS output.
- Activation of safety blanking output.

The reset of this protection is obtained by V_{CC} switch off.

S Correction. S Outputs

In the case where the "S correction" of the horizontal scanning is performed using capacitors, it is necessary to switch capacitors when the frequency changes.

For this the outputs S1, 2, 3 and 4 (Pins 9, 8, 7 and 16) give an indication about the horizontal frequency by monitoring the control voltage of the VCO (Pin 12).

The switching of the S outputs occurs for the following value of the control voltage.

S 1	2V
S 2	2.4V
S 3	3V
S 4	3.7V

The use of comparators with hysteresis avoids erratic switching of the Sout outputs if the control voltage of the VCO remains very close to a switching reference level.

SMPS

This unit generates the supply voltage for the horizontal scanning system. This supply voltage is approximately proportional to the H frequency in order to keep the scanning amplitude constant when the frequency changes. More precisely the amplitude regulation is obtained by detecting and regulating the "flyback" amplitude or EHT value.

The power supply is a step-up converter and it uses the "current-mode" regulation principle.

The power supply works in synchronism with the horizontal scanning. The switching power transistor (external to the TDA9103) is switched on at the beginning of the positive slope of the horizontal sawtooth. It is switched off as required by the integrated regulator. The current in the switching power transistor is monitored and limited, and the ratio Ton/Ton+Toff of the power transistor is limited to 75% typically providing a very good reliability to the power supply.

Figure 18 : SMPS Block Diagram

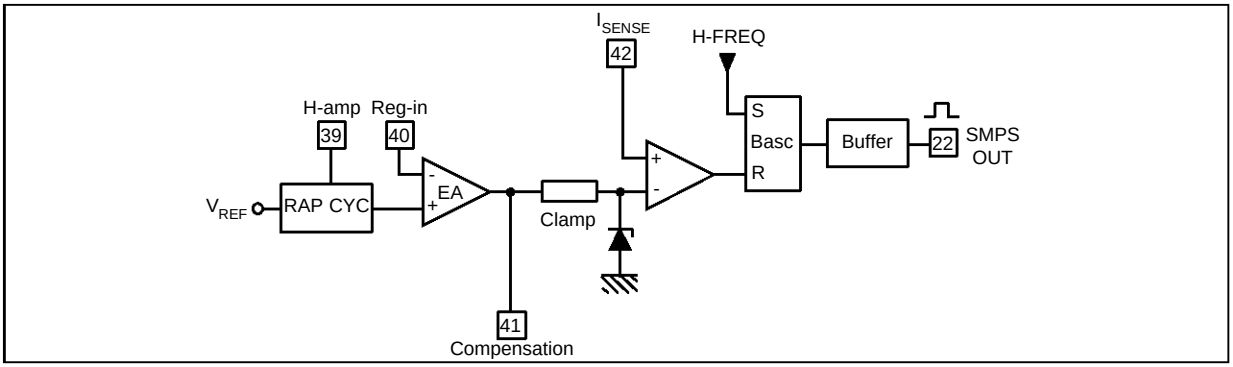


Figure 19 : SMPS Timing Diagram

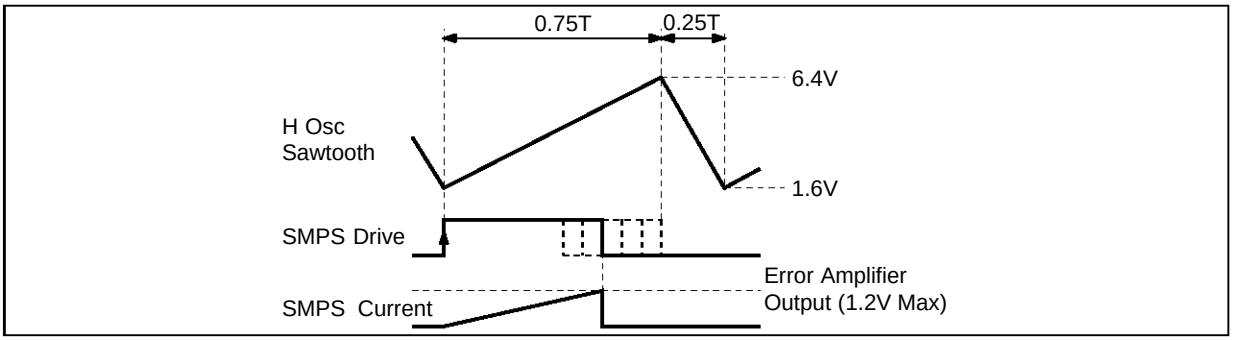
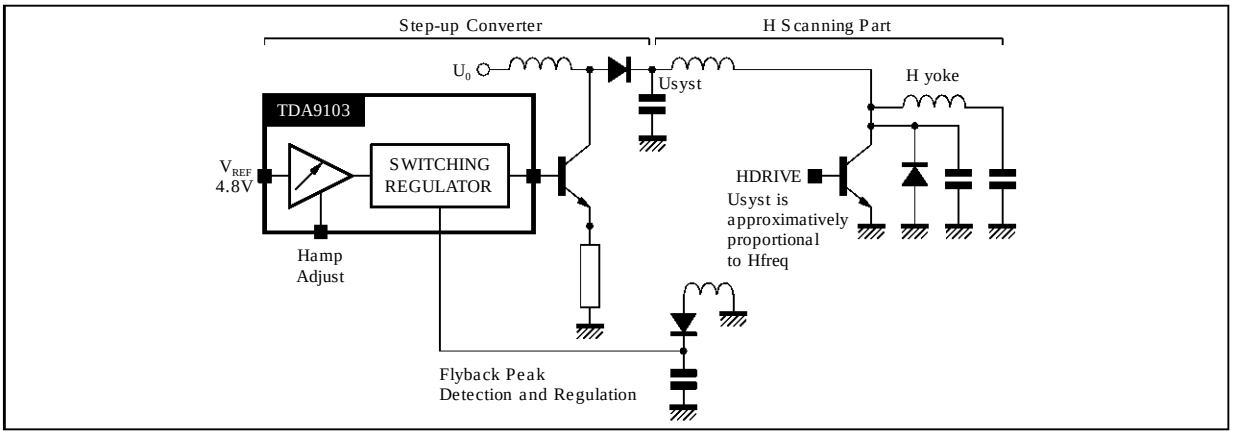


Figure 20 : H Scanning Amplitude Regulation Example



The following functions are implemented in the TDA9103 :

- A DC controlled variable gain amplifier allowing a variation of ±14% of the voltage reference. This is used to set the horizontal image amplitude.
- An error amplifier, the non inverting input of which is connected to the above mentioned adjustable voltage reference. The inverting input and the output of the error amplifier are externally accessible.
- A comparator which determines the conduction of the external transistor by comparing the output voltage of the error amplifier and the voltage applied on Pin 42 (I_{SENSE}), which is the image of the current in the power transistor (current mode principle).
- A flip-flop which memorizes the on or off state of the power transistor.
- An output buffer stage (open collector).

PARABOLA GENERATION FOR EAST-WEST CORRECTION (see Figure 21)

Starting from the vertical ramp a parabola is generated for E/W correction.

The core of the parabola generator is an analog multiplier which generates a current in the form :

$$I = k\ (V_{RAMP} - V_{MID})^2$$

Where V_{RAMP} is the vertical ramp, typically comprised between 2 and 5V, V_{MID} is a DC voltage with a nominal value of 3.5V, but adjustable in the range 3.2V $\rightarrow$ 3.8V in order to generate a dissymmetric parabola if required (keystone adjustment).

The current is converted into voltage through a variable gain transresistance amplifier. The gain, controlled by the voltage on Pin 37 (E/W-AMP) can be adjusted in the ratio 3/1.

The parabola is available on Pin 36 by the way of an emitter follower which has to be biased by an external resistor (10kΩ). It must be AC coupled with external circuitry.

The typical parabola amplitude (AC), with the DC control voltages V_{37} and V_{38} set to 4V, is 2V.

It is important to note that the parasitic parabola during the discharge of the vertical oscillator capacitor is suppressed.

VERTICAL PART (see Figure 22)

The vertical part generates a fixed amplitude ramp which can be affected by a S correction shape. Then, the amplitude of this ramp is adjusted to drive an external power stage.

The internal reference voltage used for the vertical part is available between Pin 26 and Pin 24. It can be used as voltage reference for any DC adjusment to keep a high accuracy to each adjustment. Its typical value is :

$$V_{26} = V_{REF} = 8V.$$

The charge of the external capacitor on Pin 27 (V_{CAP}) generates a fixed amplitude ramp between the internal voltages, V_L ($V_L = V_{REF}/4$) and V_H ($V_H = 5/8 \cdot V_{REF}$).

Figure 21 : Parabola Generation Principle

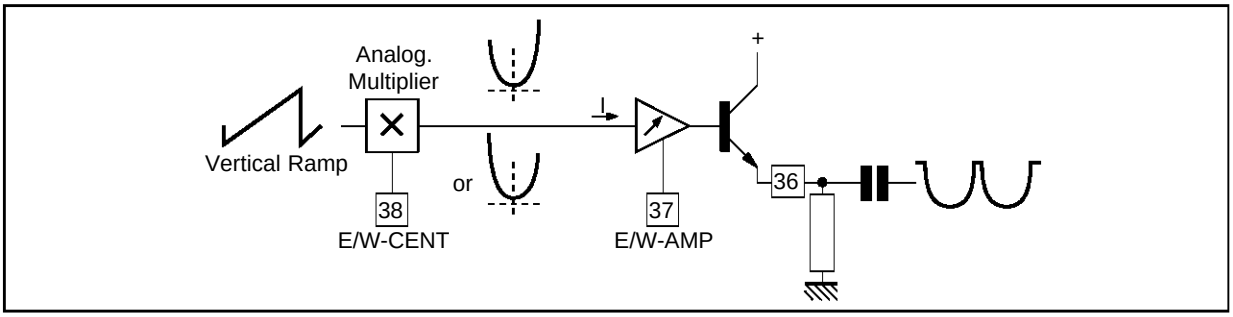
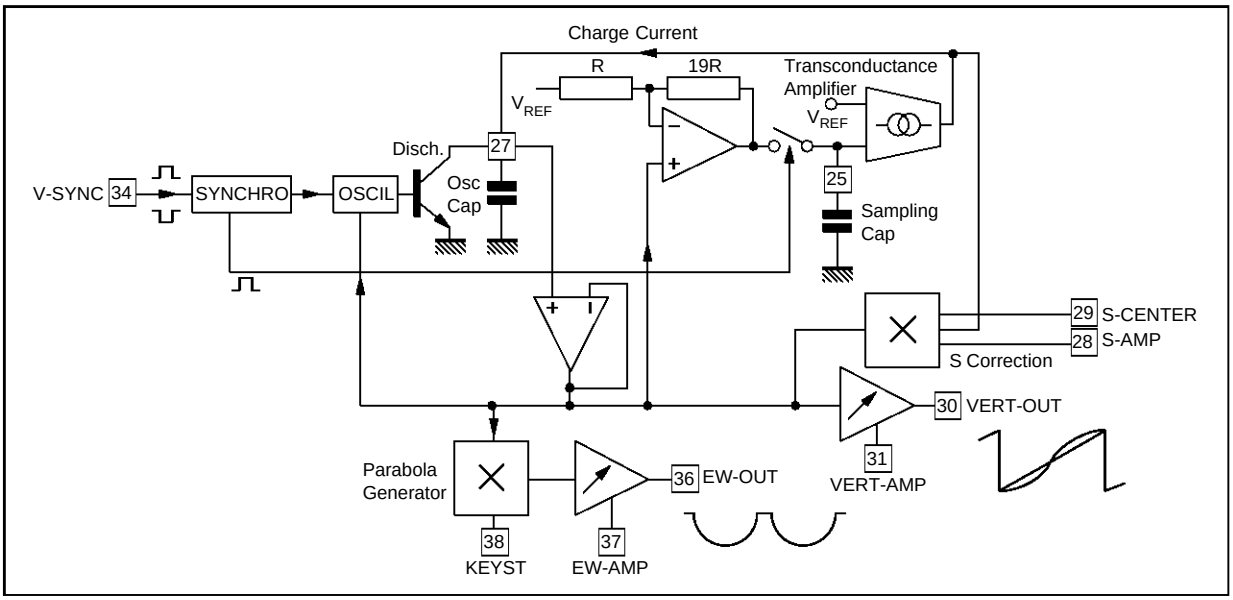


Figure 22 : Vertical Part Block Diagram



Function

When the synchronisation pulse is not present, an internal current source sets the free running frequency. For an external capacitor, C_{OSC} = 180nF, the typical free running frequency is 84Hz.

Typical free running frequency can be calculated by :

$$f_0\ (Hz) = 1.5 \cdot 10^{-5} \cdot \frac{1}{C_{OSC}\ (nF)}$$

A negative or positive TTL level pulse applied on Pin 34 (VSYNC) can synchronise the ramp in the frequency range [fmin, fmax]. This frequency range depends on the external capacitor connected on Pin 27. A capacitor in the range [150nF, 220nF] is recommanded for application in the following range : 50Hz to 120Hz.

Typical maximum and minimum frequency, at 25°C and without any correction (S correction or C correction), can be calculated by :
$f_{max} = 2.5 \cdot f_0$
$f_{min} = 0.33 \cdot f_0$

If S or C corrections are applied, these values are slighty affected.
If an external synchronisation pulse is applied, the internal oscillator is automaticaly caught but the amplitude is no more constant. An internal correction is activated to adjust it in less than half a second: the highest voltage of the ramp on Pin 27 is sampled on the sampling capacitor connected on Pin 25 (VAGCCAP) at each clock pulse and a transconductance amplifier generates the charge current of the capacitor. The ramp amplitude becomes again constant.
It is recommanded to use a AGC capacitor with low leakage current. A value lower than 100nA is mandatory.

DC Control Adjustments

Then, a S correction shape can be added to this ramp. This frequency independent S correction is generated internally; its amplitude is DC adjustable on Pin 28 (V_{SAMP}) and it can be centered to generate C correction, according to the voltage applied on Pin 29 (V_{SCENT}).
It is non effective for V_{SAMP} lower than $V_{REF}/4$ and maximum for $V_{SAMP} = 3/4 \cdot V_{REF}$.

Endly, the amplitude of this S corrected ramp can be adjusted by the voltage applied on Pin 31 (V_{AMP}). The adjusted ramp is available on Pin 30 (V_{OUT}) to drive an external power stage. The gain of this stage is typically ±30% when voltage applied on Pin 31 is in the range $V_{REF}/4$ to $3/4 \cdot V_{REF}$. The DC value of this ramp is kept constant in the frequency range , for any correction applied on it. Its typical value is :

$$V_{DCOUT} = V_{MID} = 7/16 \cdot V_{REF}.$$

A DC voltage is available on Pin 32 (V_{DCOUT}). It is driven by the voltage applied on Pin 33 (V_{POS}). For a voltage control range between $V_{REF}/4$ and $3/4 \cdot V_{REF}$, the voltage available on Pin 32 is :

$$V_{DCOUT} = 7/16 \cdot V_{REF} \pm 300mV.$$

So, the V_{DCOUT} voltage is correlated with DC value of V_{OUT}. It increases the accuracy when temperature varies.

Basic Equations

In first approximation, the amplitude of the ramp on Pin 30 (V_{OUT}) is :

$$V_{OUT} - V_{MID} = (V_{CAP} - V_{MID})\ [1 + 0.16 \cdot (V_{AMP} - V_{REF}/2)]$$

with $V_{MID} = 7/16 \cdot V_{REF}$; typically 3.5V
V_{MID} is the middle value of the ramp on Pin 27
$V_{CAP} = V_{27}$, ramp with fixed amplitude.

On Pin 32 (V_{DCOUT}), the voltage (in volts) is calculated by :

$$V_{DCOUT} = V_{MID} + 0.16 \cdot (V_{POS} - V_{REF}/2).$$

V_{POS} is the voltage applied on Pin 33.

The center of the S correction can be approximatively calculated according to the voltage applied on Pin 29 (V_{SCENT}) :

$$V_{CENTER} = V_{MID} + 0.25 \cdot (V_{SCENT} - V_{REF}/2)$$

This is an internal voltage used to adjust the C correction. The S correction can be adjusted along the ramp according to this parameter. It is ineffective when VSAMP is lower than VREF/4.

The current available on Pin 27
(when $V_{SAMP} = V_{REF}/4$) is :
$I_{OSC} = 3/8 \cdot V_{REF} \cdot C_{OSC} \cdot f$
C_{OSC} : capacitor connected on Pin 27
f synchronisation frequency

The recommanded capacitor value on Pin 25 (V_{AGC}) is 470nF. Its assumes a good stability of the internal closed loop.

INTERNAL SCHEMATICS

Figure 23

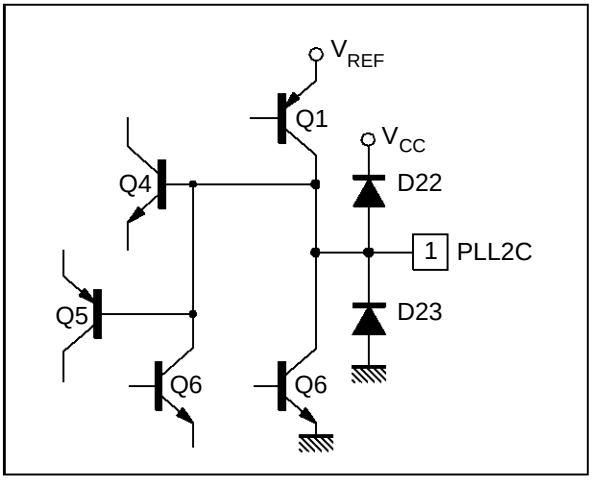


Figure 24

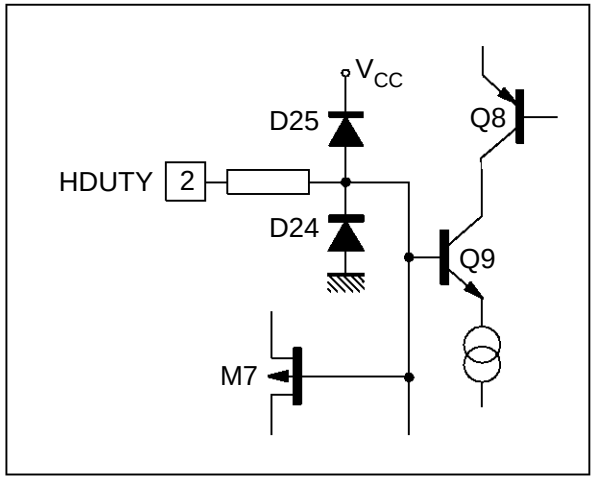


Figure 25

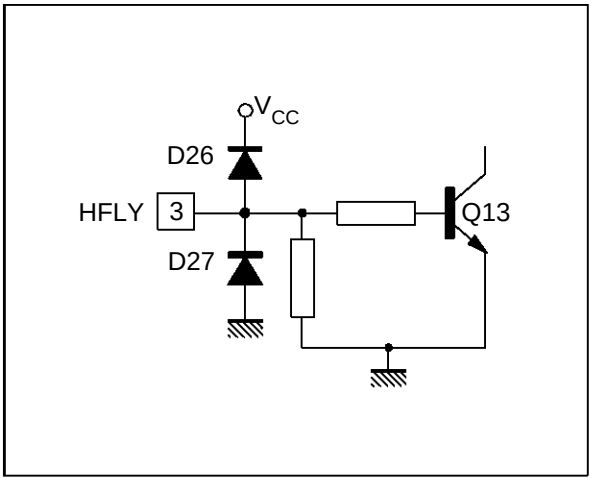


Figure 26

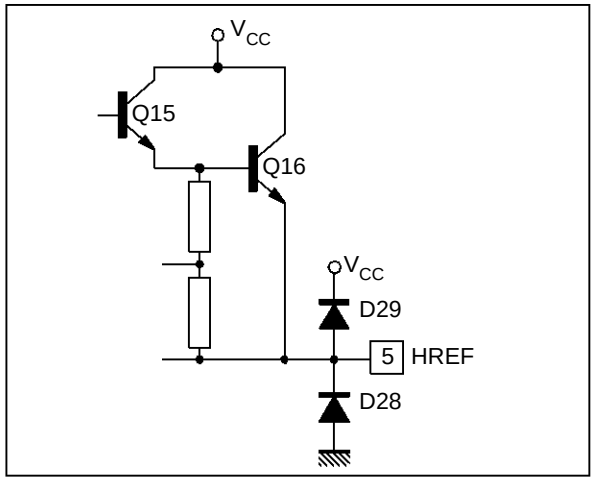


Figure 27

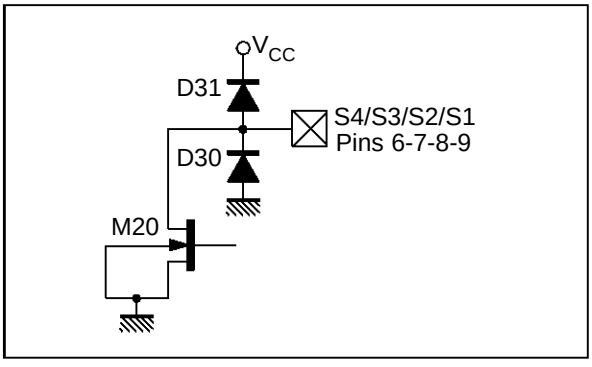
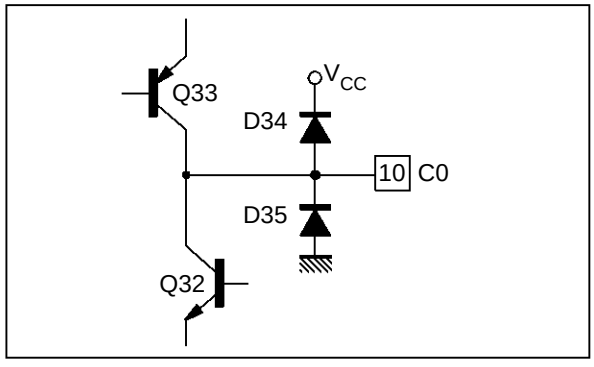


Figure 28



INTERNAL SCHEMATICS (continued)

Figure 29

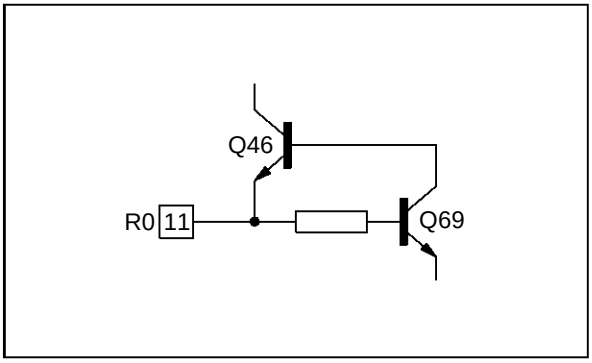


Figure 30

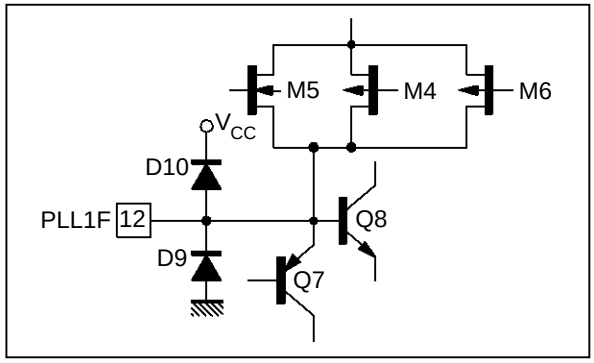


Figure 31

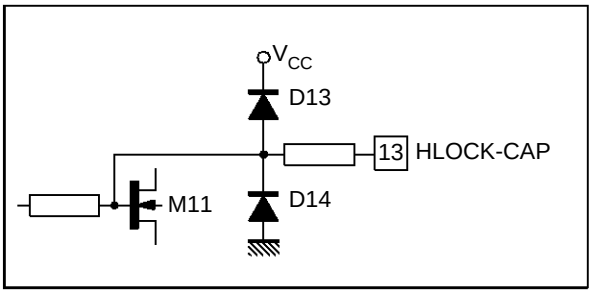


Figure 32

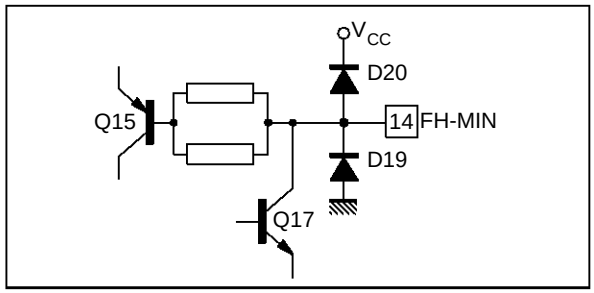


Figure 33

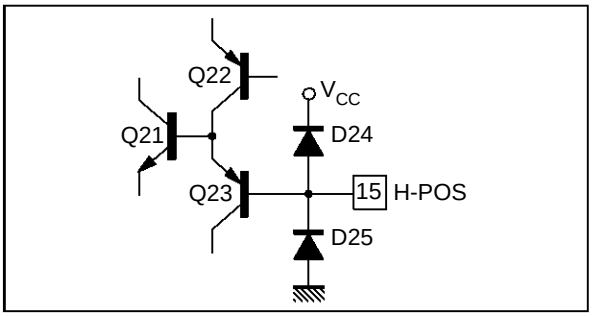


Figure 34

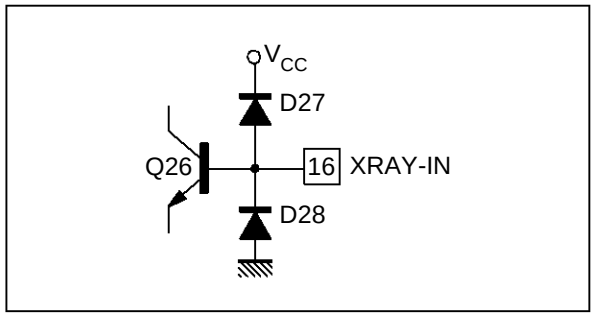


Figure 35

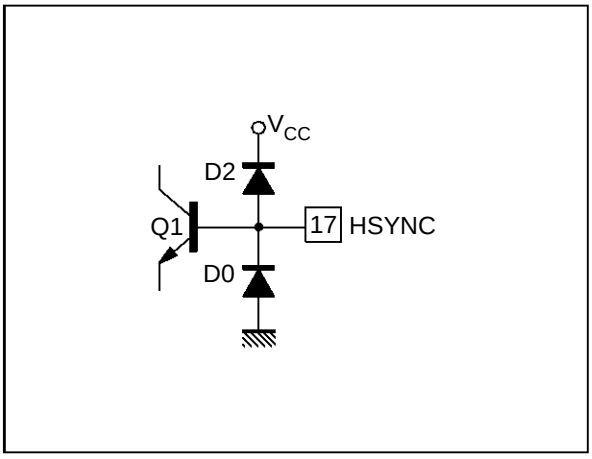
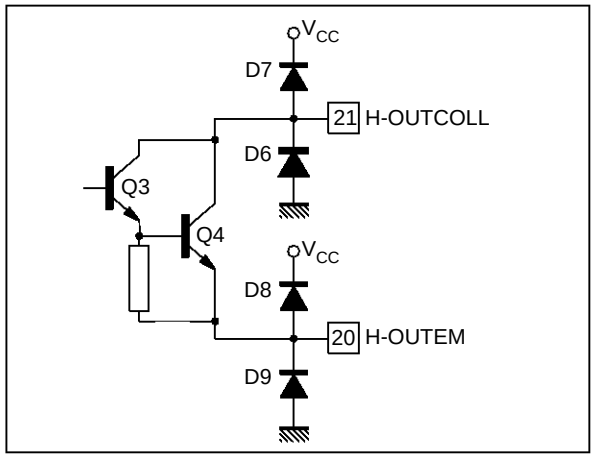


Figure 36



INTERNAL SCHEMATICS (continued)

Figure 37

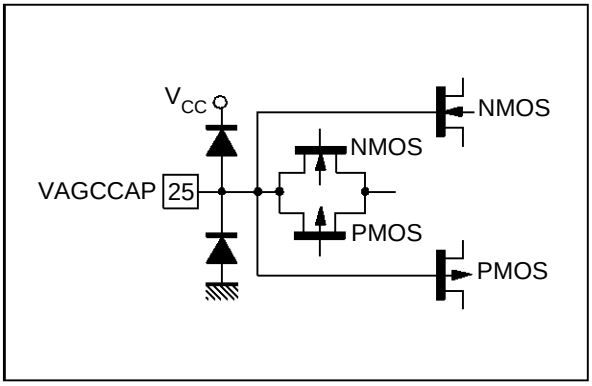


Figure 38

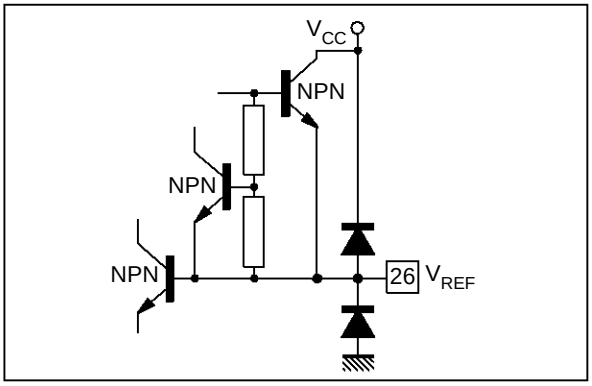


Figure 39

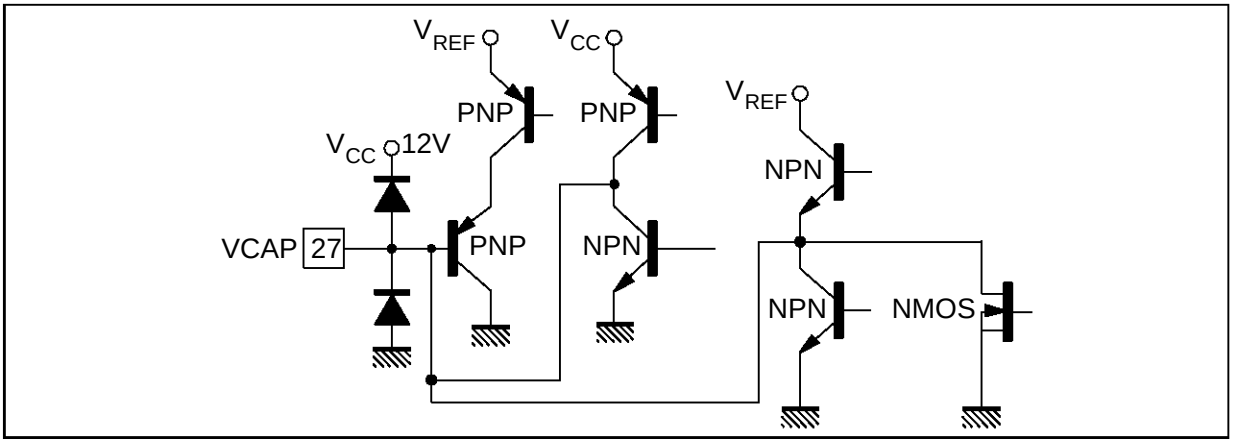


Figure 40

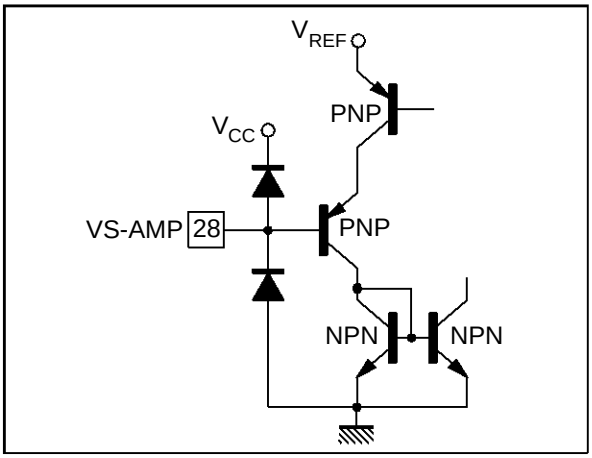
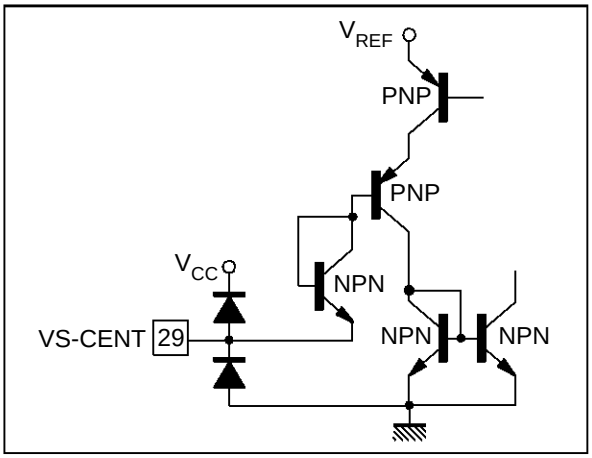


Figure 41



INTERNAL SCHEMATICS (continued)

Figure 42

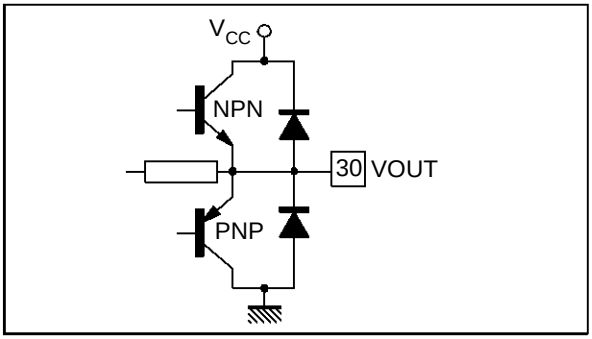


Figure 43

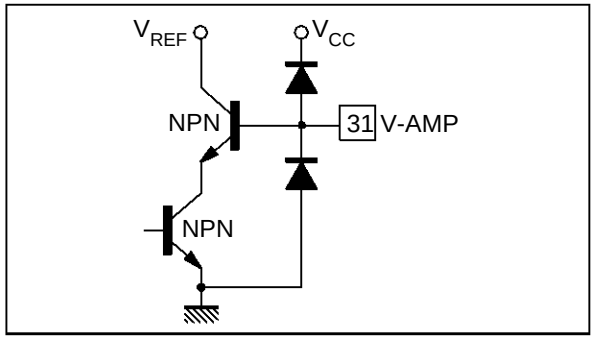


Figure 44

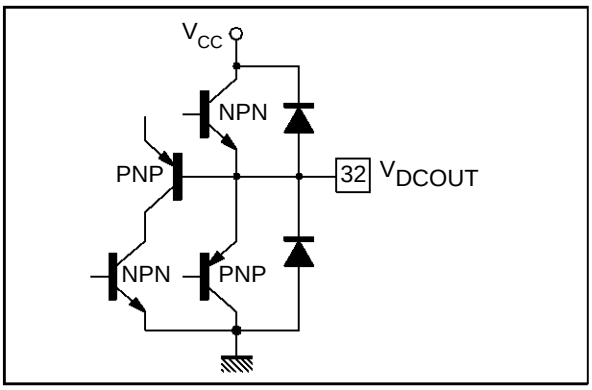


Figure 45

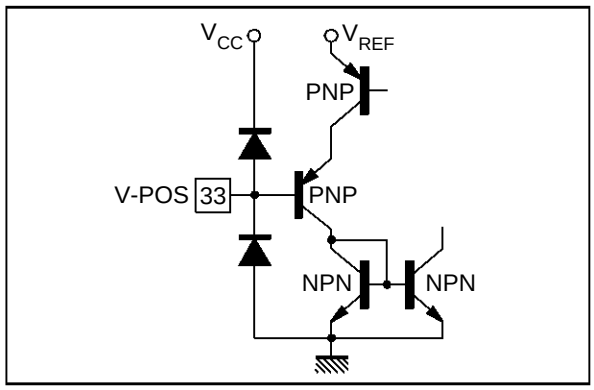


Figure 46

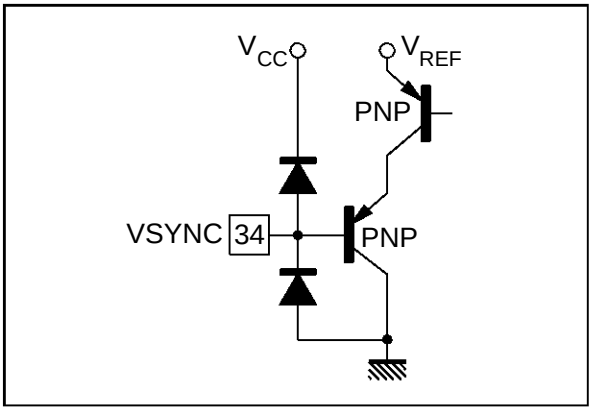
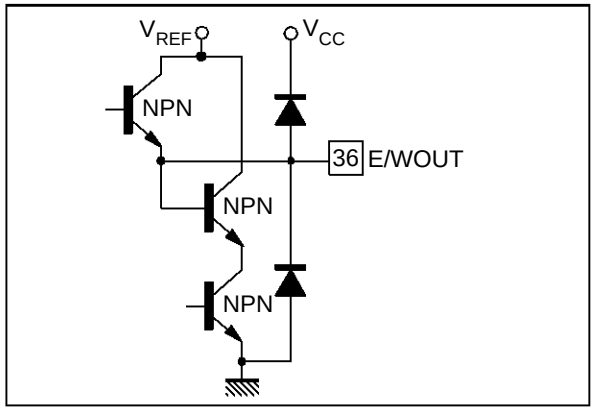


Figure 47



INTERNAL SCHEMATICS (continued)

Figure 48

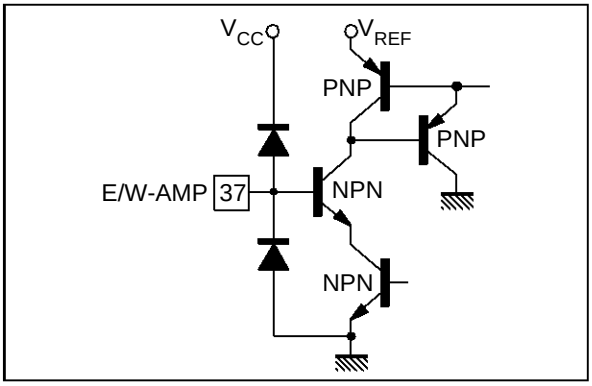


Figure 49

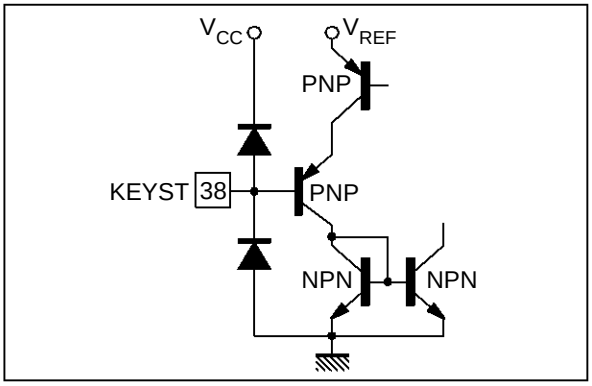


Figure 50

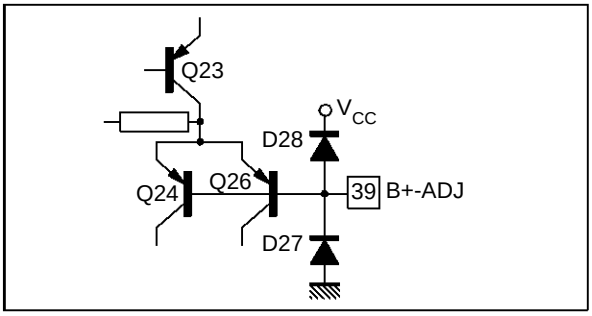


Figure 51

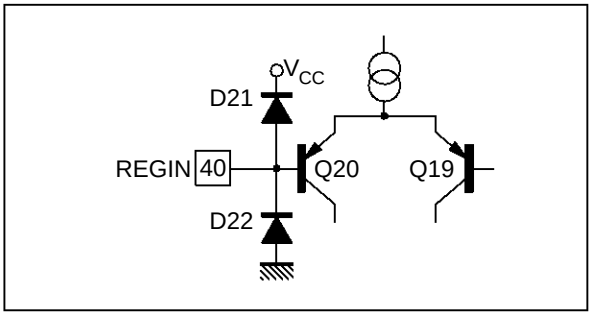


Figure 52

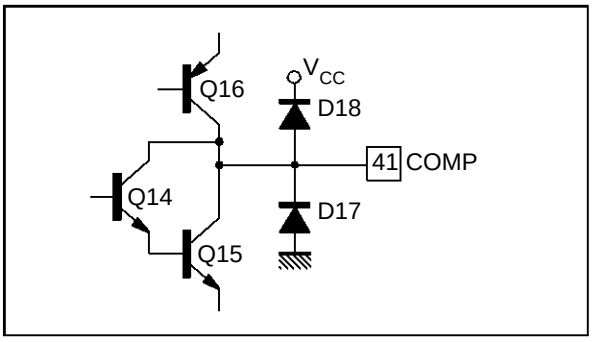
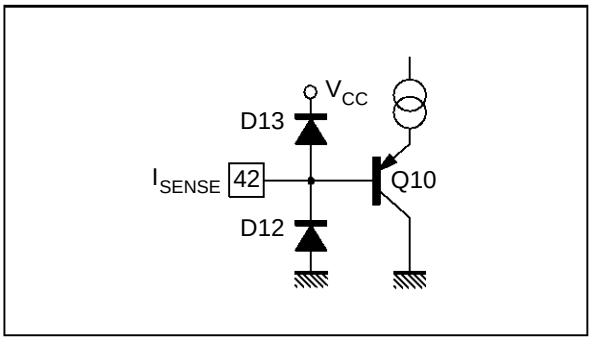
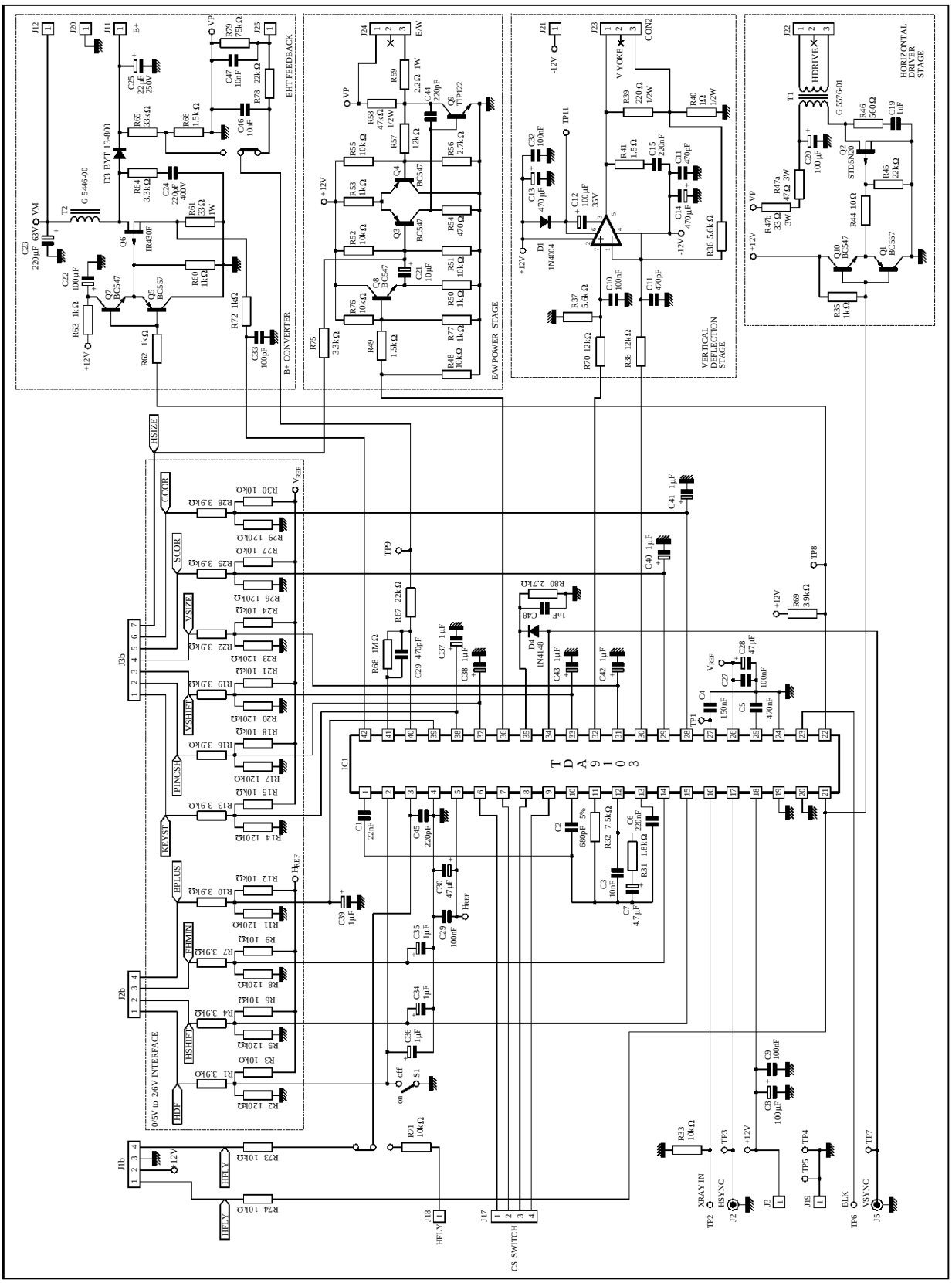


Figure 53



APPLICATION DIAGRAM



A demonstration board has been developped by SGS-THOMSON and is available through your usual SGS-THOMSON office.

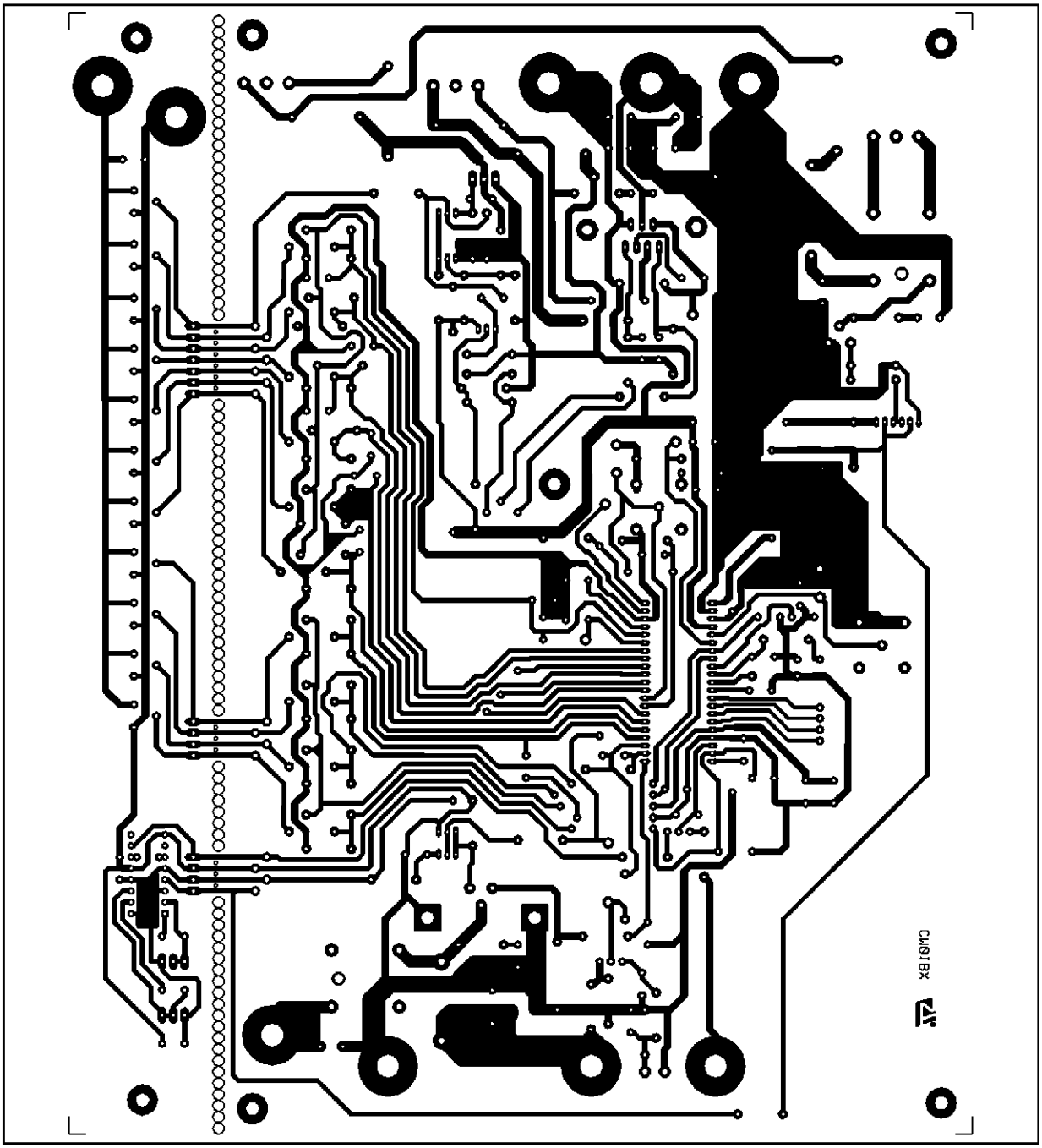
This board has been designed in order to give first the possibility to evaluate the TDA9103 in STAND ALONE, and then to be easily connected to an existing monitor.

In stand alone evaluation, for exemple, flyback simulator is implemented in order to be able to close the 2nd PLL loop, potentiometers are also present to easily adjust all functions.

Then for testing in a real application, the upper part of the board can be detached and the remaining part can be connected to real application.

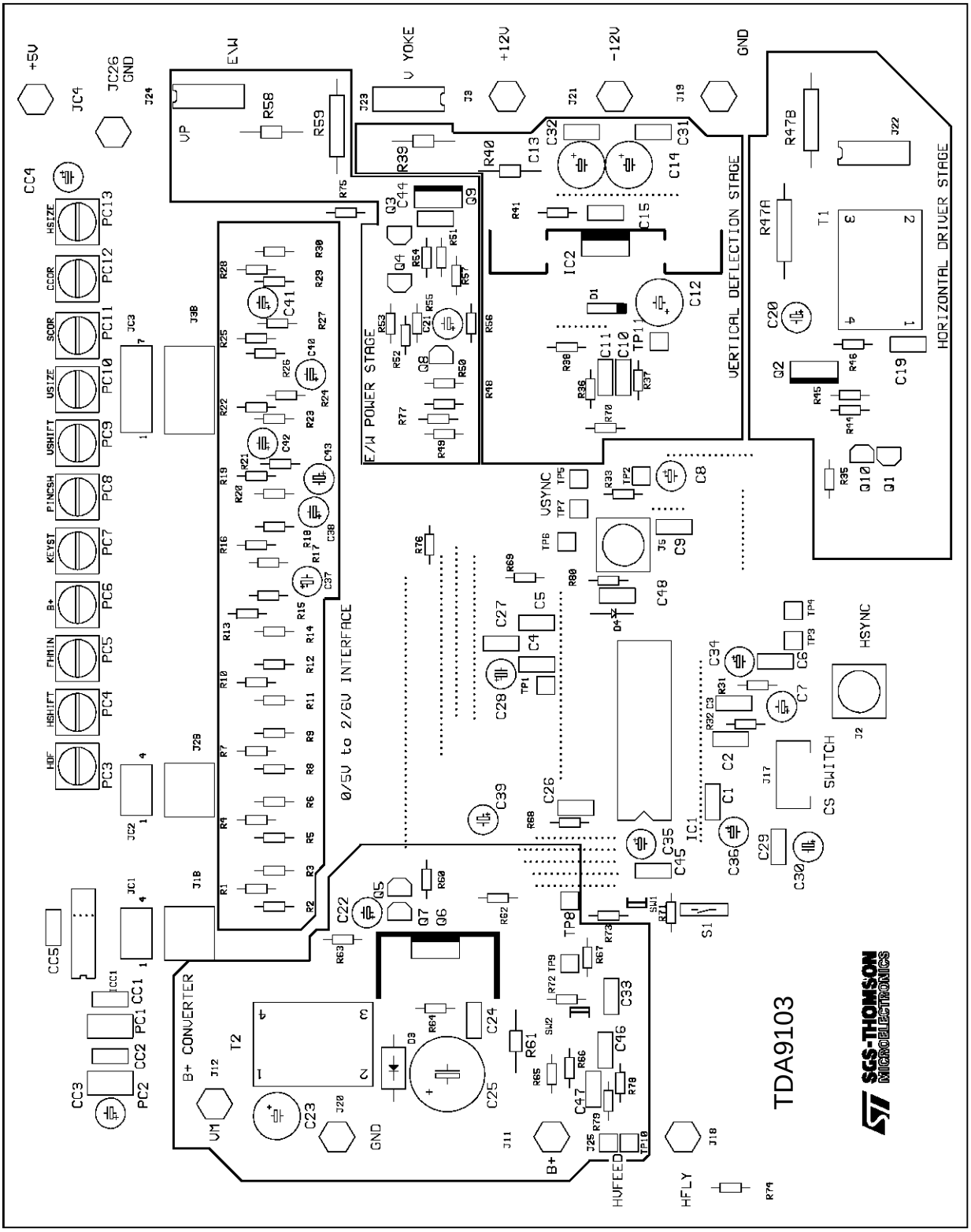
In addition to this, the application board has been volontary designed separating clearly all the blocks. This led to quite large PCB but give much more space for measuring anything on the board.

Figure 54



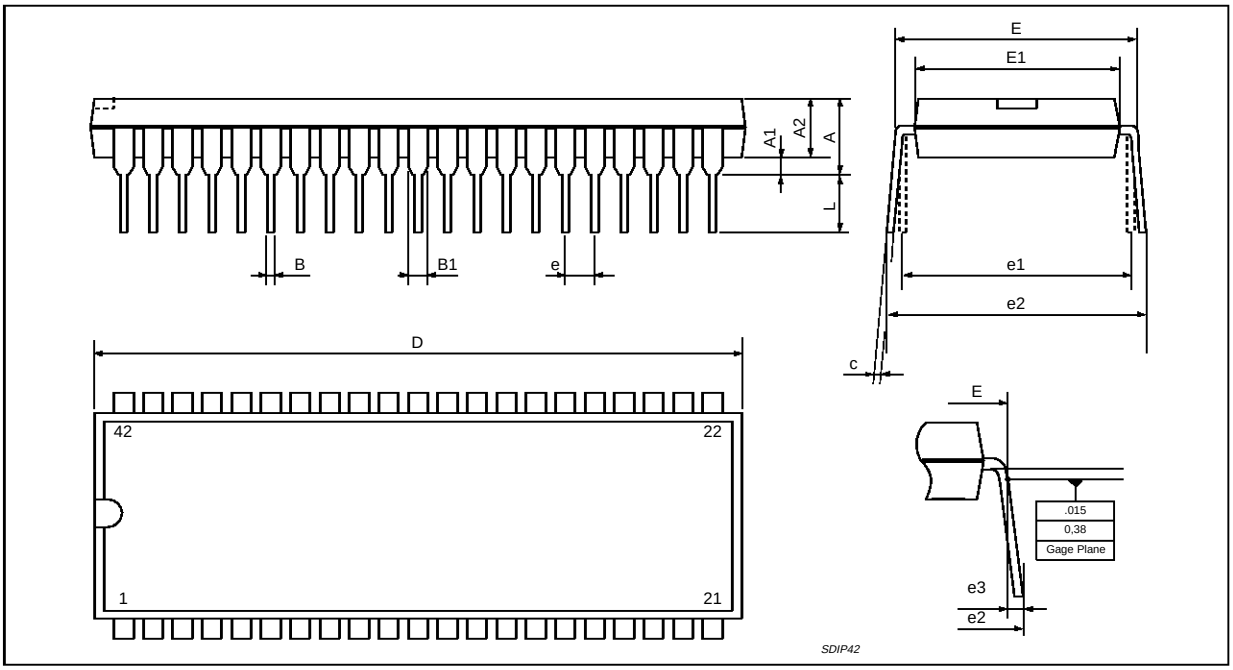
9103-60.TIF

Figure 55


+5V
JC4
JC26
GND
+12V
-12V
GND
E/W
V YOKE
VP
R58
R59
R39
R40
C13
C32
C31
C14
R47B
R47A
T1
C20
C19
Q2
R46
R45
R44
Q10
Q1
R35
VERTICAL DEFLECTION STAGE
HORIZONTAL DRIVER STAGE
E/W POWER STAGE
IC2
C12
C15
D1
C11
C10
TP11
R38
R36
R37
R70
R41
R43
R51
R54
R57
Q4
Q3
C44
Q9
R53
R52
C21
R55
R56
Q8
R50
R48
R49
R77
C41
C40
C42
C43
C38
C37
R18
R17
R16
R15
R14
R13
R12
R11
R10
R9
R8
R7
R6
R5
R4
R3
R2
R1
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
J38
J29
J18
J12
J20
J11
J25
J18
J19
J21
J23
J24
J22
J3
J5
J2
J17
J1
JC3
JC2
JC1
PC13
PC12
PC11
PC10
PC9
PC8
PC7
PC6
PC5
PC4
PC3
PC2
PC1
CC4
CC5
CC3
CC2
CC1
HSIZE
CCOR
SCOR
VSIZE
VSHIFT
PINCSH
KEYST
B+
THMIN
HSHIFT
HDF
VSYNC
HSYNC
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
C8
C9
C48
C5
C4
C27
C28
C26
C39
C22
C24
C25
C23
C33
C46
C47
C45
C35
C34
C6
C7
C2
C1
C36
C29
C30
IC1
CS SWITCH
S1
SW1
SW2
R76
R69
R68
R80
R64
R63
R62
R67
R73
R72
R61
R65
R66
R78
R79
R74
R31
R32
C3
T2
B+ CONVERTER
0/5V to 2/6V INTERFACE
VM
GND
B+
HUFEED
HFLY
TDA9103
SGS-THOMSON
MICROELECTRONICS
9103-61.EPS

PACKAGE MECHANICAL DATA

42 PINS - PLASTIC PACKAGE



PMSDIP42.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.08			0.200
A1	0.51			0.020		
A2	3.05	3.81	4.57	0.120	0.150	0.180
B	0.36	0.46	0.56	0.0142	0.0181	0.0220
B1	0.76	1.02	1.14	0.030	0.040	0.045
c	0.23	0.25	0.38	0.0090	0.0098	0.0150
D	37.85	38.10	38.35	1.490	1.5	1.510
E	15.24		16.00	0.60		0.629
E1	12.70	13.72	14.48	0.50	0.540	0.570
e		1.778			0.070	
e1		15.24			0.60	
e2			18.54			0.730
e3			1.52			0.060
L	2.54	3.30	3.56	0.10	0.130	0.140

SDIP42.TBL