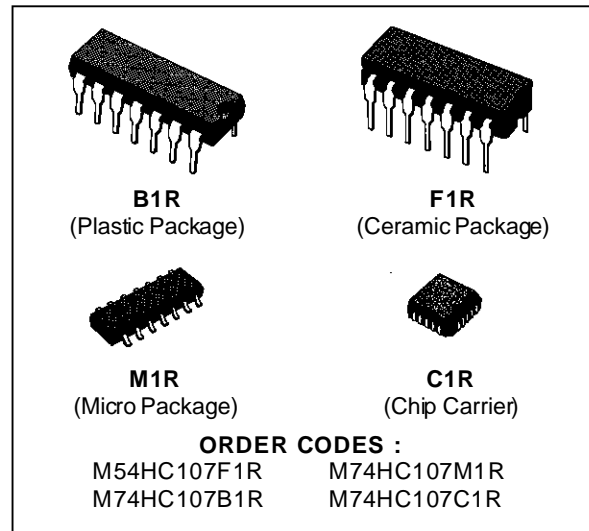


**DUAL J-K FLIP FLOP WITH CLEAR**

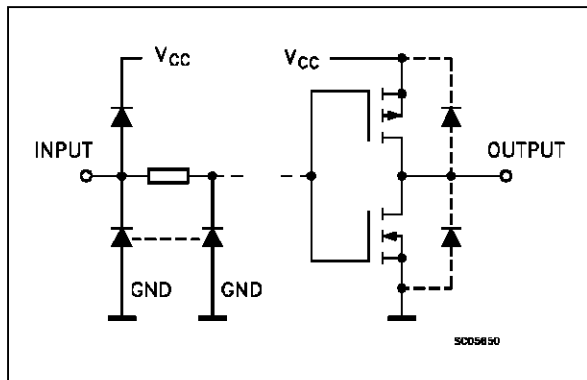
- HIGH SPEED  
f<sub>MAX</sub> = 75 MHz (TYP.) AT V<sub>CC</sub> = 5 V
- LOW POWER DISSIPATION  
I<sub>CC</sub> = 2 μA (MAX.) AT T<sub>A</sub> = 25 °C
- HIGH NOISE IMMUNITY  
V<sub>NIH</sub> = V<sub>NIL</sub> = 28 % V<sub>CC</sub> (MIN.)
- OUTPUT DRIVE CAPABILITY  
10 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE  
|I<sub>OH</sub>| = I<sub>OL</sub> = 4 mA (MIN.)
- BALANCED PROPAGATION DELAYS  
t<sub>PLH</sub> = t<sub>PHL</sub>
- WIDE OPERATING VOLTAGE RANGE  
V<sub>CC</sub> (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE WITH  
54/74LS107



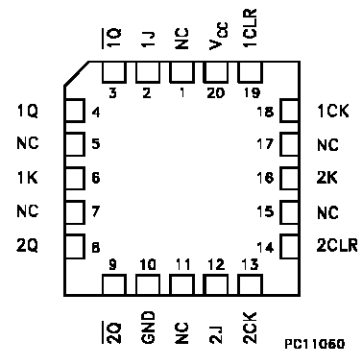
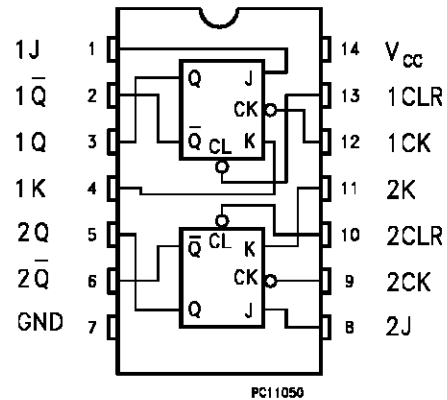
**DESCRIPTION**

The M54/74HC107 is a high speed CMOS DUAL J-K FLIP FLOP fabricated in silicon gate C<sup>2</sup>MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. These flip-flop are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Each one has independent J, K, CLOCK, and CLEAR input and Q and Q outputs. CLEAR is independent of the clock and accomplished by a logic low on the input. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

**INPUT AND OUTPUT EQUIVALENT CIRCUIT**



**PIN CONNECTIONS (top view)**



NC =  
No Internal  
Connection

# M54/M74HC107

## TRUTH TABLE

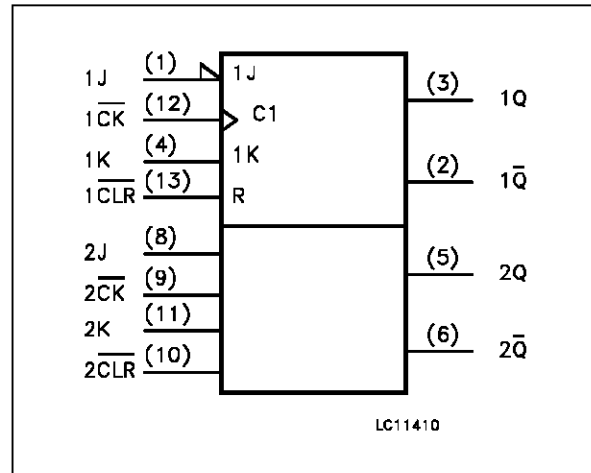
INPUTS				OUTPUTS		FUNCTION
CLR	J	K	CK	Q	$\bar{Q}$	
L	X	X	X	L	H	CLEAR
H	L	L	$\bar{\square}$	$Q_n$	$\bar{Q}_n$	NO CHANGE
H	L	H	$\bar{\square}$	L	H	
H	H	L	$\bar{\square}$	H	L	
H	H	H	$\bar{\square}$	$\bar{Q}_n$	$Q_n$	TOGGLE
H	X	X	$\square$	$Q_n$	$\bar{Q}_n$	NO CHANGE

X: Don't Care

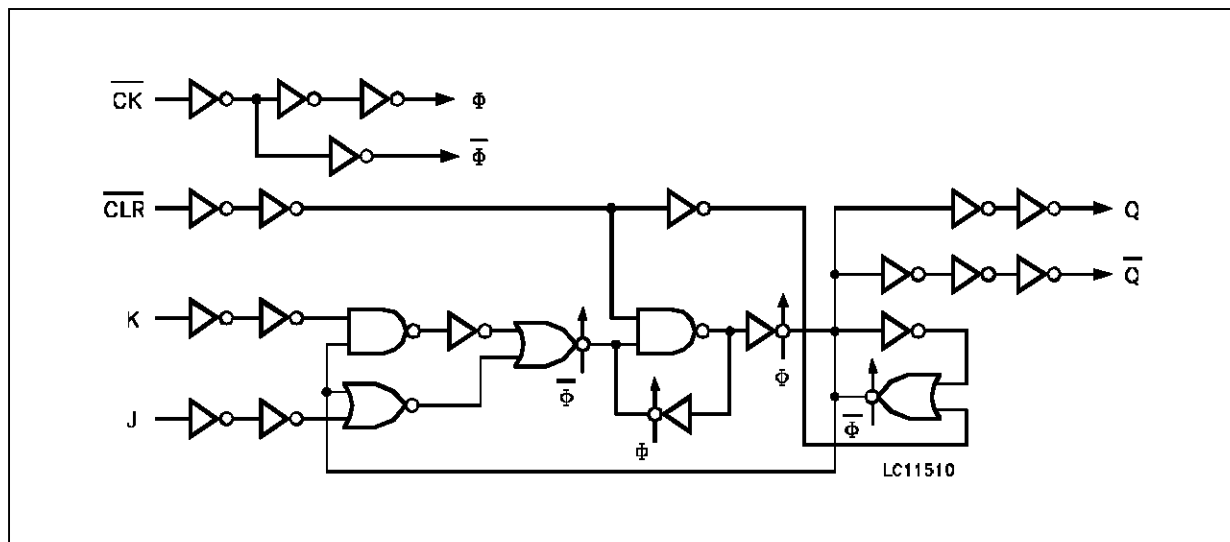
## PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1, 8, 4, 11	1J, 2J, 1K, 2K	Synchronous Inputs; Flip-Flop 1 And 2
2, 6	$1\bar{Q}$ , $2\bar{Q}$	Complement Flip-Flop Outputs
3, 5	1Q, 2Q	True Flip-Flop Outputs
12, 9	1CK, 2CK	Clock Input
13, 10	1CLR, 2CLR	Asynchronous Reset Inputs
7	GND	Ground (0V)
14	V <sub>CC</sub>	Positive Supply Voltage

## IEC LOGIC SYMBOL



## LOGIC DIAGRAM (1/2 Package)



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	-0.5 to +7	V
V <sub>I</sub>	DC Input Voltage	-0.5 to V <sub>DD</sub> + 0.5	V
V <sub>O</sub>	DC Output Voltage	-0.5 to V <sub>DD</sub> + 0.5	V
I <sub>IK</sub>	DC Input Diode Current	± 20	mA
I <sub>OK</sub>	DC Output Diode Current	± 20	mA
I <sub>O</sub>	DC Output Source Sink Current Per Output Pin	± 25	mA
I <sub>CC</sub> or I <sub>GND</sub>	DC V <sub>CC</sub> or Ground Current	± 50	mA
P <sub>D</sub>	Power Dissipation	500 (*)	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(\*) 500 mW: ≅ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit	
V <sub>CC</sub>	Supply Voltage	2 to 6	V	
V <sub>I</sub>	Input Voltage	0 to V <sub>CC</sub>	V	
V <sub>O</sub>	Output Voltage	0 to V <sub>CC</sub>	V	
T <sub>op</sub>	Operating Temperature: <b>M54HC Series</b> <b>M74HC Series</b>	-55 to +125 -40 to +85	°C °C	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time	V <sub>CC</sub> = 2 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6 V	0 to 1000 0 to 500 0 to 400	ns

**DC SPECIFICATIONS**

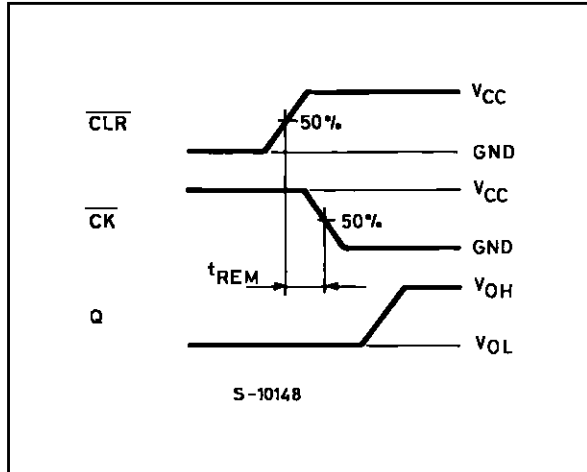
Symbol	Parameter	Test Conditions		Value						Unit		
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC			
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.	
V <sub>IH</sub>	High Level Input Voltage	2.0		1.5			1.5		1.5		V	
		4.5		3.15			3.15		3.15			
		6.0		4.2			4.2		4.2			
V <sub>IL</sub>	Low Level Input Voltage	2.0				0.5		0.5		0.5	V	
		4.5				1.35		1.35		1.35		
		6.0				1.8		1.8		1.8		
V <sub>OH</sub>	High Level Output Voltage	2.0	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = -20 μA	1.9	2.0		1.9		1.9	V	
		4.5			4.4	4.5		4.4		4.4		
		6.0			5.9	6.0		5.9		5.9		
		4.5	I <sub>O</sub> = -4.0 mA	4.18	4.31		4.13		4.10			
		6.0		I <sub>O</sub> = -5.2 mA	5.68	5.8		5.63		5.60		
V <sub>OL</sub>	Low Level Output Voltage	2.0	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 μA		0.0	0.1		0.1		0.1	V
		4.5				0.0	0.1		0.1		0.1	
		6.0				0.0	0.1		0.1		0.1	
		4.5		I <sub>O</sub> = 4.0 mA	0.17	0.26		0.33		0.40		
		6.0			I <sub>O</sub> = 5.2 mA	0.18	0.26		0.33		0.40	
I <sub>I</sub>	Input Leakage Current	6.0	V <sub>I</sub> = V <sub>CC</sub> or GND			±0.1		±1		±1	μA	
I <sub>CC</sub>	Quiescent Supply Current	6.0	V <sub>I</sub> = V <sub>CC</sub> or GND			2		20		40	μA	

AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$  pF, Input  $t_r = t_f = 6$  ns)

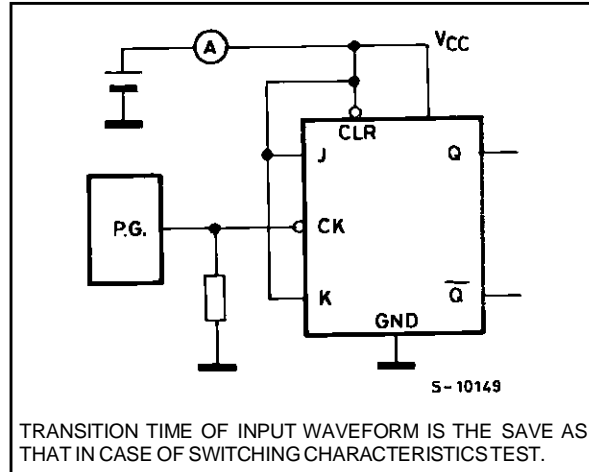
Symbol	Parameter	Test Conditions		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t <sub>TLH</sub> t <sub>THL</sub>	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (CK - Q, $\bar{Q}$ )	2.0			48	125		155		190	ns
		4.5			14	25		31		38	
		6.0			12	21		26		32	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (CLR - Q, $\bar{Q}$ )	2.0			52	140		175		210	ns
		4.5			15	28		35		42	
		6.0			13	24		30		36	
f <sub>MAX</sub>	Maximum Clock Frequency	2.0		6.2	23		5.0		4.2		MHz
		4.5		31	70		25		21		
		6.0		37	80		30		25		
t <sub>W(H)</sub> t <sub>W(L)</sub>	Minimum Pulse Width (CLOCK)	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	
t <sub>W(L)</sub>	Minimum Pulse Width (CLR)	2.0			20	75		95		110	ns
		4.5			5	15		19		22	
		6.0			4	13		16		19	
t <sub>s</sub>	Minimum Set-up Time	2.0			28	75		95		110	ns
		4.5			7	15		19		22	
		6.0			6	13		16		19	
t <sub>h</sub>	Minimum Hold Time	2.0				0		0		0	ns
		4.5				0		0		0	
		6.0				0		0		0	
t <sub>REM</sub>	Minimum Removal Time (CLR)	2.0				25		30		40	ns
		4.5				5		6		8	
		6.0				5		5		7	
C <sub>IN</sub>	Input Capacitance				5	10		10		10	pF
C <sub>PD</sub> (*)	Power Dissipation Capacitance				32						pF

(\*) C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$  (per FLIP/FLOP)

SWITCHING CHARACTERISTICS TEST

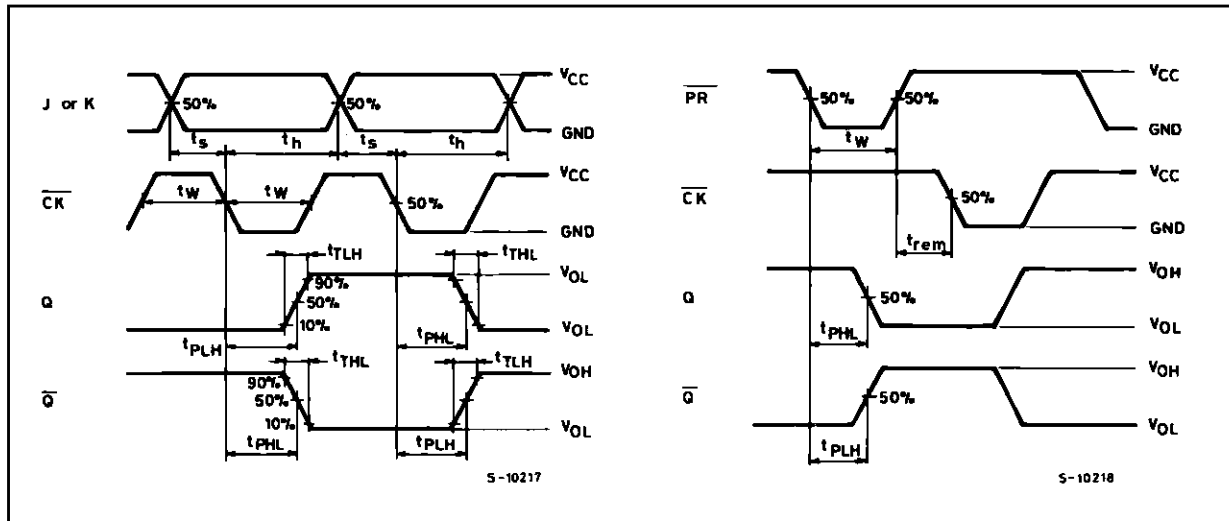


TEST CIRCUIT  $I_{CC}$  (Opr.)



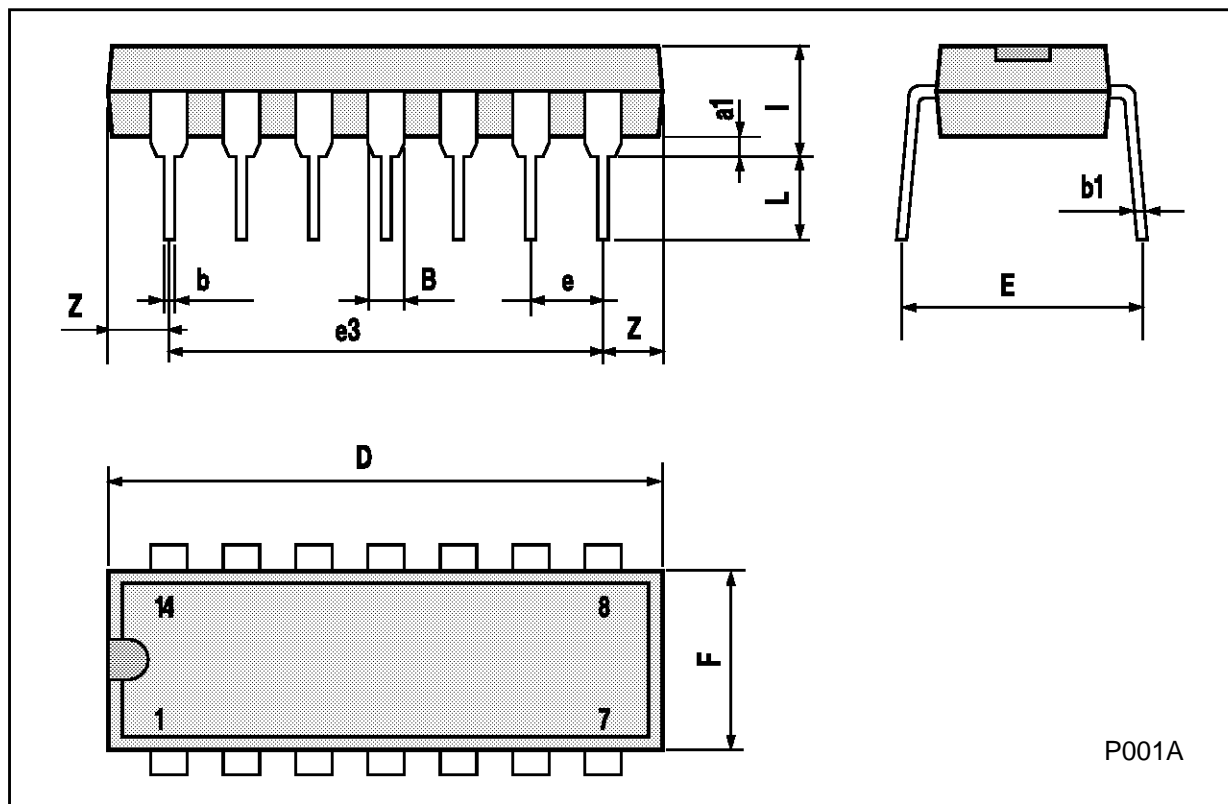
TRANSITION TIME OF INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SWITCHING CHARACTERISTICS TEST WAVEFORM



## Plastic DIP14 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100



Ceramic DIP14/1 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7.0			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		15.24			0.600	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.54	0.060		0.100
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200



P053C



## SO14 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					



PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



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