Versatile Timer Operates from Microseconds to Hours

National Semiconductor
Application Note 97
December 1973

INTRODUCTION

Timing functions, until recently, have been somewhat neglected by integrated circuit manufacturers. The primary reason was the extremely wide range of input and output signals currently incorporated in discrete designs. In addition, power supply voltages varied over a ten to one range and timing periods were as short as microseconds and as long as hours.

The LM122 timer has been designed to operate over a very wide range of input/output signal levels, supply voltages, and timing periods. It will replace most discrete designs with improved performance and reliability. This new timer overcomes many of the problems incurred in discrete or early IC designs.

First, it locks out trigger signals during the timing period to guarantee a precise output regardless of trigger level—while maintaining the ability to be retriggered almost immediately following the end of the timing pulse. (Duty cycles up to 99.9% can be achieved.) Secondly, the timing period is free from jitter caused by supply fluctuations because the timing components are driven from an internal regulated source. Supply voltage for the timer can vary from 4.5V to 40V even during the timing period! An additional feature is the ± 40V excursion allowed on the trigger input and the 40V/50 mA drive capability of the output transistor. These two specifications allow the LM122 to interface directly to present designs without level shift or power boosting problems. Finally, the LM122 will generate stable timing periods from several microseconds to hours—a useful range of eight decades. Worst case guarantees on comparator bias current and threshold level allow the user to easily select timing components for maximum accuracy.

CIRCUIT DESCRIPTION

The LM122 circuitry can be divided into five separate sections: output stage, bias network, voltage regulator, comparator, and logic. These sections are grouped on the schematic in *Figure 1* to simplify understanding of the timer.

The floating transistor output stage of the LM122 consists of Q32 through Q36. Q36 is the actual output transistor and is driven by emitter follower, Q33. Q34 and Q35 are antisaturation clamps to reduce stored charge in Q36 and to limit current through Q33. Q32 acts as a current limiter with the limit set at about 120 mA.

The regulator built into the LM122 is a $V_{BE}/\Delta V_{BE}$* type with a typical output voltage of 3.15V at up to 5.0 mA load current. Q18 and Q19 generate a 100 μA current through Q19 which has a positive temperature coefficient of 0.33%/°C. This generates 1.2V and $+4$ mV/°C TC across R21. When added to the base emitter diode voltages of Q20 and Q21, a 2.4V, zero TC reference is established at the base of Q21. R18 and R19 form a divider to raise the regulated voltage to 3.15V. (This particular voltage was chosen because it can be operated off a single 5.0V supply and because one RC time constant is exactly 2.0V out of 3.15V.) Q23 buffers Q21 from supply fluctuations and sets up the currents for the bias section of the timer. Q20 is a single stage of voltage gain for the regulator. It is buffered by the series pass transistor, Q24. Q25, Q26, R25, and R26 are included for starting purposes and do not affect operation once current is flowing in the regulator section.

*See AN-42, "On Card Regulator for Logic Circuits"

The function of the comparator is to cause an output change of state when the timing capacitor has charged to one RC time constant. Q11 through Q17 perform this function. Q14, Q15, Q16, and Q17 are a Darlington differential stage driving an active load formed by Q12 and Q13. Q11 is a second stage operating as a common emitter amplifier with R14 as its load resistor. For long timing intervals, the Darlington is run with no bleed current from Q30. Operating current for Q15 and Q16 is about 5 μA per side. The specially processed lateral PNP's have h_{FE}'s of about 200, so operating current for Q14 and Q17 is typically 25 nA. At these current levels, the substrate PNP's have h_{FE}'s of 80, giving comparator input currents of 300 pA! One side of the comparator is tied to a divider (R16 and R17) which is set at 63.2% of the reference voltage — one RC time constant. The other side is connected to the external timing resistor and capacitor.

The logic section of the LM122 performs four functions: first, it provides a latching action to make the circuitry immune to retriggering during the timing interval; second, it simulates the action of an exclusive OR gate to generate a logic reverse function; additionally, it translates the low level output from the comparator to the high level swing needed to drive the floating transistor output; and finally, it drives the discharge transistor to reset the timing capacitor. Q2 and Q3 makeup the TTL compatible trigger input to the logic section. Q3 is a lateral PNP with 60V reverse emitter-base breakdown voltage, allowing negative inputs are high as -40V without harm to the chip. R5 is an epitaxial resistor which pinches off at 30V and has a breakdown of 80V. This allows positive input voltages of up to 40V on the trigger terminal even when operating the timer from a supply voltage of only 5.0V. Typical current drawn by the trigger terminal is 40 μA at 2.0V and 600 μA at 40V. Q4 and Q6 form a latch which self-limits at about 400 μA and can be turned off by Q2. Q5 and Q7 interface the latch to the comparator so that the comparator can fire the latch at the end of the timing period. Q8, Q9, and Q10 perform the level shifting required to drive the output transistor and double as an exclusive OR gate, with the emitters of Q8 and Q9 as one input and the collectors of Q5 and Q11 as the second input. Grounding the Q8 and Q9 emitters reverses the effect of a signal appearing at the collector of Q11.

Biasing for the various circuits in the timer is generated by a string of PNP current sources consisting of Q27 through Q31. Current levels are established by the constant current source, Q23, driving diode connected Q28. The current from Q23 is 400 μA, setting the drop across the emitter resistor, R28 plus R29, at 200 mV. Q29 delivers 10 μA to the comparator and Q31 supplies a total of 100 μA to the output transistor and logic circuitry. Part of Q29's collector is returned to Q27 to avoid having to use a large value resistor for R30. Q30 is completely off when using the timer for long timing periods. Shorting the boost terminal of V^+ adds

©1995 National Semiconductor Corporation RRD-B30M115/Printed in U. S. A.

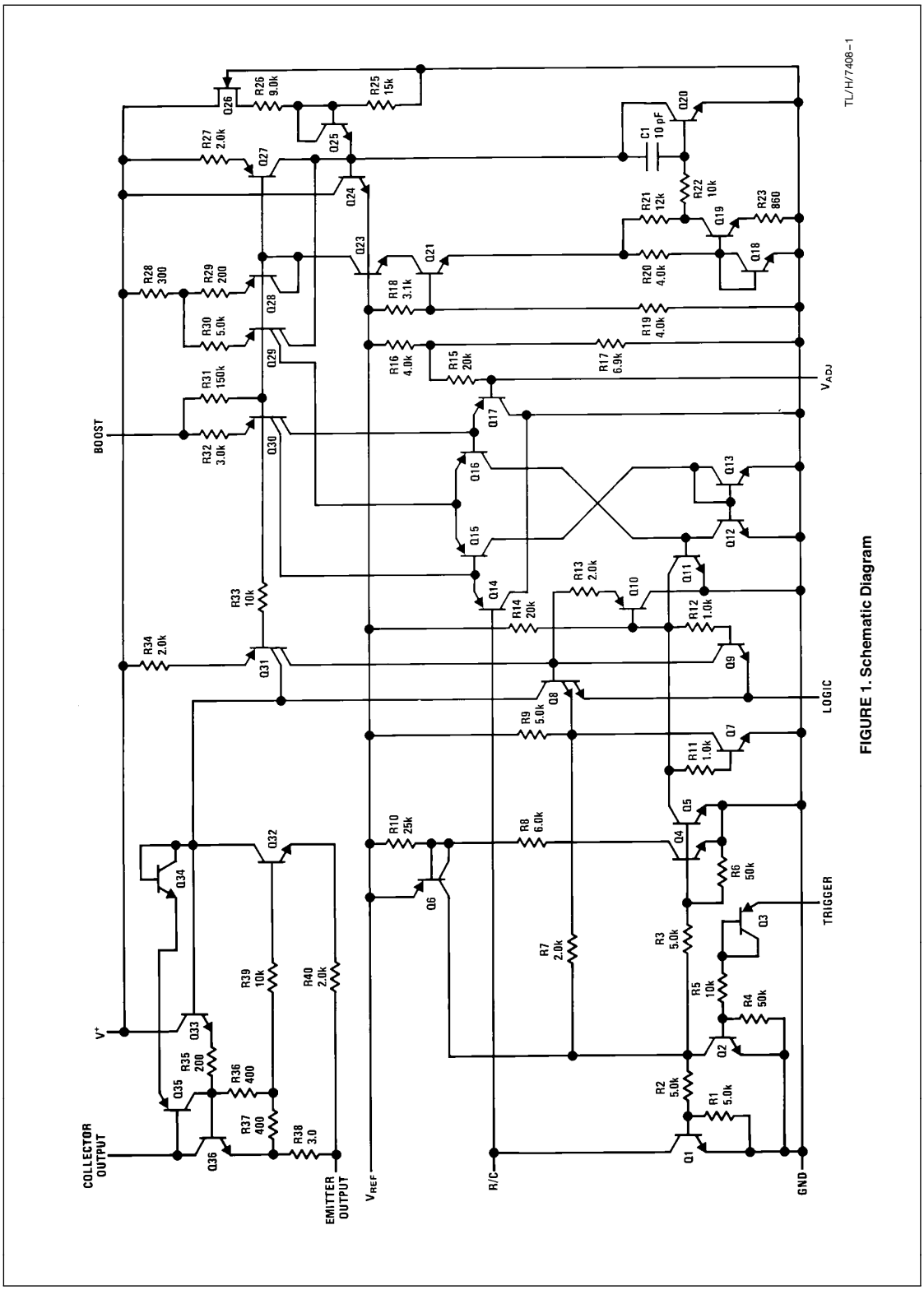


FIGURE 1. Schematic Diagram

about 5 μA bleed current at the emitters of Q14 and Q17. This extra current is needed to slew the emitters of the comparator for timing periods less than 1 ms.

DESCRIPTION OF PIN FUNCTIONS

One of the main features of the LM122 is its great versatility. Since this device is unique, a description of the functions and limitations of each pin is in order. This will make it much easier to follow the discussion of the various applications presented in this note.

V^+ is the positive supply terminal of the LM122. When using a single supply, this terminal may be driven by any voltage between 4.5V and 40V. The effect of supply variations on timing period is less than 0.005%/V, so supplies with high ripple content may be used without causing pulse width changes. Supply bypassing on V^+ is not generally needed but may be necessary when driving highly reactive loads. Quiescent current drawn from the V^+ terminal is typically 2.5 mA, independent of the supply voltage. Of course, additional current will be drawn if the reference is externally loaded.

The V_{REF} pin is the output of a 3.15V series regulator referenced to the ground pin. Up to 5.0 mA can be drawn from this pin for driving external networks. In most applications the timing resistor is tied to V_{REF}, but it need not be in situations where a more linear charging current is required. The regulated voltage is very useful in applications where the LM122 is not used as a timer; such as switching regulators, variable reference comparators, and temperature controllers. Typical temperature drift of the reference is less than 0.01%/°C.

The trigger terminal is used to start timing. Threshold is typically 1.6V at +25°C and has a temperature dependence of −5.0 mV/°C. Current drawn from the trigger source is typically 20 μA at threshold, rising to 600 μA at 30V, then leveling off due to FET action of the series resistor, R5. For negative input trigger voltages, the only current drawn is leakage in the nA region.

If the trigger terminal is held high as the timing period ends, the output pulse will appear normally, but the timing capacitor will not be discharged. This is a necessary circuit action to prevent repetitive cycles when the trigger is held high. After the timing period, the capacitor is discharged when the trigger decreases below the threshold, without affecting the output.

The R/C pin is tied to the uncommitted side of the comparator and to the collector of the capacitor discharge transistor. Timing ends when the voltage on this pin reaches 2.0V (1 RC time constant referenced to the 3.15V regulator). The internal discharge transistor turns on only if the trigger voltage has dropped below threshold. In comparator or regulator applications of the timer, the trigger is held permanently high and the R/C pin acts just like the input to an ordinary comparator. The maximum voltages which can be applied to this pin are +5.5V and −0.7V. Input current to the R/C pin is typically 300 pA when the voltage is negative with respect to the V_{ADJ} terminal. For higher voltages, the current drops to leakage levels. In the boosted mode, input current is 30 nA. Gain of the comparator is very high, 200,000 or more depending on the state of the logic reverse pin and the connection of the output transistor.

The ground pin of the LM122 need not necessarily be tied to system ground. It can be connected to any positive or negative voltage as long as the supply is negative with respect to the V^+ terminal. Level shifting may be necessary for the input trigger if the trigger voltage is referred to system ground. This can be done by capacitive coupling or by actual resistive or active level shifting. One point must be kept in mind; the emitter output must not be held above the ground terminal with a low source impedance. This could occur, for instance, if the emitter were grounded when the ground pin of the LM122 was tied to a negative supply.

The terminal labeled V_{ADJ} is tied to one side of the comparator and to a voltage divider between V_{REF} and ground. The divider voltage is set at 63.2% of V_{REF} with respect to ground—exactly one RC time constant. The impedance of the divider is increased to about 30k with a series resistor to present a minimum load on external signals tied to V_{ADJ}. This resistor is a pinched type with a typical variation in absolute value of ±100% and a TC of 0.7%/°C. For this reason, external signals (typically a pot between V_{REF} and ground) connected to V_{ADJ} should have a source resistance as low as possible. For small changes in V_{ADJ}, up to several kΩ is all right, but for large variations 250Ω or less should be maintained. This can be accomplished with a 1.0k pot, since the maximum impedance from the wiper is 250Ω. If a voltage is forced on V_{ADJ} from a hard source, voltage should be limited to −0.5, and +5.0V, or current limited to ±1.0 mA. This includes capacitively coupled signals because even small values of capacitors contain enough energy to degrade the input stage if the capacitor is driven with a large, fast slewing signal. The V_{ADJ} pin may be used to abort the timing cycle. Grounding this pin during the timing period causes the timer to react just as if the capacitor voltage had reached its normal RC trigger point; the capacitor discharges and the output charges state. An exception to this occurs if the trigger pin is held high when the V_{ADJ} pin is grounded. In this case, the output changes state, but the capacitor does not discharge. If the trigger drops with V_{ADJ} is being held low, discharge will occur immediately and the cycle will be over. If the trigger is still high when V_{ADJ} is released, the output may or may not change state, depending the voltage across the timing capacitor. For voltages below 2.0V across the timing capacitor, the output will change state immediately, then once more as the voltage rises past 2.0V. For voltages above 2.0V, no change will occur in the output.

In noisy environments or in comparator-type applications, a bypass capacitor on the V_{ADJ} terminal may be needed to eliminate spurious outputs because it is high impedance point. The size of the cap will depend on the frequency and energy content of the noise. A 0.1 μF will generally suffice for spike suppression, but several μF may be used if the timer is subjected to high level 60 Hz EMI.

The emitter and the collector outputs of the timer can be treated just as if they were an ordinary transistor with 40V minimum collector-emitter breakdown voltage. Normally, the emitter is tied to the ground pin and the signal is taken from the collector, or the collector is tied to V^+ and the signal is taken from the emitter. Variations on these basic connections as possible. The collector can be tied to any positive voltage up to 40V when the signal is taken from the emitter. However, the emitter will not be pulled higher than the supply voltage on the V^+ pin. Connecting the collector to a voltage less than the V^+ voltage is allowed. The emitter should not be connected to a hard source other than that to which the ground pin is tied. The transistor has built-in current limiting with a typical knee current of 120 mA. Temporary short circuits are allowed; even with collector-emitter voltages up to 40V. The power time product, however, must

not exceed 15 watt•seconds for power levels above the maximum rating of the package. A short to 30V, for instance, can not be held for more than 4 seconds. These levels are based on a 40°C maximum initial chip temperature. When driving inductive loads, always use a clamp diode to protect the transistor from inductive kick-back.

A boost pin is provided on the LM122 to increase the speed of the internal comparator. The comparator is normally operated at low current levels for lowest possible input current. For short time intervals where low input current is not needed, comparator operating current can be increased several orders of magnitude for fast operation. Shorting the boost terminal to V^+ increases the emitter current of the vertical PNP drivers in the differential stage from 25 nA to 5.0 μA.

With the timer in the unboosted state, timing periods are accurate down to about 1 ms. In the boosted mode, loss of accuracy due to comparator speed is only about 800 ns, so timing periods of several microseconds can be used.

The ''Logic'' pin is used to reverse the signal appearing at the output transistor. An open or ''high'' condition on the logic pin programs the output transistor to be ''off'' during the timing period and ''on'' all other times. Grounding the logic pin reverses the sequence to make the transistor ''on'' during the timing period. Threshold for the logic is typically 150 mV with 150 μA flowing out of the terminal. If an active drive to the logic pin is desired, a saturated transistor drive is recommended, either with a discrete transistor or the open collector output of integrated logic. A maximum V_{SAT} of 75 mV of 200 μA is required. A typical example of active drive to the logic pin is the pulse width discriminator shown in *Figure 16*.

CALCULATING WORST CASE TIMING ERROR

Timing errors for the LM122 come from the following sources:

1. Timing ratio error
2. Capacitor saturation voltage
3. Internal switching delays
4. Comparator bias current
5. External resistor and capacitor tolerance
6. Capacitor and board leakage

In general, errors 1 and 5 are the most significant, so they will be treated first.

For most applications, the major contribution to timing error from the LM122 itself is variation in timing ratio, which is the ratio of the comparator threshold voltage (typically 2.0V) to the voltage at the V_{REF} pin. A 1% error in this ratio results in a 1.8% initial timing error. Timing ratio error comes from variations in the internal divider ratio and from offset voltage in the comparator. The LM122 is specified to have a timing ratio from 0.626 to 0.638 at $+25°C$, giving a $\pm 1.8\%$ worst case contribution to initial timing period error. Over temperature, the worst case figures doubles to $\pm 3.6\%$. If the initial error is trimmed out externally however, timing error drift due to timing ratio will generally be less than $\pm 0.5\%$ over temperature.

Adding all the contributions to timing error from the LM122 itself will usually give a figure in the 2% to 3% range at $+25°C$. External timing components (R_t and C_t) will normally contribute much more error than this unless selected components are used. $\pm 5\%$ tolerance on R_t and C_t will increase the worst case error to 12% to 13%. By trimming out initial component errors, an exact initial timing period can be obtained, but temperature drift then becomes the limiting factor. For most applications, the contributions to timing period drift due to the LM122 itself will be in the 0.005%/°C to 0.02%/°C range.

If accurate timing over temperature is required, low drift components must be used for R_t and C_t. Capacitors are available with temperature coefficients of 100 to 200 ppm/°C. Resistors, at least in the lower ranges, are available with TC's much better than this. Above 1 MΩ, however, care must be used in the selection of a low TC resistor. Units are available up to 100 MΩ with less than 100 ppm/°C drift.

Capacitor saturation voltage is the voltage still remaining on the timing capacitor after it has been reset to as near ground as the internal discharge transistor can drive it. For timing resistors 1 MΩ or greater, this remaining voltage is typically 2.5 mV. For smaller timing resistors, the capacitor saturation voltage can be calculated by the following: formula:

$$V_C \approx 2.5\ \text{mV} + \frac{(V_{REF})^* (80\Omega)}{R_t}$$

*$V_{REF} = 3.15V$

The effect of V_C on timing period is linear at 0.03%/mV. Temperature dependence of V_C is typically $+0.2\%/°C$ for $R_t \leq 300\ k\Omega$, rising to 0.4%/°C for $R_t = 10\ k\Omega$. This gives a typical temperature coefficient of timing error *due to* V_C of (0.002) (2.5 mV) (0.03%/mV) = 0.0015%/°C for $R_t \geq 1\ M\Omega$ and (0.004) (24 mV) (0.03%/mV) $\approx$ 0.003%/°C for $R_t = 10\ k\Omega$. Since most applications can use timing resistors in the range of 100 kΩ and up, error *from capacitor saturation voltage* rarely exceeds 0.15% initially, with $\pm 0.05\%$ variation over the full temperature range.

Internal switching delays cause errors which tend to be a fixed time rather than a percentage of the timing period. In the boosted mode this delay is typically 800 ns, and with the boost off; the delay is about 25 μs. These times can be

added directly to the calculated timing period for worst case analysis. For timing periods longer than 25 ms, the 25 μs delay gives an error of 0.1% or less. In the range of 1 or 25 ms, error due to delays is 0.1% or less for the boosted mode, rising to a maximum of 4.0% in the unboosted mode. At $\tau = 10$ μs, delay is the major contribution to timing error ($\approx$ 8%).

Comparator bias current contributes a negligible timing error for all but very long time timing periods. Error can be calculated with a simple formula:

Error (%) $= -50 \times R_t \times I_b$ (Note sign)

I_b = Comparator Bias Current

R_t = Timing Resistor

For $R_t = 100$ MΩ and $I_b = 0.3$ nA (typical) a 1.5% reduction in timing period is incurred. For worst case calculations at $+25$°C, an I_b of 1 nA maximum is specified in the unboosted mode and 100 nA in the boosted mode. At temperatures below $+25$°C, these numbers still hold. At $+125$°C, I_b increases due to leakage to a maximum of ± 5 nA unboosted. For worst case calculations below $+125$°C, the leakage error (5 nA) can be assumed to halve for each 10°C drop below $+125$°C. At $+95$°C for instance, the leakage component of I_b would be (5 nA/8) $\approx$ 0.6 nA for a total I_b of 1.6 nA worst case. For the commercial LM322 and LM3905, worst case I_b is 2 nA at $+75$°C, and for the LM2905 I_b is 2 nA maximum at $+85$°C. For temperatures between -25°C and $+85$°C, the TC of I_b is typically 5 pA/°C in the unboosted mode and 100 pA/°C in the boosted mode. For a 100 MΩ R_t, this 5 pA/°C contributes -0.025%/°C to timing period drift.

Error (%/°C) $= (-50)\,(\Delta I_b/\Delta T)(R_t)$

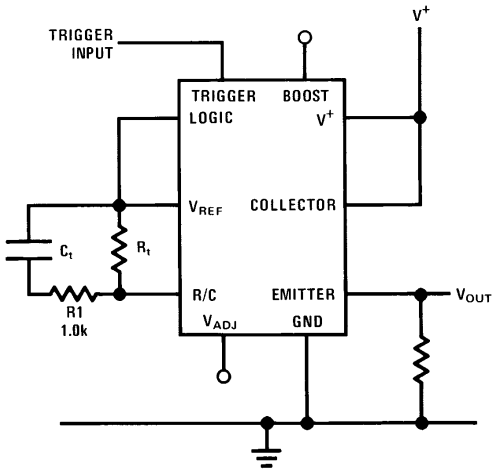
For worst case calculations a $\Delta I_b/\Delta T$ ($-25 \leq T_A \leq +85$°C) of 12 pA/°C may be used for the LM122/LM222 and 20 pA/°C for the LM322 and LM2905/LM3905.

External leakage paths may cause timing errors for large values of R_t and high board temperatures. Connections made to the R/C pin should be kept free of dust, moisture, and soldering flux if long time intervals are to be kept accurate. All package types have the R/C pin located between V_{REF} and the ground pin to minimize these leakages.

DESIGN HINTS

ELIMINATING TIMING CYLCE UPON INITIAL APPLICATION OF POWER

The LM122 will start a timing cycle automatically (with no trigger input) when V^+ is first turned on. If this characteristic is undesirable, it can be defeated by tying the timing capacitor to V_{REF} instead of ground as shown in *Figure 2*. This connection does not affect operation of the timer in any other way. If an electrolytic timing capacitor is used, be sure the negative end is tied to the R/C pin and the positive end to V_{REF}. A 1.0 kΩ resistor should be included in series with the timing capacitor to limit the surge current load on V_{REF} when the capacitor is discharged.



TL/H/7408–2

FIGURE 2. Eliminating Initial Timing Cycle

USING ELECTROLYTIC TIMING CAPACITORS

Electrolytic capacitors are not usually recommended for timing because of their unstable capacitance and high leakage. For long timing periods ($>$ 10 seconds) at moderate temperatures (0°C to 50°C) however, an electrolytic may be attractive because of its low cost per microfarad. Solid tantalum capacitors such as the Kemet* C series T310 (molded epoxy) or T110 (hermetic) are recommended. These units have long term stabilities of 2% to 3% and a temperature coefficient of $+0.2$%/°C. Selected units are available for timing use with very low leakage.

RESET TIME

The timing capacitor used with the LM122 is reset with an internal transistor which has a collector offset voltage of 2.5 mV @ 1 μA with approximately 80Ω of collector resistance. The time required to reset this capacitor determines the minimum time between timing pulses. An approximate formula for reset time is:

$$\text{Reset Time} = (80\Omega)\,(C_t^{\dagger})\ (5)$$

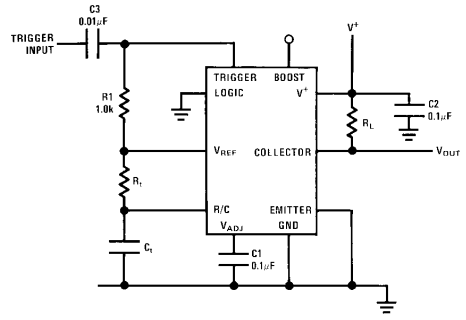
$^{\dagger}C_t$ = External timing capacitor.

NOISY ENVIRONMENTS

The LM122 is relatively insensitive to noise on supply lines and to radiated energy. In *extremely* noisy environments however, it may be necessary to configure the LM122 differently, both to eliminate false triggering and to prevent premature end of a timing period. The circuit ''a'' shown in *Figure 3* has been set up for maximum noise rejection. C1 bypasses the V_{ADJ} pin because of the relatively high impedance ($\cong$ 30 kΩ) of this point. Negative spikes on the V_{ADJ} pin will cause premature end of the timing period. C2 bypasses the supply for rejection of fast transients. R1 sets up the trigger pin to a ''normally high'' condition. This prevents extremely high electromagnetic fields from triggering the internal flip-flop during a timing period. The input trigger signal is capacitively coupled through C3. Triggering occurs on the *negative* edge of the trigger pulse as shown in the waveform sketch next to *Figure 21*.

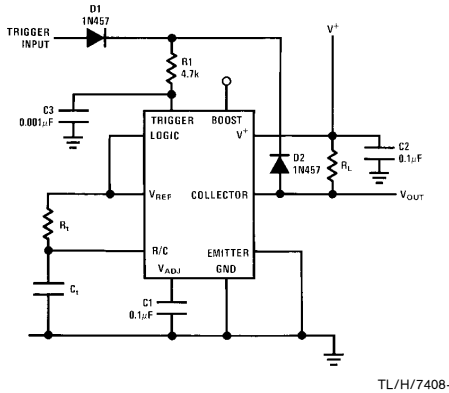
*Manufactured by Union Carbide

If the output voltage from the LM122 can be set up to go ''high'' during the timing cycle, the alternate connection shown in ''b'' can be used. Here, the trigger is held high by D2 during the timing period. When the output goes low after the timing period is over, the circuit may be retriggered immediately via D1. R1 and C3 suppress unwanted spikes at the trigger input.



TL/H/7408–3

(A)



TL/H/7408–4

(B)

FIGURE 3. Maximum Noise Immunity

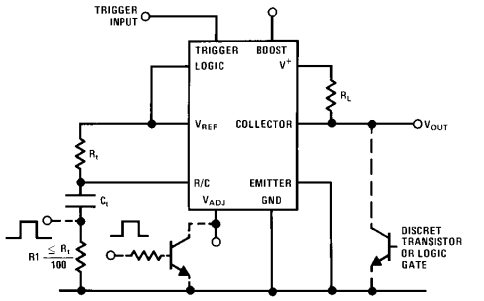
ABORTING A TIMING CYCLE (*Figure 4*)

The LM122 does not have an input specifically allocated to a stop-timing function. If such a function is desired, it may be accomplished several ways:

- Ground V_{ADJ}
- Raise R/C more positive than V_{ADJ}
- Wire ''OR'' the output

Grounding V_{ADJ} will end the timing cycle just as if the timing capacitor had reached its normal discharge point. A new timing cycle can be started by the trigger terminal as soon as the ground is released. A switching transistor is best for driving V_{ADJ} to as near ground as possible. Worst case sink current is about 300 μA.

A timing cycle may be also ended by a positive pulse to a resistor ($R \leq R_t/100$) in series with the timing capacitor. The pulse amplitude must be at least equal to V_{ADJ} (2.0V), but should not exceed 5.0V. When the timing capacitor discharges, a negative spike of up to 2.0V will occur across the resistor, so some caution must be used if the drive pulse is used for other circuitry.



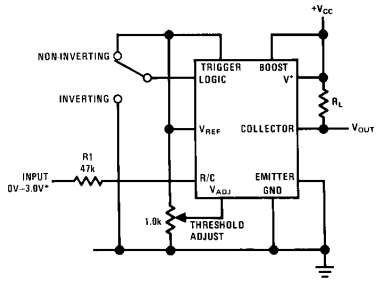
TL/H/7408–5

FIGURE 4. Cycle Interrupt

The output of the timer can be wire ORed with a discrete transistor or an open collector logic gate output. This allows overriding of the timer output, but does not cause the timer to be reset until its normal cycle time has elapsed.

USING THE LM122 AS A COMPARATOR

A built-in reference and zero volt common mode limit make the LM122 very useful as a comparator. Threshold may be adjusted from zero to three volts by driving the V_{ADJ} terminal with a divider tied to V_{REF}. Stability of the refrence voltage is typically $\pm$1% over a temperature range of $-$55°C to $+$125°C. Offset voltage drift in the comparator is typically 25 μV/°C in the boosted mode and 50 μV/°C unboosted. A resistor can be inserted in series with the input to allow overdrives up to $\pm$50V as shown in *Figure 5*. There is actually no limit on input voltage as long as current is limited to



TL/H/7408–6

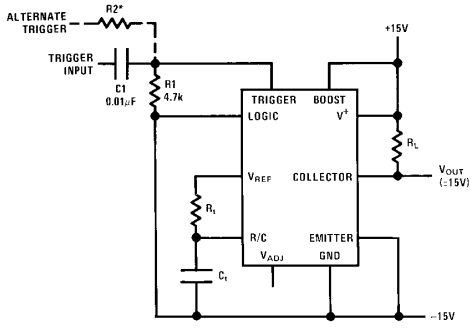
*Timer Protected Against Damage for Up to $\pm$50V

FIGURE 5. Comparator with 0 Volts to 3.0 Volts Threshold

$\pm$1 mA. The resistor shown contributes a worst case of 5 mV to initial offset. In the unboosted mode, the error drops to 0.25 mV maximum. The capability of operating off a single 5V supply should make this comparator very useful.

USING DUAL SUPPLIES

The LM122 can be operated off dual supplies as shown in *Figure 6*. The only limitation is that the emitter terminal cannot be tied to ground, it must either drive a load referred to V^- or be actually tied to V^- as shown. Although capacitive coupling is shown for the trigger input (to allow 5V triggering), a resistor can be substituted for C1. R2 must be chosen to give proper level shifting between the trigger signal and the trigger pin of the timer. Worst case "I_O" on the trigger pin (with respect to V^-) is 0.8V, and worst case "high" is 2.5V. R2 may be calculated from the divider equation with R1 to give these levels.



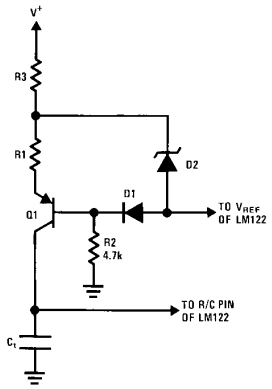
*Select For Proper Level Shift TL/H/7408–7

Emitter Terminal Or Emitter Load Must Be Tied To GND Pin Of Timer.

FIGURE 6. Operating Off Dual Supplies

LINEARIZING THE CHARGING SWEEP

In some applications (such as a linear pulse width modulator) it may be desirable to have the timing capacitor charge from a constant current source. A simple way to accomplish this is shown in the accompanying sketch.



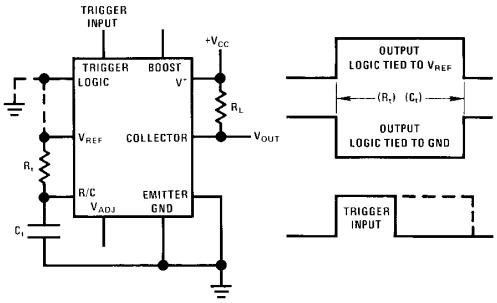
TL/H/7408–8

Q1 converts the current through R1 to a current source independent of the voltage across C_t. R2, R3, D1, and D2 are added to make the current through R1 independent of supply variations and temperature changes. (D2 is a low TC type) D2 and R3 can be omitted if the V^+ supply is stable and D1 and R2 can be omitted also if temperature stability if not critical. With D1 and R2 omitted, the current through R1 will change about 0.015%/°C with a 15V supply and 0.1%/°C with a 5.0V supply.

APPLICATIONS

BASIC TIMERS

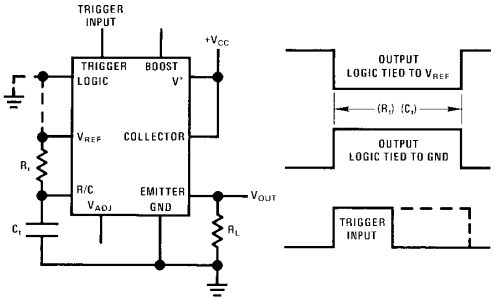
Figure 7 is a basic timer using the collector output. R_t and C_t set the time interval with R_L as the load. During the timing interval the output may be either high or low depending on the connection of the logic pin. Timing waveforms are shown in the sketch alongside *Figure 7*.



TL/H/7408–9

FIGURE 7. Basic Timer-Collector Output and Timing Chart

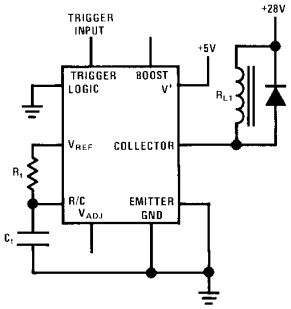
Figure 8 is again a basic timer, but with the output taken from the emitter of the output transistor. As with the collector output, either a high or low condition may be obtained during the timing period.



TL/H/7408–10

FIGURE 8. Basic Timer-Emitter Output and Timing Chart

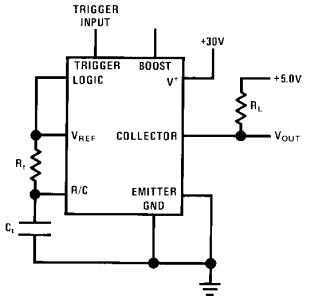
Figure 9 shows the timer interfacing 5V logic to a high voltage relay. Although the V^+ terminal could be tied to the $+28V$ supply, this would be an unnecessary waste of power in the IC. In any case, the threshold for the trigger is 1.6V regardless of where V^+ is tied.



TL/H/7408–11

FIGURE 9. 5 Volt Logic Supply Driving 28 Volt Relay

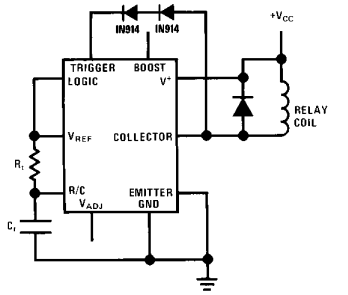
Figure 10 indicates the ability of the timer to interface to digital logic when operating off a high supply voltage. V_{OUT} swings between +5V and ground with a minimum fanout of 5 for medium speed TTL.



TL/H/7408–12

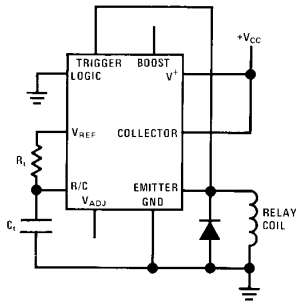
FIGURE 10. 30 Volt Supply Interfacing to 5 Volt Logic

Figure 11 is an application where the LM122 is used to simulate a thermal delay relay which prevents power from being applied to other circuitry until the supply has been on for some time. The relay remains de-energized for R_t C_t seconds after V_{CC} is applied, then closes and stays energized until V_{CC} is turned off. *Figure 12* is a similar circuit except that the relay is energized as soon as V_{CC} is applied. R_t C_t seconds later, the relay is de-energized and stays off until the V_{CC} supply is recycled.



TL/H/7408–13

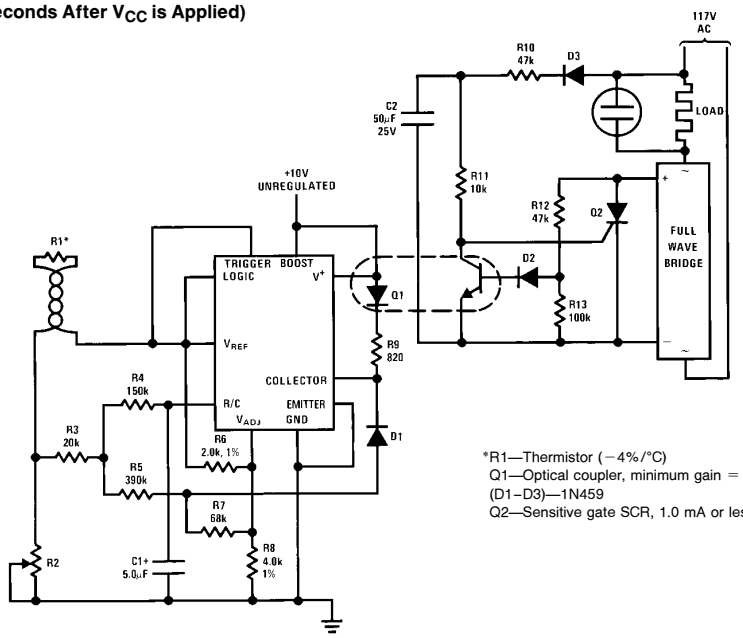
FIGURE 11. Time Out on Power Up (Relay Energized R_tC_t Seconds After V_{CC} is Applied)



TL/H/7408–14

FIGURE 12. Time Out on Power Up (Relay Energized *Until* R_tC_t Seconds After V_{CC} is Applied)

Figure 13 is a more advanced application of the LM122 as a proportioning temperature controller with optical isolation and synchronized zero crossing features. The timing function is not used. Instead the trigger terminal is held high and the LM122 is used as a high gain comparator with a built in reference. R1 is a thermistor with a −4%/°C temperature coefficient used as the sensor. R2 is used to set the temperature to be controlled by R1. R3 through R8 set up the proportioning action. R3 raises the impedance of the R1/R2 divider so that R5 sees a relatively constant impedance independent of the set point temperature. R6 and R8 reduce the V_{ADJ} impedance so that internal variations in divider impedance do not affect proportioning action. R5 and R7



*R1—Thermistor (−4%/°C)
Q1—Optical coupler, minimum gain = ½ at 1.0 mA
(D1–D3)—1N459
Q2—Sensitive gate SCR, 1.0 mA or less

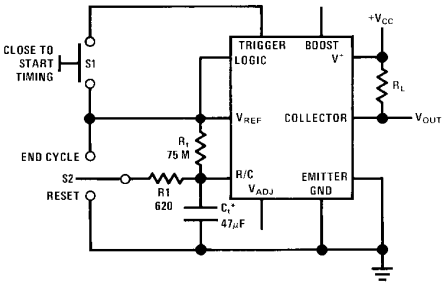
TL/H/7408–15

FIGURE 13. Proportioning Temperature Controller with Synchronized Zero-Crossing

set the actual width of the proportioning band and can be scaled as necessary to alter the width of the band. Larger resistors make the band narrower. The values shown give approximately a 1°C band. R4 and C1 determine the proportioning frequency which is about 1 Hz with the values shown. C1 or R4 can change to alter frequency, but R4 should be between 50k and 500k, and C1 must be a low leakage type to prevent temperature shifts. D1 prevents supply voltage fluctuations from affecting set point or proportioning band. Any unregulated supply between 6V and 15V is satisfactory.

Q1 is an optical isolator with a minimum gain of 0.5. With the values shown for R9, R10, and R11, Q1 is over-driven by at least 3 to 1 to insure deep saturation for reliable turn off of the SCR. Q2 must be a sensitive gate device with a worst case gate firing current of 0.5 mA. R12, R13, and D2 implement the synchronized zero-crossing feature by preventing Q1 from turning off after the voltage across Q2 has climbed above 2.5V. D3, R10, and C2 provide a source of semifiltered dc current must have a minimum breakdown of 200V.

Figure 14 shows the LM122 connected as a one hour timer with manual controls for start, reset, and cycle end. S1 starts timing, but has no effect after timing has started. S2 is a center off switch which can either end the cycle prematurely with the appropriate change in output state and discharging of C_t, or cause C_t to be reset to 0V without a change in output. In the latter case, a new timing period starts as soon as S2 is released. The average charging current through R_t is about 30 nA, so some attention must be paid to parts layout to prevent stray leakage paths. The suggested timing capacitor has a typical self time constant of 300 hours and a guaranteed minimum of 25 hours at +25°C. Other capacitor types may be used if sufficient data is available on their leakage characteristics.

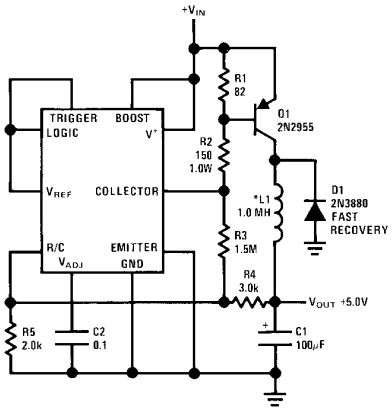


TL/H/7408–16

*Dearborn Electronics LP9A1A476K Polycarbonate

FIGURE 14. One Hour Timer with Reset and Manual Cycle End

Figure 15 is another application where the LM122 does not use its timing function. A switching regulator is made using the internal reference and comparator to drive a PNP switch transistor. Features of this circuit include a 5.5V minimum input voltage at 1A output current, low part count, and good efficiency (> 75%) for input voltages to 10V. Line and load regulation are less than 0.5% and output ripple at the switching frequency is only 30 mV. Q1 is an inexpensive plastic device which does not need a heatsink for ambient temperature up to 50°C. D1 should be a fast switching diode. Output voltage can be adjusted between 1V and 30V by choosing proper values for R2, R3, R4, and R5. For outputs less than 2V, a divider with 250Ω the Thevinin resistance must be connected between V_{REF} and ground with its tap point tied to V_{ADJ}.

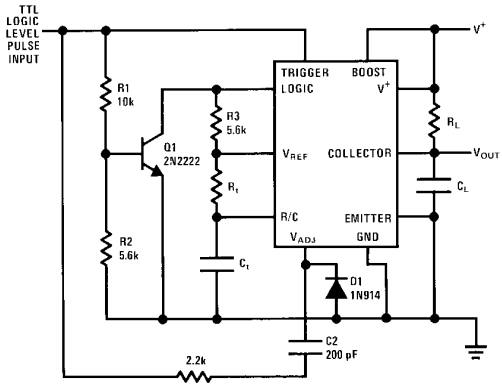


TL/H/7408–17

*No. 22 Wire Wound On Molybdenum Permalloy Core

FIGURE 15. 5 Volt Switching Regulator with 1.0 Amp Output and 5.5 Volt Minimum Input

By driving the logic terminal of the LM122 simultaneous to the trigger input, a simple, accurate pulse width detector can be made (*Figure 16*).



*V_{OUT} = 0 For W < R_t C_t

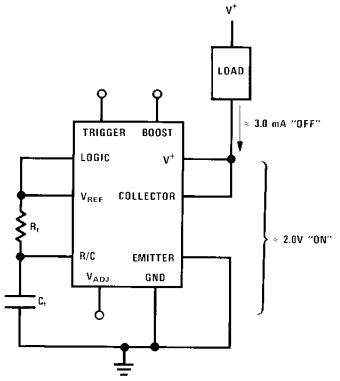
Pulse Out = W − R_t C_t For W > R_t C_t

TL/H/7408–18

FIGURE 16. Pulse Width Detector

In this application the logic terminal is normally held high by R3. When a trigger pulse is received, Q1 is turned on, driving the logic terminal to ground. The result of triggering the timer and reversing the logic at the same time is that the output does not change from its initial low condition. The only time the output will change states is when the trigger input stays high longer than one time period set by R_t and C_t. The output pulse width is equal to the input trigger width minus $R_t \bullet C_t$. C2 insures no output pulse for short (< RC) trigger pulses by prematurely resetting the timing capacitor when the trigger pulse drops. C_L filters the narrow spikes which would occur at the output due to interval delays during switching.

The LM122 can be used as a two terminal time delay switch if an ''on'' voltage drop of 2V to 3V can be tolerated. In

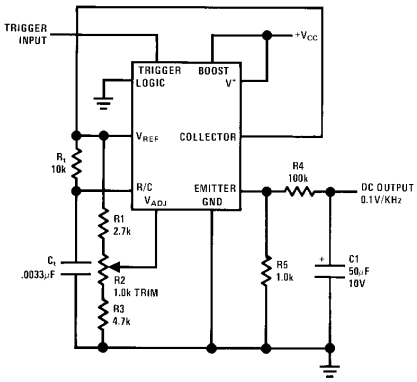


TL/H/7408–19

FIGURE 17. Two-Terminal Time Delay Switch

Figure 17, the timer is used to drive a relay "on" R_t C_t seconds after application of power "off" current of the switch is 4 mA maximum, and "on" current can be as high as 50 mA.

An accurate frequency to voltage converter can be made with the LM122 by averaging output pulses with a simple one pole filter as shown in *Figure 18*. Pulse width is adjusted with R2 to provide initial calibration at 10 kHz. The collector of the output transistor is tied to V_{REF}, giving constant amplitude pulses equal to V_{REF} at the emitter output. R4 and C1 filter the pulses to give a dc output equal to, (R_t) (C_t) (V_{REF}) (f). Linearity is about 0.2% for a 0V to 1V output. If better linearity is desired R5 can be tied to the summing node of an op amp which has the filter in the feedback path. If a low output impedance is desired, a unity gain buffer such as the LM110 can be tied to the output. An analog meter can be driven directly by placing it in series with R5 to ground. A series RC network across the meter to provide damping will improve response at very low frequencies.

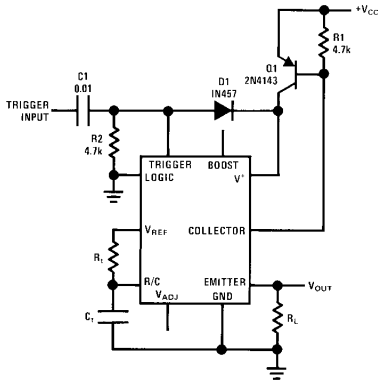


TL/H/7408–20

FIGURE 18. Frequency to Voltage Converter (Tachometer) Output Independent of Supply Voltage

In some applications it is desirable to reduce supply drain to zero between timing cycles. In *Figure 19* this is accomplished by using an external PNP as a latch to drive the V+ pin of the timer.

Between timing periods Q1 is off and no supply current is drawn. When a trigger pulse of 5V minimum amplitude is

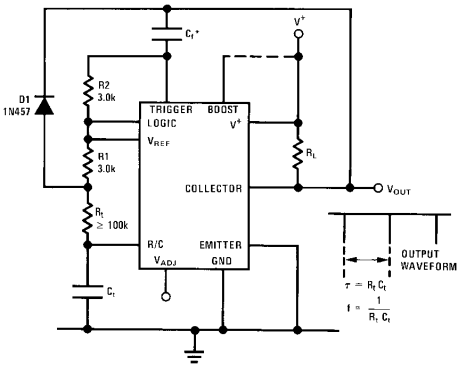


TL/H/7408–21

FIGURE 19. Zero Power Dissipation Between Timing Intervals

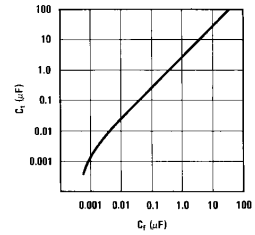
received, the LM122 output transistor and Q1 latch for the duration of the timing period. D1 prevents coupling back into the trigger signal from the dc load created by the trigger input. If the trigger input is a short pulse, C1 and R2 may be eliminated. R_L must have a minimum value of $(V_{CC})/(2.5\ mA)$.

The LM122 can be made into a self-starting oscillator by feeding the output back to the trigger input through a capac-



*See Chart

TL/H/7408–22



TL/H/7408–23

FIGURE 20. Oscillator

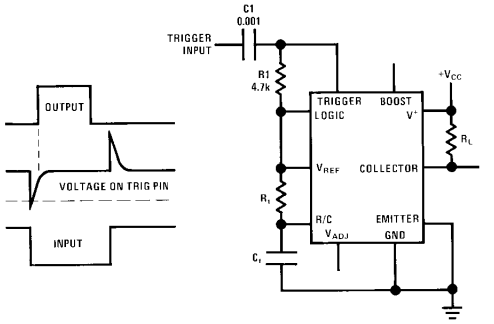
itor as shown in *Figure 20*. Operating frequency is $1/(R_t\ C_t)$. The output is a narrow negative pulse whose width is approximately $2R_2\ C_f$. For optimum frequency stability, C_f should be as small as possible. The minimum value is determined by the time required to discharge C_t through the internal discharge transistor. A conservative value for C_f can be

chosen from the graph included with *Figure 20*. For frequencies below 1 kHz, the frequency error introduced by C_f is a few tenths of one percent or less for $R_t > 500k$.

Although the LM122 is triggered by a positive going trigger signal, a differentiator tied to a normally ''high'' trigger will result in negative edge triggering. In *Figure 21*, R1 serves the dual purpose of holding the trigger pin normally high and differentiating the input trigger pulse coupled through C1. The timing diagram included with *Figure 21* shows that triggering actually occurs a short time after the negative going trigger, while positive going triggers have no effect. The delay time between a negative trigger signal and actual starts of timing is approximately 0.5 to 1.5 R1 C1 depending on the trigger amplitude, or about 2.5 to 7.5 μs with the values shown. This time will have to be increased for C_t larger than 0.01 μF because C_t is charged to V_{REF} whenever the trigger pin is kept high and must reset itself during the short time that the trigger pin voltage is low. A conservative value for C1 is:

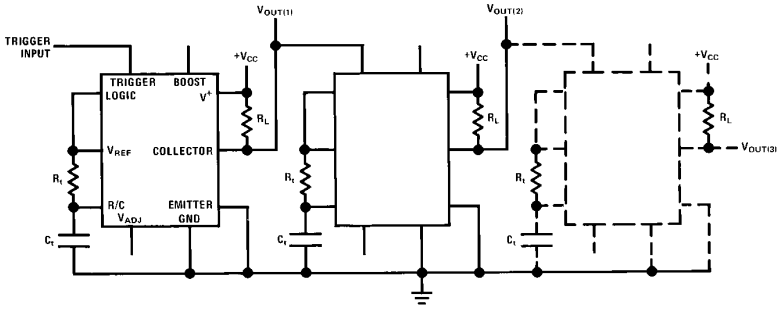
$$C1 \geq \frac{C_t}{10}$$

The LM122 can be connected as a chain of timers quite easily with no interface required. In *Figure 22A* and *22B*, two possible connections are shown. In both cases, the output of the timer is low during the timing period so that the positive going signal at the end of timing period can trigger the next timer. There is no limitation on the timing period of one timer with respect to any other timer before or after it, because the trigger input to any timer can be high or low when that timer ends its timing period.



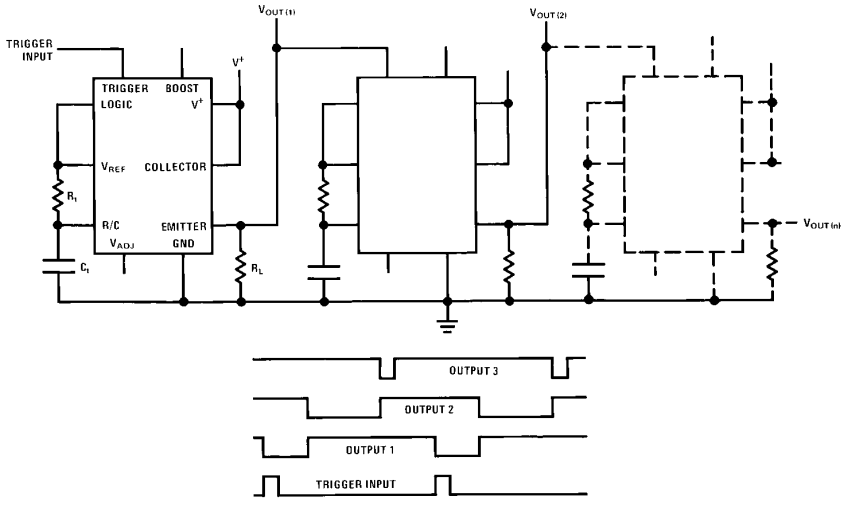
TL/H/7408–24

FIGURE 21. Timer Triggered by Negative Edge of Input Pulse



TL/H/7408–25

(A)



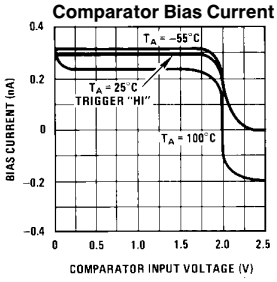
TL/H/7408–26

(B)

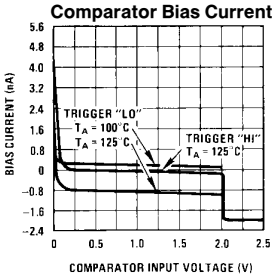
FIGURE 22. Chain of Timers

Typical Performance Characteristics

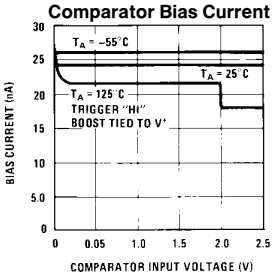
Comparator Bias Current



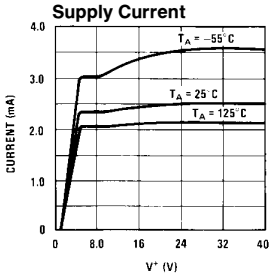
Comparator Bias Current



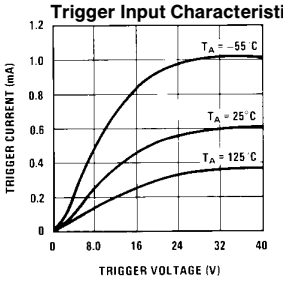
Comparator Bias Current



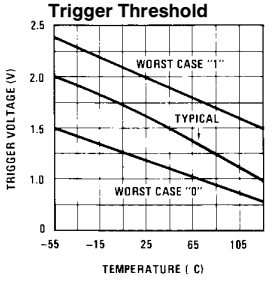
Supply Current



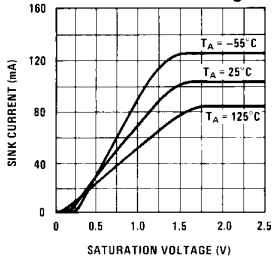
Trigger Input Characteristics



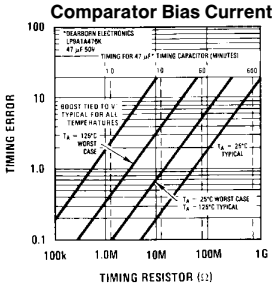
Trigger Threshold



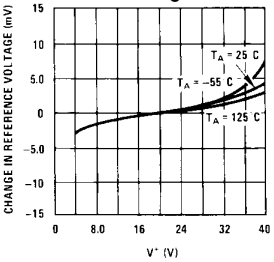
Collector Output Saturation Characteristics at High Current



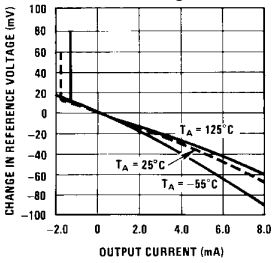
Timing Error Due to Comparator Bias Current



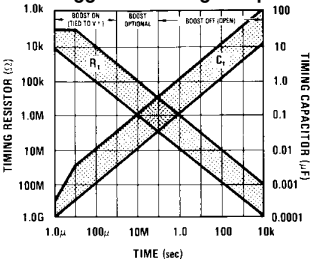
Reference Regulation



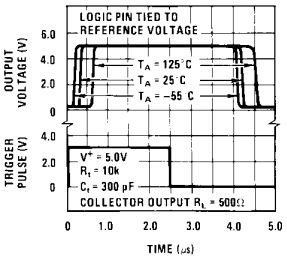
Reference Regulation



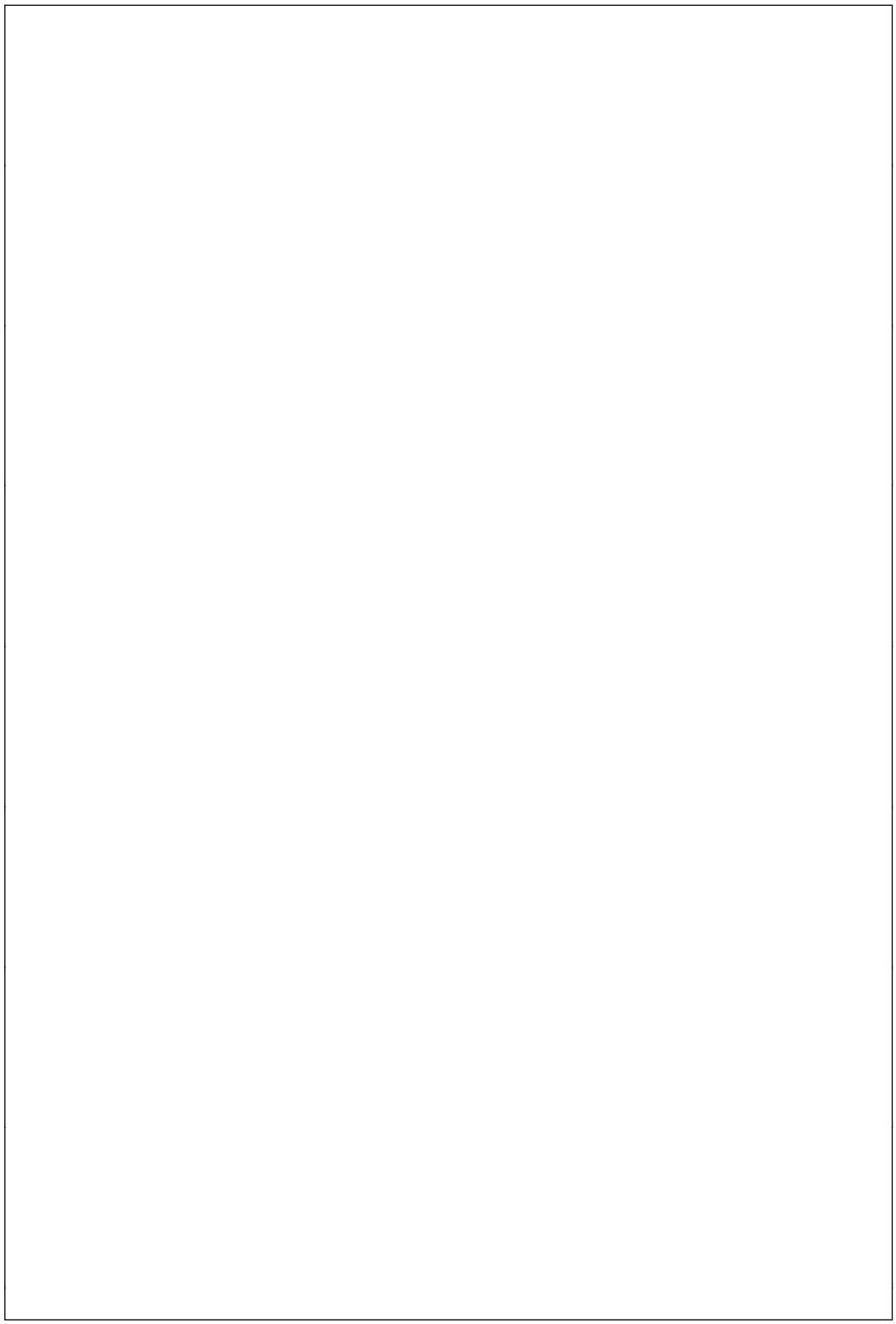
Suggested Timing Components



Short Output Pulse



TL/H/7408–27



LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.