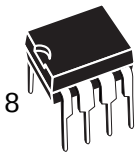
M95640, M95320
M95160, M95080

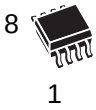
64K/32K/16K/8K Serial SPI EEPROM with High Speed Clock and Positive Clock Strobe

PRELIMINARY DATA

- 100,000 ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- SINGLE SUPPLY VOLTAGE
  - 4.5V to 5.5V for M95xxx
  - 2.7V to 5.5V for M95xxx-V
  - 2.5V to 5.5V for M95xxx-W
  - 1.8V to 3.6V for M95xxx-R
- SPI BUS COMPATIBLE SERIAL INTERFACE
- 5 MHz CLOCK RATE MAX
- STATUS REGISTER
- HARDWARE PROTECTION of the STATUS REGISTER
- 32 BYTE PAGE MODE
- SIZEABLE READ ONLY EEPROM AREA
- SELF-TIMED PROGRAMMING CYCLE
- E.S.D.PROTECTION GREATER than 4000V
- SUPPORTS POSITIVE CLOCK SPI MODES



PSDIP8 (BN)
0.25mm Frame



SO8 (MN)
150 mil Width

DESCRIPTION

The M95xxx is a family of electrically erasable programmable memories (EEPROM) fabricated with STMicroelectronics' High Endurance Double Polysilicon CMOS technology. Each memory is accessed by a simple SPI bus compatible serial interface.

Table 1. Signal Names

C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

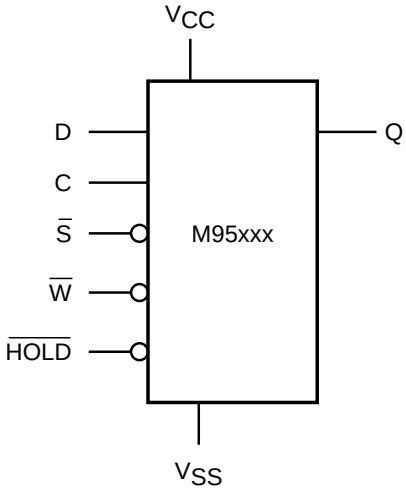


Figure 2A. DIP Pin Connections

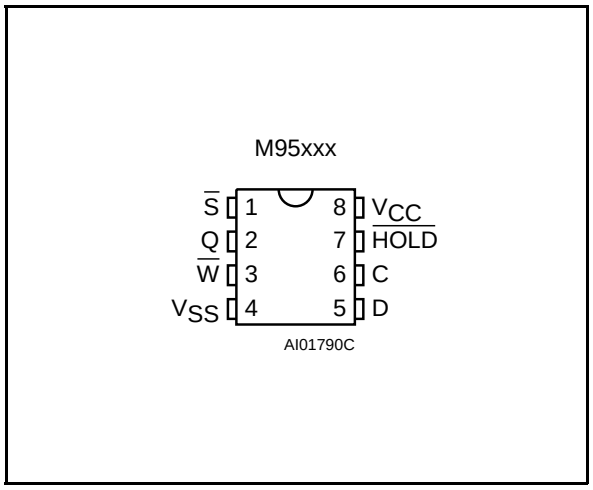


Figure 2B. SO Pin Connections

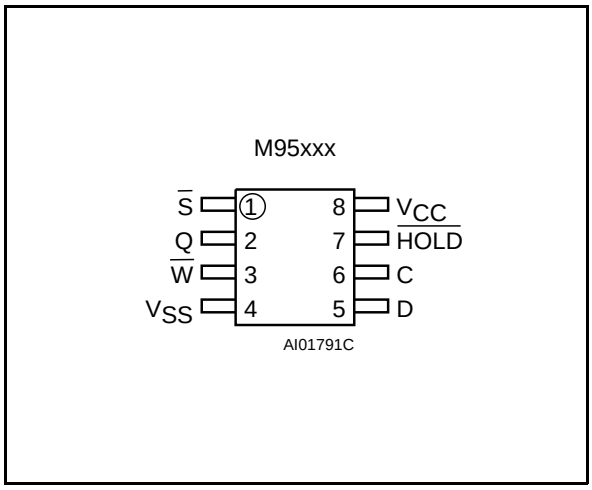


Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature			–40 to 125	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_O	Output Voltage			–0.3 to V_{CC} +0.6	V
V_I	Input Voltage with respect to Ground			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			400	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. DMIL-STD-883C, 3015.7 (100pF, 1500Ω)
3. EIAJ IC-121 (Condition C) (200pF, 0Ω)

DESCRIPTION (cont'd)

The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q).

The device connected to the bus is selected when the chip select input ($\overline{S}$) goes low. Communications with the chip can be interrupted with a hold input ($\overline{HOLD}$).

Data is clocked in during the low to high transition of clock C, data is clocked out during the high to low transition of clock C.

SIGNALS DESCRIPTION

Serial Output (Q). The output pin is used to transfer data serially out of the memory. Data is shifted out on the falling edge of the serial clock.

Serial Input (D). The input pin is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Input is latched on the rising edge of the serial clock.

Serial Clock (C). The serial clock provides the timing of the serial interface. Instructions, addresses, or data present at the input pin are latched

Figure 3. Data and Clock Timing

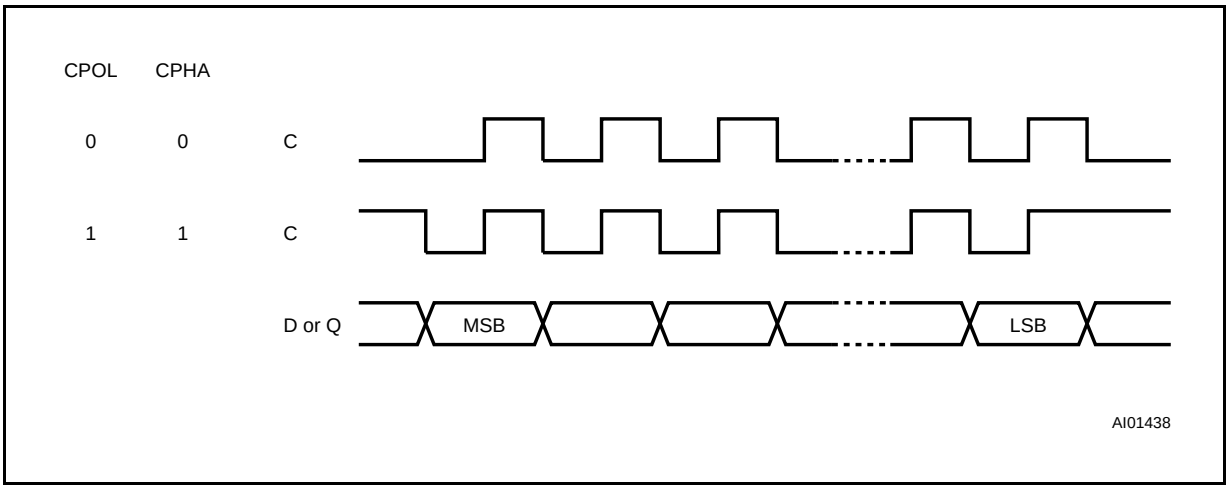
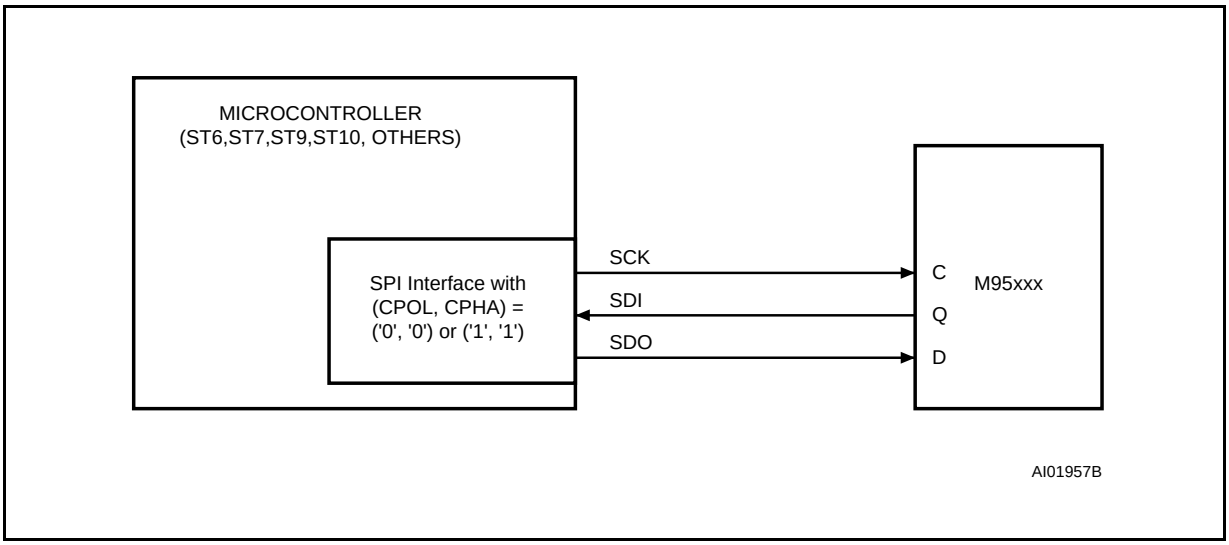


Figure 4. Microcontroller and SPI Interface Set-up



on the rising edge of the clock input, while data on the Q pin changes after the falling edge of the clock input.

Chip Select ($\overline{S}$). When $\overline{S}$ is high, the memory is deselected and the Q output pin is at high impedance and, unless an internal write operation is underway the memory will be in the standby power mode. $\overline{S}$ low enables the memory, placing it in the active power mode. It should be noted that after power-on, a high to low transition on $\overline{S}$ is required prior to the start of any operation.

Write Protect ($\overline{W}$). This pin is for hardware write protection of the status register (SR); except WIP and WEL bits. When bit 7 (SRWD) of the status register is 0 (the initial delivery state); it is possible to write the SR once the WEL (Write Enable Latch) has been set and whatever is the status of pin $\overline{W}$ (high or low).

Note: SRWD stands for; Status Register Write Disable.

Table 3. Protection Feature

$\overline{W}$	SRWD	Status Register (SR)	Data Bytes (Protected Area)	Mode	Data Bytes (Unprotected Area)
X	0	Writable after setting WEL	Software Write protected by the BPn bits of the Status Register	SPM	Writable after setting WEL
1	1	Writable after setting WEL	Software Write protected by the BPn bits of the Status Register	SPM	Writable after setting WEL
0	1	Hardware Write protected	Hardware Write protected	HPM	Writable after setting WEL

Notes: 1. SPM stands for Software Protected Mode.
2. BPn are BP0 to BP1 bits of the Status Register.
3. SPM and HPM are also described in the Write Status Register (WRSR) section.

SIGNALS DESCRIPTION (cont'd)

Once bit 7 (SRWD) of the status register has been set to 1; the possibility to rewrite the SR depends on the logical level present at pin $\overline{W}$:

– If $\overline{W}$ pin is high; it will be possible to rewrite the status register after having set the WEL (Write Enable Latch).

– If $\overline{W}$ pin is low; any attempt to modify the status register will be ignored by the device even if the WEL was set. As a consequence: all the data bytes in the EEPROM area protected by the BPn bits of the status register are also hardware protected against data corruption and can be seen as a Read Only EEPROM area from the microcontroller. This mode is called the Hardware Protected Mode (HPM).

It is possible to enter the Hardware Protected Mode (HPM) by setting SRWD bit after pulling down the $\overline{W}$ pin or by pulling down the $\overline{W}$ pin after setting SRWD bit.

The only way to abort the Hardware Protected Mode once entered is to pull high the $\overline{W}$ pin.

If $\overline{W}$ pin is permanently tied to high level; the Hardware Protected Mode will never be activated and the memory will only allow the user to software protect a part of the memory with the BPn bits of the status register. All protection features of the device are summarized in Table 3.

Hold ($\overline{HOLD}$). The $\overline{HOLD}$ pin is used to pause serial communications with an SPI memory without resetting the serial sequence. To take the Hold condition into account, the product must be selected ($\overline{S}$ = 0). Then the Hold state is validated by a high to low transition on $\overline{HOLD}$ when C is low. To resume the communications, $\overline{HOLD}$ is brought high while C is low. During the Hold condition D, Q, and C are at a high impedance state.

When the memory is under the Hold condition, it is possible to deselect the device. However, the serial communications will remain paused after a reselect, and the chip will be reset.

The memory can be driven by a microcontroller with its SPI peripheral running in either of the two following modes: (CPOL, CPHA) = ('0', '0') or (CPOL, CPHA) = ('1', '1').

For these two modes, input data is latched in by the low to high transition of clock C, and output data is available from the high to low transition of Clock (C).

The difference between (CPOL, CPHA) = (0, 0) and (CPOL, CPHA) = (1, 1) is the stand-by polarity: C remains at '0' for (CPOL, CPHA) = (0, 0) and C remains at '1' for (CPOL, CPHA) = (1, 1) when there is no data transfer.

OPERATIONS

All instructions, addresses and data are shifted in and out of the chip MSB first. Data input (D) is sampled on the first rising edge of clock (C) after the chip select ($\overline{S}$) goes low. Prior to any operation, a one-byte instruction code must be entered in the chip. This code is entered via the data input (D), and latched on the rising edge of the clock input (C). To enter an instruction code, the product must have been previously selected ($\overline{S}$ = low). Table 4 shows the instruction set and format for device operation. If an invalid instruction is sent (one not contained in Table 4), the chip is automatically deselected.

Write Enable (WREN) and Write Disable (WRDI)

The memory contains a write enable latch. This latch must be set prior to every WRITE, WRSR operation. The WREN instruction will set the latch and the WRDI instruction will reset the latch. The latch is reset under the following conditions:

– Power on,
– WRDI instruction completion,
– WRSR instruction completion,
– WRITE instruction completion.

As soon as the WREN or WRDI instruction is received, the circuit executes the instruction and enters a wait mode until it is deselected.

Read Status Register (RDSR)

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write to the memory operation.

As soon as the 8th bit of the status register is read out, the memory enters a wait mode (data on D is not decoded, Q is in Hi-Z) until it is deselected.

The status register format is as follows:

b7							b0
SRWD	X	X	X	BP1	BP0	WEL	WIP

BP0, BP1: Read and write bits
WEL, WIP: Read only bits.
SRWD: Read and Write bit.

During a write to the memory operation: all bits BP0, BP1, WEL, WIP are valid and can be read. During a write to the status register, only the bits WEL and WIP are valid and can be read. The values of BP1 and BP0 read at that time correspond to the previous contents of the status register.

The Write-In-Process (WIP) read-only bit indicates whether the memory is busy with a write operation. When set to a '1' a write is in progress, when set to a '0' no write is in progress.

The Write Enable Latch (WEL) read-only bit indicates the status of the write enable latch. When set to a '1' the latch is set, when set to a '0' the latch is reset. The Block Protect (BP0 and BP1) bits indicate the extent of the protection employed. These bits are set by the user issuing the WRSR instruction. These bits are non-volatile.

Table 4. Instruction Set

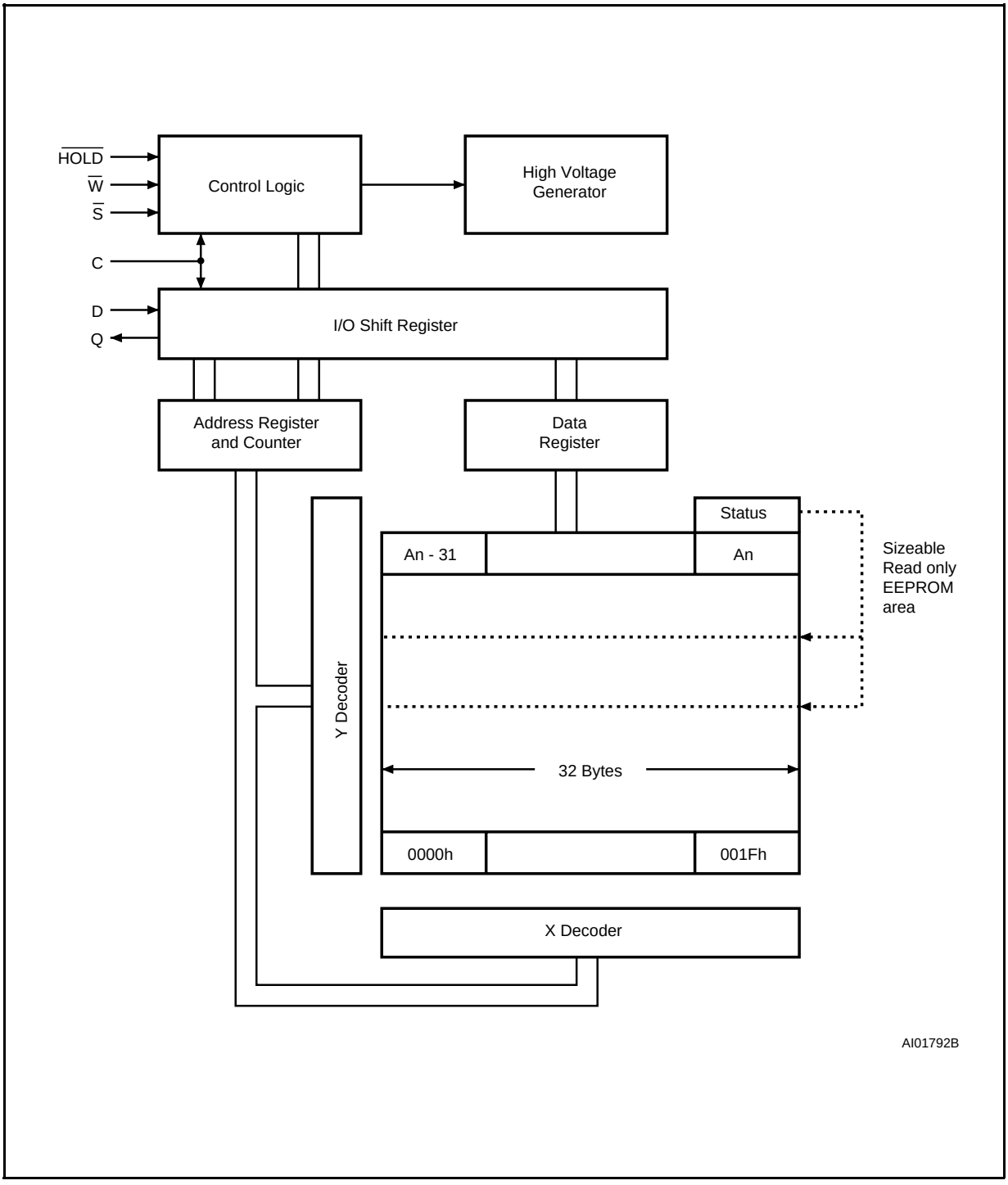
Instruction	Description	Instruction Format
WREN	Set Write Enable Latch	0000 0110
WRDI	Reset Write Enable Latch	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read Data from Memory Array	0000 0011
WRITE	Write Data to Memory Array	0000 0010

Table 5. Address Range Bits

Device	M95080	M95160	M95320	M95640
Address Bit	A0-A9	A0-A10	A0-A11	A0-A12

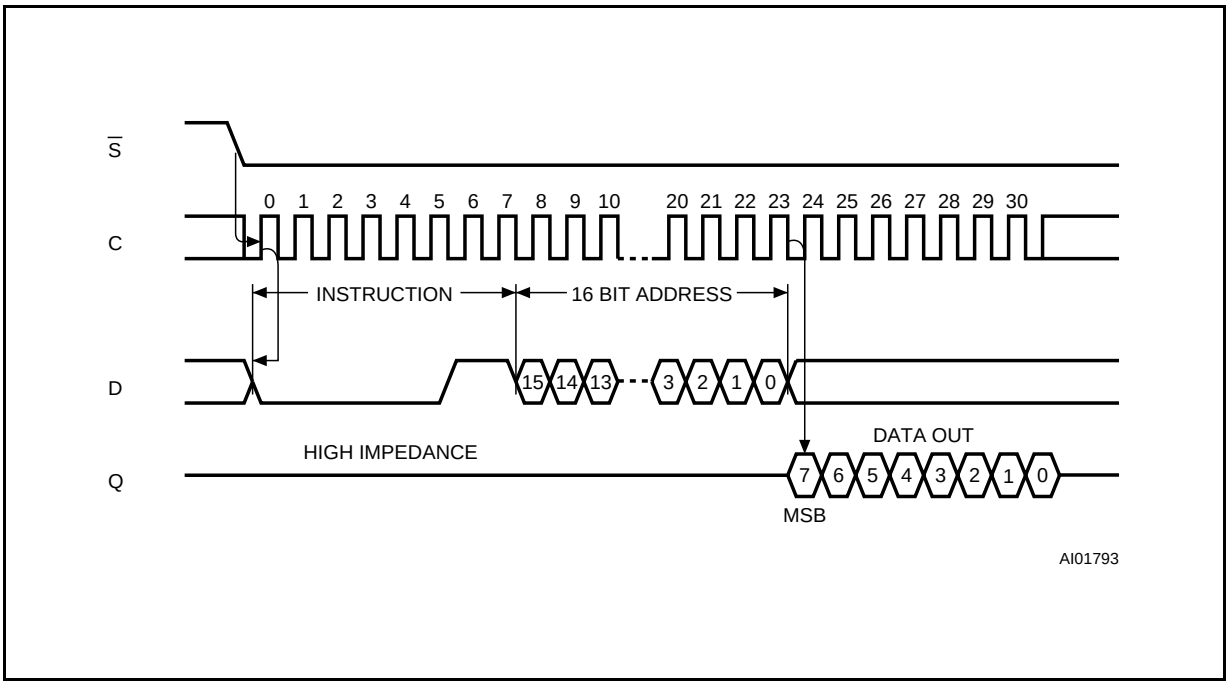
Note: Address bits up to A15 not specified are don't care.

Figure 5. Block Diagram



Note: An is the top address of the memory.

Figure 6. Read EEPROM Array Operation Sequence



Note: Depending on the memory size, most significant address bits are don't care.

Table 6. Write Protected Block Size

Status Register Bits		Protected Block	Array Addresses Protected			
BP1	**BP0**		**M95080**	**M95160**	**M95320**	**M95640**
0	0	none	none	none	none	none
0	1	Upper quarter	0300h - 03FFh	0600h - 07FFh	0C00h - 0FFFh	1800h - 1FFFh
1	0	Upper half	0200h - 03FFh	0400h - 07FFh	0800h - 0FFFh	1000h - 1FFFh
1	1	Whole Memory	0000h - 03FFh	0000h - 07FFh	0000h - 0FFFh	0000h - 1FFFh

Write Status Register (WRSR)

When the WRSR instruction and the 8 bits of the Status Register are latched-in, the internal write cycle is then triggered by the rising edge of $\overline{S}$. This rising edge of $\overline{S}$ must appear just before the rising edge of the 17 th clock pulse (see Serial input timing Figure 14), otherwise the internal write sequence is not performed.

The WRSR instruction allows the user:

1. to select the size of the memory to be protected,
2. to choose the protection level between the SPM (Software Protected Mode) and the HPM (Hardware Protected Mode).

Size Selection. The way to select the size of the EEPROM area to be protected is common to both SPM and HPM. BP1 and BP0 bits (initial delivery states = 00; that is size = 0) of the Status Register have to be written once the data to be protected are stored in the EEPROM. The Table 6 summarizes the size selection functions of the memory.

Figure 7. Write Enable Latch Sequence

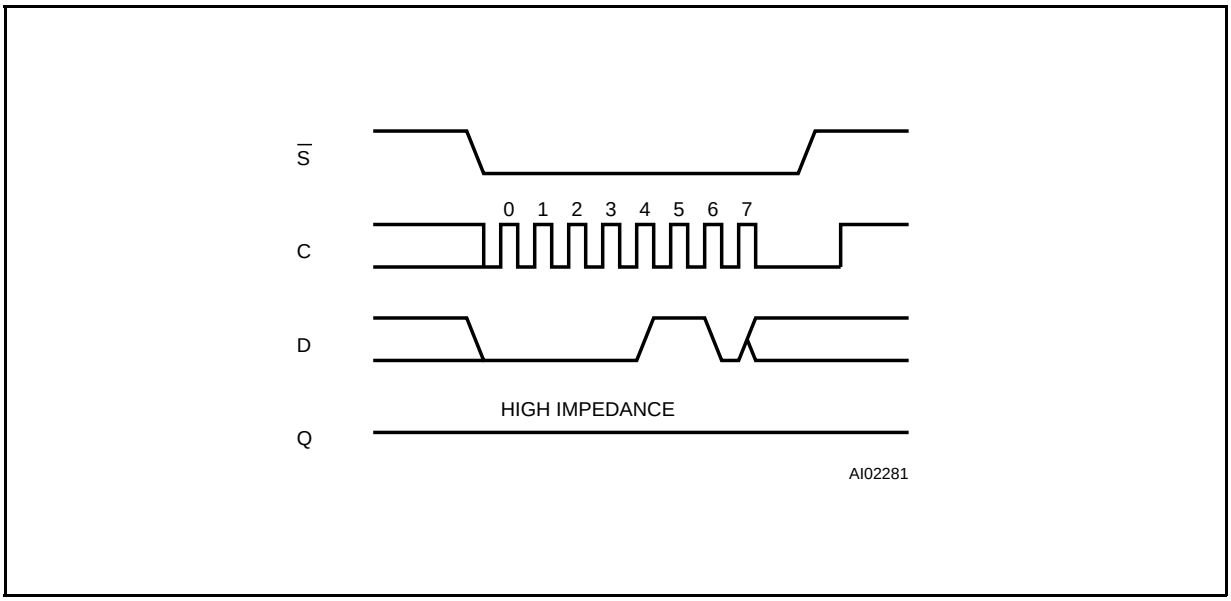
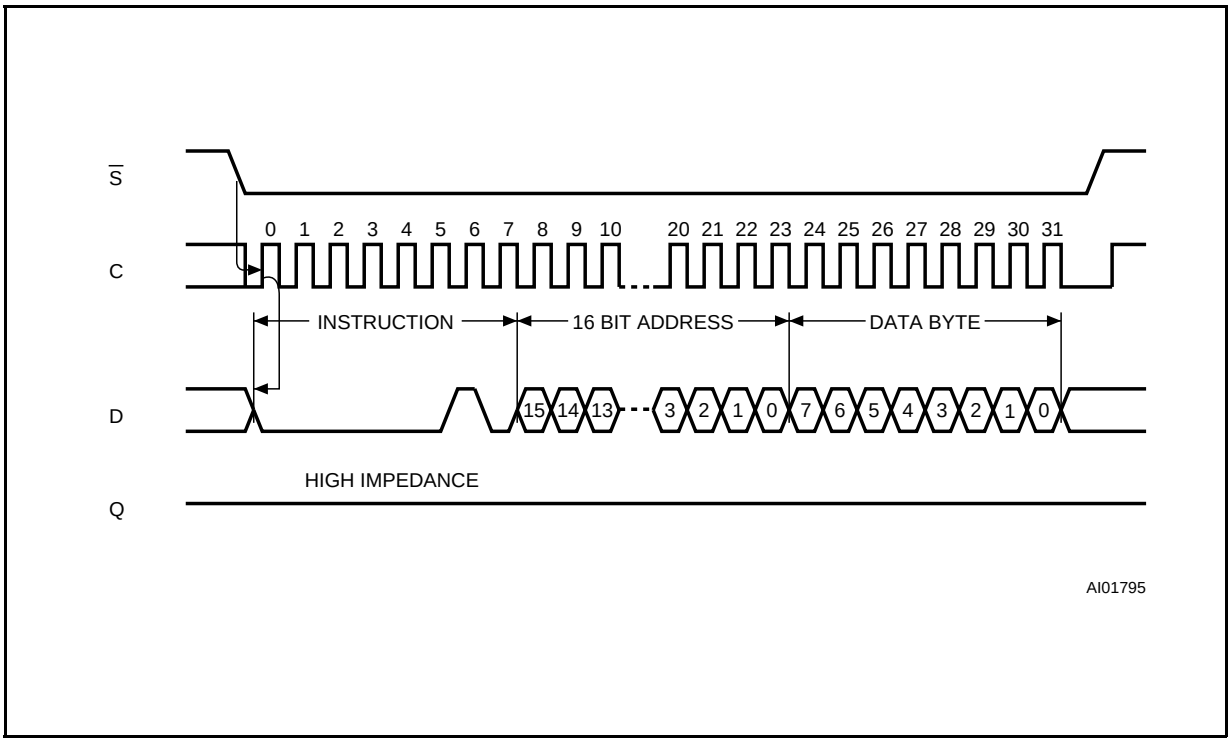
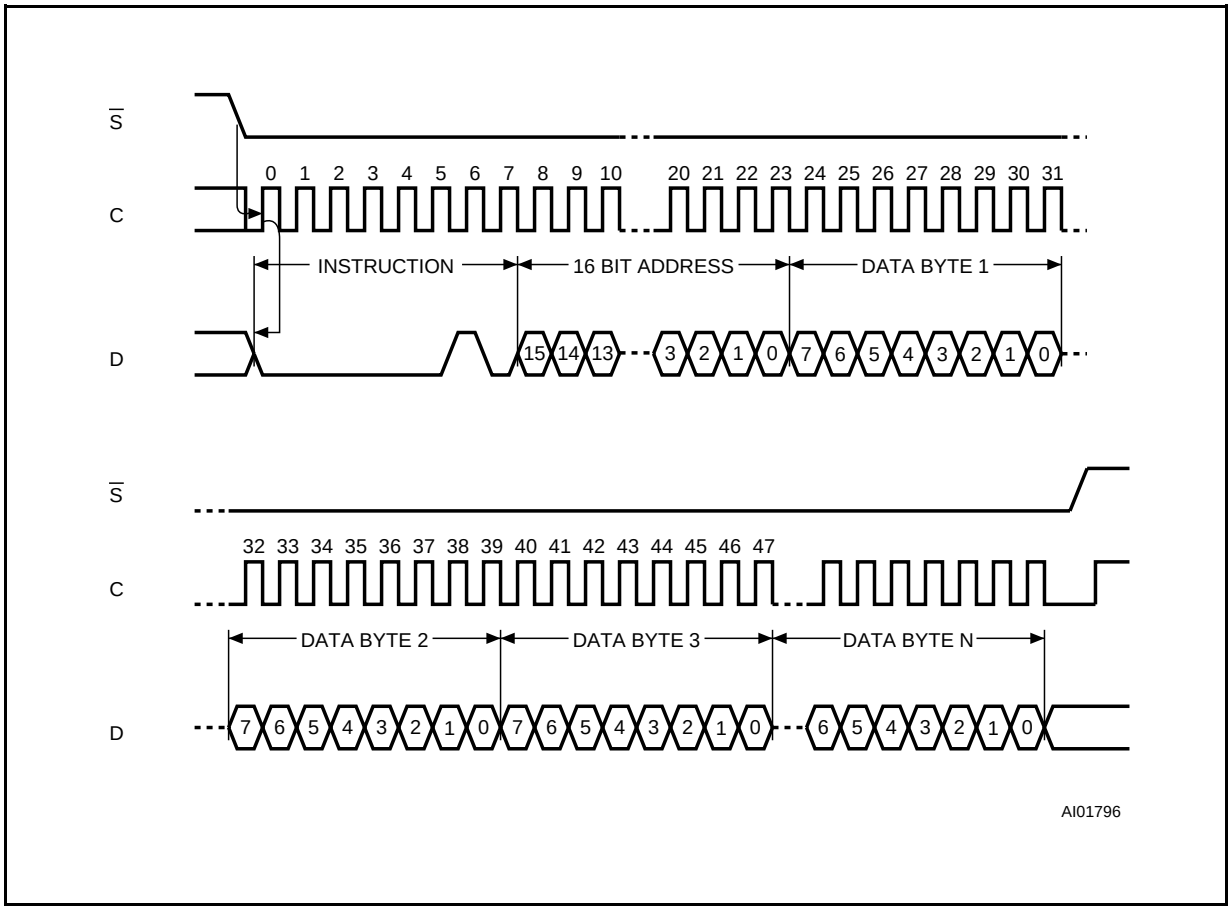


Figure 8. Byte Write Operation Sequence



Note: Depending on the memory size, most significant address bits are don't care.

Figure 9. Page Write Operation Sequence



Note: Depending on the memory size, most significant address bits are don't care.

Figure 10. RDSR: Read Status Register Sequence

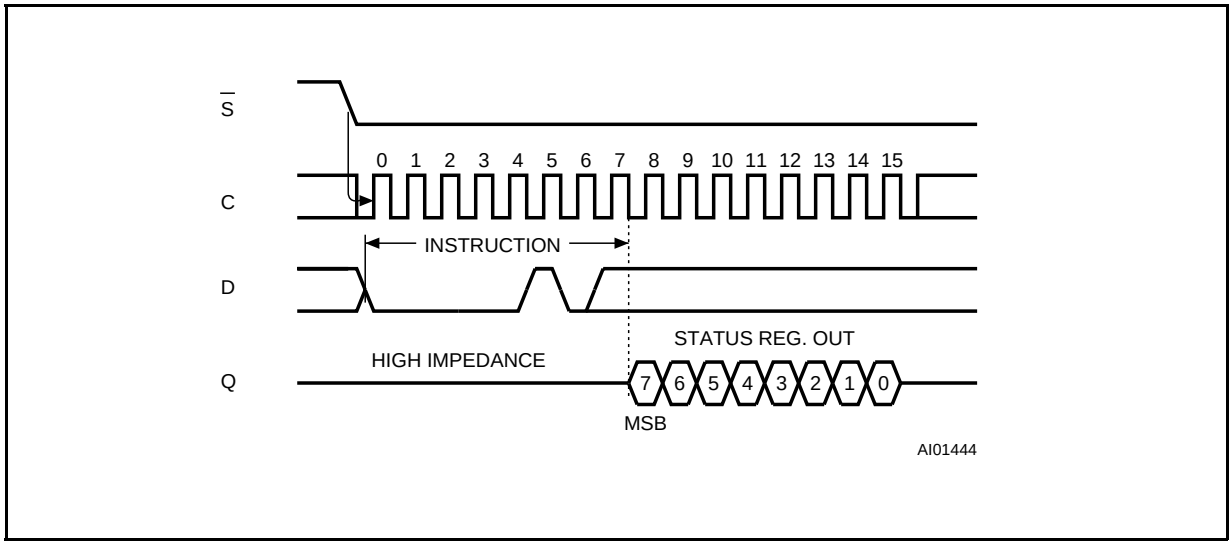
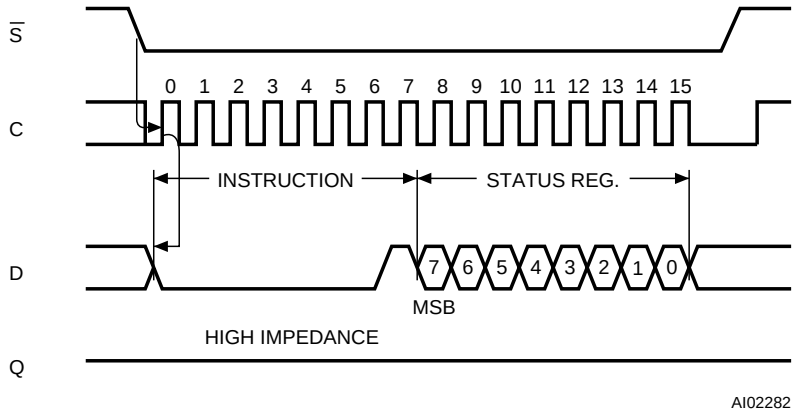


Figure 11. WRSR: Write Status Register Sequence



Selection of the Protection Level

– Once BP0 and BP1 bits are written; **the Software Protected Mode (SPM) is entered.** This means that any attempt to write a byte or a page in the protected area will be ignored even if the Write Enable Latch was set before the write instruction. In this Software Protected Mode; BP0 and BP1 bits can be rewritten with the WSR instruction after having set the WEL.

– If a higher level of protection is needed; **the Hardware Protected Mode (HPM)** can be selected. It is possible to enter the HPM by setting SRWD bit after pulling down the $\overline{W}$ pin or by pulling down the $\overline{W}$ pin after setting SRWD. In both cases, the SRWD is set by using the WSR instruction after having set the WEL bit. It should also be noted that the SRWD can be set after writing BP0 and BP1 or at the same time.

– Once the HPM is entered, the content of the Status Register and all data bytes in the protected area are Hardware Protected against write attempts. The only way to write again the status register is to abort the HPM by pulling high the $\overline{W}$ pin. Aborting the HPM will put the device in the SPM with BP0 and BP1 bits unchanged.

Note: See also the Write Protect pin ($\overline{W}$) description on page 3).

Typical Applications

– The $\overline{W}$ pin can be dynamically driven by an output port of a microcontroller but can also be connected directly or through a pull-down resistor to V_{SS}.

– With such a PCB (Printed Circuit Board):

a) the memory in the initial delivery state can be soldered directly. After power on, the microcontroller can write data to be protected in the memory. Then write BP0, BP1 and set the SRWD to enter the HPM.

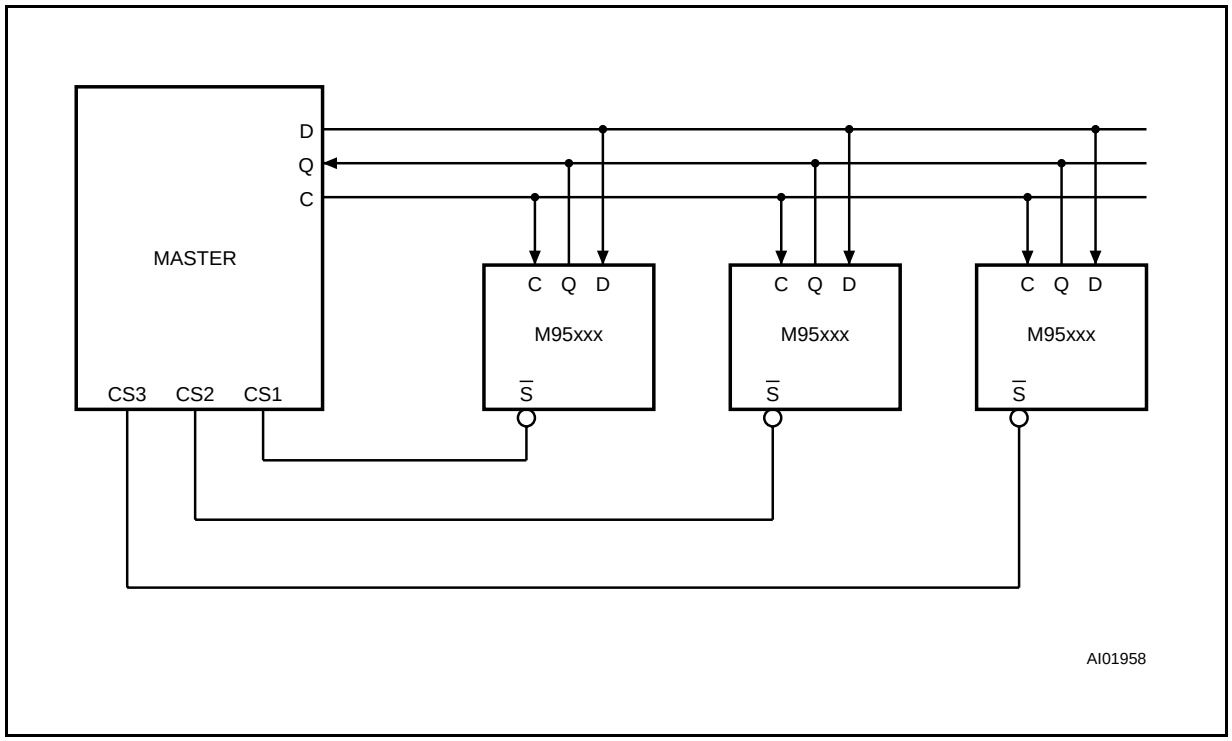
b) data to be protected, BP0, BP1 can be written and SRWD can be set before soldering the memory. As a consequence, once soldered, the memory is immediately placed in the HPM.

In these two cases, the only way to abort the HPM will be to remove the memory from the PCB or to apply V_{CC} on the $\overline{W}$ pin through an external equipment when a pull-down resistor is inserted between the pin and V_{SS}.

Read Operation

The chip is first selected by putting $\overline{S}$ low. The serial one byte read instruction is followed by a two bytes address (A15-A0), each bit being latched-in during the rising edge of the clock (C).

Figure 12. EEPROM and SPI Bus



Then the data stored in the memory at the selected address is shifted out on the Q output pin; each bit being shifted out during the falling edge of the clock (C). The data stored in the memory at the next address can be read in sequence by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to "0h" allowing the read cycle to be continued indefinitely. The read operation is terminated by deselecting the chip. The chip can be deselected at any time during data output. Any read attempt during a write cycle will be rejected and will deselect the chip.

Byte Write Operation

Prior to any write attempt, the write enable latch must be set by issuing the WREN instruction. First the device is selected ($\overline{S}$ = low) and a serial WREN instruction byte is issued. Then the product is deselected by taking $\overline{S}$ high. After the WREN instruction byte is sent, the memory will set the write enable latch and then remain in standby until it is deselected. Then the write state is entered by selecting the chip, issuing three bytes of instruction and address, and one byte of data.

Chip Select ($\overline{S}$) must remain low for the entire duration of the operation. The product must be deselected just after the eighth bit of data has been latched in. If not, the write process is cancelled. As soon as the product is deselected, the self-timed write cycle is initiated. While the write is in progress, the status register may be read to check BP1, BP0, WEL and WIP. WIP is high during the self-timed write cycle. When the cycle is completed, the write enable latch is reset.

Page Write Operation

A maximum of 32 bytes of data may be written during one non-volatile write cycle. All 32 bytes must reside on the same page. The page write mode is the same as the byte write mode except that instead of deselecting the device after the first byte of data, up to 31 additional bytes can be shifted in prior to deselecting the chip. Any address of the memory can be chosen as the first address to be written. If the address counter reaches the end of the page (xxxx xxx1 1111) and the clock continues, the counter will roll over to the first address of the page (xxxx xxx0 0000) and overwrite any previously written data. The programming cycle will only start if the $\overline{S}$ transition occurs just after the eighth bit of data of a word is received.

POWER ON STATE

After a Power up the memory is in the following state:

– The device is in the low power standby state.
– The chip is deselected.
– The chip is not in hold condition.
– The write enable latch is reset.
– b7 to b2 bits of the status register are unchanged (non-volatile bits).

DATA PROTECTION AND PROTOCOL SAFETY

– Non valid $\overline{S}$ and $\overline{HOLD}$ transitions are not taken into account.
– $\overline{S}$ must come high at the proper clock count in order to start a non-volatile write cycle (in the memory array or in the status register), that is the Chip Select $\overline{S}$ must rise during the clock pulse following the introduction of a multiple of 8 bits.
– Access to the memory array during non-volatile programming cycle is ignored; however, the programming cycle continues.
– After any of the operations WREN, WRDI, RDSR is completed, the chip enters a wait state and waits for a deselect.
– The write enable latch is reset upon power-up.

INITIAL DELIVERY STATE

The device is delivered with the memory array in a fully erased state (all data set at all "1's" or FFh). The Status Register Bits are initialized to 00.

Status Register:

b7							b0
0	0	0	0	0	0	0	0

Table 7. Input Parameters (1) (T_A = 25 °C, f = 5 MHz)

Symbol	Parameter	Min	Max	Unit
C_{OUT}	Output Capacitance (Q)		8	pF
C_{IN}	Input Capacitance (other pins)		6	pF

Note: 1. Sampled only, not 100% tested.

Table 8. AC Measurement Conditions

Input Rise and Fall Times	≤ 50ns
Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$
Input and Output Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$
Output Load	C_L = 100pF

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 13. AC Testing Input Output

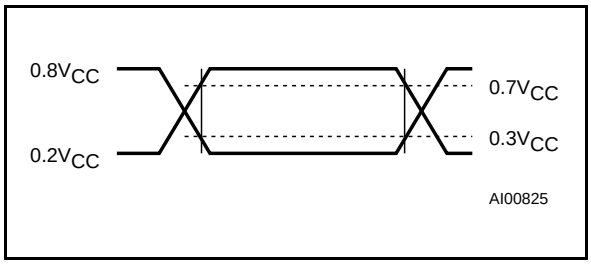


Table 9. DC Characteristics
(T_A = 0 to 70°C; –40 to 85°C or –40 to125°C; V_{CC} = 4.5V to 5.5V)
(T_A = 0 to 70°C; –40 to 85°C; V_{CC} = 2.7V to 5.5V)
(T_A = 0 to 70°C; –40 to 85°C; V_{CC} = 2.5V to 5.5V)
(T_A = 0 to 70°C; –20 to 85°C; V_{CC} = 1.8V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current			±2	µA
I_{LO}	Output Leakage Current			±2	µA
I_{CC}	Supply Current	C = 0.1 V_{CC}/0.9 V_{CC}, at 5 MHz, V_{CC} = 5V, Q = Open		4	mA
		C = 0.1 V_{CC}/0.9 V_{CC}, at 2 MHz, V_{CC} = 5V, Q = Open, Note 2		4	mA
	Supply Current (V series)	C = 0.1 V_{CC}/0.9 V_{CC}, at 5 MHz, V_{CC} = 2.7V, Q = Open		3	mA
	Supply Current (W series)	C = 0.1 V_{CC}/0.9 V_{CC}, at 2 MHz, V_{CC} = 2.5V, Q = Open		2	mA
	Supply Current (R series)	C = 0.1 V_{CC}/0.9 V_{CC}, at 1 MHz, V_{CC} = 1.8V, Q = Open		2	mA
I_{CC1}	Standby Current	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V		10	µA
		$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5V, Note 2		10	µA
	Standby Current (V series)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.7V		2	µA
	Standby Current (W series)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 2.5V		2	µA
	Standby Current (R series)	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 1.8V		1	µA
V_{IL}	Input Low Voltage		–0.3	0.3 V_{CC}	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 1	V
V_{OL} (1)	Output Low Voltage	I_{OL} = 2mA, V_{CC} = 5V		0.4	V
		I_{OL} = 2mA, V_{CC} = 5V, Note 2		0.4	V
	Output Low Voltage (V series)	I_{OL} = 1.5mA, V_{CC} = 2.7V		0.4	V
	Output Low Voltage (W series)	I_{OL} = 1.5mA, V_{CC} = 2.5V		0.4	V
	Output Low Voltage (R series)	I_{OL} = 0.15mA, V_{CC} = 1.8V		0.3	V
V_{OH} (1)	Output High Voltage	I_{OH} = –2mA, V_{CC} = 5V	0.8 V_{CC}		V
		I_{OH} = –2mA, V_{CC} = 5V, Note 2	0.8 V_{CC}		V
	Output High Voltage (V series)	I_{OH} = –0.4mA, V_{CC} = 2.7V	0.8 V_{CC}		V
	Output High Voltage (W series)	I_{OH} = –0.4mA, V_{CC} = 2.5V	0.8 V_{CC}		V
	Output High Voltage (R series)	I_{OH} = –0.1mA, V_{CC} = 1.8V	0.8 V_{CC}		V

Notes: 1. The device meets output requirements for both TTL and CMOS standards.
2. Test performed at –40 to 125°C temperature range, grade 3.

Table 10A. AC Characteristics

Symbol	Alt	Parameter	M95640 / 320 / 160 / 080				Unit
			V_{CC} = 4.5V to 5.5V, T_A = 0 to 70°C, T_A = –40 to 85°C		V_{CC} = 4.5V to 5.5V, T_A = –40 to 125°C		
			Min	Max	Min	Max	
f_C	f_C	Clock Frequency	D.C.	5	D.C.	2	MHz
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup Time	90		200		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	90		200		ns
t_{CH} (1)	t_{CLH}	Clock High Time	90		200		ns
t_{CL} (1)	t_{CLL}	Clock Low Time	90		200		ns
t_{CLCH} (2)	t_{RC}	Clock Rise Time		1		1	µs
t_{CHCL} (2)	t_{FC}	Clock Fall Time		1		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	20		40		ns
t_{CHDX}	t_{DH}	Data In Hold Time	30		50		ns
t_{DLDH} (2)	t_{RI}	Data In Rise Time		1		1	µs
t_{DHDL} (2)	t_{FI}	Data In Fall Time		1		1	µs
t_{HHCH}	t_{CD}	$\overline{HOLD}$ Setup Time	70		140		ns
t_{HLCH}	t_{CD}	Clock Low Hold Time	40		90		ns
t_{CLHL}	t_{HD}	$\overline{HOLD}$ Hold Time	0		0		ns
t_{CLHH}	t_{HD}	Clock Low Setup Time	0		0		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	90		200		ns
t_{SHCH}		$\overline{S}$ Not Active Setup Time	90		200		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	100		200		ns
t_{SHQZ} (2)	t_{DIS}	Output Disable Time		100		250	ns
t_{CLQV}	t_V	Clock Low to Output Valid		60		150	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		0		ns
t_{QLQH} (2)	t_{RO}	Output Rise Time		50		100	ns
t_{QHQL} (2)	t_{FO}	Output Fall Time		50		100	ns
t_{HHQX} (2)	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z		50		100	ns
t_{HLQZ} (2)	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		100		250	ns
t_W	t_{WP}	Write Cycle Time		10		10	ms

Notes: 1. $t_{CH} + t_{CL} \geq 1/fc$
2. Value guaranteed by characterization, not 100% tested in production.

Table 10B. AC Characteristics

Symbol	Alt	Parameter	M95640 / 320 / 160 / 080						Unit
			V_{CC} = 2.7V to 5.5V, T_A = 0 to 70°C, T_A = –40 to 85°C		V_{CC} = 2.5V to 5.5V, T_A = 0 to 70°C, T_A = –40 to 85°C		V_{CC} = 1.8V to 3.6V, T_A = 0 to 70°C, T_A = –20 to 85°C		
			Min	Max	Min	Max	Min	Max	
f_C	f_C	Clock Frequency	D.C.	5	D.C.	2	D.C.	1	MHz
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup Time	90		200		400		ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time	90		200		400		ns
t_{CH} (1)	t_{CLH}	Clock High Time	90		200		400		ns
t_{CL} (1)	t_{CLL}	Clock Low Time	90		200		400		ns
t_{CLCH} (2)	t_{RC}	Clock Rise Time		1		1		1	µs
t_{CHCL} (2)	t_{FC}	Clock Fall Time		1		1		1	µs
t_{DVCH}	t_{DSU}	Data In Setup Time	20		40		60		ns
t_{CHDX}	t_{DH}	Data In Hold Time	30		50		100		ns
t_{DLDH} (2)	t_{RI}	Data In Rise Time		1		1		1	µs
t_{DHDL} (2)	t_{FI}	Data In Fall Time		1		1		1	µs
t_{HHCH}	t_{CD}	$\overline{HOLD}$ Setup Time	70		140		350		ns
t_{HLCH}	t_{CD}	Clock Low Hold Time	40		90		200		ns
t_{CLHL}	t_{HD}	$\overline{HOLD}$ Hold Time	0		0		0		ns
t_{CLHH}	t_{HD}	Clock Low Setup Time	0		0		0		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ Active Hold Time	90		200		400		ns
t_{SHCH}		$\overline{S}$ Not Active Setup Time	90		200		400		ns
t_{SHSL}	t_{CS}	$\overline{S}$ Deselect Time	100		200		300		ns
t_{SHQZ} (2)	t_{DIS}	Output Disable Time		100		250		500	ns
t_{CLQV}	t_V	Clock Low to Output Valid		60		150		380	ns
t_{CLQX}	t_{HO}	Output Hold Time	0		0		0		ns
t_{QLQH} (2)	t_{RO}	Output Rise Time		50		100		200	ns
t_{QHQL} (2)	t_{FO}	Output Fall Time		50		100		200	ns
t_{HHQX} (2)	t_{LZ}	$\overline{HOLD}$ High to Output Low-Z		50		100		250	ns
t_{HLQZ} (2)	t_{HZ}	$\overline{HOLD}$ Low to Output High-Z		100		250		500	ns
t_W	t_{WP}	Write Cycle Time		10		10		10	ms

Notes: 1. $t_{CH} + t_{CL} \geq 1/fc$
2. Value guaranteed by characterization, not 100% tested in production.

Figure 14. Serial Input Timing

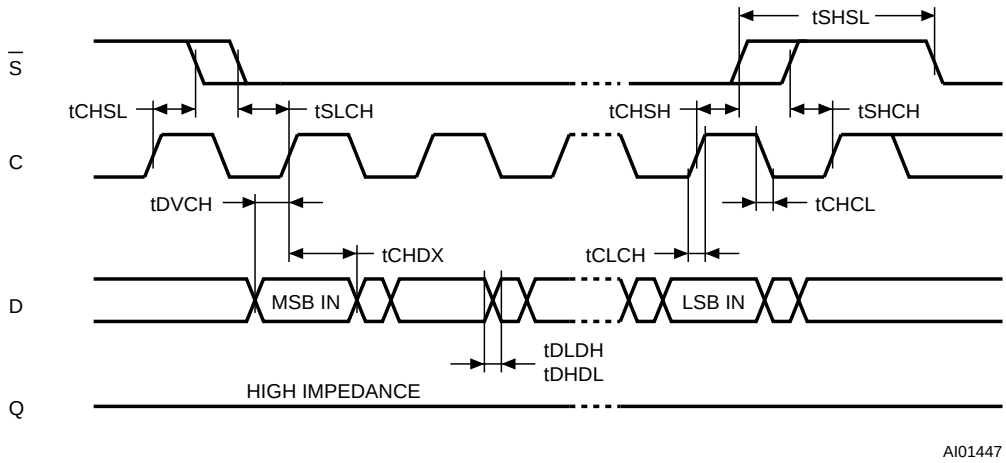


Figure 15. Hold Timing

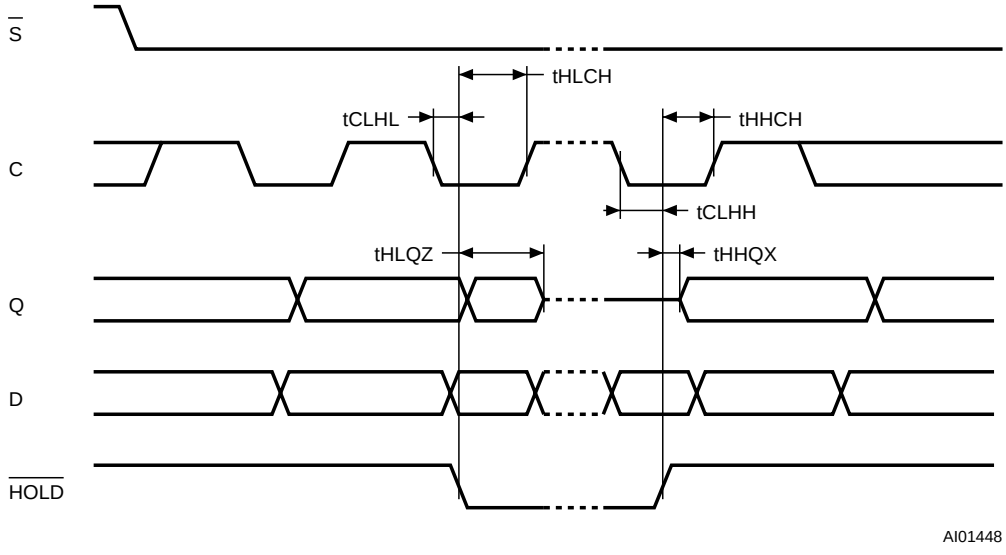
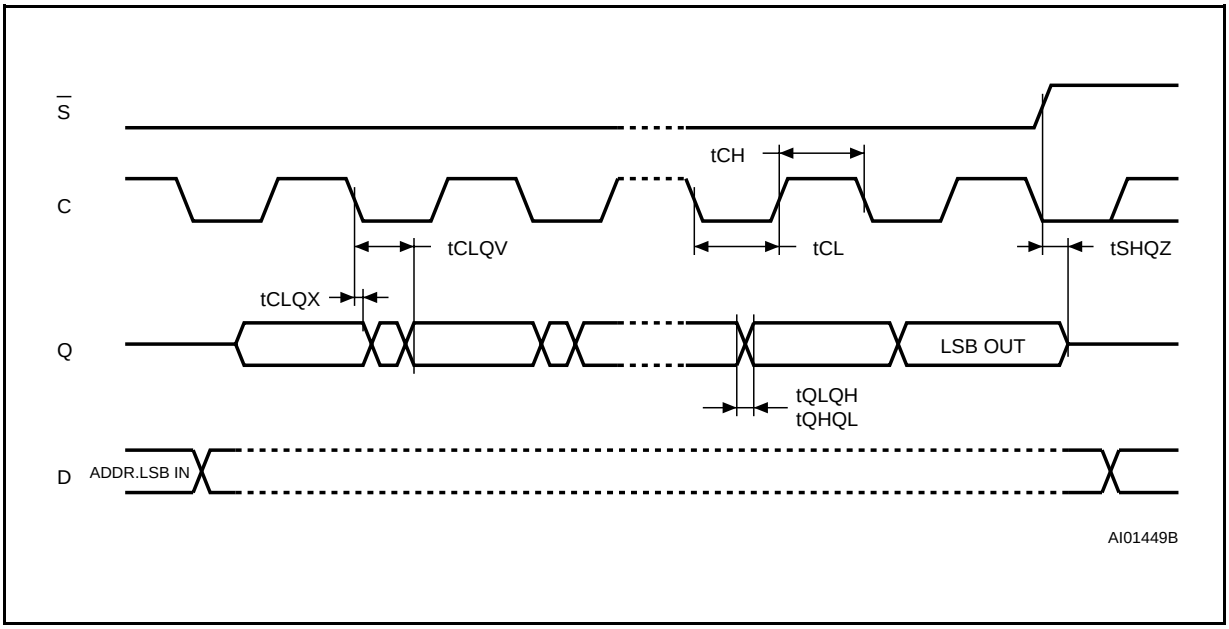
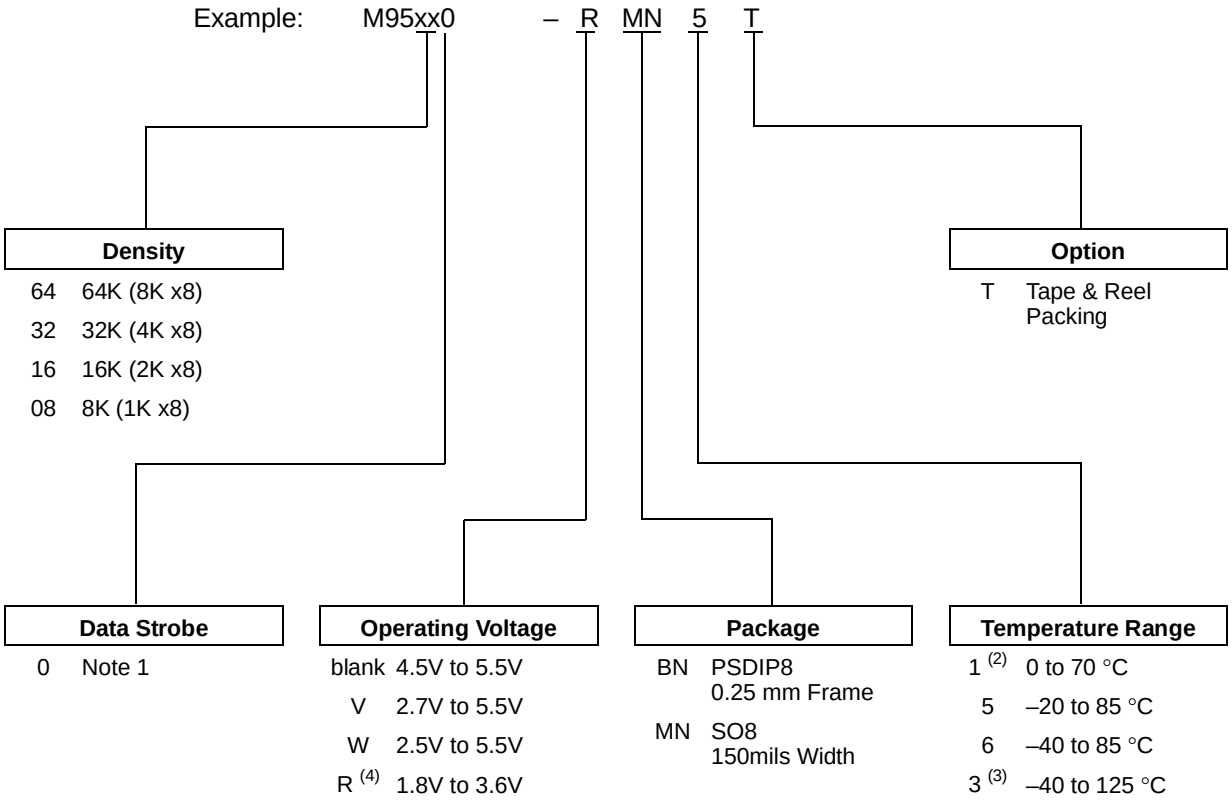


Figure 16. Output Timing



ORDERING INFORMATION SCHEME



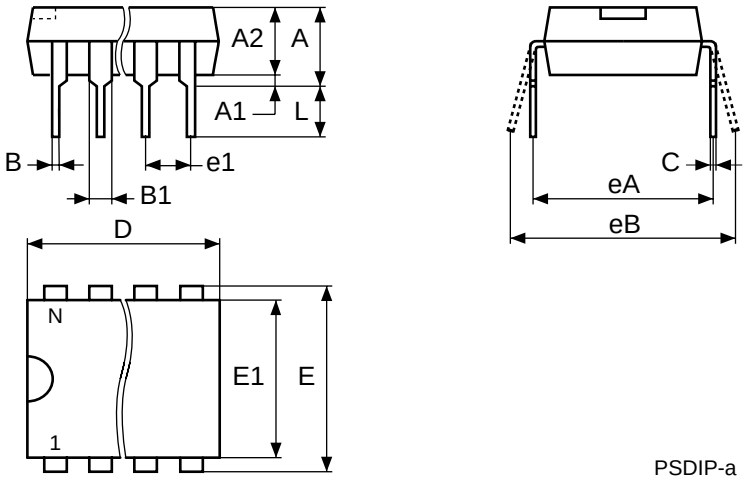
Notes: 1. Data In is strobed on rising edge of the clock (C) and Data Out is synchronized from the falling edge of the clock.
2. Temperature range on request only,
3. Produced with High Reliability Certified Flow (HRCF), in V_{CC} range 4.5V to 5.5V only.
4. -R version (1.8V to 3.6V) are only available in temperature ranges 5 or 1.

Devices are shipped from the factory with the memory content set at all "1's" (FFh).

For a list of available options (Operating Voltage, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		
CP			0.10			0.004

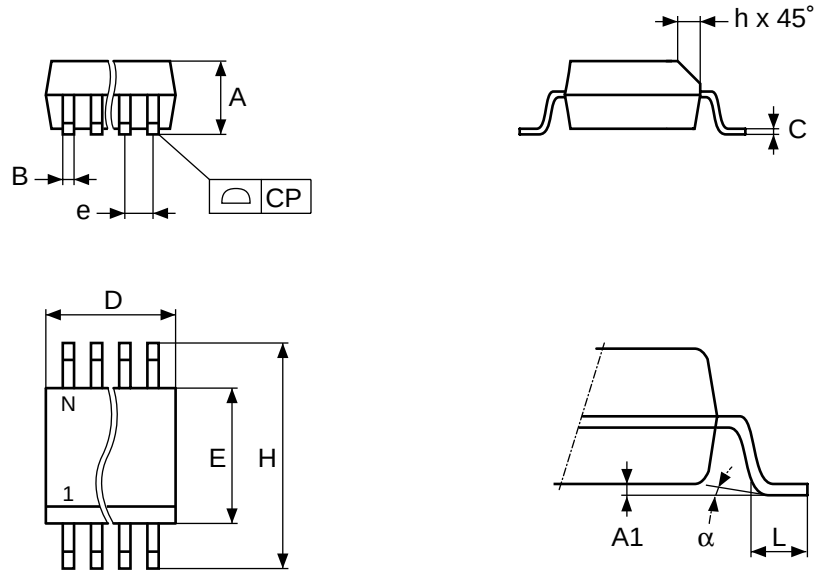


PSDIP-a

Drawing is not to scale.

SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004



SO-a

Drawing is not to scale.